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Improved phase shedding technique in a multiphase converter system

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IMPROVED PHASE SHEDDING TECHNIQUE IN A MULTIPHASE CONVERTER SYSTEM

by

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ABSTRACT

Multiphase converters are increasingly gaining prominence in the field ofpower electronics. The main advantage of a multiphase converter is its increased efficiency in comparison to a single phase converter. The one major drawback of a multiphase converter is its light load efficiency. Light load efficiency in multiphase converters is very poor when compared to single phase converters. Phase shedding is one of the approaches used to improve this light load efficiency but the transient output voltage response of the system shows large deviations during the process of phase change. This thesis proposes a new technique, called the ramp control technique, to improve this transient behavior. Ramp control technique, proposes to gradually shed a phase or phases of the converter at light loads, instead of abruptly shutting it down. This is done by decreasing the duty cycle of the phase gradually to zero. In this thesis, a moving average model of the ramp control technique is constructed and the slope required for this technique is calculated on the basis of different parameters. The performance of the ramp control technique is also compared with the various conventional methods proposed in literature and it has been proved analytically and through simulation results that the ramp control technique has better dynamic performance when compared to the conventional methods.

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1. INTRODUCTION

1.1 MULTIPHASE CONVERTERS

Multiphase converters can be defined as a parallel combination of 'N' DC-DC converters, with a phase difference of 360^0/N in the output current of the adjacent converters. Multiphase converters are also known as interleaved converters. The main focus of this thesis is a multiphase Buck converter.

A simple Buck converter is the building block of a multiphase Buck converter and is as given in Figure 1.1.

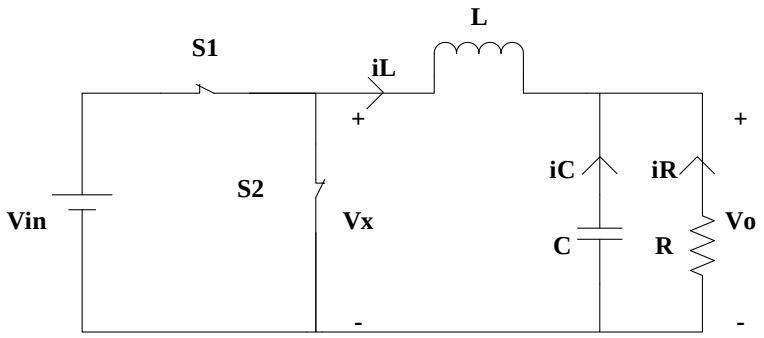

Figure 1.1 Buck converter schematic

One of the major challenges in this converter is sizing of the inductor L. A greater value of L reduces the ripple current Δi_L of the inductor, as seen in equation 2.10 of reference [1], but such an inductor will also slow down the response time of the converter. A smaller value of L, on the other hand, gives a faster response time but increases the ripple current. Hence the sizing of the inductor is always a trade-off in a simple converter. And also the current carrying capacity of a simple converter is limited by the input voltage of the converter.

One solution to the challenges faced by simple converters is a multiphase converter. Multiphase converters have a fast response and also a reduced value of ripple

current for smaller size of the inductor L. This reduced ripple current is attributed to the ripple cancellation effect due to the phase difference between adjacent converters and Figure 1.2 from reference [4], illustrates the ripple cancellation effect as a function of the duty cycle for a multiphase converter. In addition to this, multiphase converters can deliver a larger load current in comparison to simple converters, for a given input voltage. These advantages give multiphase converters an edge over simple converters.

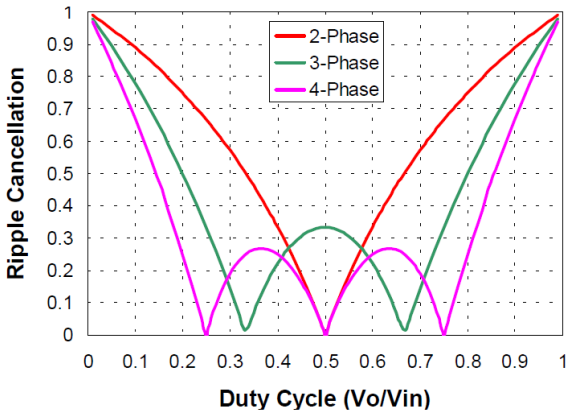

Figure 1.2 Ripple cancellations in a multiphase converter for different number of phases as a function of the duty cycle [4]

1.2 ADVANTAGES OF MULTIPHASE CONVERTERS

Multiphase converters offer numerous advantages over simple converters. Few of them are discussed in this section.

1.2.1 Compact Size. Sizing of the inductors in all individual converters of a multiphase converter is smaller when compared to simple converters. In addition to this, the load current of a multiphase converter is divided equally between all individual converters, thus reducing the size of the switches used in individual converters.

1.2.2 Reduction in Ripple Current. Ripple cancellation effect in multiphase converters reduces the ripple current at both the input and the output of the converter. This reduces the output ripple voltage as well.

1.2.3 Increase in Efficiency. At nominal loads, efficiency of a multiphase converter is greater than that of a simple converter. Efficiency of a converter is a function of its losses. Smaller the losses, greater is the efficiency of the system. The calculation of losses in a simple converter and a multiphase converter are illustrated by the equations given below. The formula for calculating the losses in any system is given by I^2R where 'I' is the current flowing through the system and 'R' is the parasitic resistance of the system. In a two-phase converter, the total current 'I' of the system gets divided equally between the two phases. Assuming constant parasitic resistance 'R' in both the converters, the losses in the individual converters is given by $(I/2)^2 R$ and the total losses in the two-phase converter is given by $I^2R/2$. It is obvious that the efficiency of a multiphase converter is greater than that of a simple converter.

1.2.4 Increased Current Carrying Capacity. For a given input voltage, a multiphase converter can deliver a much larger load current when compared to a simple converter.

1.3 CHALLENGES OF A MULTIPHASE CONVERTER

There are a lot of challenges in the implementation of a multiphase converter- current sharing between the different phases, complex control architecture- to name a few. But the biggest drawback is its poor efficiency at light load condition. This drawback forms the core of this thesis and different techniques to overcome it are discussed in the subsequent sections.

2. MATHEMATICAL MODEL OF A MULTIPHASE BUCK CONVERTER

2.1 INTRODUCTION

Mathematical model of a system can be defined as the description of any system in mathematical language. These models make it easy to understand the working of any system and are important in the analysis of the dynamics of the same.

For example, the mathematical model of a single phase Buck converter in Figure 1.1 is derived as given below. From the Kirchhoff's Voltage Law, it is known that,

$$V_L = V_X - V_O - i_L R_L \tag{1}$$

And from the basic inductor equation, it is known that,

$$V_L = L\frac{di_L}{dt} \tag{2}$$

$$i_L = \frac{1}{L}\int i_L dt \tag{3}$$

V_X in equation (1) is a variable term, which is V_{IN} when switch S is ON and '0' when switch S is OFF. This switching state is denoted as 'SS' in this text. Therefore, V_X can be rewritten as given below:

$$V_X = V_{IN} SS \tag{4}$$

Equations (1), (2), (3) and (4) constitute the first set of equations. Now, from Kirchhoff's Current law, it is known that,

$$i_C = i_L - i_R \tag{5}$$

And from the basic capacitor equation, it is known that,

$$i_C = C\frac{dV_C}{dt} \tag{6}$$

$$V_O = V_C = \frac{1}{C}\int i_C dt \tag{7}$$

Equations (5), (6) and (7) constitute the second set of equations. These set of equations, together, constitute the mathematical model of the Buck converter.

One platform used for constructing the mathematical model of any system is Simulink. Simulink is a software tool developed by MathWorks to model, simulate and analyze dynamic systems. It has a set of pre-defined math blocks which can be used to construct mathematical model of any system. The main aim of this section is to model and simulate a two-phase, interleaved Buck converter in Simulink which includes designing a closed loop voltage or current mode control and a current sharing control for the same. These form the focal points of the rest of the section.

2.2 CLOSED LOOP MODEL OF MULTIPHASE CONVERTER

A closed loop control is a feedback control system where the responses are measured, compared and fed back to drive the system and modify the responses to be as close as possible to the desired response. A closed loop control for a Buck converter can be illustrated by the Figure 2.1 given below.

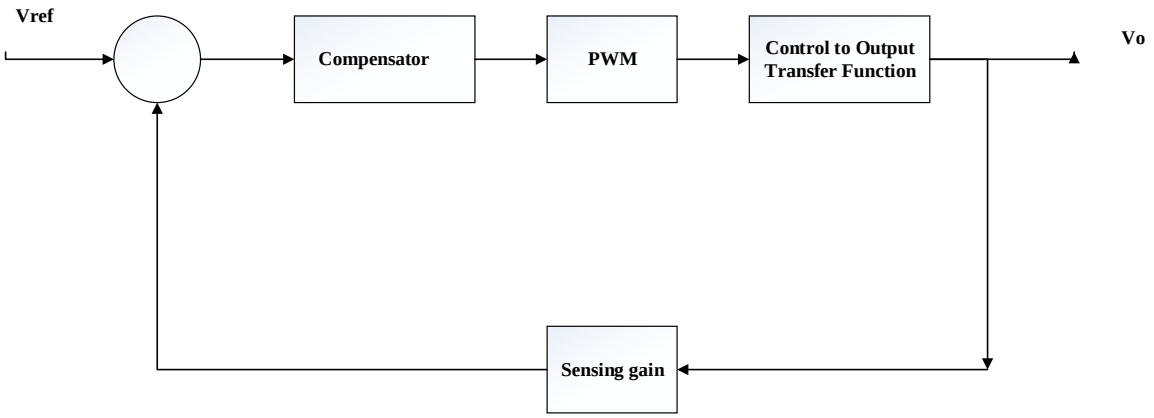

Figure 2.1 Closed loop control schematic of a Buck converter

From section-8 of reference [1], the control to output transfer function is derived as follows:

$$\text{Control to output transfer function} = G(s) = \frac{V_{IN}}{s^2 LC + sRC + 1} \tag{8}$$

The transfer function of PWM is equal to the reciprocal of the magnitude of the external ramp value in PWM control, which is taken as 5 V in this case. The circuitry of the PWM control is discussed in the subsequent sections.

The value of V_{REF}, for the control designed here, is taken as 2.45 and hence the feedback gain, H(s), will be $2.45/V_O$. Now, a compensator, $G_c(s)$ needs to be designed so as to ensure the stability of the system as a whole. The design of this compensator, PWM circuit, output to control model is discussed in the following sub sections.

There are two converter configurations of a two-phase converter which are analyzed in this thesis. These configurations are obtained on the basis of the rising and falling slopes of the inductor current in the system. The rising slope of the

inductor current is $\frac{V_{IN}-V_O}{L}$ while the falling slope of the inductor current is $\frac{V_O}{L}$. Converter-1's ratings are such that the rising slope of the current is greater than its falling slope while converter-2's ratings are such that the rising slope of the current is less than its falling slope. The specifications of both the converters are as given below:

Converter-1		Converter-2	
V_{IN}	= 48 V	V_{IN}	= 48 V
V_O	= 12 V	V_O	= 36 V
I_O	= 4 A	I_O	= 4 A
L	= 220 uH	L	= 220 uH
C	= 10 uF	C	= 10 Uf

2.2.1 Output to Control Transfer Function. The output to control model of the converter is an open loop model of the Buck converter. This is modeled in Simulink as shown in the Figure 2.2.

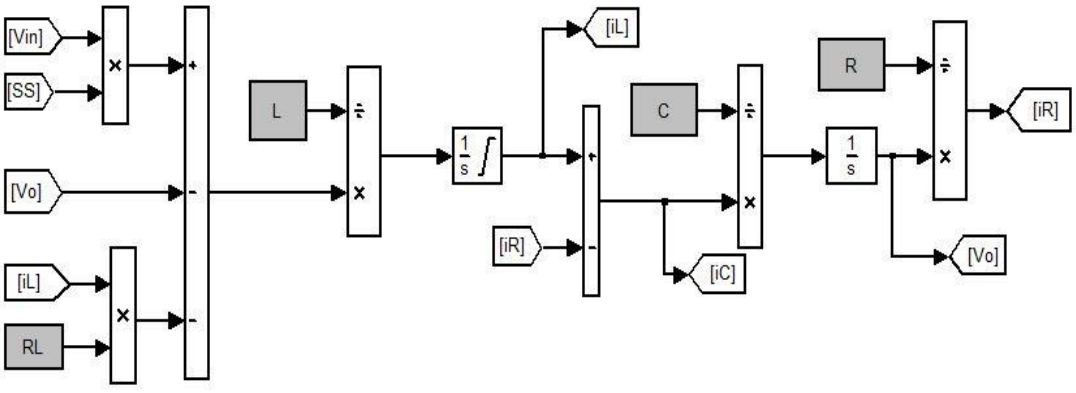

Figure 2.2 Single-phase Buck converter model

This model can be duplicated and edited to give a two phase Buck converter model. The mathematical model of a two phase Buck converter is similar to the single phase one except for equation (5) in the second set of equations which is modified where i_L is replaced by $i_{L1}+i_{L2}$. i_{L1} and i_{L2} represent the inductor currents of the first and the second converter respectively. Hence the two-phase Buck converter model is as given in Figure 2.3.

$$i_C = i_{L1} + i_{L2} - i_R \tag{9}$$

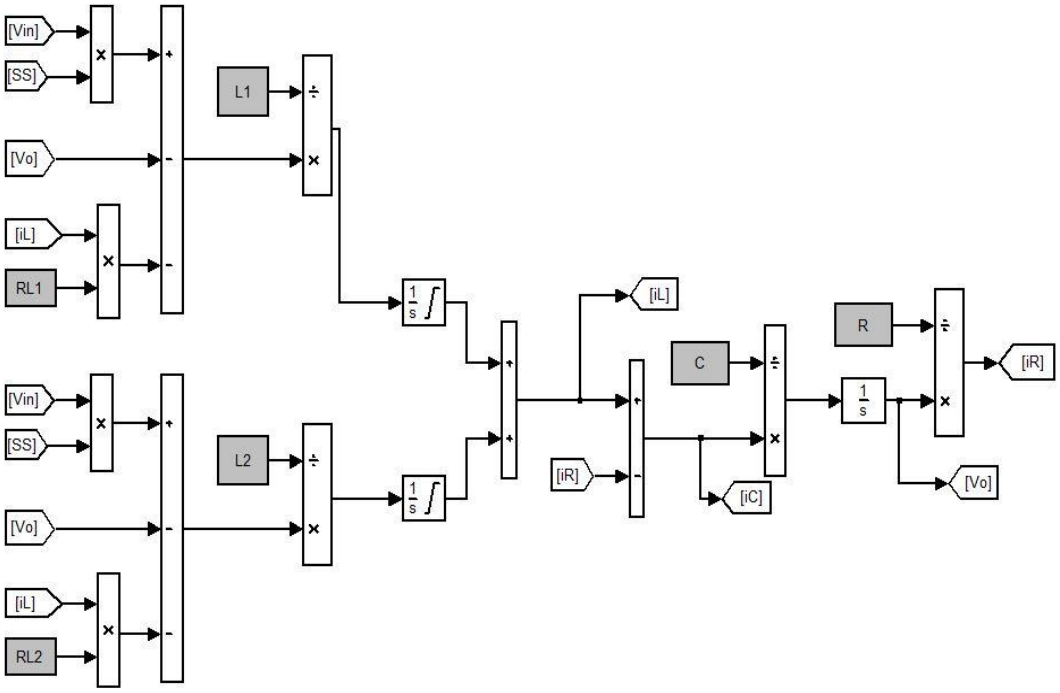

Figure 2.3 Two phase Buck converter model

The only drawback of this model is that it is an open loop model. An open loop control, unlike a closed loop control, is devoid of feedback and hence, makes

the system susceptible to perturbations in the input voltage, output current, and duty cycle. Hence a closed loop control is preferred.

2.2.2 Compensator Design. Very important tools to analyze the stability of any system and design suitable compensators for the same are the Bode plots. Bode plot is the mapping of gain and phase of any open loop transfer function with respect to frequency, plotted on a logarithmic scale. Phase margin observed from these plots play an important role in the compensator design. Bode plots will be extensively used in this section to design the compensator.

Before going into the stability aspect of compensator design, it is important to concentrate on eliminating the steady state error. The input signal V_{REF}, in Figure 2.3, is a step signal and from [2], it is known that to eliminate steady state error in a system with a step input signal, a type-1 compensator is to be used. Thus, the basic compensator used for these converters is going to be $1/s$ i.e. $G_C(s) = 1/s$. Hence the open loop transfer function of the uncompensated or rather the steady state error compensated system is as given below:

$$T(s) = G(s)G_C(s)PWM(s)H(s) \tag{10}$$

$$T(s) = \frac{V_{IN}}{s^2LC + sRC + 1}\left(\frac{1}{s}\right)\left(\frac{1}{5}\right)\left(\frac{2.45}{V_O}\right) \tag{11}$$

In order to design the compensator, for any system, few design rules are followed.
Step1: Choose the bandwidth of the system. Bandwidth determines the response of a system. Higher the bandwidth, quicker is the response of the system. Bandwidth is usually taken to be equal to one fifth of switching frequency of the system which is 20 kHz in this case. In Bode plots, bandwidth is taken to be approximately equal to the gain crossover frequency of the system.
Step 2: Adjust the gain of the compensator according to the bandwidth of the system. At the gain crossover frequency, the gain of the system is usually taken to be unity.

Step 3: Observe the bode plot of the system with new gain and note down the phase margin of the system.

Step 4: Calculate the angular difference between the desired phase margin and actual phase margin of the system. Design an appropriate lead compensator from the steps given in section-9 of reference [1].

The compensators for the two converter configurations are designed separately. Converter 1 is discussed first. The steady state error compensated system is considered initially. A gain, which gives a bandwidth of 20 kHz, needs to be obtained. This gain can be obtained by running the MATLAB program, given below, and for converter-1, the required gain is calculated as 2.24×10^6. The bode plot of the system with this new gain is given in Figure 2.4

```
Vin=48;
Vo=12;
L=220e-6;
C=10e-6;
Io=4;
R=Vo/Io;
w=1/(sqrt(L*C));
Q=R/(L*w);
s=1i*2*pi*20000;
G=(Vin*w^2)/((s)^2+((s*w^2)/(Q*w))+w^2);
H=2.45/Vo;
PWM=1/5;
Gc1=1/s;
T=G*Gc1*H*PWM;
A=abs(T)
K=1/A
```

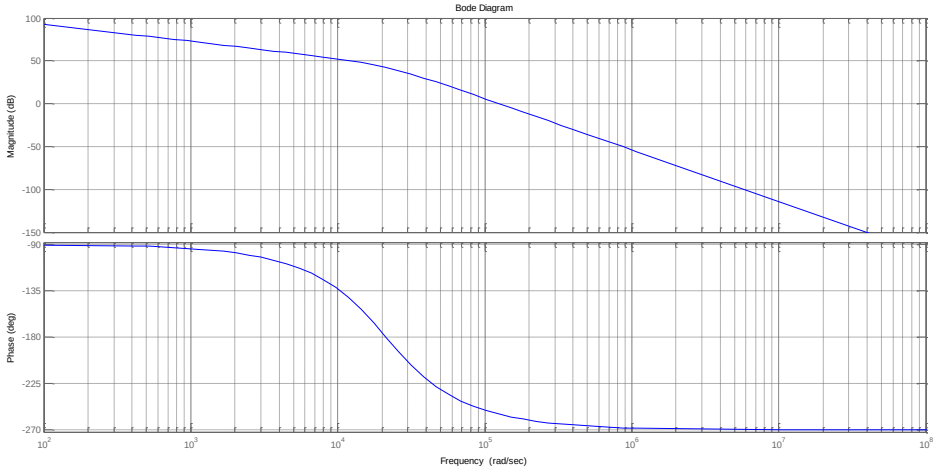

Figure 2.4 Bode plot of the system for BW of 20 kHz (Converter 1)

The phase margin of the system in Figure 2.4 is approximately -75˚ and the required phase margin for the system is 45˚. Hence the total angular compensation to be provided by the lead compensators is 120˚. A single lead compensator can give an angular contribution of 90˚ maximum which means there is a need for two lead compensators in this case, each contributing an angle of 60˚. Based on [2], the lead compensators are designed and hence the final compensator is as given below and the Bode plot for the same is given in Figure 2.5.

$$T(s)=\frac{48}{s^2LC+sRC+1}\left(\frac{165\times10^3}{s}\left(\frac{1+s(33648)^{-1}}{1+s(469299)^{-1}}\right)\left(\frac{1+s(33648)^{-1}}{1+s(469299)^{-1}}\right)\right)\left(\frac{1}{5}\right)\left(\frac{2.45}{12}\right) \quad (12)$$

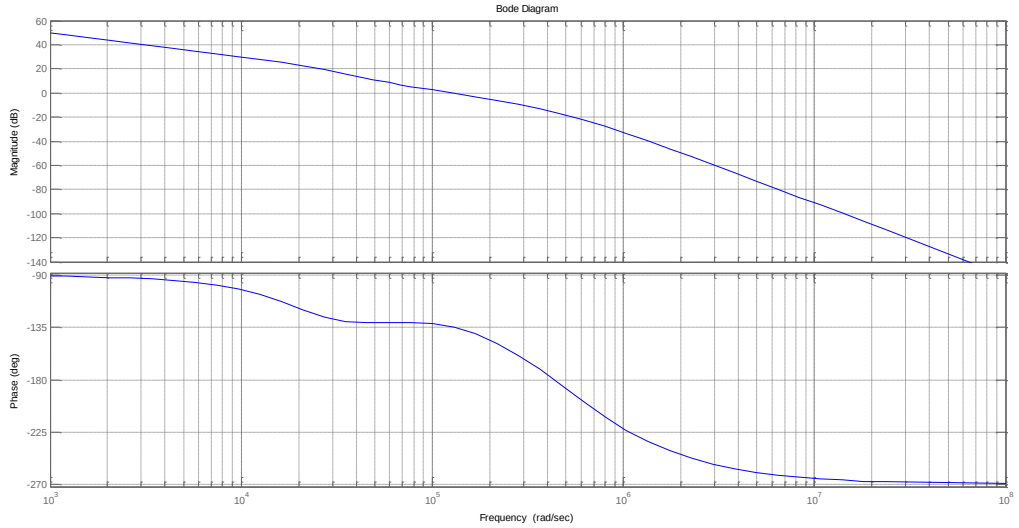

Figure 2.5 Bode plot of the compensated system (Converter 1)

The same process is repeated for converter-2. A new gain needs to be obtained such that the bandwidth of the steady state error compensated system is 20 kHz. This new gain is obtained by the same program, given in the previous paragraph, except that the output voltage is now changed to 36 V. The gain, for converter-2, is obtained as 6.51×10^{6}. Figure 2.6 gives the Bode plot of the new system and it is seen that the phase margin of the system is -85°. Hence an angular contribution of 65°, each, needs to be provided by the lead compensators. The final compensator equation is given below and Bode plot for the same is given in Figure 2.7.

$$T(s)=\frac{48}{s^2LC+sRC+1}\left(\frac{320\times10^3}{s}\left(\frac{1+s(27859)^{-1}}{1+s(567392)^{-1}}\right)\left(\frac{1+s(27859)^{-1}}{1+s(567392)^{-1}}\right)\right)\left(\frac{1}{5}\right)\left(\frac{2.45}{36}\right) \quad (13)$$

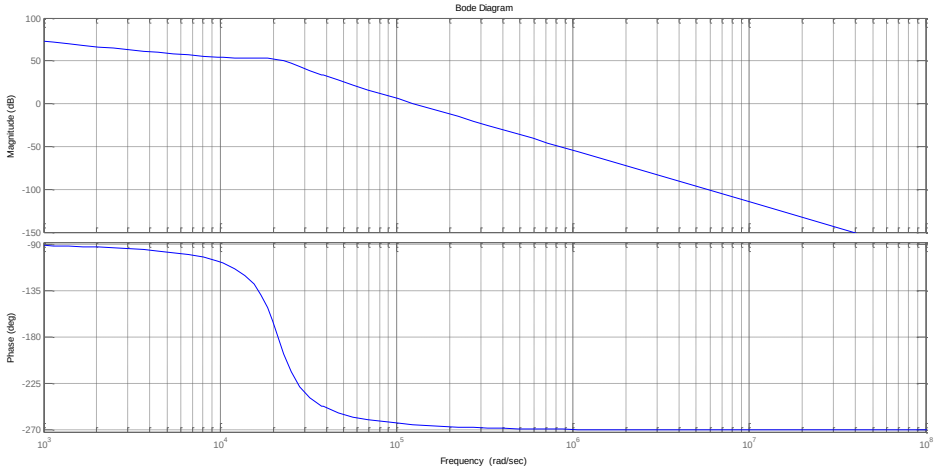

Figure 2.6 Bode plot of the system for BW of 20 kHz (Converter 2)

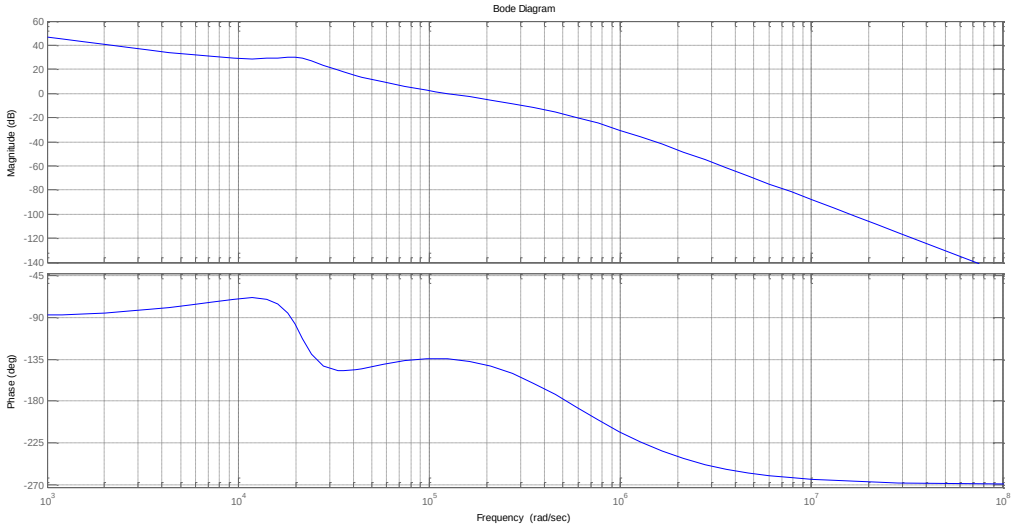

Figure 2.7 Bode plot of the compensated system (Converter 2)

The closed loop system in Figure 2.1, with the exception of PWM block, can be implemented in Simulink using some basic, predefined blocks as shown in Figure 2.8. Figure 2.8 shows converter-1's implementation; converter-2 can be implemented similarly with its transfer function.

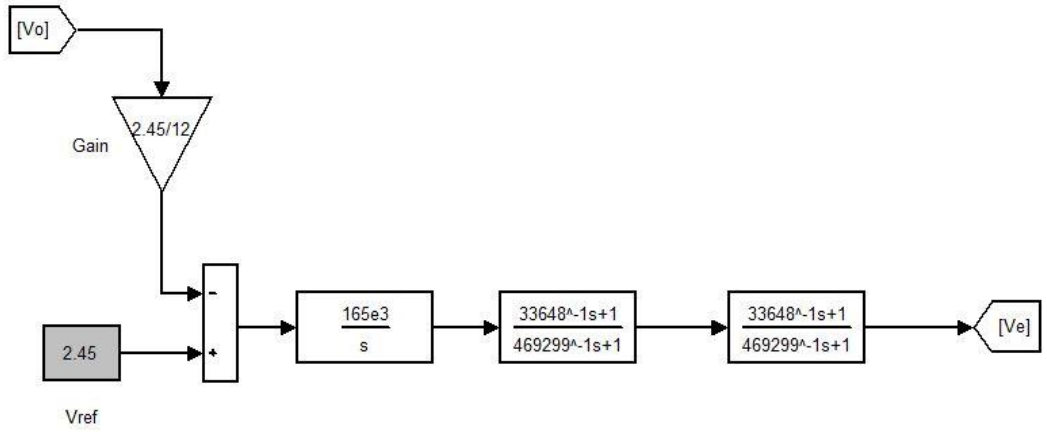

Figure 2.8 Closed loop system implementation in Simulink (Converter 1)

2.2.3 PWM Control Circuit. Duty cycle required for the converter is generated by the PWM circuit shown in the block diagram in Figure 2.1. The type of control determines the PWM circuit used. There are two types of control- Voltage Mode Control (VMC) and Current Mode Control (CMC). In this thesis, Voltage Mode Control is used which is illustrated in Figure 2.9.

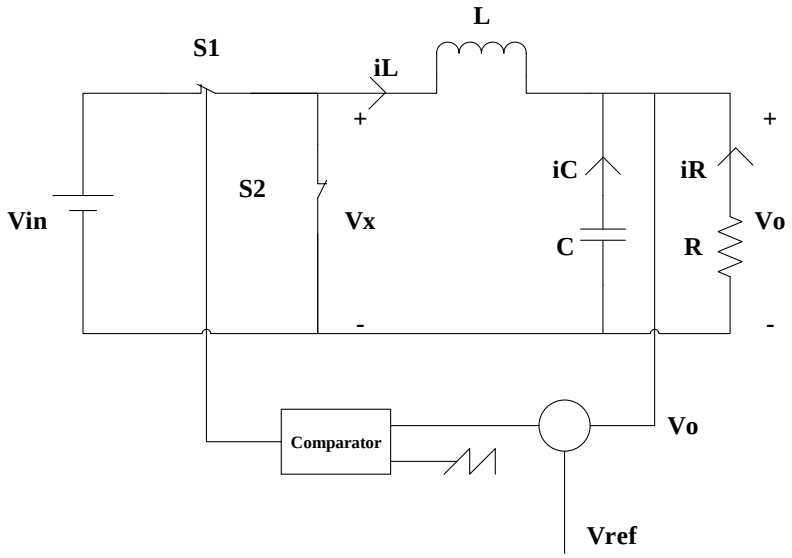

Figure 2.9 Voltage mode control schematic of the Buck converter

This control compares the error voltage with an external ramp. As long as the magnitude of the error voltage is greater than that of the external ramp, switch S1 remains ON and once the magnitude falls below that of the external ramp, switch turns OFF. Figure 2.10 shows the implementation of this circuit in Simulink. The switching signal, generated in this implementation, is used as SS in the mathematical model of the converter in Figure 2.1

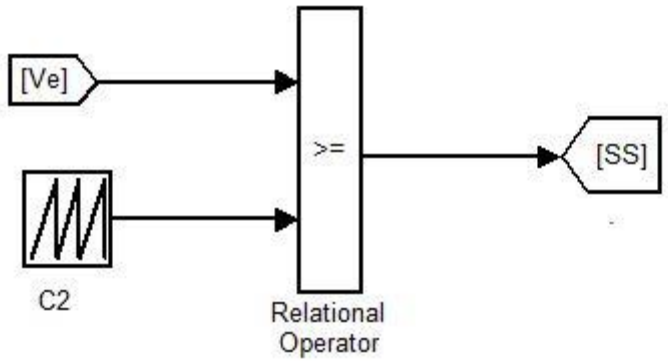

Figure 2.10 VMC control implementation in Simulink

The phase difference between the inductor currents in a multiphase converter is generated by a shift in the external ramp of the PWM circuit. For a two phase converter, a shift of 180° in the external ramp in the second phase of the converter produces the required shift in the inductor current as well.

2.3 CURRENT SHARING IN MULTIPHASE CONVERTERS

Current sharing in parallel systems is a very challenging task. This is because a slight output voltage mismatch can cause large circulating currents in the system and cause the load to be shared unequally between the two modules. There are numerous methods, reference [2],[3], [4] and [5], to obtain accurate current sharing in a system like droop control, master-slave control, democratic control etc. but the most commonly used

techniques for current sharing are the master-slave control and the democratic control techniques.

For the multiphase converters, discussed here, master-slave technique of current sharing, as in [3], is used with a slight modification. In the conventional master-slave control, one module is chosen as the master module and all the other modules are considered as the slave modules. It is only the master module's output voltage that is fed back and compared with the reference voltage to generate the required error voltage. All the slave modules use this error voltage to generate the required duty cycle. This is illustrated in the Figure 2.11 from reference [3]. The one disadvantage in this method is that, should the master fail, the entire system collapses.

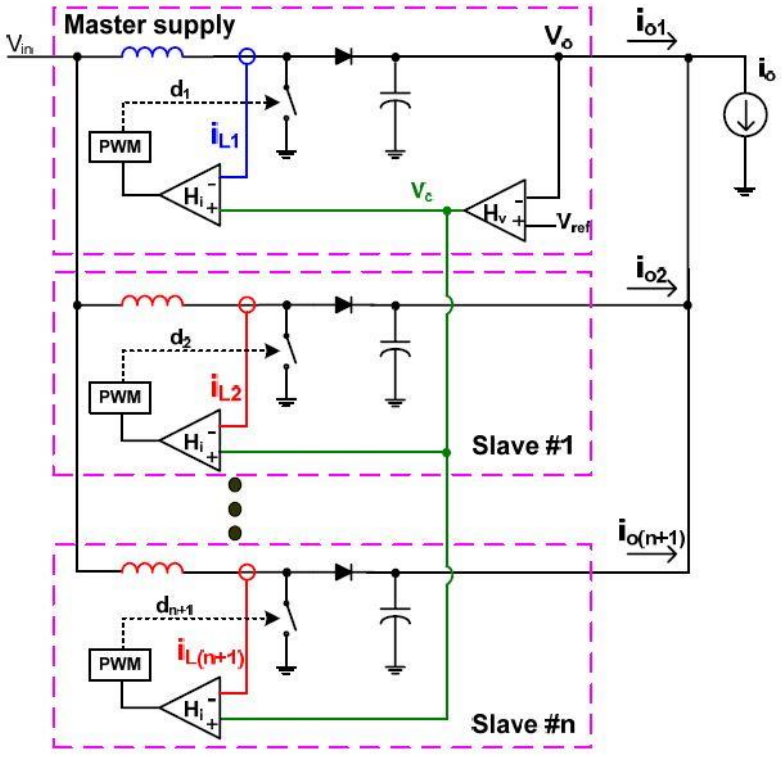

Figure 2.11 Master-slave control of the Buck converter [4]

In this thesis, master-slave control is used but there is no single module defined as the master. The output voltage of the system as a whole is fed back and compared to generate the error voltage. This error voltage is used by all the modules to generate their respective duty cycles.

Figure 2.3, 2.8, 2.10 and 2.11 together constitute the mathematical model of closed loop, two-phase Buck converter in Simulink. This model is used throughout the thesis to analyze the behavior of multiphase converters.

3. PHASE SHEDDING IN MULTIPHASE CONVERTERS

3.1 INTRODUCTION TO PHASE SHEDDING

Efficiency, in multiphase converters, is a function of both switching losses and conduction losses in the system. Switching losses can be defined as the losses created in the system due to high voltage and current experienced by the switch when transitioning from on to off state and vice versa while conduction losses are caused due to the losses in the internal passive components of the system. The conduction losses in multiphase converters are reduced greatly in comparison to the simple Buck converter but the switching losses gain prominence due to the greater number of switches present. Switching losses are insignificant at nominal to heavy loads but at light loads, switching losses become significant, thus reducing the efficiency of the multiphase converter system as a whole.

One way to reduce switching losses, at light loads, is to decrease the number of switches which are in operation i.e. reducing the number of phases in operation. This procedure is known as phase shedding. Therefore, phase shedding is defined as the process of being able to shed phases, when the load current decreases below a certain limit. The vice versa process is defined as phase adding. One major advantage of phase shedding is the increase in the efficiency of the converter at light loads. This is illustrated in Figure 3.1 from reference [8]. The figure shows the efficiency graphs, right from a single phase converter to a four phase converter. It is observed that at light loads, as the number of phases increases, the efficiency of the system deteriorates. The dotted blue line in the figure denotes the efficiency of a four phase converter with the phase shedding concept implemented. It is seen that the efficiency of the system greatly improves.

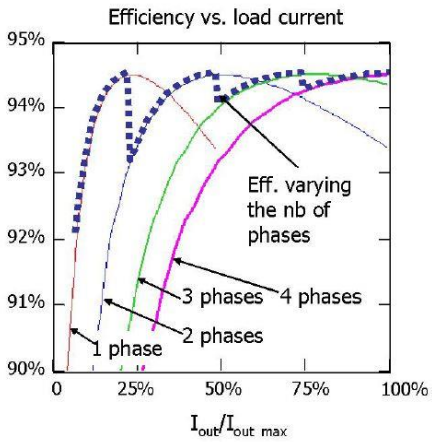

Figure 3.1 Efficiency graphs of a multiphase converter for different phases [8]

There are numerous challenges in implementing the phase shedding and phase adding technique. One major challenge is the distorted transient behavior of the system during these processes which is reflected in its output voltage. This thesis proposes a unique technique to address this issue and it is discussed in the subsequent sections.

3.2 PHASE SHEDDING MODEL

Generally in multiphase converters, phase shedding and phase adding control is obtained by measuring the total load current of the system, i.e., if the load current goes below or above a certain threshold, the number of phases in operation is decreased or increased respectively. For example, in a three phase system, a threshold can be set such that for a current range of 0-100 A, one phase operates, for 100-200 A, two phases operate and for 200-300 A, three phases operate. But in this thesis, this control in the system is assumed to be external and independent of the load current. This makes the study of the transient behavior of the system, during the process of phase change, easier without any influence of the load transients.

Phase shedding is implemented in Simulink using a simple step signal block, C_2. C_2 is programmed to output a 1 as long as the phase needs to operate and once the phase needs to be shed, it is programmed to output a 0. This C_2 is multiplied with the error signal V_e, shown in Figure 2.10, to generate the required phase shedding effect. In the

two-phase converter, discussed in section-2, it is assumed that it is the second phase of the converter which is to be shed or added. Figure 3.2 shows the PWM control model for the same. The first and second phases of the converter are denoted as phase-1 and phase-2 respectively throughout the section.

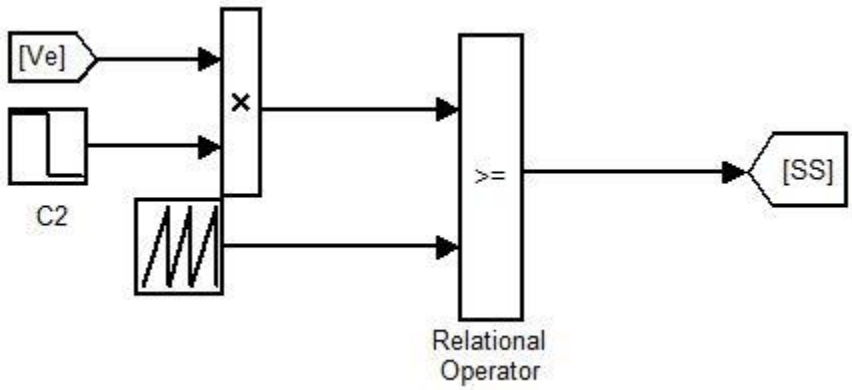

Figure 3.2 Phase shedding PWM control implementation in Simulink

3.2.1 Converter-1. Figures 2.3, 2.8, 2.10, 3.2 and 2.11, together, form the mathematical model of the two-phase, phase shedding incorporated Buck converter. This model is simulated in Simulink, for converter-1 (which was described in section-2) over a period of 0.2 s, where the second phase is shed at 0.06 s and then added at 0.12 s. The results of this simulation are shown by the figures given below.

For phase shedding, the phase-2 current, as observed in Figure 3.4, drops to zero at 0.06 s with a falling slope of $-V_O/L$, i.e. $-12/L$, and it takes approximately four switching cycles for it to reach zero. From close observation of Figure 3.4, it is seen that the phase-1 current undergoes no change in the first switching cycle and this causes the initial dip in the total current of the system, as in Figure 3.6. This perturbation in the total current is reflected in the output voltage (in figure 3.12) as well because V_O is a function of the total inductor current as seen in the equation (11).

$$V_O = i_L R_L \tag{11}$$

Phase adding in converter-1 is comparatively smooth, as observed from the figures of the phase currents, total current and the output voltage as in Figures 3.5, 3.7 and 3.13 respectively. The only major drawback in phase adding is the large amount of time required to attain equal current sharing, which is addressed in the subsequent sections. Figure 3.8, 3.9, 3.10 and 3.11 illustrate the behavior of the error voltage of phase-1 and phase-2 of converter-1. An important point to note here is the instantaneous drop in the error voltage of phase-2, during the process of phase change.

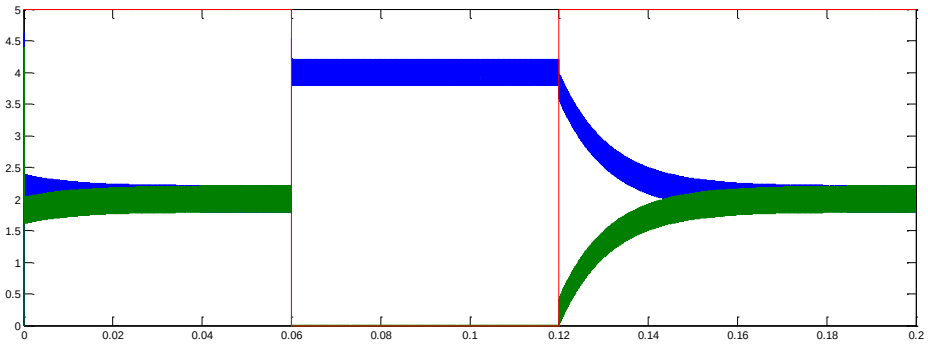

Figure 3.3 Phase currents in converter-1

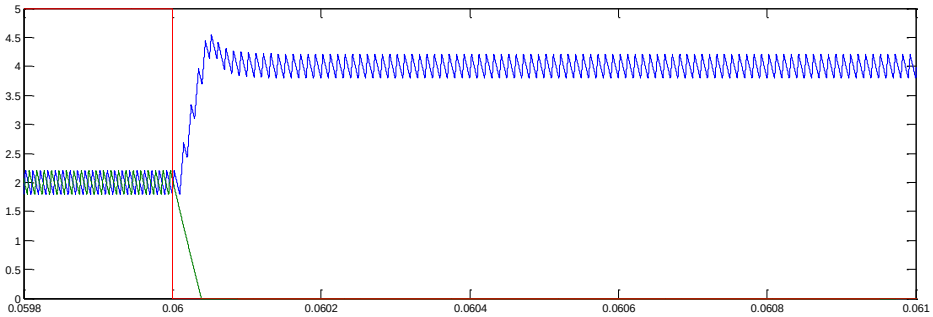

Figure 3.4 Zoomed in phase currents in converter-1 at the point of phase shedding

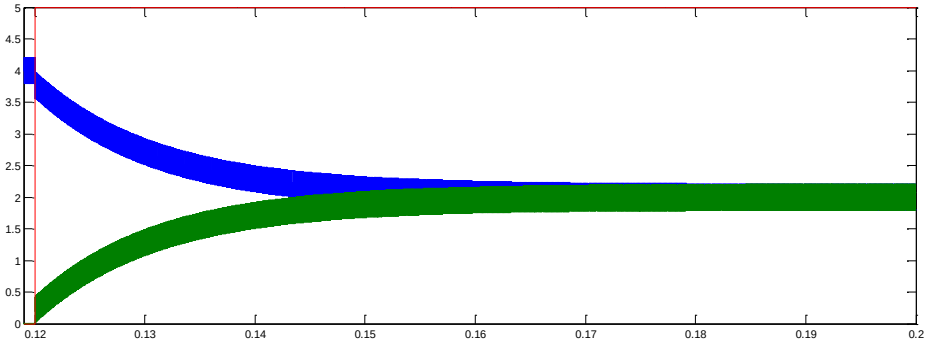

Figure 3.5 Zoomed in phase currents in converter-1 at the point of phase adding

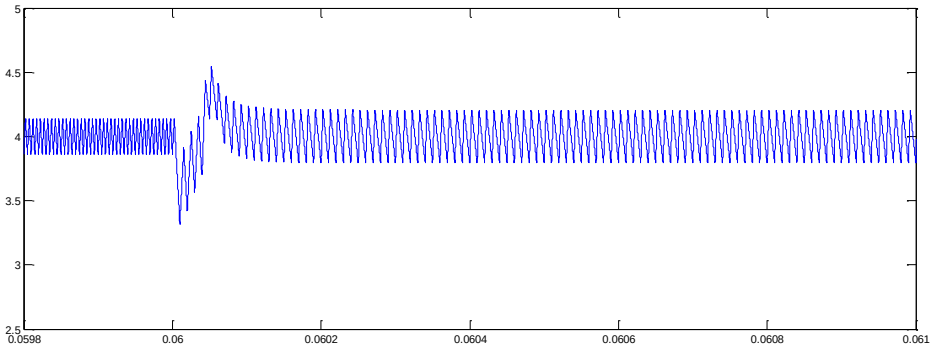

Figure 3.6 Total current in converter-1 at the point of phase shedding

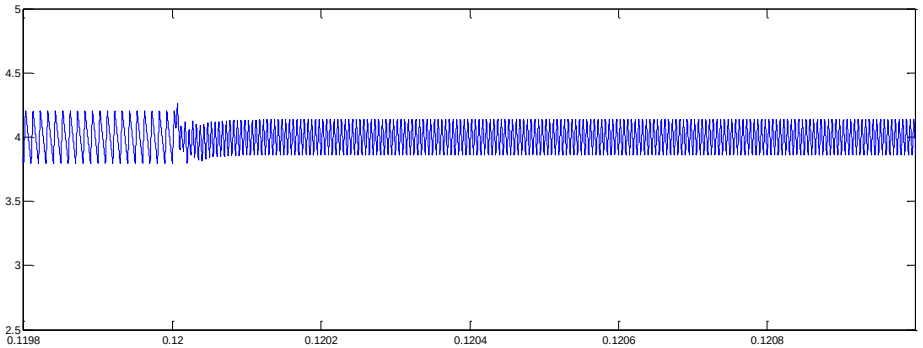

Figure 3.7 Total current in converter-1 at the point of phase adding

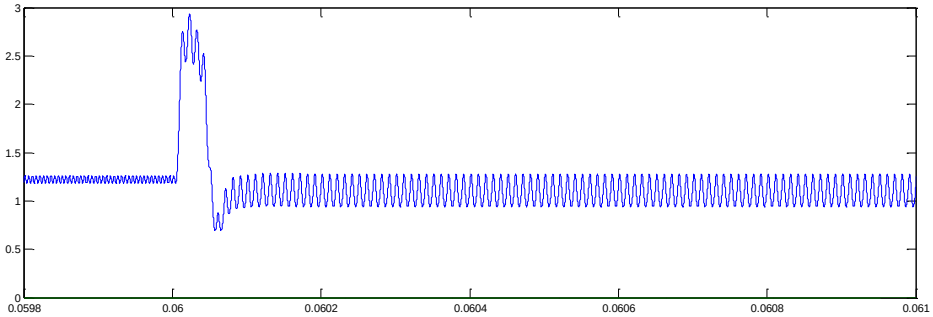

Figure 3.8 Phase-1's error voltage in converter-1 at the point of phase shedding

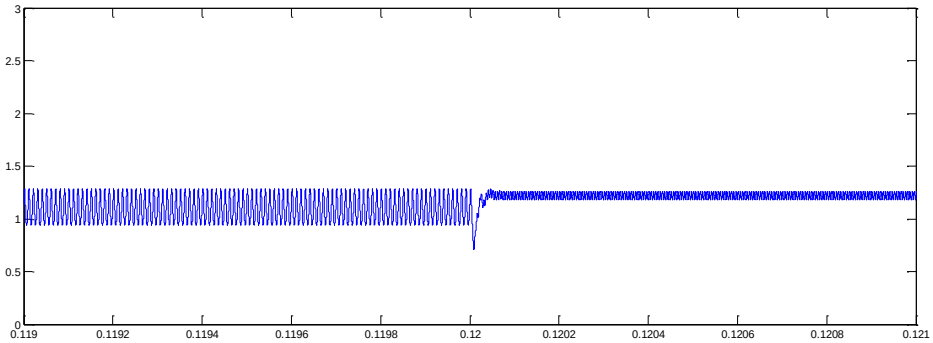

Figure 3.9 Phase-1's error voltage in converter-1 at the point of phase adding

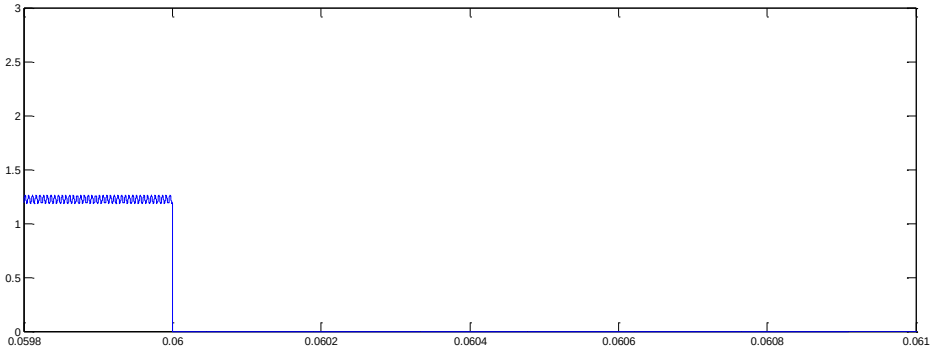

Figure 3.10 Phase-2's error voltage in converter-1 at the point of phase shedding

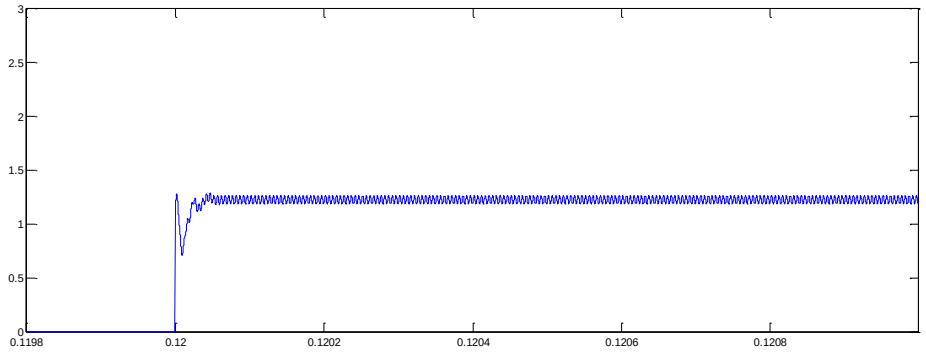

Figure 3.11 Phase-2's error voltage in converter-1 at the point of phase adding

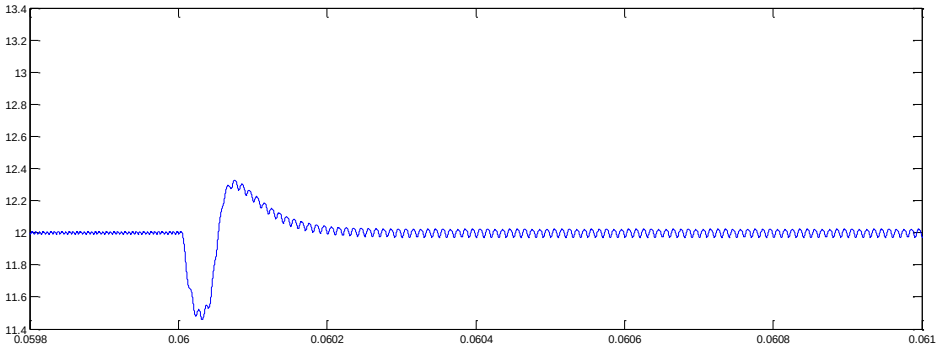

Figure 3.12 Output voltage of converter-1 at the point of phase shedding

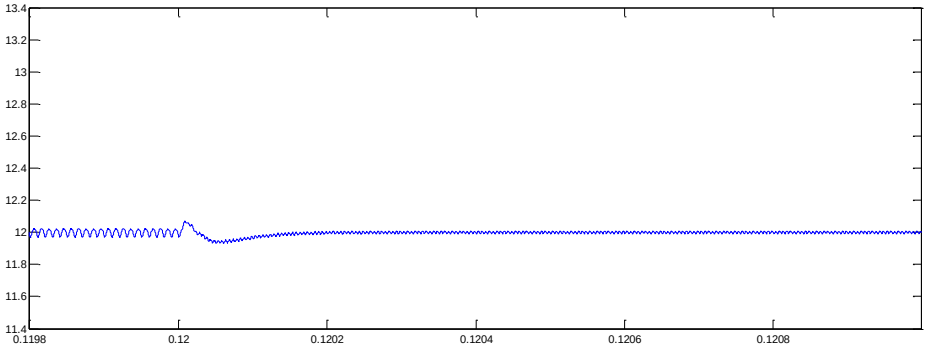

Figure 3.13 Output voltage of converter-1 at the point of phase adding

3.2.2 Converter-2. Converter-2 (which was described in section-2) is simulated under the same conditions as in the previous section and the results of this simulation are as given below. Table 3.1 and 3.2 tabulate the transient rise and drop in converter-1 and converter-2 in terms of percentage of the output voltage, during the process of phase shedding and phase adding respectively.

From Table 3.1, it is observed that the percentage voltage drop in converter-2 is much larger than that in converter-1. This can be attributed to the fact that the falling slope in converter-2, $-36/L$, is much larger than its rising slope, $12/L$. Thus the phase-2 current of converter-2 goes to zero in little more than one switching cycle and it is difficult for the phase-1 current to match it with its rising slope, as observed in Figure 3.15. This causes a huge dip in the total current which is again reflected in the output voltage as in Figure 3.17 and Figure 3.23 respectively. Phase adding, on the other hand, is a smooth process as observed from the Figures 3.16, 3.18 and 3.24 with negligible transients as observed in the Table 3.2. The instantaneous drop and rise of the phase-2's error voltage is also noted here as in Figures 3.21 and 3.22.

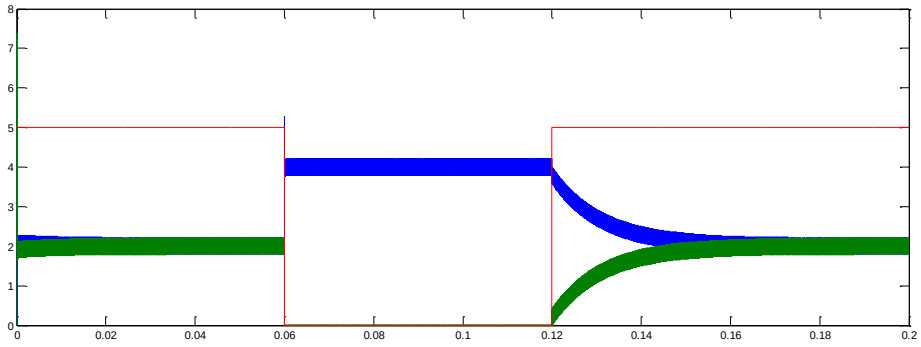

Figure 3.14 Phase currents in converter-2

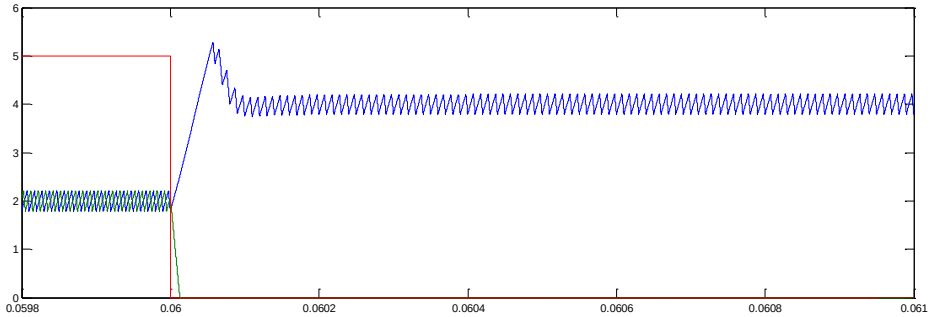

Figure 3.15 Zoomed in phase currents in converter-2 at the point of phase shedding

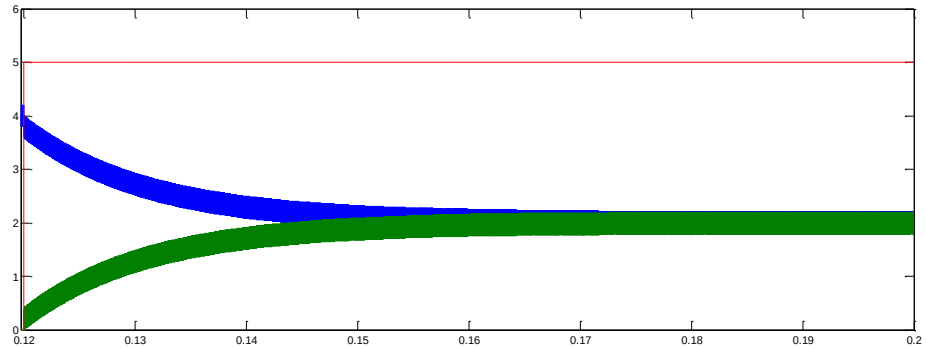

Figure 3.16 Zoomed in phase currents in converter-2 at the point of phase adding

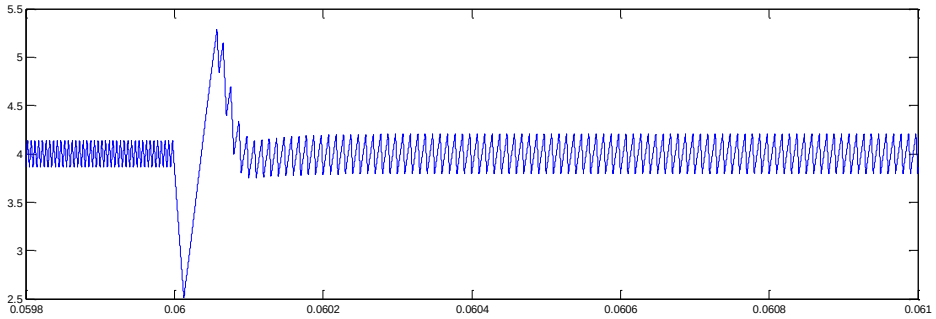

Figure 3.17 Total current in converter-2 at the point of phase shedding

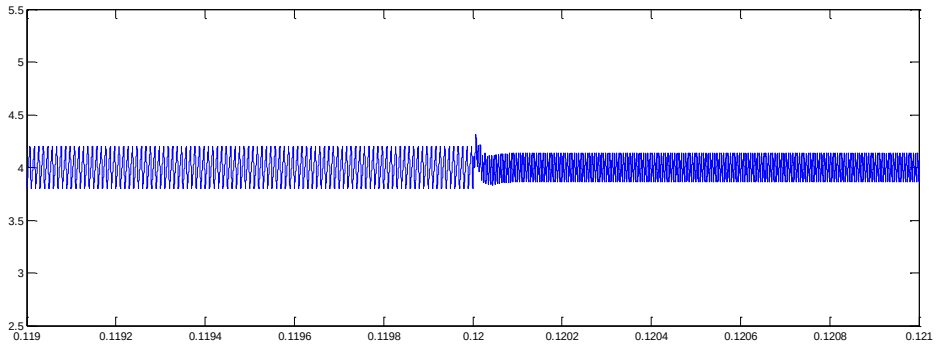

Figure 3.18 Total current in converter-2 at the point of phase adding

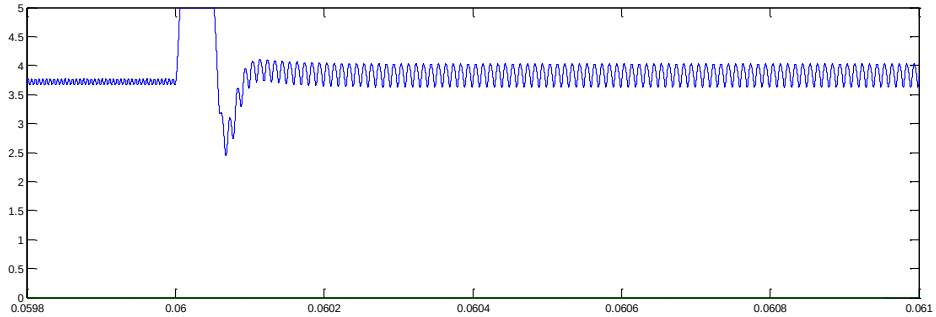

Figure 3.19 Phase-1's error voltage in converter-2 at the point of phase shedding

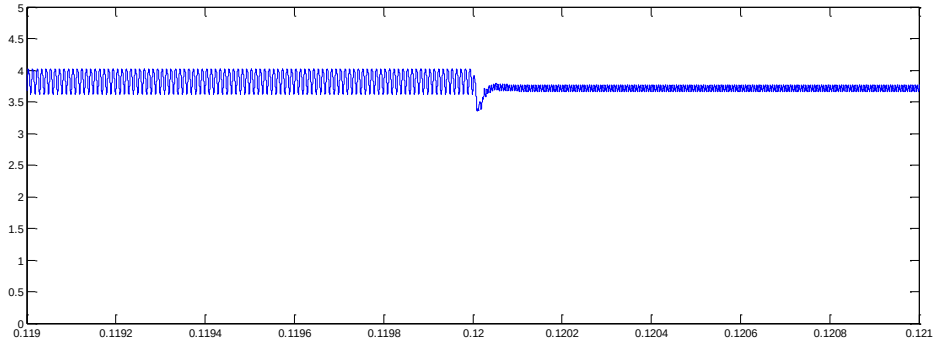

Figure 3.20 Phase-1's error voltage in converter-2 at the point of phase adding

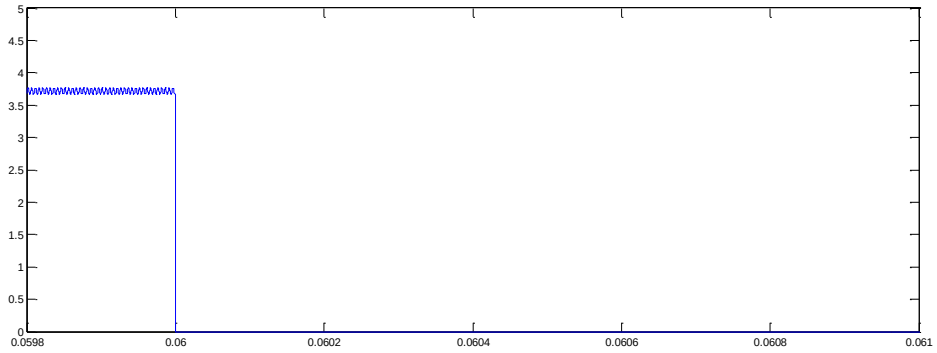

Figure 3.21 Phase-2's error voltage in converter-2 at the point of phase shedding

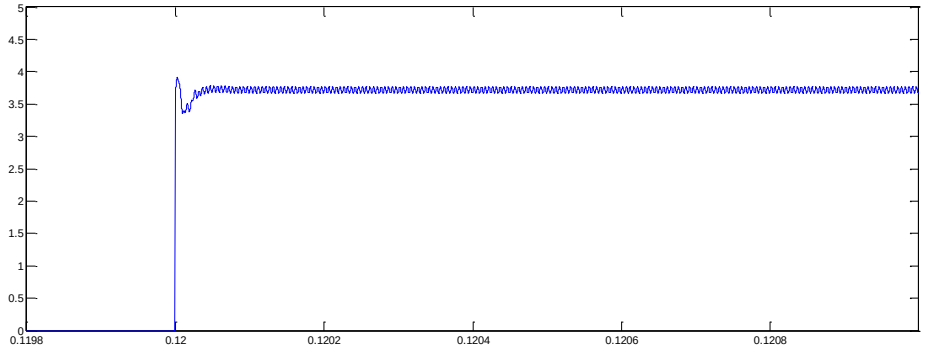

Figure 3.22 Phase-2's error voltage in converter-2 at the point of phase adding

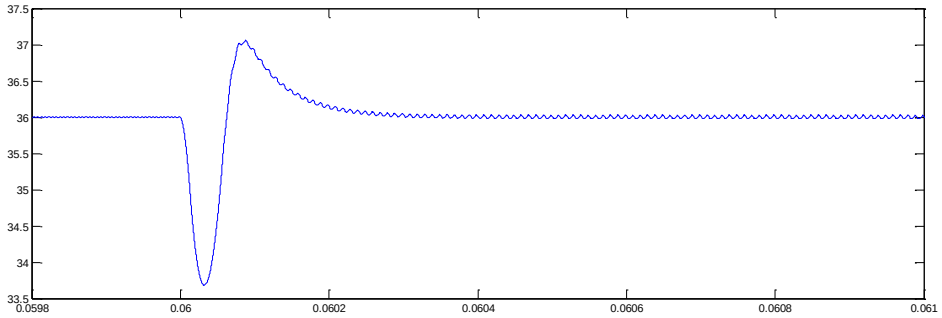

Figure 3.23 Output voltage of converter-2 at the point of phase shedding

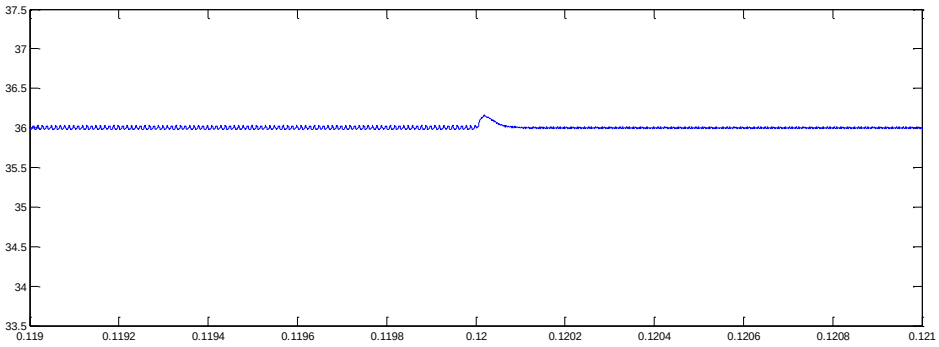

Figure 3.24 Output voltage of converter-2 at the point of phase adding

Table 3.1 Rise and dip in the output voltage for the two converter configurations during the phase shedding process

Converter Configuration	Type of control	Percentage output voltage dip	Percentage output voltage rise
Converter-1	Simple	4.58	2.5
Converter-2	Simple	6.38	3.33

Table 3.2 Rise and dip in the output voltage for the two converter configurations during the phase adding process

Converter Configuration	Type of control	Percentage output voltage dip	Percentage output voltage rise
Converter-1	Simple	0.833	0.416
Converter-2	Simple	-	0.694

3.3 CONVENTIONAL PHASE SHEDDING TECHNIQUES

Numerous techniques have been proposed to improve the transient behavior of a multiphase converter during phase change as in references [6]-[11]. One such technique is the 'feed forward' technique proposed in [6]. This reference proposes to temporarily increment the duty cycle of the phase in on state, for phase shedding process, and the phase to be transitioned to on state, for the phase adding process, by δ_{SS}. This value of δ_{SS} is to be calculated by the equations given below. Equation (13) is the value of δ_{SS} for phase shedding process while equation (14) is the value of δ_{SS} for phase adding process. D represents the standard duty cycle in equation (13) and (14).

$$\delta_{SS} = D\frac{N_{TURNED-OFF}}{N_{ON-AFTER-PS}} \tag{13}$$

$$\delta_{SS} = D\frac{N_{ON-BEFORE-PS}}{N_{TURNED-ON}} \tag{14}$$

This section sees the implementation of phase change in the converters using this technique. The feed forward duty cycle for the two-phase converters-converter-1 and converter-2- can be calculated using equations (13) and (14). Thus, δ_{SS} for converter-1 is calculated as 0.25 and δ_{SS} for converter-2 is calculated as 0.75. This makes the incremented duty cycle 0.5 and 1.5 for converter-1 and converter-2 respectively. Since duty cycle cannot have a value greater than 1, the incremented duty cycle for converter-2 is taken as 1.

This technique can be implemented in Simulink using an OR block, where one input to the OR block is the output of the PWM controller while the other input is a phase shifted, pulse signal whose pulse width is equal to the incremented duty cycle value. The second input is applied only for a certain period of time. Figure 3.25 and 3.26 show this control, implemented in Simulink, for phase-1 and phase-2 of a two-phase converter. In a

two phase converter, feed forward control is implemented on phase-1 for the phase shedding process and phase-2 for the phase adding process.

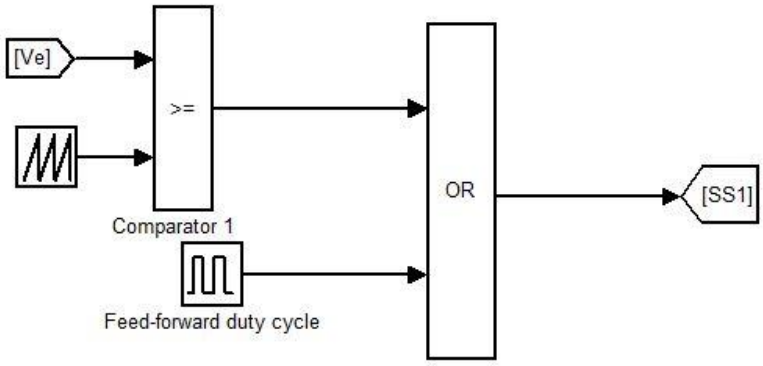

Figure 3.25 Feed-forward control implementation for phase-1 in Simulink

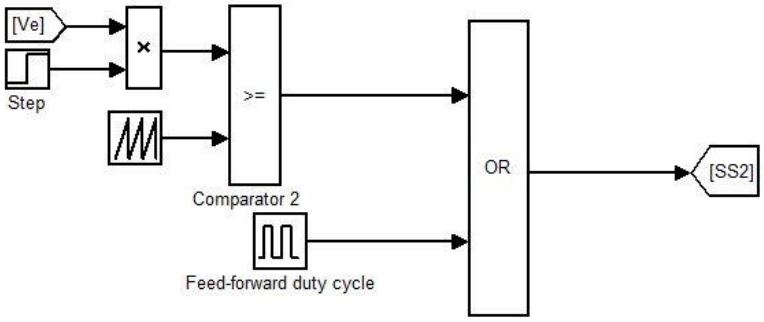

Figure 3.26 Feed-forward control implementation for phase-2 in Simulink

3.3.1 Converter-1. The value of δ_{SS} for converter-1 is calculated as 0.25 and hence second input of this converter is a phase shifted, pulse signal with a pulse width of 25%. For the phase shedding process, this pulse signal is implemented till the phase-2 current reaches zero and for the phase adding process, the pulse signal is implemented till the phase-2 current reaches the average inductor current value. These time periods are approximated to be about four switching cycles. Thus, the feed forward model of

converter-1, implemented using the PWM controllers in Figure 3.25 and 3.26, is simulated over a period of 0.2s and the second phase is shed at 0.06 s and added again at 0.12 s.

Figures 3.32 and 3.33 show the zoomed in view of the switching state of the phase-1 and phase-2 respectively and it is observed that, as per the feed forward technique, for a period of four switching cycles, duty cycle is increased to 0.5. Figure 3.4 and 3.28 are compared and it is observed that in feed forward control, the phase-1 current rises faster and immediately after the phase shedding begins. This eliminates the initial dip in the total current as in Figure 3.31, which is again reflected in the output voltage as well, as in Figure 3.34. However, for the phase adding process, though the feed forward technique decreases the time taken to attain equal current sharing as observed in Figure 3.27, it is observed from the output voltage graphs, in Figure 3.12 and 3.35, that the transient behavior deteriorates. This renders the feed forward technique largely ineffective for the phase adding process.

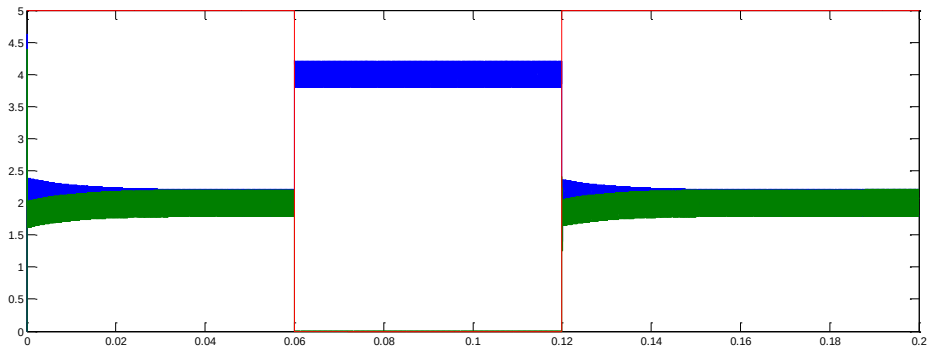

Figure 3.27 Phase currents of converter-1 in a feed-forward control system

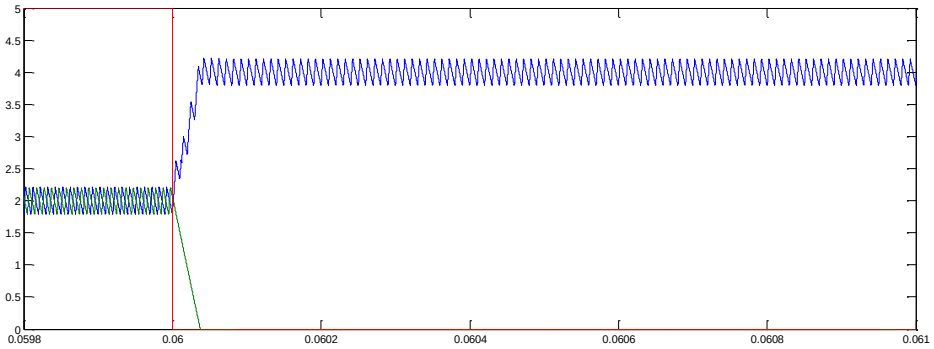

Figure 3.28 Zoomed in phase currents of converter-1 in a feed-forward control system

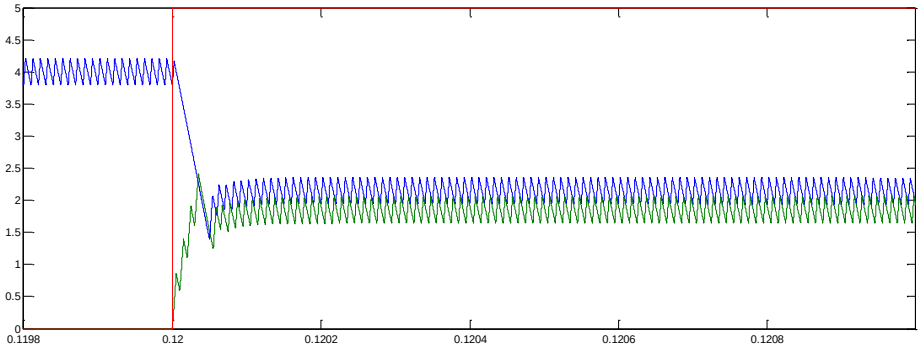

Figure 3.29 Zoomed in phase currents of converter-1 during phase adding in a feed-forward control system

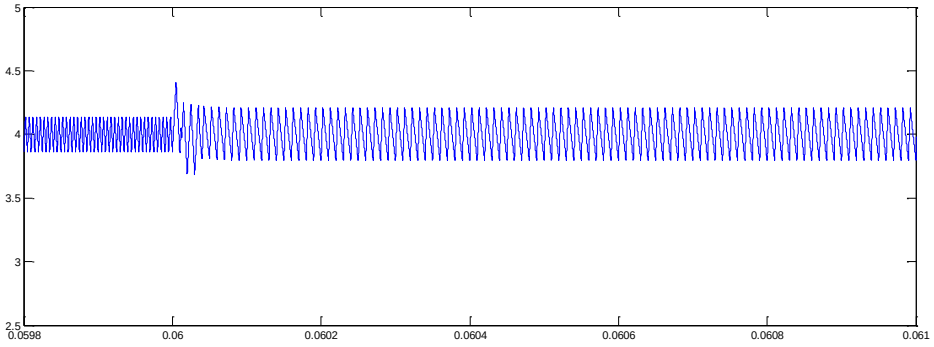

Figure 3.30 Total current of converter-1 during phase shedding in a feed-forward control system

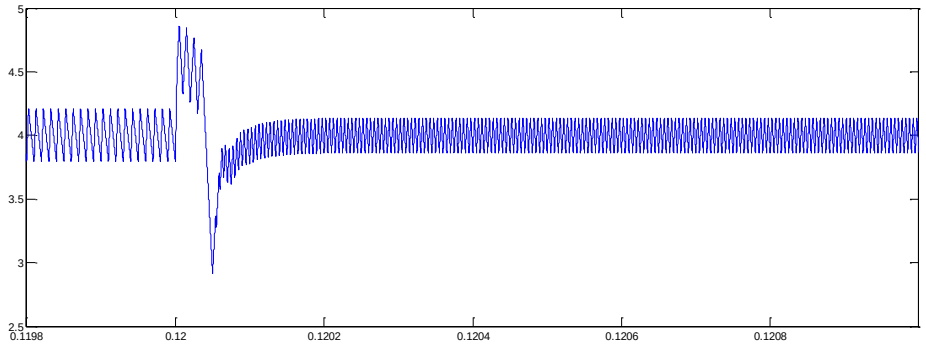

Figure 3.31 Total current of converter-1 during phase adding in a feed-forward control system

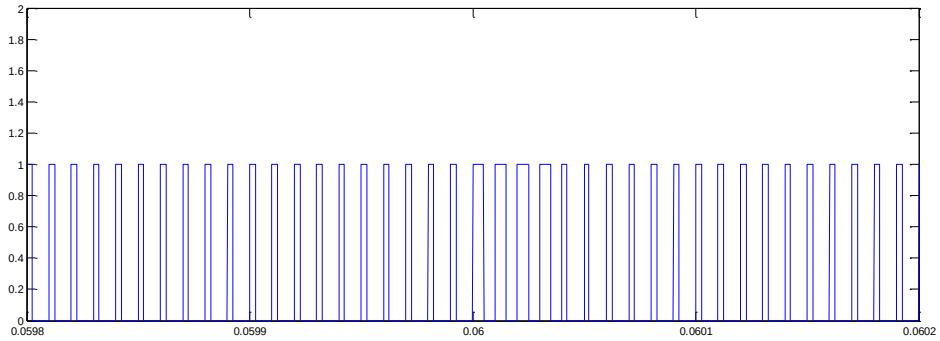

Figure 3.32 Zoomed in view of the switching state of phase-1 in converter-1 during phase shedding for feed-forward control

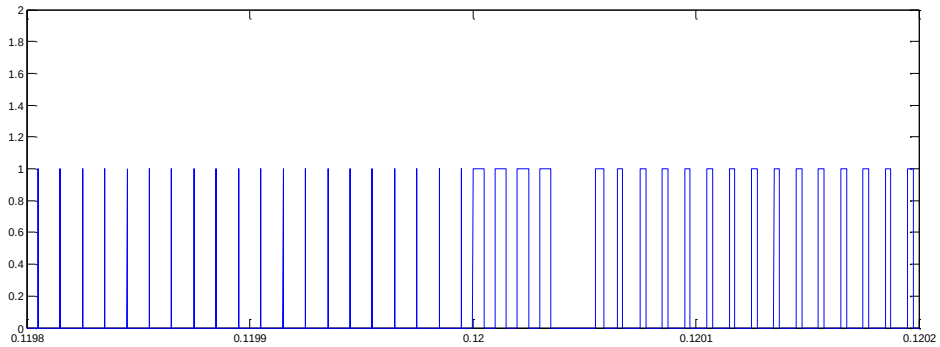

Figure 3.33 Zoomed in view of the switching state of phase-2 in converter-1 during phase adding for feed-forward control

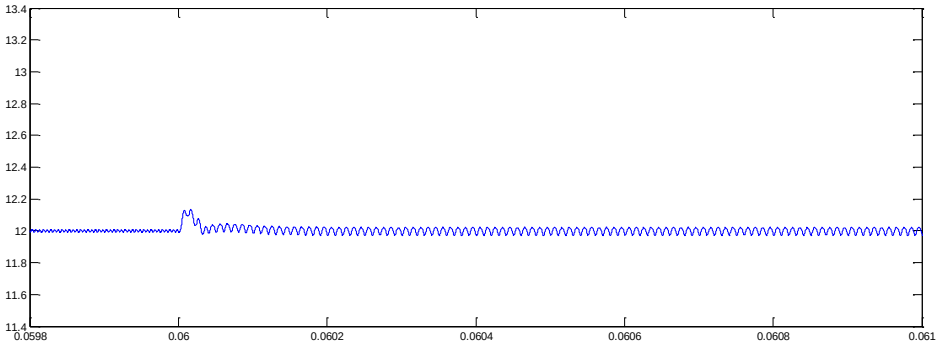

Figure 3.34 Output voltage of converter-1 during phase shedding in a feed forward control system

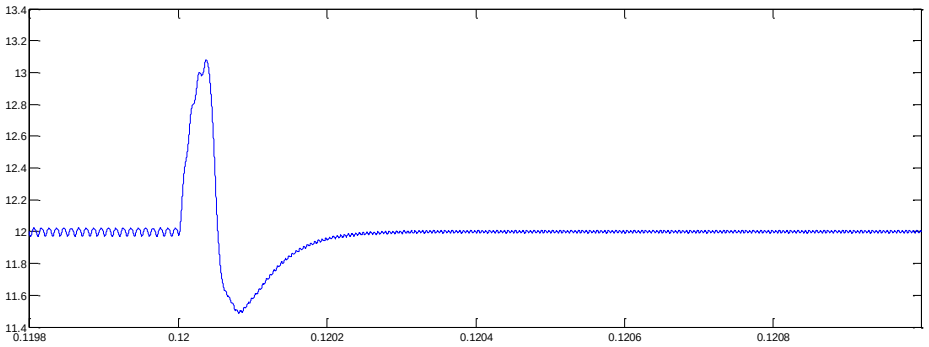

Figure 3.35 Output voltage of converter-1 during phase adding in a feed forward control system

3.3.2 Converter-2. Converter-2 is simulated with the same conditions as in the previous section and the results of this simulation are as given below. Table 3.3 and Table 3.4 tabulate the rise and drop in converter-1 and converter-2 in terms of percentage of output voltage for the phase shedding and the phase adding process respectively.

Figures 3.23 and 3.43 are compared and it is observed that, though this control does improve the transient behavior of the output voltage to a certain extent, it largely remains ineffective for converter-2. This is attributed to the relatively larger value of the converter's falling slope in comparison to its rising slope. Hence, even with unity duty cycle, the phase-1 current cannot rise fast enough to match the speed of the phase-2

current's fall. For the phase adding process, conclusions similar to that of converter-1 can be drawn and it is seen that though the equal current sharing is attained faster, it is at the cost of deteriorated transient behavior as seen from the comparison between the Figures 3.24 and 3.44.

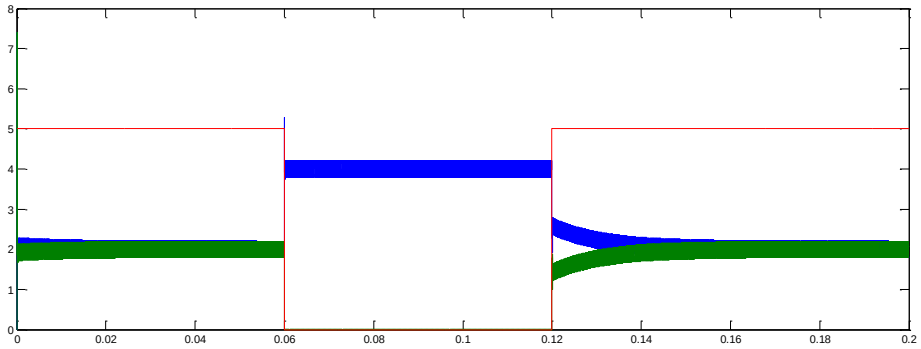

Figure 3.36 Phase currents of converter-2 in a feed-forward control system

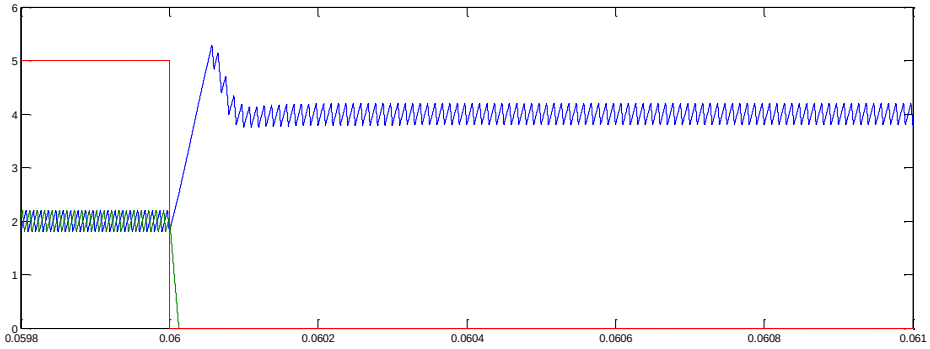

Figure 3.37 Zoomed in phase currents of converter-2 during phase shedding in a feed-forward control system

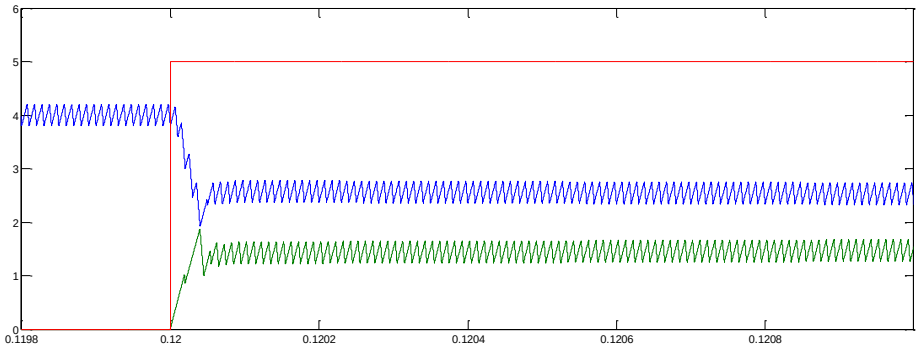

Figure 3.38 Zoomed in phase currents of converter-2 during phase adding in a feed-forward control system

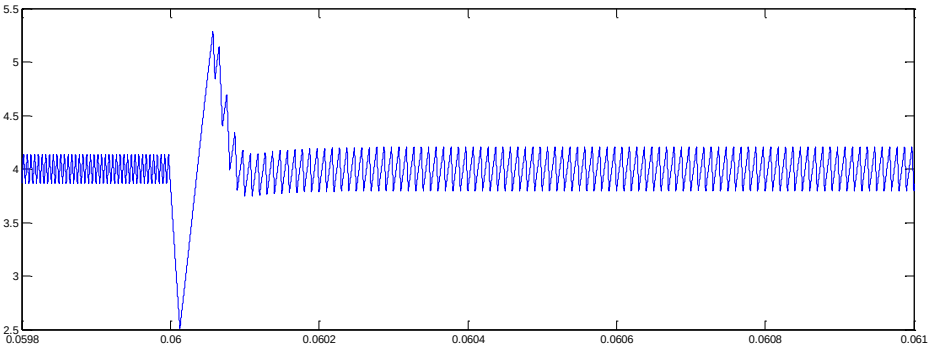

Figure 3.39 Total current of converter-2 during phase shedding in a feed-forward control system

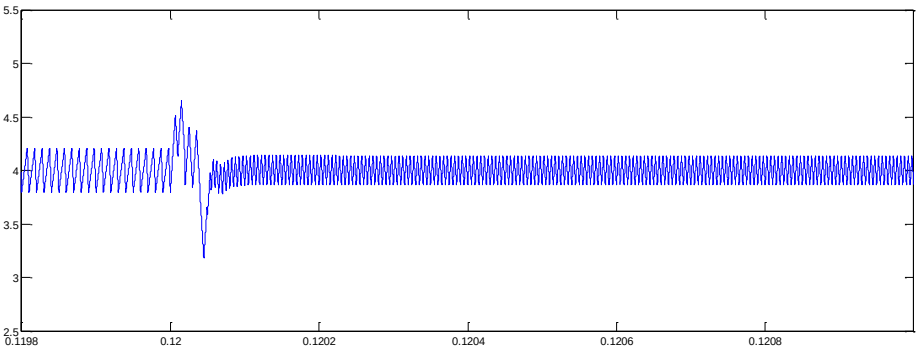

Figure 3.40 Total current of converter-2 during phase adding in a feed-forward control system

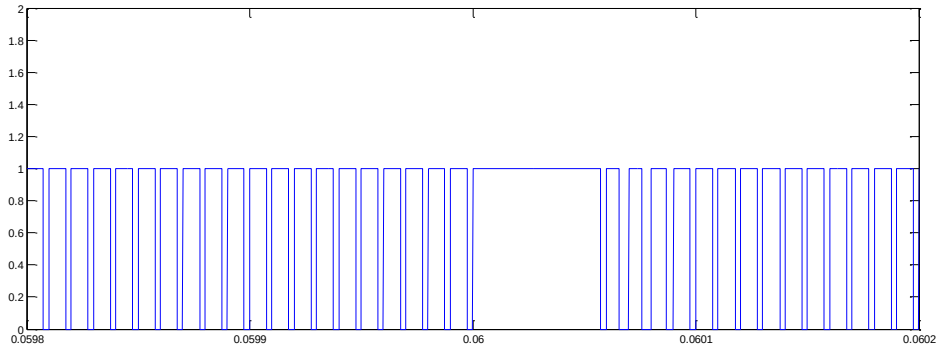

Figure 3.41 Zoomed in view of the switching state of phase-1 in converter-2 during phase shedding for feed-forward control

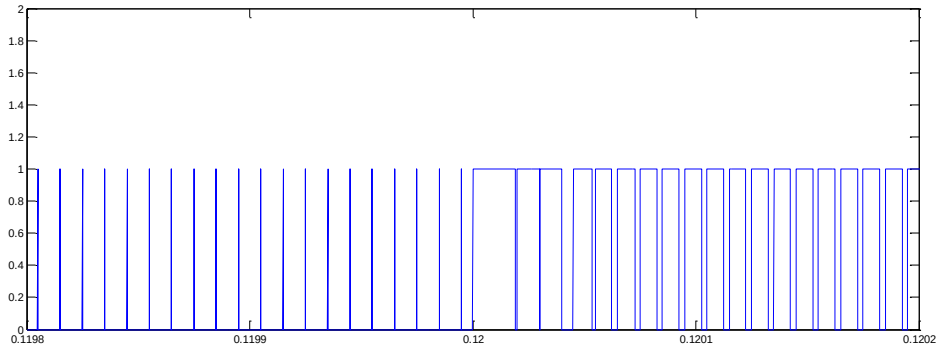

Figure 3.42 Zoomed in view of the switching state of phase-2 in converter-2 during phase adding for feed-forward control

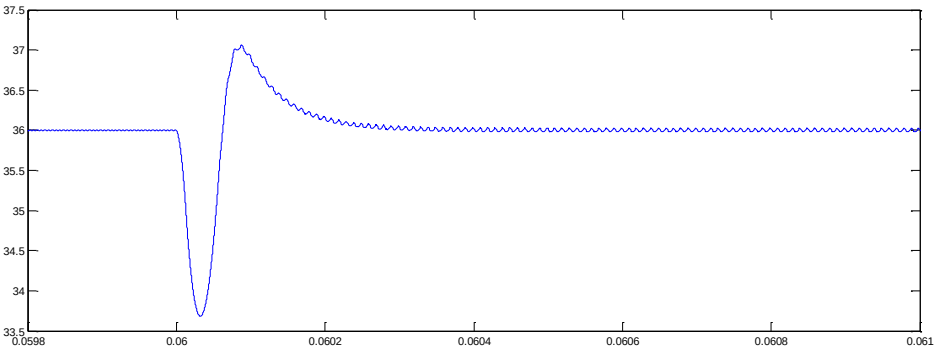

Figure 3.43 Output voltage of converter-2 during phase adding in a feed forward control system

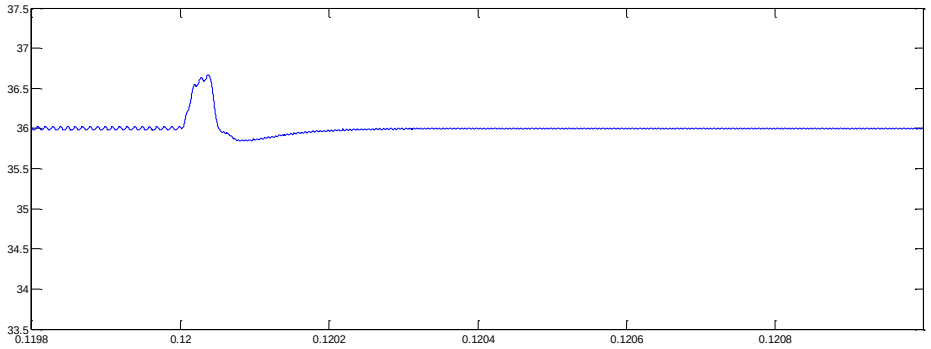

Figure 3.44 Output voltage of converter-2 during phase adding in a feed forward control system

Comparing Table 3.1 and 3.3, it is seen that feed-forward control does improve the transient behavior of the converter system. It is very effective in reducing the dip and rise for converter-1 configuration but does not do much for converter-2 configuration. This is one major drawback of this control. It is ineffective for converters whose falling slope exceeds their rising slope. Apart from this, this technique deteriorates the transient behavior of the system during the phase adding process which is unacceptable. To overcome these drawbacks, a new technique called the ramp control, is proposed in this thesis, which is discussed in the next section. Same conclusion can be drawn for phase adding process by comparing table 3.2 and 3.4.

Table 3.3 Rise and dip in the output voltage for the two converter configurations during the phase shedding process

Converter Configuration	Type of control	Percentage output voltage dip	Percentage output voltage rise
Converter-1	Feed forward	-	1.08
Converter-2	Feed forward	4.86	1.66

Table 3.4 Rise and dip in the output voltage for the two converter configurations during the phase adding process

Converter Configuration	Type of control	Percentage output voltage dip	Percentage output voltage rise
Converter-1	Feed forward	4.33	9.16
Converter-2	Feed forward	0.694	1.66

4. RAMP CONTROLLED PHASE SHEDDING

4.1 RAMP CONTROL TECHNIQUE

This section introduces a new phase shedding technique for multiphase converters called 'ramp control' technique. In the ramp control technique, phase shedding is implemented by gradually ramping down the duty cycle of the phase that is to be turned off and phase adding is implemented by gradually ramping up the duty cycle of the phase that is to be turned on. In a two-phase converter, this increases the time taken for phase-2 current to go to zero during the phase shedding process, thus giving ample time for phase-1 current to rise to the desired value. This improves the transient behavior of the system. Whereas in phase adding procedure, ramp control decreases the time taken by phase-2 current to reach the average value, thereby improving the current sharing in the system. The implementation of ramp control technique in a multiphase converter is discussed in this section.

From section 7 of reference [1], it is known that the slope of the moving average of inductor current of the buck converter is given by equation (15)

$$\frac{di_{L(AVG)}(t)}{dt} = \frac{D_{(AVG)}(t)V_{IN(AVG)}(t) - V_{O(AVG)}(t)}{L} \tag{15}$$

During the process of phase shedding, it is assumed that there are no perturbations in the input voltage i.e. $V_{IN(AVG)}(t) = V_{IN}$ and it is also desired that the output voltage not exhibit any perturbations which implies $V_{O(AVG)}(t) = V_O$. In a ramp controlled phase shedding process, the duty cycle is a linearly decreasing function given by equation (16) where 'm_d' is the ramping down slope. In a ramp controlled phase adding process, the duty cycle is a linearly increasing function given by equation (17) where 'm_u' is the ramping up slope. For the phase adding procedure, the slope m_u is found, indirectly. This is discussed in the next paragraph.

$$D_{(AVG)}(t) = D - m_d t \tag{16}$$

$$D_{(AVG)}(t) = m_u t \tag{17}$$

Substituting the values of $V_{IN(AVG)}(t)$, $V_{O(AVG)}(t)$ and $D_{(AVG)}(t)$, equation (15) can rewritten as in equation (18) for the phase shedding process.

$$\frac{di_{L(AVG)}(t)}{dt} = \frac{-m_d V_{IN} t}{L} \tag{18}$$

Integrating on both sides, the moving average of the inductor current is given by equation (19) where $i_{L(AVG)}(0)$ is the average current at the instant phase shedding begins.

$$i_{L(AVG)}(t) = i_{L(AVG)}(0) - \frac{m_d V_{IN}}{2L} t^2 \tag{19}$$

Thus the slope m_d of the converter, as seen from equation (19), is a function of t. If at $t=T_d$, the moving average of the inductor current in equation (19) goes to zero, m_d can be expressed as in equation (20).

$$m_d = \frac{i_{L(AVG)}(0)(2L)}{V_{IN} T_d^{\,2}} \tag{20}$$

In a buck converter, duty cycle, D(t) is related to the error voltage $V_E(t)$ by the fundamental equation of a PWM controller given in equation (21) where V_R is the magnitude of the external ramp of the PWM controller.

$$\frac{D_{(AVG)}(t)}{V_{E(AVG)}(t)} = \frac{1}{V_R} \tag{21}$$

Substituting equation (16) for $D_{(AVG)}(t)$, equation (21) is modified as given in equation (22) and (23) for phase shedding and the phase adding respectively.

$$V_{E(AVG)}(t) = DV_R - m_d V_R t \tag{22}$$

$$V_{E(AVG)}(t) = m_u V_R t \tag{23}$$

Thus, $V_{E(AVG)}(t)$ can be written as a combination of two parts, $V_E = DV_R$ and $V_{RAMP} = mV_R t$ where the value of m takes the value of m_d for phase shedding process and takes the value of m_u for phase adding process. The slope of the ramp 'mV_R' is represented as 'K' in this thesis. For the phase adding procedure, the value of 'K' is directly calculated. It is calculated so as to decrease the time taken for current sharing in a system, while maintaining acceptable transient behavior of a system.

Therefore, during the process of phase shedding, i.e., when transitioning from on to off state, V_E of phase-2, as in Figure 2.10, is replaced by V_E-V_{RAMP} and when transitioning from off to on state, V_E is replaced by just the V_{RAMP}. Under steady state off condition, V_E is replaced by 0 and under steady state on condition; V_E remains the same.

The main challenge in implementing this ramp control technique is designing the controls required to turn the ramp on and off as required. For example, the ramp needs to be turned on when the process of phase shedding starts in a system and the same ramp needs to be turned off, once the phase current of the phase that is turned off reaches zero which may prove to be cumbersome in analog domain or rather the Simulink domain. One way to implement these controls in Simulink is by using state diagrams which convert any complicated schematic into a simple flip flop solution. State diagrams and their implementation are discussed in the next section.

4.2 STATE DIAGRAM IMPLEMENTATION

A state diagram is defined as an illustration of the states a system can attain and also the transition between the states for a given transition condition. Hence, to implement a state diagram for any system, it is important to define the states and also the transition conditions for transition between different states.

For the ramp controlled phase shedding process, two states, Q_1 and Q_2, one for the error voltage V_E and another for the ramp voltage V_{RAMP} are defined respectively. There are four possible combinations of these two states- Q_1 Q_2 - 00,01,10,11. At any given point of time, as discussed in the previous section, phase-2 of the converter is in one of these four states.

Three transition conditions, C_2, Y and Z, are also defined. C_2 condition shows if phase-2 is in an on or off mode. Its value is '1' when the phase-2 is on and '0' when it is off. Y detects the zero crossing point of the phase-2 current. Its value is '1' if the phase-2 current is non-zero else it is '0'. Z detects the point when the phase-2 current reaches, i_L/N, defined in the previous section. Its value is '1' when the current is equal to i_L/N else it is '0'. This control is in general used for the phase adding process.

The first step towards implementing the state diagram into the simulation is by designing the states and controls used in the state diagram. State V_E has already been designed in the previous sections, as illustrated in Figure 2.8, while state V_{RAMP} is generated in Simulink using an integrator block which integrates a constant K to give a ramp signal with slope K set to an external reset at the rising and falling edge of Q_2

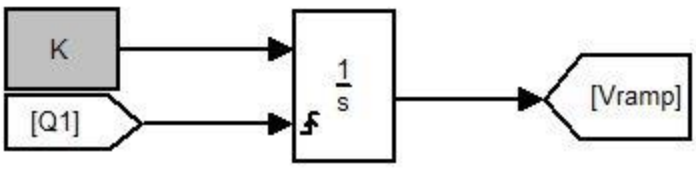

Figure 4.1 Implementation of the state V_{RAMP}

The transition conditions are Y and Z are designed in Simulink as illustrated in the Figures 4.2 and 4.3. Transition condition C_2 is already discussed in the section 3.2 of section-3.

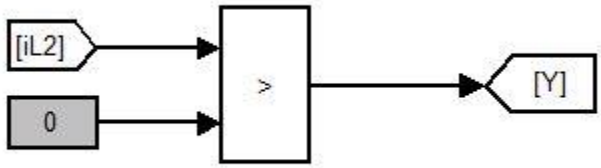

Figure 4.2 Implementation of the transition condition Y

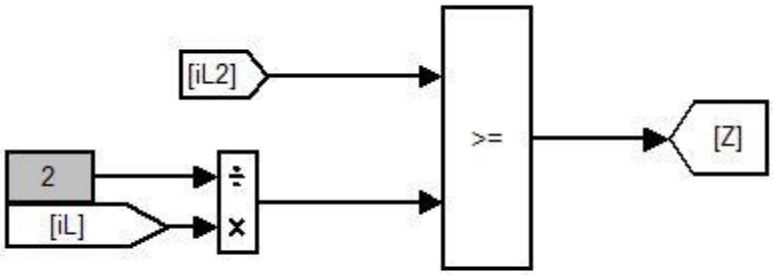

Figure 4.3 Implementation of the transition condition Z

Now the state diagram, for the control technique, is generated and converted into a flip flop schematic through a series of steps as given below.

Step 1: Defining the state diagram

Figure 4.4 depicts the state diagram for a ramp controlled phase change process. This control is implemented for phase-2 of the two-phase converter system, discussed in this thesis. During the steady state operation, the system is in the state 10 (V_E is 1 and V_{RAMP} is 0) and when the phase shuts down, i.e. C_2 becomes 0; irrespective of the value of Y and Z, the state changes to 11 (V_{RAMP} is negative here). The state changes to 00 when the value of Y goes to zero. Once again as the phase becomes on, i.e. C_2 becomes 1, irrespective of the value of Y and Z, the system is in the state 01. And as the value of Z equals 1, the state of the system changes to 10.

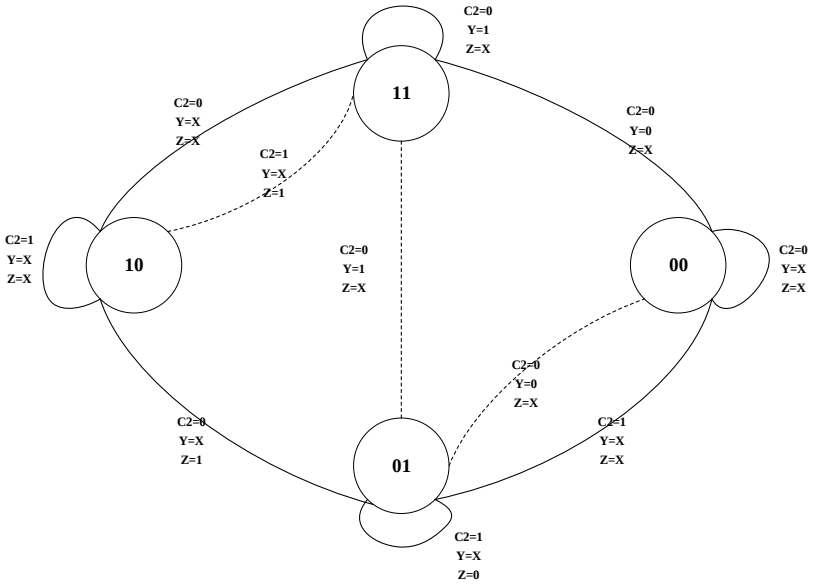

Figure 4.4 State diagrams for a ramp controlled phase change process

Step 2: JK flip flop table

The state diagram is implemented with JK flip flops and hence it is important to know the values of the J and K for different combinations of input-output. Table 4.1 illustrates the same.

Table 4.1 J-K flip flop table

Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 3: Defining the next state table

From the state diagram given in step 1, the next state table can be derived as given in Table 4.2.

Table 4.2 Next state table

Present state V_E	Present state V_{RAMP}	Control Y	Control Z	Control C2	Next state V_E	Next state V_{RAMP}
0	0	0	0	1	0	1
0	0	0	1	1	1	0
0	0	1	0	1	0	1
0	0	1	1	1	1	0
0	1	0	0	1	0	1
0	1	0	1	1	1	0
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	1	1	0
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	1	1	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1
1	1	1	1	1	1	0

Table 4.2 Next state table (cont.)

Present state V_E	Present state V_{RAMP}	Control Y	Control Z	Control C2	Next state V_E	Next state V_{RAMP}
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	1	1
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	1	1
1	0	1	1	0	1	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	1
1	1	1	1	0	1	1

The next state table gives us the values of the next state, given the present state and the control signals.

Step 4: K map representation

The K maps of the next state table are given in Table 4.3. J_1 and K_1 represent the K maps of the state V_E while J_2 and K_2 represent the K maps of the state V_{RAMP}.

Table 4.3 K-map table

J_1	00	01	11	10	J_1	00	01	11	10
00	0	0	0	0	00	1	0	0	1
01	X	X	X	X	01	X	X	X	X
11	X	X	X	X	11	X	X	X	X
10	0	0	1	1	10	0	0	0	0

Table 4.3 K-map table (cont.)

K_1	00	01	11	10	K_1	00	01	11	10
00	X	X	X	X	00	X	X	X	X
01	1	1	0	0	01	0	1	1	0
11	1	1	0	0	11	0	1	0	1
10	X	X	X	X	10	X	X	X	X

J_2	00	01	11	10	J_2	00	01	11	10
00	0	0	0	0	00	0	1	1	0
01	0	0	1	1	01	0	1	1	0
11	X	X	X	X	11	X	X	X	X
10	X	X	X	X	10	X	X	X	X

K_2	00	01	11	10	K_2	00	01	11	10
00	X	X	X	X	00	X	X	X	X
01	X	X	X	X	01	X	X	X	X
11	1	1	0	0	11	0	0	0	0
10	1	1	0	0	10	0	0	0	0

From the K maps, we know that the inputs to the J and K terminals of the flip flop are as given below:

$$J_1 = Q_2 Y \overline{C_2} + \overline{Q_2}\,\overline{Z} C_2$$

$$K_1 = \overline{C_2}\,\overline{Y} + \overline{Q_2} Z C_2 + Q_2 Y \overline{Z} C_2 + \overline{Y} Z C_2$$

$$J_2 = Q_1 Y \overline{C_2} + Z C_2$$

$$K_2 = \overline{Y}\,\overline{C_2}$$

Step 5: Flip flop implementation

The flip flop implementation of the above formulae of J_1, J_2, K_1 and K_2 are as given below.

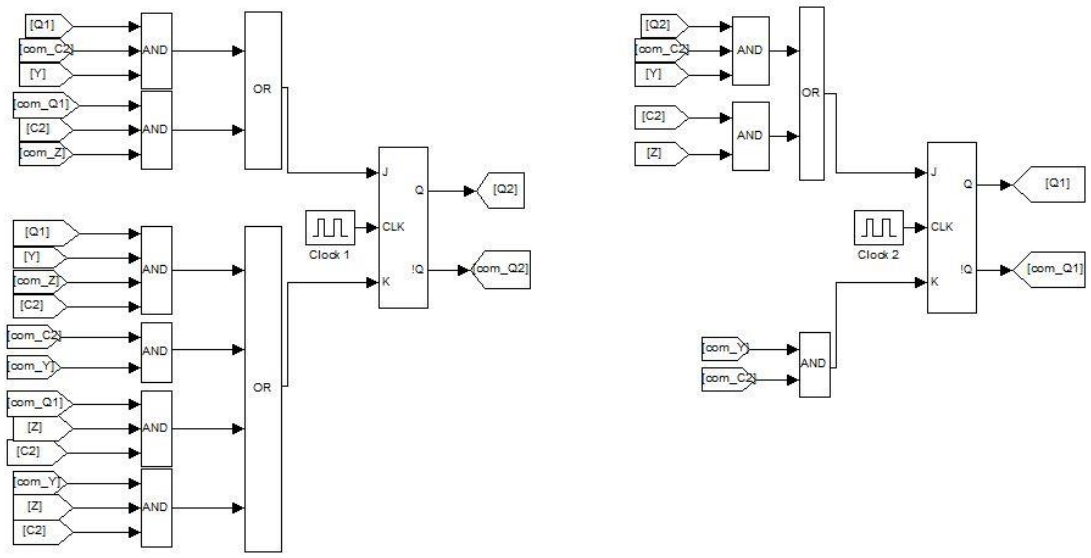

Figure 4.5 Flip-flop implementation of the state diagram

4.3 RAMP CONTROL MODEL OF A MULTIPHASE CONVERTER

For implementing the ramp control in Simulink, the slope of V_{RAMP} needs to be found. From equation (20), slope of the duty cycle m_d, for the phase shedding process, can be calculated. From the converters' specifications, as in section-1 it is known that V_{IN}=48 V, L=220 μH and $i_{L(AVG)}(0)$=2 A. Hence equation (24) expresses the slope as a function of T_d.

$$m_d = \frac{-(2\times 220\times 10^{-6})\cdot 2}{48\cdot T_d^{\,2}} \tag{24}$$

It is known that $K = mV_R$ from section 4.1. From section-2, the value of V_R is 5 V. Hence K can be expressed as in equation (25).

$$K = m\times 5 \tag{25}$$

Therefore, for zero crossing times of T_d=100 μs, T_d=500 μs and T_d=1000 μs, the values of K can be calculated as '1833.33×5', '73.33×5' and '18.33×5' respectively.

During the phase adding process, it is known that VE(t) is given by the equation (26). Substituting the value of VE(t) from equation (21), the value of K is as given in equation (27). If at t=Tu, VE(t) reaches the steady state value, then D(t)=D and K can now be expressed as in equation (28). From the converter's specifications, the values of D and VR are known.

$$V_E(t) = V_{RAMP} = Kt \tag{26}$$

$$K = \frac{D(t) \cdot V_R}{t} \tag{27}$$

$$K = \frac{D \cdot V_R}{T_u} \tag{28}$$

From repeated experiments, it has been seen that for the values of Td, 500 μs and 1 ms, the phase adding process exhibits a good transient behavior along with improved current sharing. Hence, the values of K are calculated as 2500 and 1250 respectively, for converter-1; 7500 and 3750 respectively, for converter-2. The ramp controlled phase change model is implemented in Simulink by adding the flip-flop implementation, in Figure 4.5, to the simple model discussed in 3.2 of section-3 and by modifying the error voltage of phase-2 to the ones given in Figures 4.6 and 4.7.

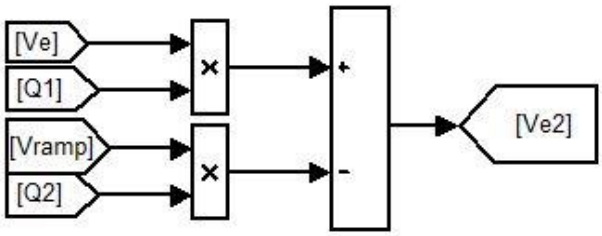

Figure 4.6 Error voltage of phase-2 in ramp control technique

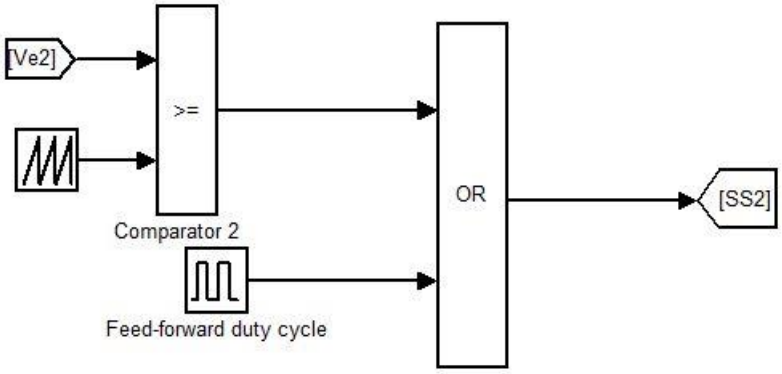

Figure 4.7 Ramp control implementation for phase-2 in Simulink

Thus, from the above discussions, a ramp controlled phase change Simulink model can be generated for converter-1 and converter-2 configurations. This model is simulated for a period of 0.2 s, where phase-2 is shed at 0.06 s and then added back at 0.12 s. Section 4.4 discusses the phase shedding process in these converters while section 4.5 discusses the phase adding process for the same.

4.4 RAMP CONTROLLED PHASE SHEDDING IN A MULTIPHASE CONVERTER

4.4.1 Converter 1. Ramp control is implemented for the zero crossing times- 100 μs, 500 μs and 1000μs- and the results are compared with simple control and feed forward control. The first case considered is for the zero crossing time of 100 μs and the results are as given below.

It is observed from Figure 4.8 that the zero crossing time, T_d, is not exactly 100 μs. This insignificant error can be attributed to the delay in error voltage response of phase-1 when a ramp is applied to the phase-2. Comparing Figure 4.13 and Figure 3.12, it is observed that the output voltage behavior improves significantly when compared to the simple control case but when compared to the output of the feed-forward control, as in Figure 3.34, it is observed that the feed-forward control responds better. This result is specific to T_d=100 μs and it is seen from the subsequent paragraphs that as the zero crossing time, T_d, increases, the output voltage response of the system gets better. One important point to note here is that the error voltage, as in Figure 4.12, unlike the error voltage in simple control, does not go to zero abruptly but linearly decreases to zero and this increases the time taken by the phase-2 current to go to zero, thus giving an advantage over simple control. Now, the system is simulated for zero crossing time of 500 μs and the results are as given below.

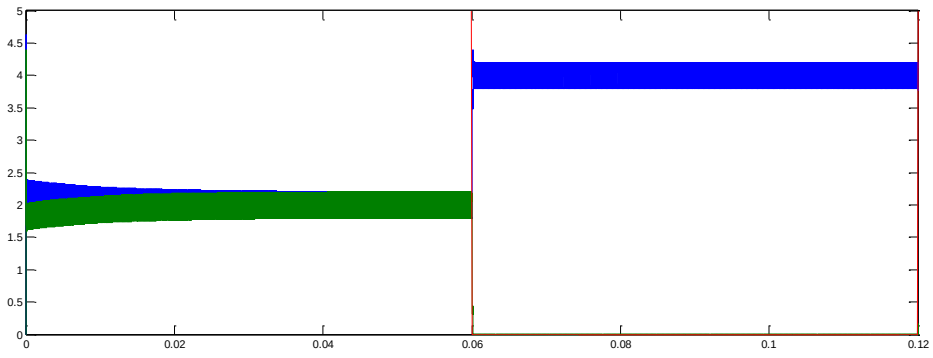

Figure 4.8 Phase current in converter-1 for T_d=100 μs

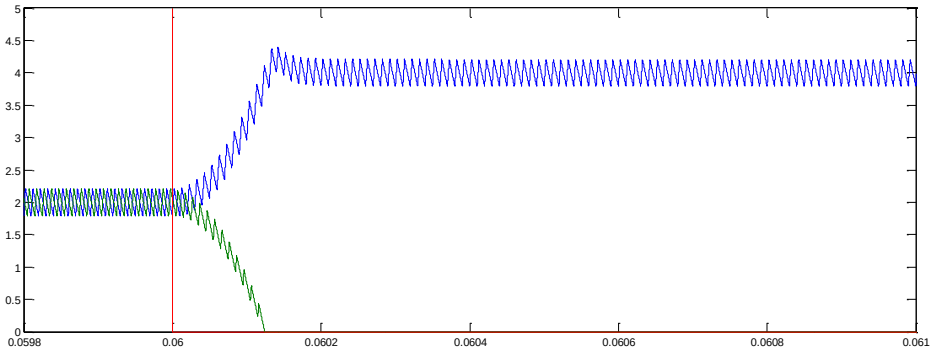

Figure 4.9 Zoomed in phase currents in converter-1 for T_d=100 μs

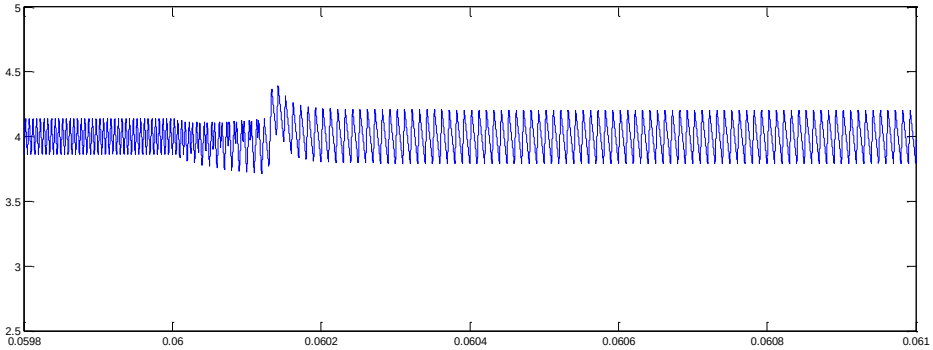

Figure 4.10 Total current in converter-1 for T_d=100 μs

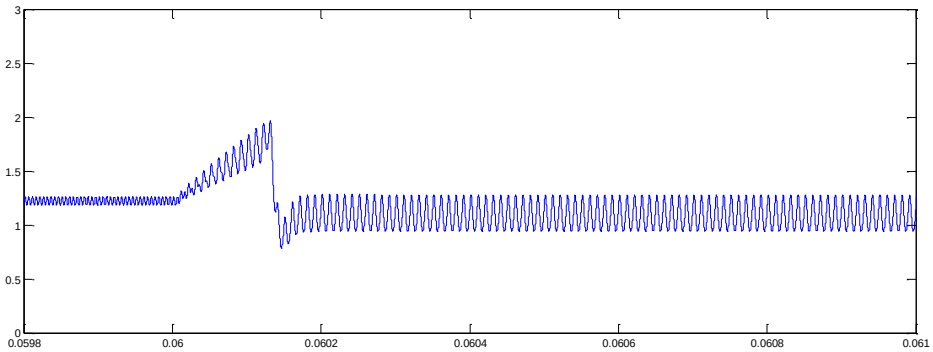

Figure 4.11 Phase-1's error voltage in converter-1 for T_d=100 μs

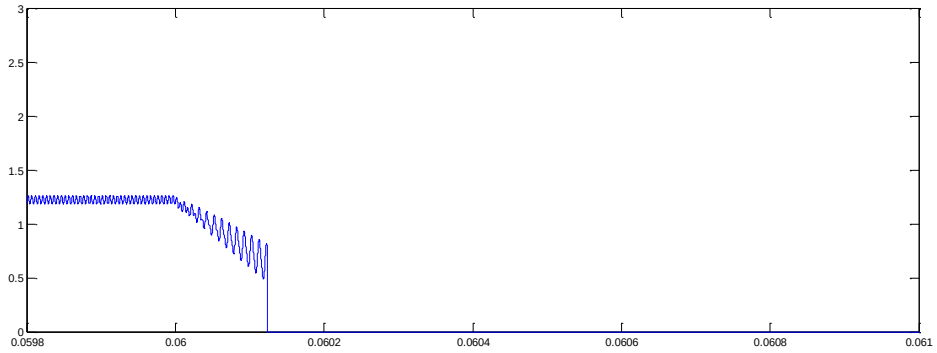

Figure 4.12 Phase-2's error voltage in converter-1 for T_d=100 μs

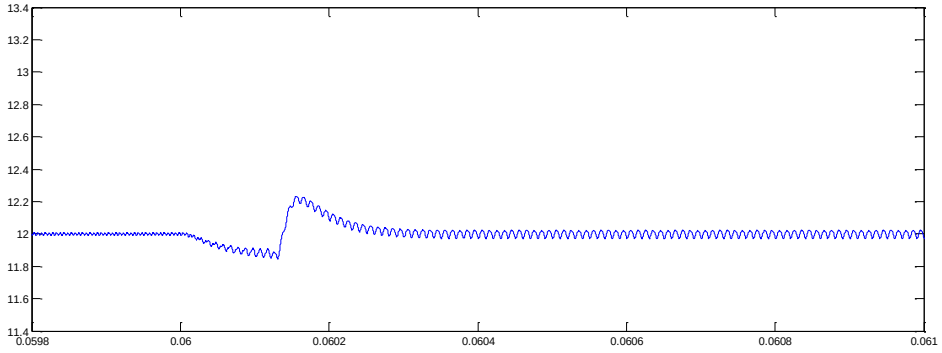

Figure 4.13 Output voltage of converter-1 for T_d=100 μs

Now, the system is simulated for zero crossing time of 500 μs and the results are as given below. The output voltage in Figure 4.19 is observed to have improved considerably when compared with the previous case, but still lags in performance, when compared to the feed-forward control's output. Hence it is observed that as the value of T_d increases, i.e. the value of slope m_d decreases, the performance of the system improves. But it is true only till a certain point and if the slope is increased beyond a certain limit, the performance starts to deteriorate, as observed in the subsequent paragraphs.

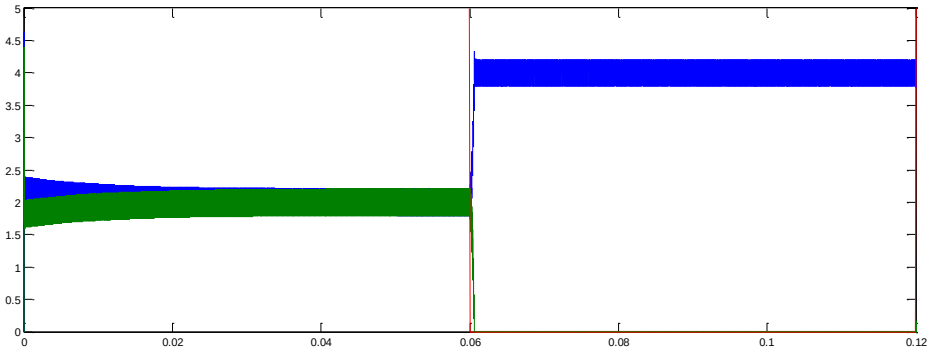

Figure 4.14 Phase current in converter-1 for T_d=500 μs

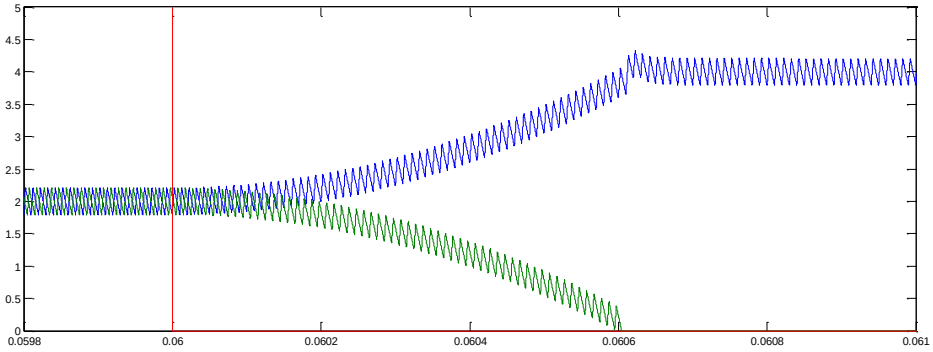

Figure 4.15 Zoomed in phase currents in converter-1 for T_d=500 μs

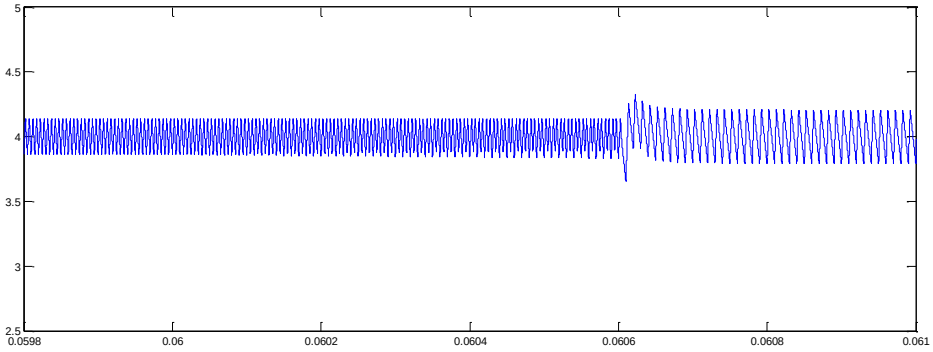

Figure 4.16 Total current in converter-1 for T_d=500 μs

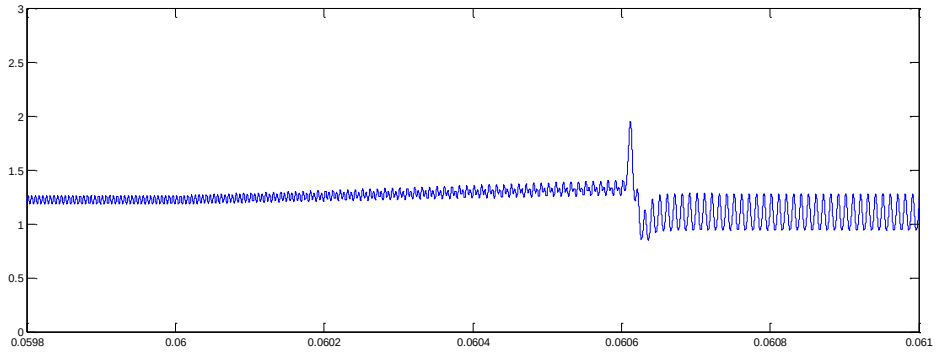

Figure 4.17 Phase-1's error voltage in converter-1 for T_d=500 μs

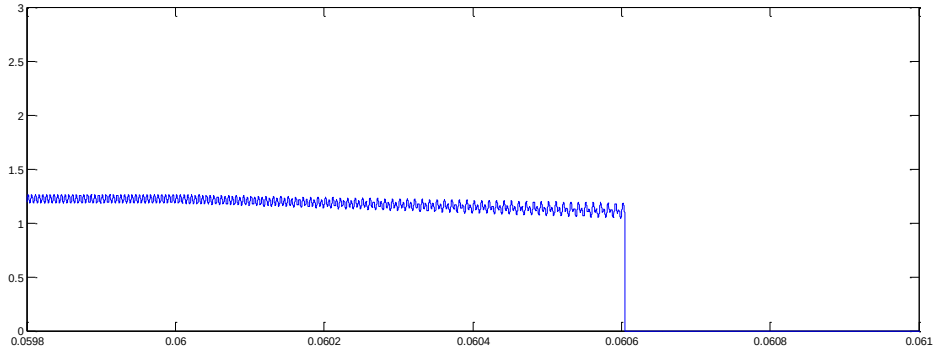

Figure 4.18 Phase-2's error voltage in converter-1 for T_d=500 μs

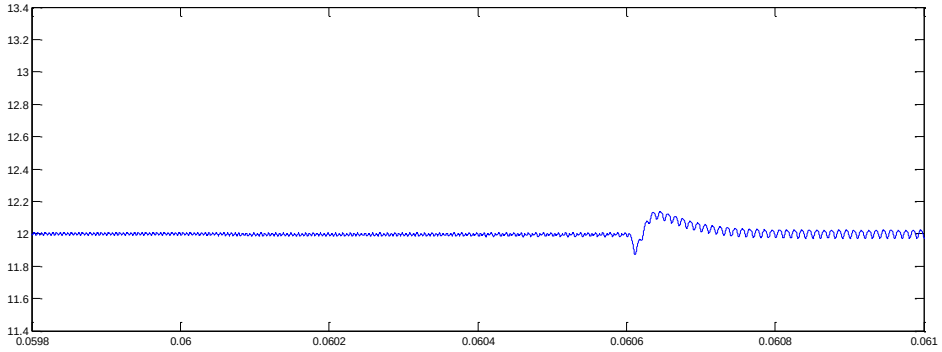

Figure 4.19 Output voltage of converter-1 for T_d=500 μs

Now, the system is simulated for zero crossing time of 1000 µs and the results are as given below. Comparing Figures 4.19 and 4.25, it is observed that the output voltage's transient behavior remains almost the same for T_d= 1000 µs, though it is expected to perform better. This is attributed to mainly to the inaccurate zero crossing time of the system. According to the definition of the transition condition Y, the value of Y is 0 when the average inductor current of phase-2 becomes zero but for the simplicity of the control, the average inductor current has been approximated to the inductor current in this thesis. This approximation works fine for a larger value of m_d but fails as the value of m_d decreases. And this advances the zero crossing time, thereby causing a dip in the system. Table 4.4 tabulates the transient rise and dip in the converter-1 system in terms of percentage of output voltage for the phase shedding process. It is observed that in case of converter-1, feed forward-control works the best.

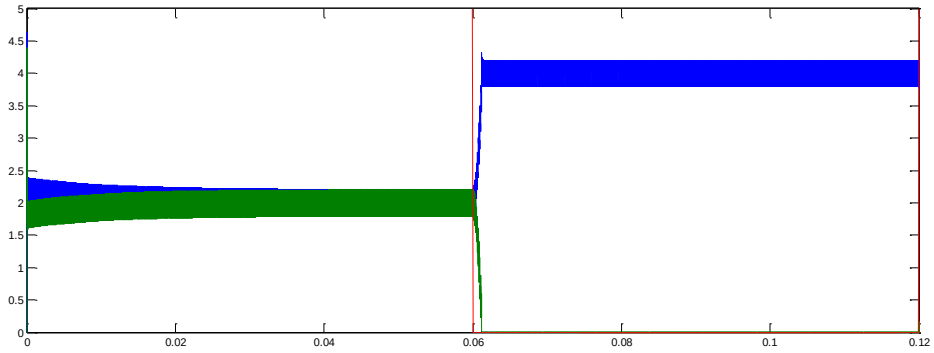

Figure 4.20 Phase current in converter-1 for T_d=1000 µs

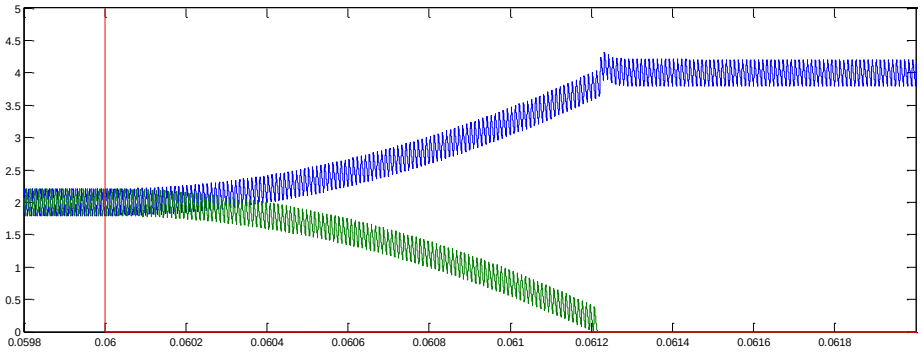

Figure 4.21 Zoomed in phase currents in converter-1 for T_d=1000 μs

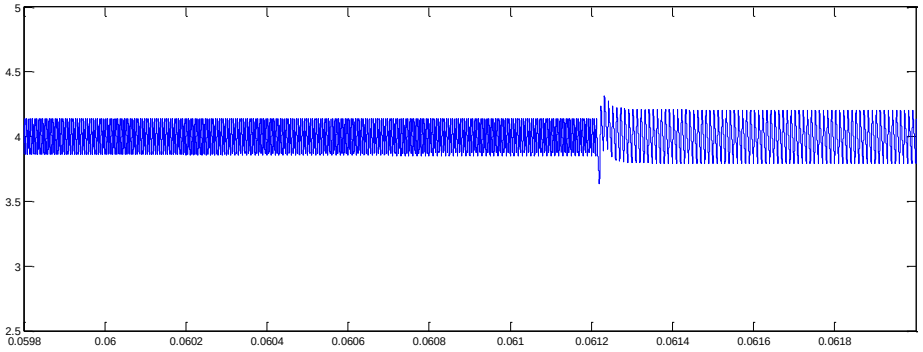

Figure 4.22 Total current in converter-1 for T_d=1000 μs

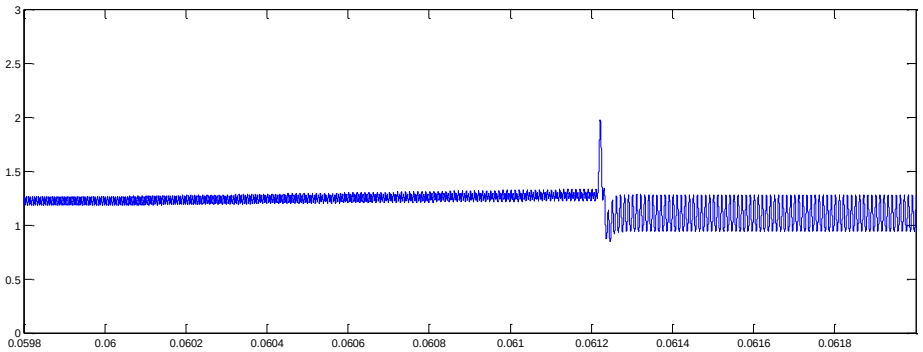

Figure 4.23 Phase-1's error voltage in converter-1 for T_d=1000 μs

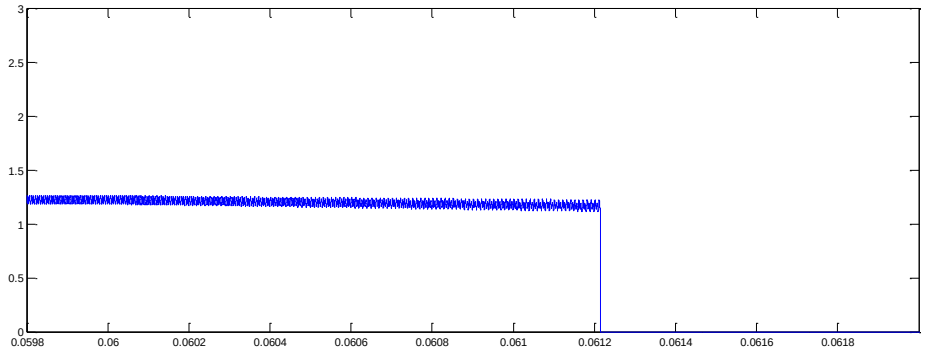

Figure 4.24 Phase-2's error voltage in converter-1 for T_d=1000 μs

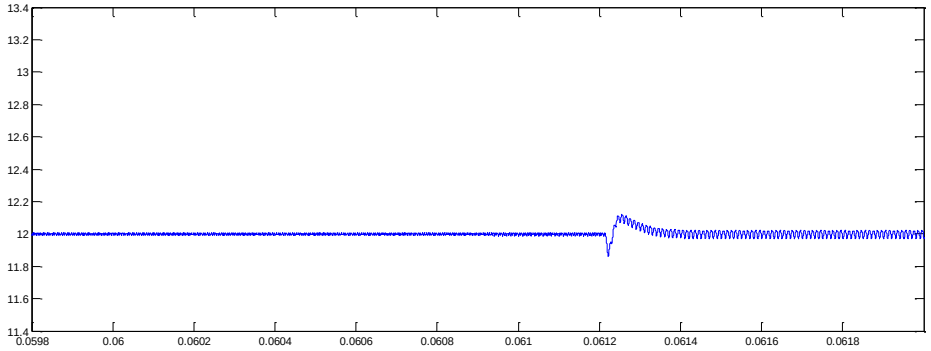

Figure 4.25 Output voltage of converter-1 for T_d=1000 μs

Table 4.4 Rise and dip in the output voltage for converter-1 during the process of phase shedding

Converter Configuration	Type of Control	Zero crossing time T_d	Percentage output voltage dip	Percentage output voltage rise
Converter-1	Simple control	-	4.58	2.5
Converter-1	Feed-forward control	-	-	1.08
Converter-1	Ramp control	100 μs	1.33	2.08
Converter-1	Ramp control	500 μs	1.166	1.25
Converter-1	Ramp control	1000 μs	1.166	1.25

4.4.2 Converter-2. Ramp control is implemented for converter-2 with similar zero crossing times as converter-1 - 100 μs, 500 μs and 1000 μs- and the results are compared with the simple control and feed forward control. The first case considered is for the zero crossing time of 100 μs and the results are as given below.

Comparing Figure 4.31 and Figure 3.23, it is observed that the output voltage behavior improves significantly when compared to the simple control case. Similar conclusions can be drawn when compared to the feed-forward control's output as in Figure 3.43. This improvement is attributed to the linearly decreasing error voltage, as in Figure 4.30 which increases the time taken for the phase-2 current to go to zero.

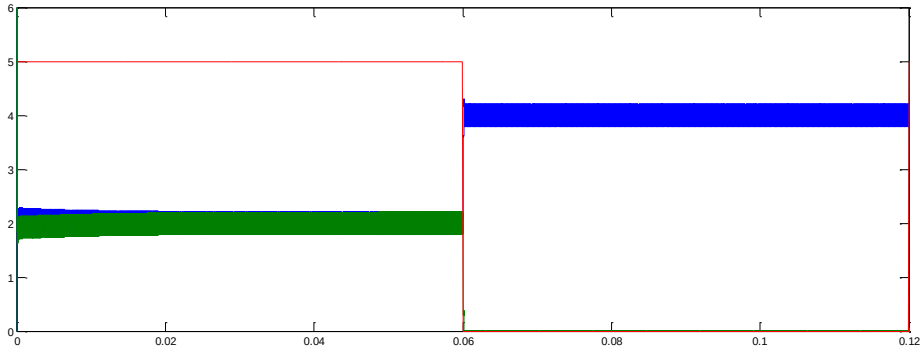

Figure 4.26 Phase current in converter-2 for T_d=100 μs

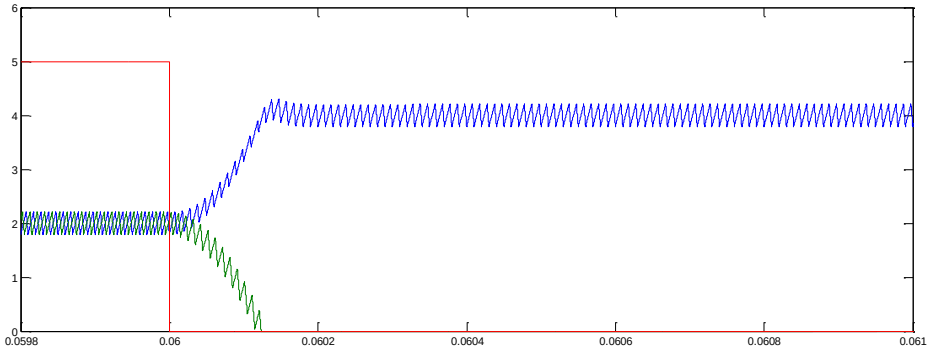

Figure 4.27 Zoomed in phase currents in converter-2 for T_d=100 μs

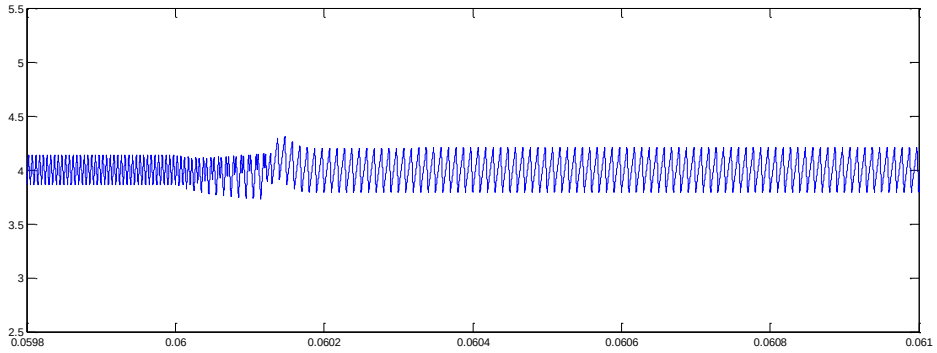

Figure 4.28 Total current in converter-2 for T_d=100 μs

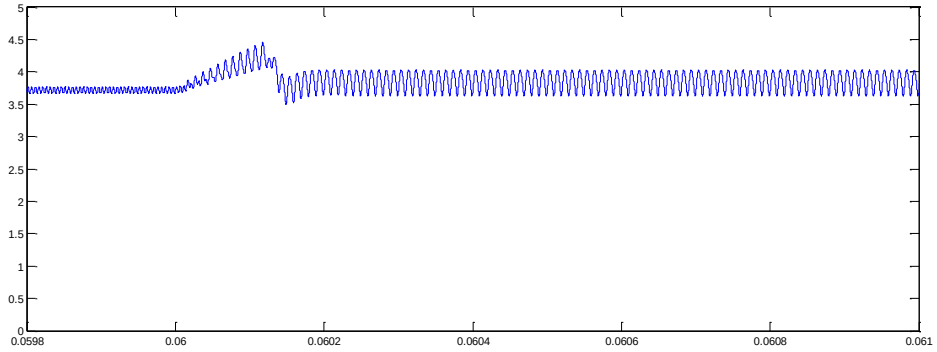

Figure 4.29 Phase-1's error voltage in converter-2 for T_d=100 μs

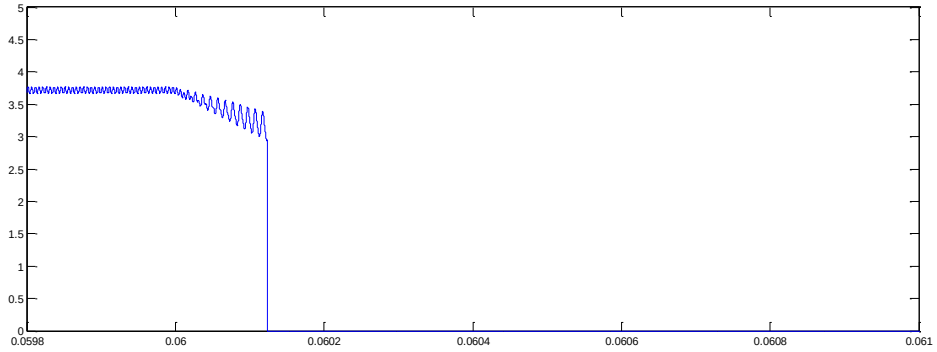

Figure 4.30 Phase-2's error voltage in converter-2 for T_d=100 μs

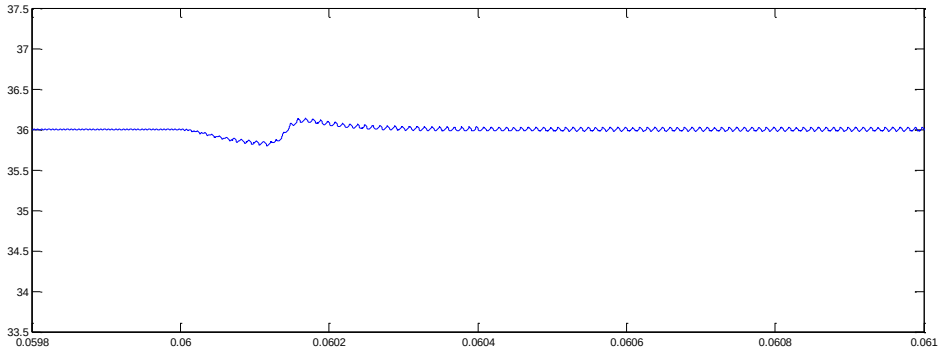

Figure 4.31 Output voltage of converter-2 for T_d=100 μs

Now, the system is simulated for zero crossing time of 500 μs and the results are as given below. The output voltage in Figure 4.37, is observed to have improved to a certain extent when compared with the previous case.

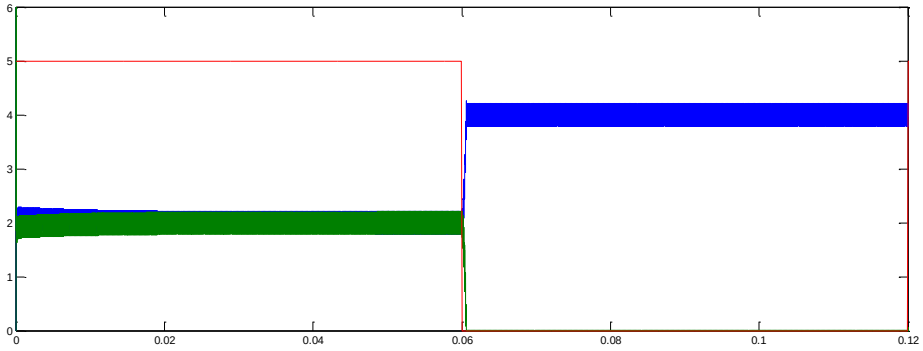

Figure 4.32 Phase current in converter-2 for T_d=500 μs

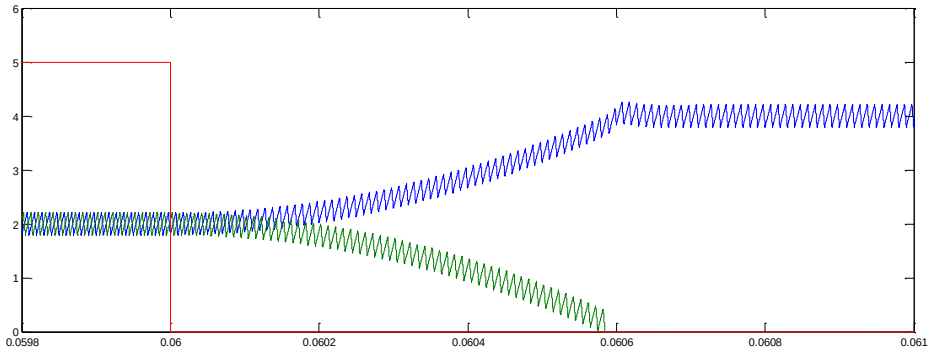

Figure 4.33 Zoomed in phase currents in converter-2 for T_d=500 μs

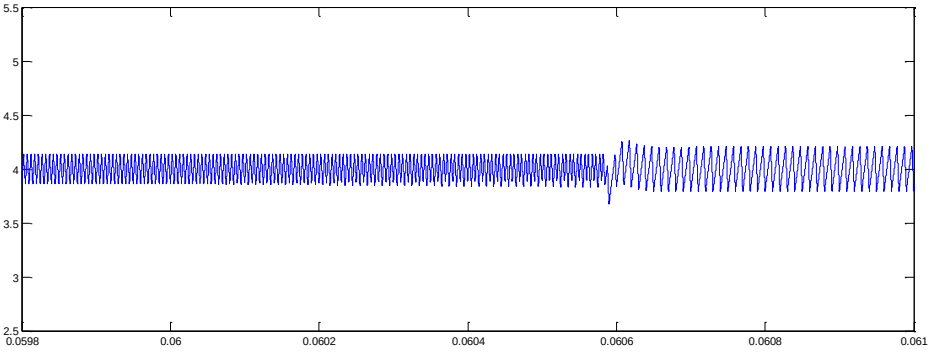

Figure 4.34 Total current in converter-2 for T_d=500 μs

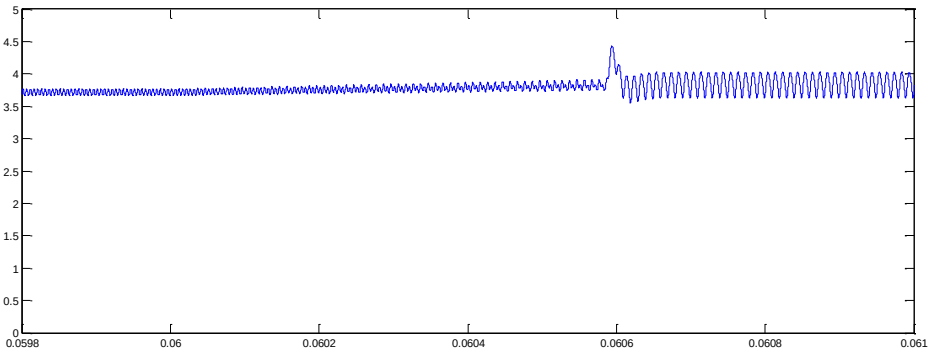

Figure 4.35 Phase-1's error voltage in converter-2 for T_d=500 μs

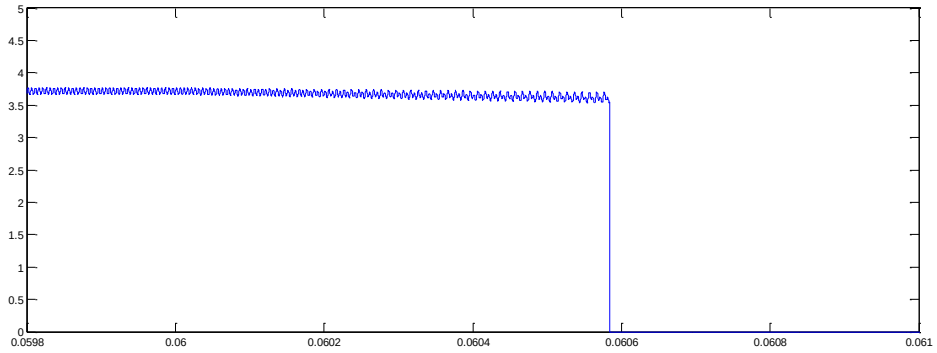

Figure 4.36 Phase-2's error voltage in converter-2 for T_d=500 μs

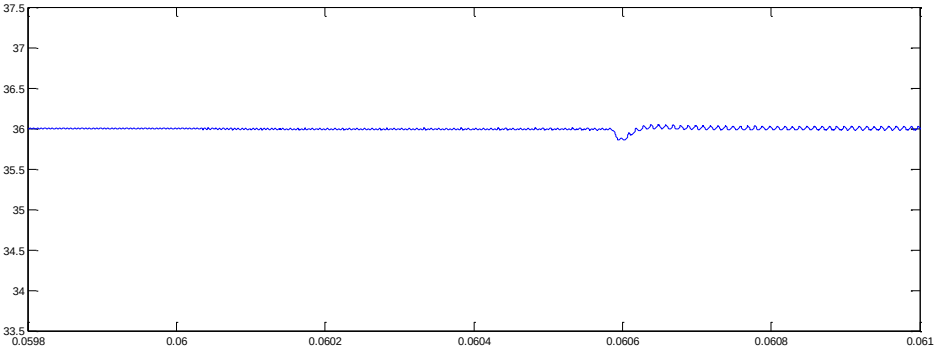

Figure 4.37 Output voltage of converter-2 for T_d=500 μs

Now, the system is simulated for zero crossing time of 1000 μs and the results are as given below. Comparing Figures 4.37 and 4.43, it is observed that the output voltage's transient behavior shows a little deterioration for T_d= 1000 μs. Table 4.5 tabulates the transient rise and dip in the converter-2 system in terms of percentage of output voltage for the phase shedding process. It is observed that in case of converter-2, the performance of ramp control surpasses that of simple control and feed forward control.

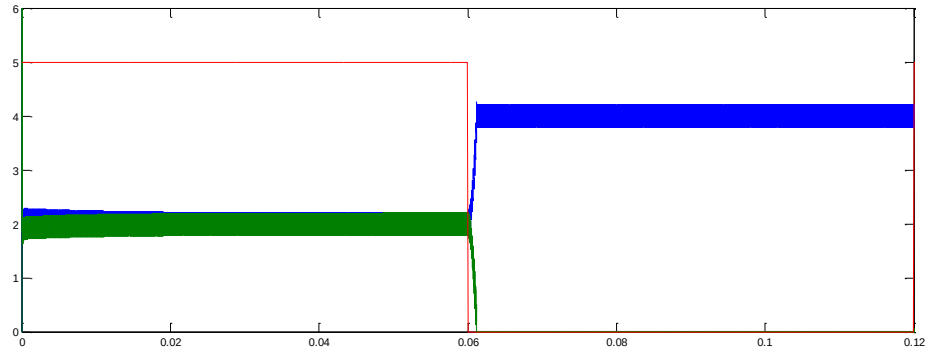

Figure 4.38 Phase current in converter-2 for T_d=1000 μs

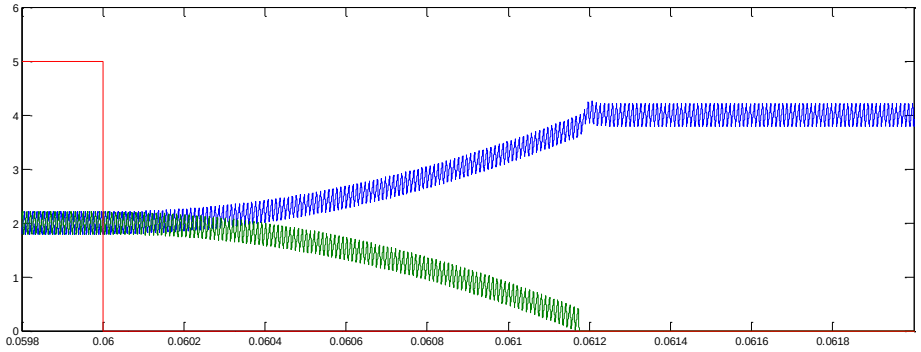

Figure 4.39 Zoomed in phase currents in converter-2 for T_d=1000 μs

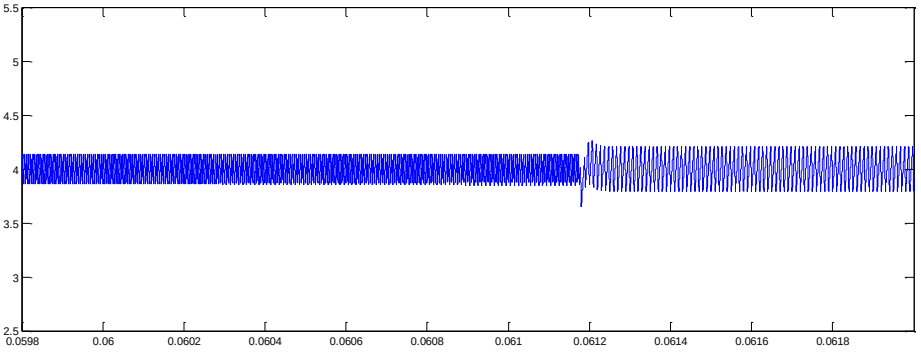

Figure 4.40 Total current in converter-2 for T_d=1000 μs

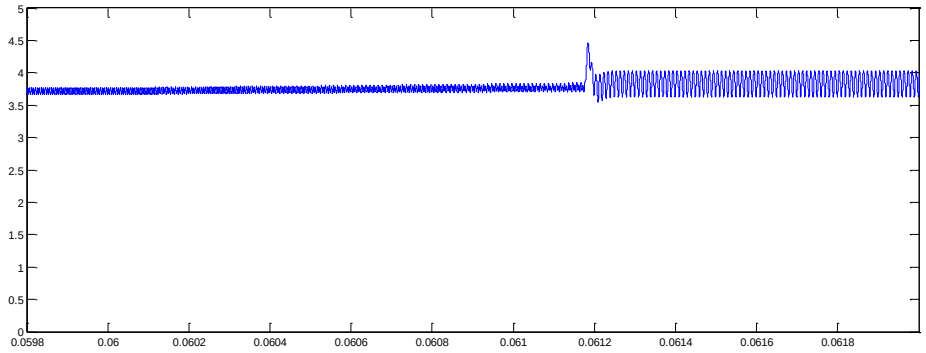

Figure 4.41 Phase-1's error voltage in converter-2 for T_d=1000 μs

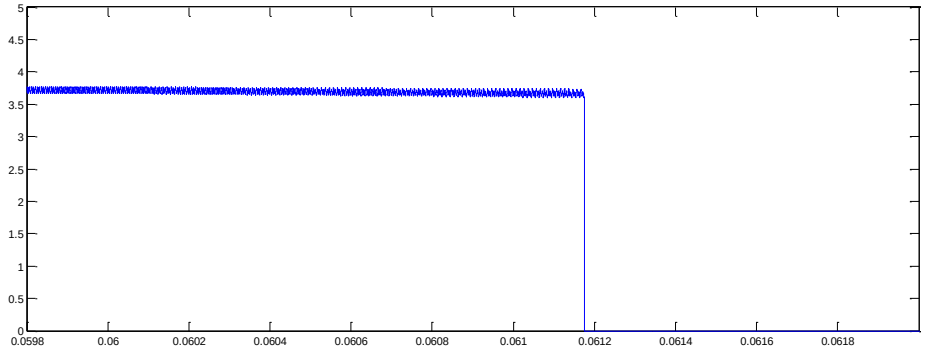

Figure 4.42 Phase-2's error voltage in converter-2 for T_d=1000 μs

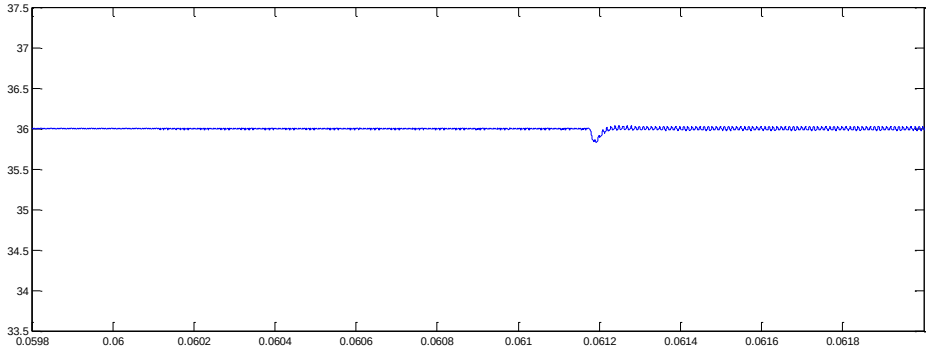

Figure 4.43 Output voltage of converter-2 for T_d=1000 μs

Table 4.5 Rise and dip in the output voltage for converter-2 during the process of phase shedding

Converter Configuration	Type of Control	Zero crossing time T_d	Percentage output voltage dip	Percentage output voltage rise
Converter-2	Simple control	-	6.38	3.33
Converter-2	Feed-forward control	-	4.86	1.66
Converter-2	Ramp control	100 μs	0.555	0.4166
Converter-2	Ramp control	500 μs	0.4166	0.138
Converter-2	Ramp control	1000 μs	0.472	-

4.5 RAMP CONTROLLED PHASE ADDING IN A MULTIPHASE CONVERTER

4.5.1 Converter 1. Ramp control is implemented for the values of T_u- 500 μs and 1 ms- and the results are compared with that of simple control and feed forward control. The first case considered is for the zero crossing time of 500 μs and the results are as given below.

The most important observation to make here is the improved current sharing behavior, as in Figure 4.44, when compared to the simple control case, as in Figure 3.5. This improved current sharing behavior equals that observed in feed-forward control, as in Figure 3.31, as well. Now, comparing Figure 4.49 with Figure 3.13 and Figure 3.35, it is observed that the output voltage behavior deteriorates a little when compared to the simple control case but improves significantly when compared to the feed-forward control case. Thus, ramp control helps achieve an improved current sharing behavior with minimized transients. The deterioration in transient behavior is attributed to the transition condition Z. Z becomes 1 only when the phase-2 current equals the average value of i_L/N and as observed from the Figure 4.47, the error voltage continues to increase and goes beyond the steady state value before Z reaches 1. This causes the transients in the system. As the value of T_u increases, the transient behavior of the system improves but at the cost of delayed current sharing.

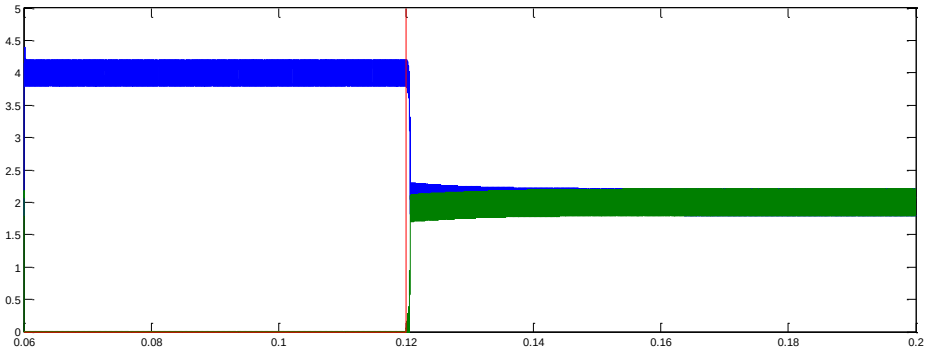

Figure 4.44 Phase current in converter-1 for T_u=500 μs

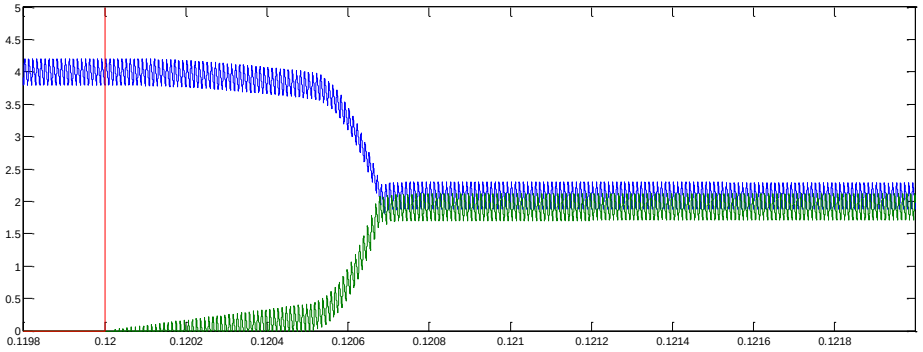

Figure 4.45 Zoomed in phase currents in converter-1 for T_u=500 μs

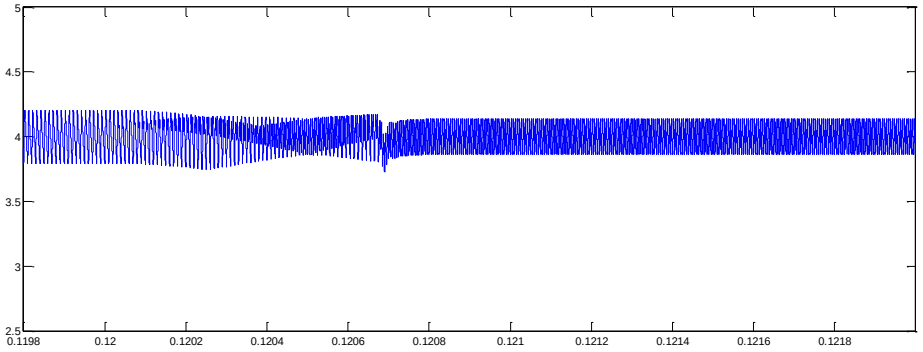

Figure 4.46 Total current in converter-1 for T_u=500 μs

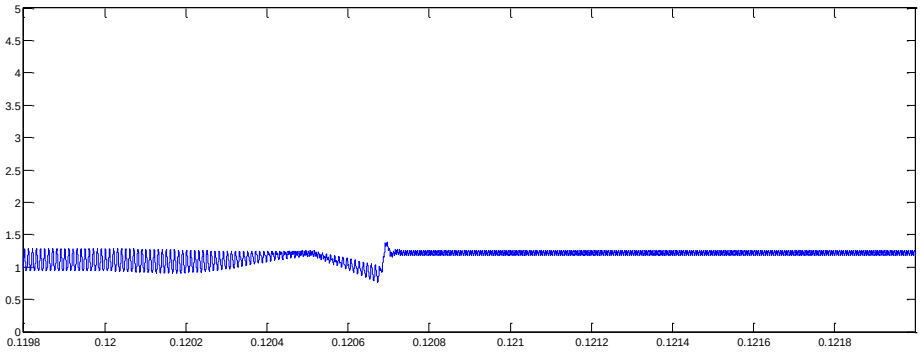

Figure 4.47 Phase-1's error voltage in converter-1 for T_u=500 μs

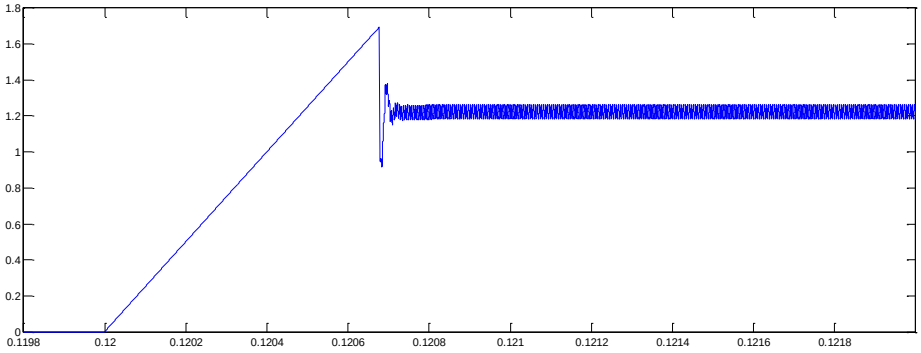

Figure 4.48 Phase-2's error voltage in converter-1 for T_u=500 μs

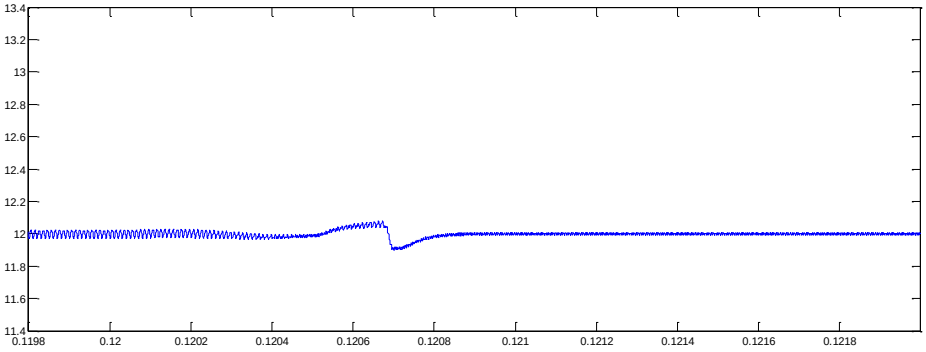

Figure 4.49 Output voltage of converter-1 for T_u=500 μs

Now the converter system is simulated for T_u=1 ms. The output voltage in Figure 4.55 is observed to have improved in transient behavior when compared with the previous case, but the current sharing is delayed by a certain period as observed in Figure 4.51. Hence it is observed that as the value of T_u increases, transient behavior improves at the cost of current sharing. Table 4.5 tabulates the transient rise and dip in the converter-1 system in terms of percentage of output voltage for the phase adding process. It is observed that in case of converter-1, though the ramp control technique is a trade-off, it works the best for phase adding process.

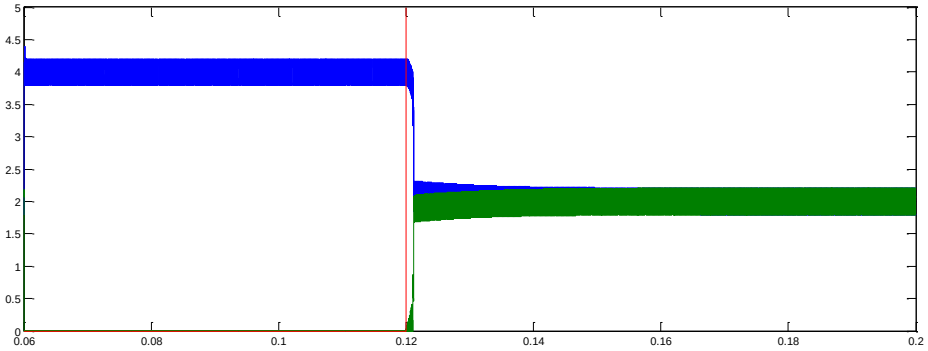

Figure 4.50 Phase current in converter-1 for T_u=1 ms

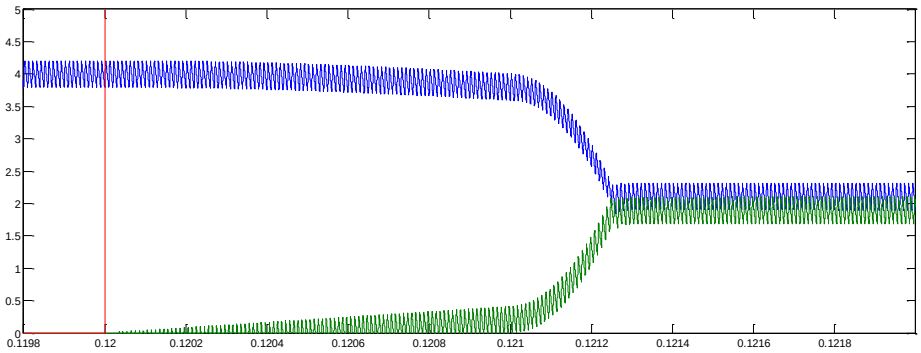

Figure 4.51 Zoomed in phase currents in converter-1 for T_u=1 ms

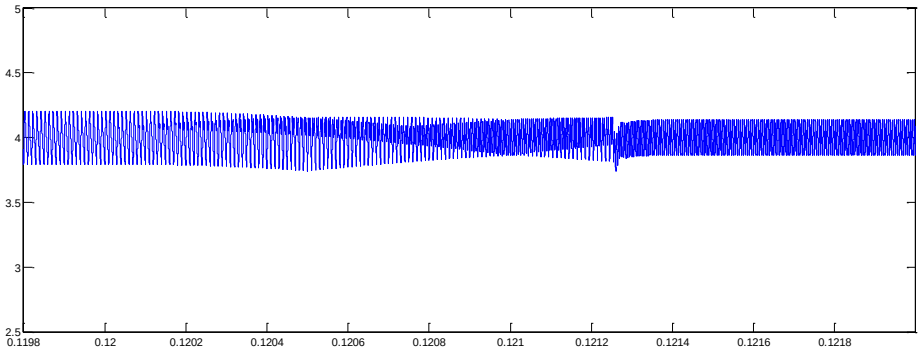

Figure 4.52 Total current in converter-1 for T_u=1 ms

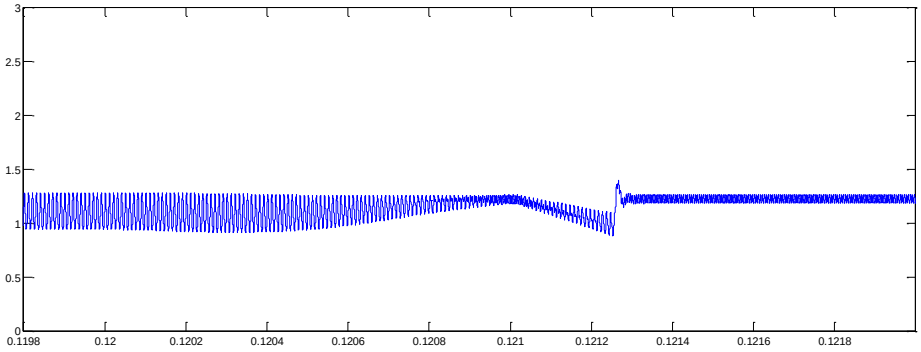

Figure 4.53 Phase-1's error voltage in converter-1 for T_u=1 ms

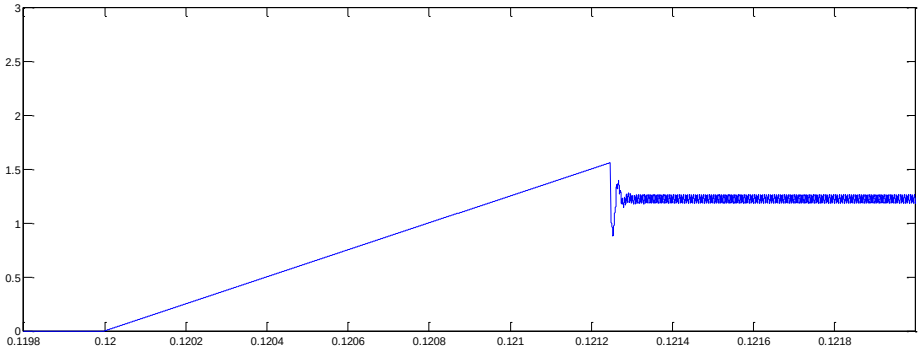

Figure 4.54 Phase-2's error voltage in converter-1 for T_u=1 ms

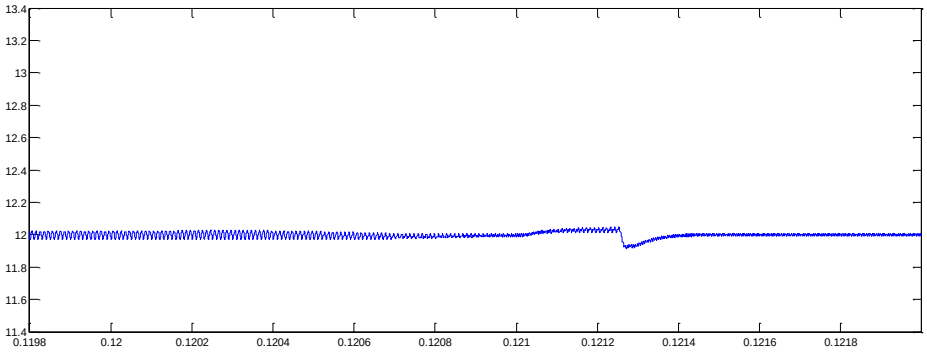

Figure 4.55 Output voltage of converter-1 for T_u=1 ms

Table 4.6 Rise and dip in the output voltage for converter-1 during the process of phase adding

Converter Configuration	Type of Control	Zero crossing time T_u	Time required to achieve current sharing	Percentage output voltage dip	Percentage output voltage rise
Converter-1	Simple control	-	0.05 s	0.833	0.416
Converter-1	Feed-forward control	-	0.03 s	4.33	9.16
Converter-1	Ramp control	500 μs	0.02 s	0.833	0.667
Converter-1	Ramp control	1 ms	0.025 s	0.667	0.416

4.5.2 Converter-2. Ramp control is implemented for converter-2 with similar values of T_d as converter and the results are compared with that of the simple control and feed forward control. The first case considered is for the T_u=500 μs and the results are as given below.

An improved current sharing behavior is observed, as in Figure 4.57, when compared to the simple control case, as in Figure 3.16. This improved current sharing behavior exceeds that observed in feed-forward control, as in Figure 3.40, as well. Now, comparing Figure 4.61 with Figure 3.24 and Figure 3.44, it is observed that the output voltage behavior deteriorates when compared to the simple control case but improves significantly when compared to the feed-forward control case. Thus, ramp control technique in converter-2, similar to converter-1, helps achieve an improved current sharing behavior with minimized transients.

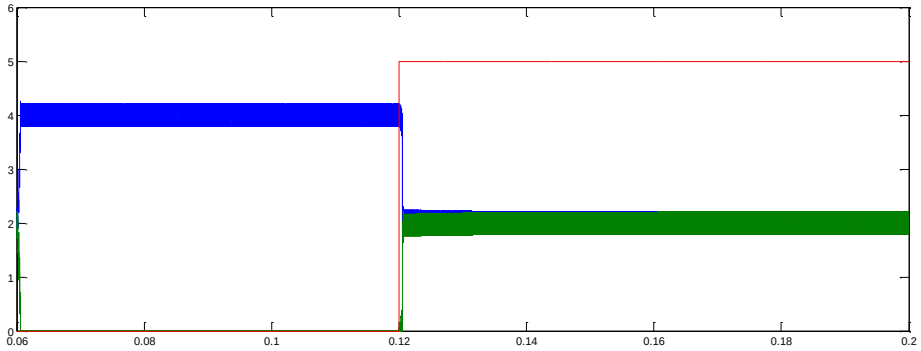

Figure 4.56 Phase current in converter-2 for T_u=500 μs

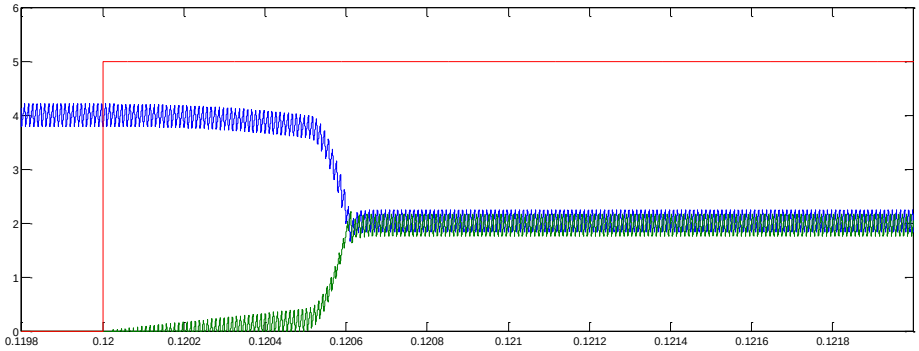

Figure 4.57 Zoomed in phase currents in converter-2 for T_u=500 μs

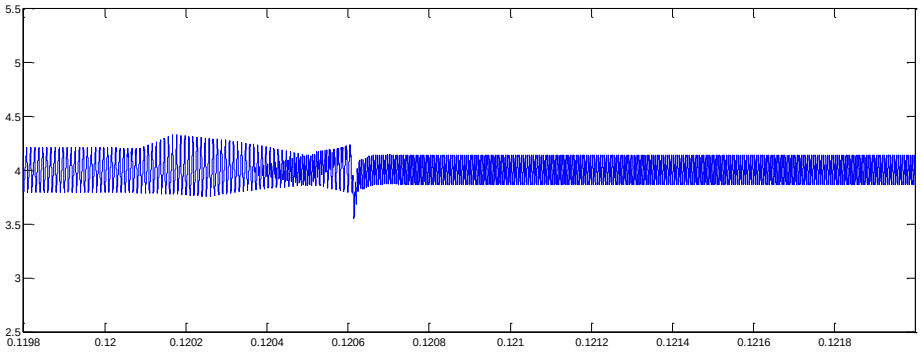

Figure 4.58 Total current in converter-2 for T_u=500 μs

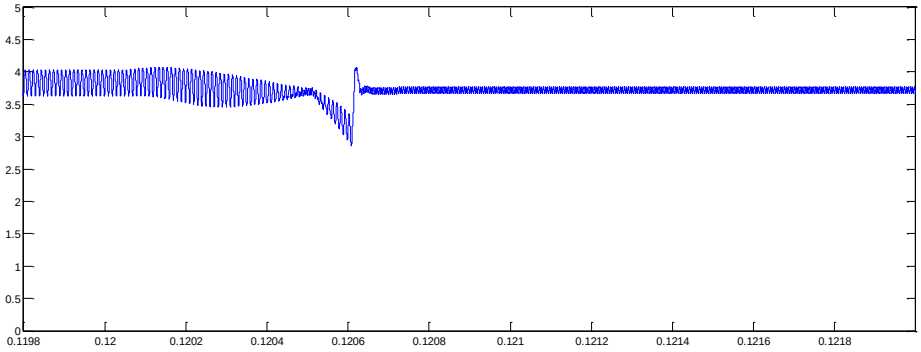

Figure 4.59 Phase-1's error voltage in converter-2 for T_u=500 μs

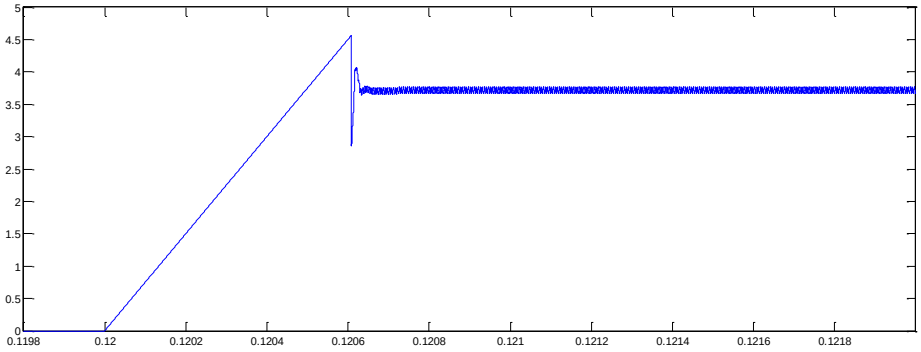

Figure 4.60 Phase-2's error voltage in converter-2 for T_u=500 μs

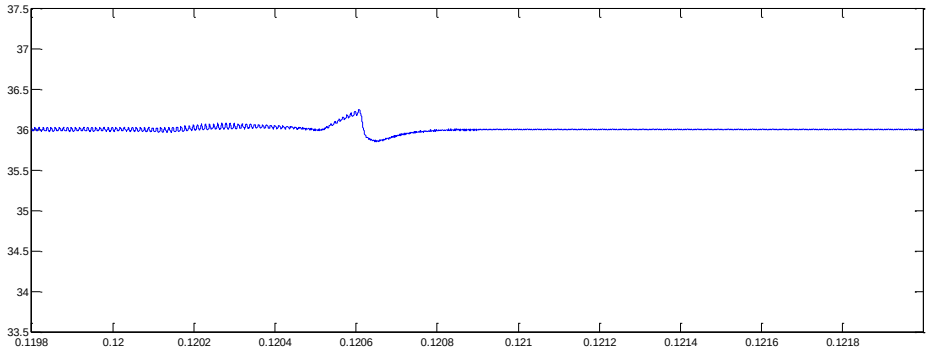

Figure 4.61 Output voltage of converter-2 for T_u=500 μs

Now the converter system is simulated for T_u=1 ms. Similar conclusions, as in converter-1, can be made here. Table 4.6 tabulates the transient rise and dip in the converter-1 system in terms of percentage of output voltage for the phase adding process.

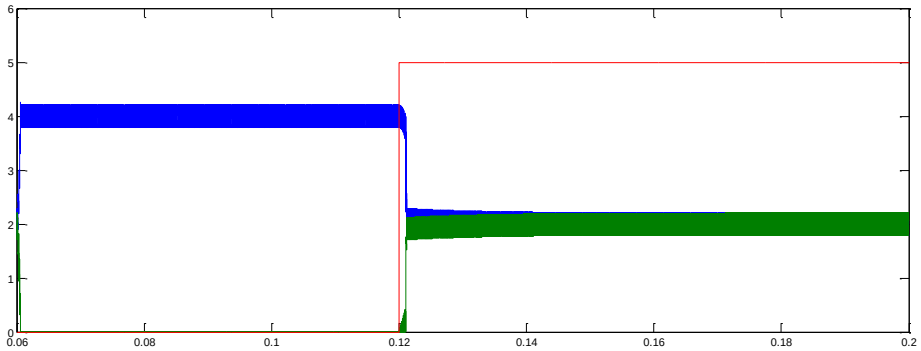

Figure 4.62 Phase current in converter-2 for T_u=1 ms

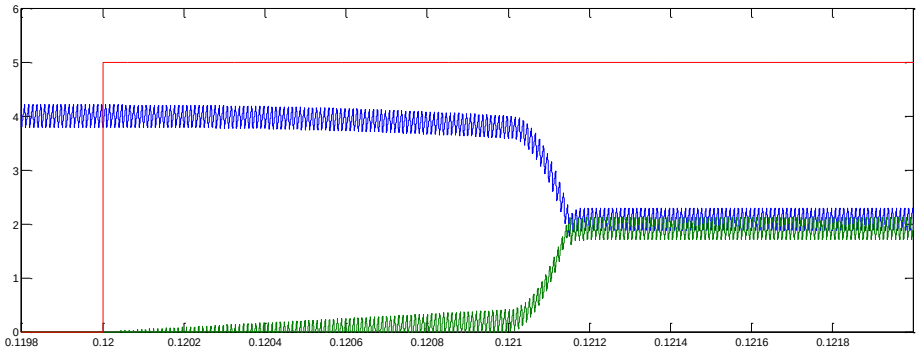

Figure 4.63 Zoomed in phase currents in converter-2 for T_u=1 ms

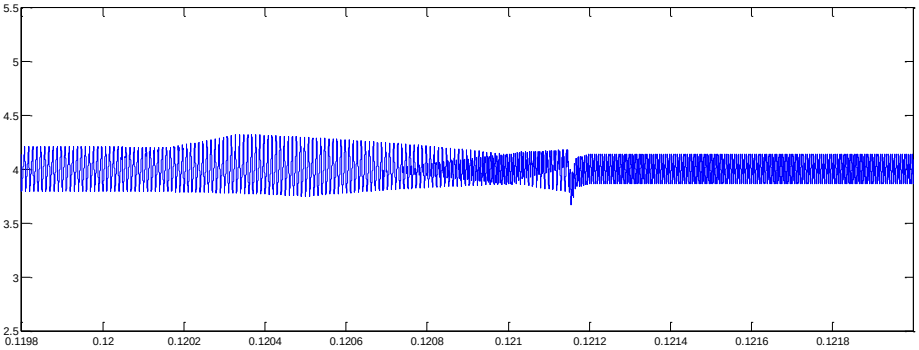

Figure 4.64 Total current in converter-2 for T_u=1 ms

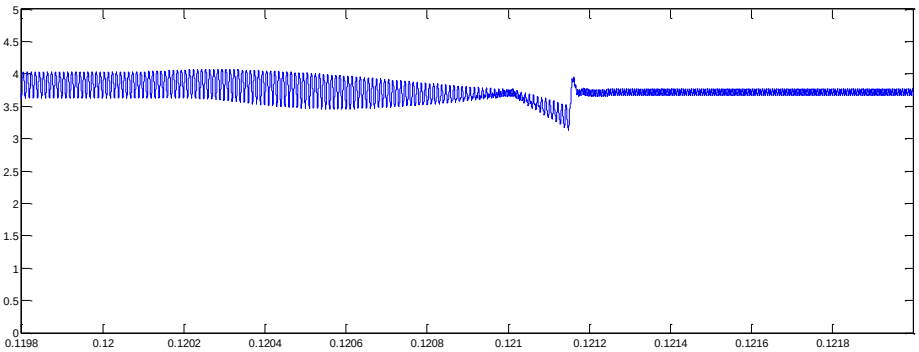

Figure 4.65 Phase-1's error voltage in converter-2 for T_u=1 ms

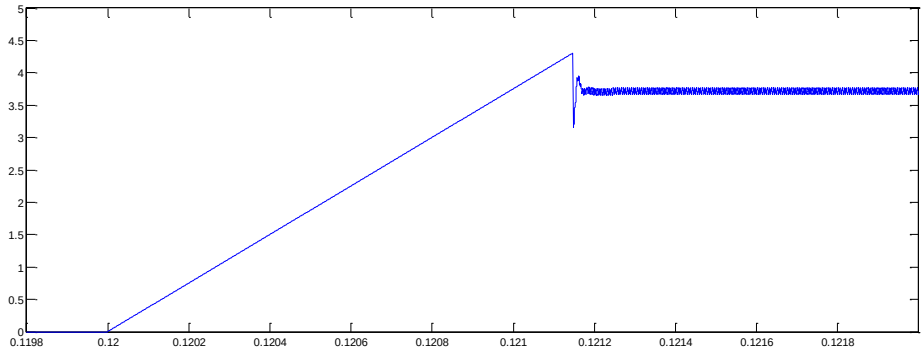

Figure 4.66 Phase-2's error voltage in converter-2 for T_u=1 ms

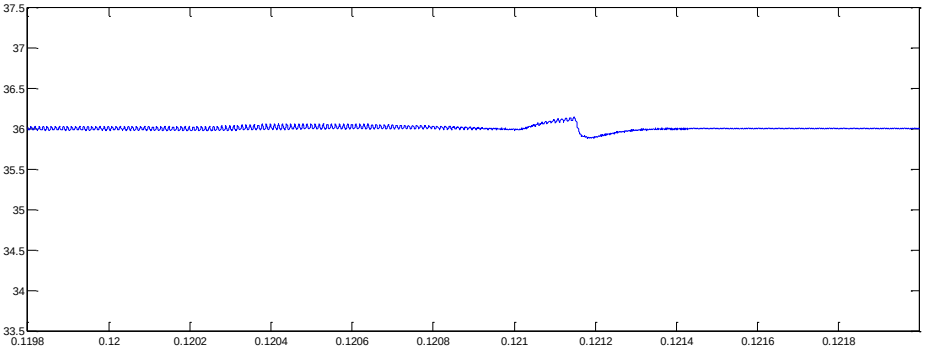

Figure 4.67 Output voltage of converter-2 for T_u=1 ms

Table 4.7 Rise and dip in the output voltage for converter-2 during the process of phase adding

Converter Configuration	Type of Control	Zero crossing time T_d	Time required to achieve current sharing	Percentage output voltage dip	Percentage output voltage rise
Converter-2	Simple control	-	0.05 s	-	0.694
Converter-2	Feed-forward control	-	0.04 s	0.694	1.66
Converter-2	Ramp control	500 µs	0.006 s	0.4166	0.694
Converter-2	Ramp control	1 ms	0.006 s	0.33	0.416

From the discussion above, it is observed that ramp control improves the performance of any converter system as a whole.

5. CONCLUSION

In this thesis, phase shedding and adding techniques in a multiphase converter have been discussed. Mathematical model of a multiphase converter is designed and constructed to observe the transient behavior of the system during the process of phase change. A new phase change technique called the ramp control technique has been proposed in this thesis. State diagrams are used to construct the appropriate controls required for this technique. Moving average analysis of the ramp control technique is done in order to estimate the slope of the duty cycle for the ramp control technique, given a certain set of parameters. Mathematical models of simple phase shedding, conventional phase shedding and ramp controlled phase shedding have been simulated in Simulink and the transient behavior of the output voltage is observed. It has been proved through simulations that the proposed ramp control technique exhibits a better dynamic performance compared to the conventional techniques in most of the cases. In phase adding technique, ramp control exhibits an improved current sharing behavior at the cost of much lesser transients unlike the conventional technique. Hence this thesis proves the superiority of the ramp control technique over the conventional methods

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VITA

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