Interferogram decodification on Nios II soft-core

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Abstract

This paper describes the implementation of an interferogram decoding system based on a Nios II embedded microprocessor. The interferograms are obtained by using the

classical Michelson Interferometer configured as the four step phase shifting profiler. This work includes the phase unwrapping solution implemented with the minimum norm method and the SoPC architecture developed with C and Verilog languages. The processing system was successfully implemented on the Nios II in a Cyclone IV FPGA. We found that the system needs an application specific hardware accelerator to improve its performance, but regardless this drawback, its capacity to unwrap is similar to other state of the art techniques.

Keywords: interferometry, Nios II soft-core, optical metrology.

1. Introduction

In modern industry, especially on micromachining, exists a special interest in techniques to perform non-destructive testing (NDT). Such techniques are used to evaluate device characteristics, such as planicity, manufacturing defects, rigidity, among others. One of the NDT methods is based on optical profilometry, a measuring technique that exploits the wave nature of light in order to estimate the surface of an object.

The key part of the optical profilometry is the interference phenomena which exploits the detection of phase change due to the path length traveled by two interfering beams. Thus, the relative heights in the sample surface are mapped into phase changes in the interfering beams, producing an interferogram; similar to the level curves in topography science. This interferograms (images) are captured by a CCD (Charge Coupled Device) and processed by the Nios II processor.

In [1] an opto-mechanical technique was used, joining the interferometry data and a nanoindentation technique with a Twyman-Green interferometer for cantilever characterization, while in [2] the technique used was white light phase shifting interferometry for micro-electro-mechanical systems (MEMS) measurement.

For most interferometry applications a general purpose system is used, to fully implement the capture and processing system or to partially do one or more tasks. In [2], the whole

acquisition, processing and display operations were done in a computer, in [3] a computer was used for the fringe processing with Fourier, and in [4] general purpose processor was used for image acquisition and 3D profile visualization.

In this paper, a system for decodification of interferograms on a self-contained Nios II based architecture is described. The interferograms contain the information of micrometric surfaces of MEMS. The Nios II is embedded on a Cyclone IV FPGA on a DE2-115 board.

2. Interferometry system

In order to measure surfaces using interferometry, an instrument capable of generating the interference and capturing the resulting signal is needed. The instrument, called interferometer, can be configured in different setups based on what is to be measured [5]. For the present project, a Michelson interferometer was used, and its configuration is shown on Fig. 1.

The interferometer has a coherent monochromatic light source, with wave length λ. The fractions of reflected light, $I'(x,y)$ and $I''(x,y)$, are captured on the CCD camera, yielding a spatial distribution of intensities that form the image or interferogram, which is mathematically expressed in (1).

$$I(x,y) = I'(x,y) + I''(x,y) + 2\sqrt{I'(x,y)I''(x,y)}\cos(\phi(x,y)) \quad (1)$$

The sample information, contained in the $h(x,y)$ argument, is part of the optical path difference information encapsulated in the $\phi(x,y)$ argument, as shown in (2). The surface information can be extracted from (2) since L_1 and L_2 are known lengths.

$$\phi(x,y) = \frac{4\pi}{\lambda}(L_1 - (L_2 - h(x,y))) \quad (2)$$

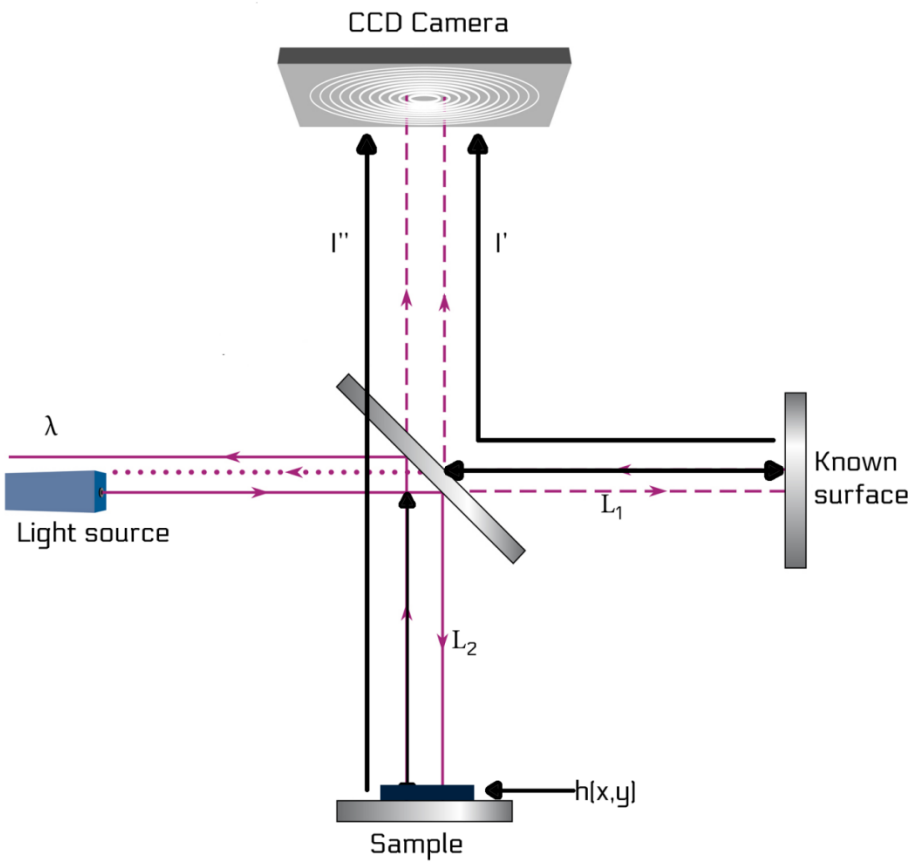

Fig. 1. Michelson interferometer.

Since there are three unknown variables in (1), a technique called phase shifting interferometry (PSI) is used to create equations by collecting a series of images with different known phases [5]. The use of PSI for the acquisition of four images, I_1 to I_4, leads to (3), which contains the data of interest [6].

$$\phi(x,y) = tan^{-1}\left[\frac{I_4(x,y) - I_2(x,y)}{I_1(x,y) - I_3(x,y)}\right] \tag{3}$$

At this point the information of the surface has been acquired but has been wrapped by the inverse tangent function. In order to get the surface information of the sample, a bidimensional phase unwrapping processing must be done on a computational architecture.

3. Bidimensional phase unwrapping on Nios II

The wrapping problem, induced by the inverse tangent on (3), refers to the bounding of all values of $\phi(x,y)$ on the $(-\pi,\pi]$ interval. There are several algorithms for phase unwrapping, which still is an open problem, depending on the source of interference, level of noise, and other parameters. For instance, on [7] two minimum L^p norm were used (PUMA and CUNWRAP), while [8] uses optimization with local weight, and [9] uses a minimal discontinuity method.

In this paper a global optimization method based on minimum L^p norm, with $p = 2$, is used [10]. In this case, the minimum square phase unwrapping problem is reduced to the solution of the Poisson equation, defined in (4), where ϕ corresponds to the estimated resulting image (surface) and ψ corresponds to the wrapped image obtained with (3).

$$\phi_{xx} + \phi_{yy} = \psi_{xx} + \psi_{yy} \tag{4}$$

Since the problem is on the discrete domain, (4) is discretized with the finite difference method for its implementation on Nios II using mirrored boundary conditions and is expressed as (5),

$$\left(\phi_{i+1,j} - 2\phi_{i,j} + \phi_{i-1,j}\right) + \left(\phi_{i,j+1} - 2\phi_{i,j} + \phi_{i,j-1}\right) = \rho_{i,j}, \tag{5}$$

where

$$\rho_{i,j} = W\{\psi_{i+1,j} - \psi_{i,j}\} - W\{\psi_{i,j} - \psi_{i-1,j}\} + W\{\psi_{i,j+1} - \psi_{i,j}\} - W\{\psi_{i,j} - \psi_{i,j-1}\},$$

and the W operator assures that all values are on the $(-\pi,\pi]$ interval. The values i,j determine the position of the pixel on a rectangular grid of M columns and N rows, respectively. Based on the equation for each pixel on the image, a total of $K = M \times N$ unknows are obtained. All K equations are organized into a linear system of the form $Ax = b$.

Some properties of the resulting A matrix are: square, sparse, large, and non-symmetric. A numeric simulation was performed with the numeric methods present at the MATLAB software package, test shown in table 1, and the one that yielded best results in terms of iterations and memory usage was the stabilized biconjugate gradient (BiCGSTAB). The method with less iterations is *bicgstabl*, followed by *bicgstab*, and the *qmr*-based. However, the *bicgstabl* method requires more memory as the l increases ($l = 2$ doubles the memory, and $l = 1$ equals the bicgstab method). Taking into consideration memory usage, the *bicgstab* method was chosen.

Numeric method (MATLAB name)	**Iterations at image dimensión**		
	256x256	**512x512**	**1024x1024**
bicg	844	1633	3191
bicgstab	604	1169	2940
bicgstabl	330	573	1331
cgs	822	1449	3047
gmres	11325	53455	156660
lsqr	19020	38063	38991
minres	935	1872	3578
qmr	768	1479	2803
symmlq	1138	2409	4826
tfqmr	836	1445	2805

Table 1. Iteration number comparison.

After the numeric method was chosen, the implementation of the algorithm for phase unwrapping with application in optical interferometry was made by coding the solution on C language and downloading it into the Nios II architecture. The needed numeric representation was set at double-precision floating point because the other representations, single precision float and fixed point, did not converge to correct solution.

The software architecture, shown in Fig. 2, was coded using the C language. The functions include image reading from SD card, creation of wrapped image from four input images, calculation of ρ vector, the numeric solver, and image display on LCD screen.

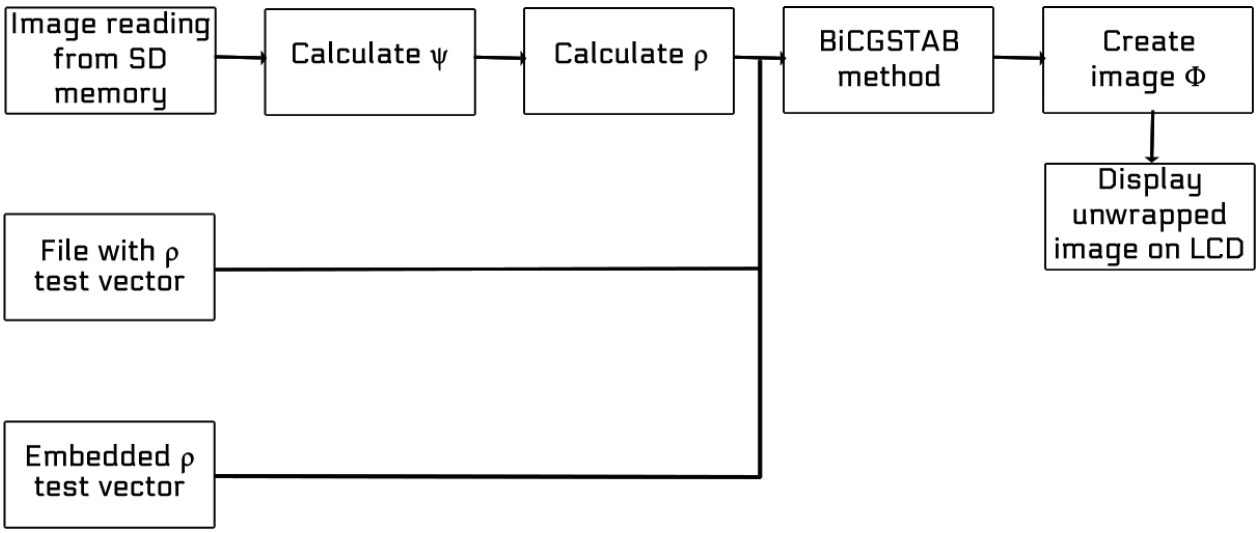

Fig. 2. Software architecture for phase unwrapping system.

The BiCGSTAB algorithm, and functions related to the image acquisition and processing, were programmed in C language since the Nios II embedded processor supports most of the language standard. The Nios II is contained within an FPGA that has access to other peripherals, e.g. RAM memory, Ethernet port, VGA output, and the communication with these devices must be made using a hardware description language (HDL). The hardware architecture, described with the Verilog HDL, is shown in Fig. 3 and is deployed in a TerASIC VEEK-MT (DE2-115) board with an Altera Cyclone IV FPGA.

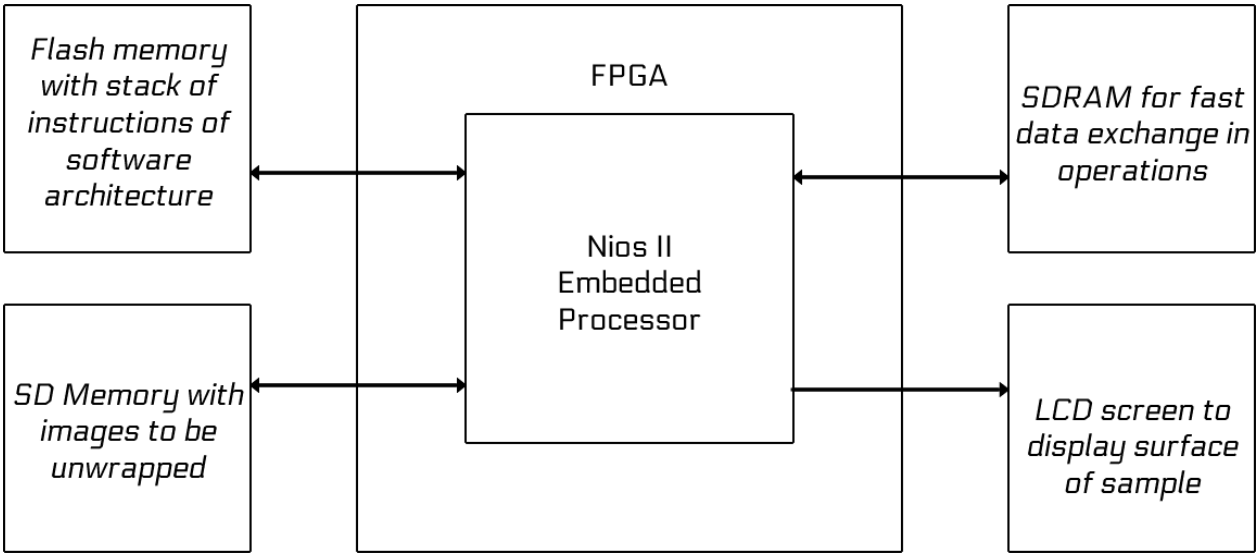

Fig. 3. Hardware architecture for phase unwrapping system.

In the figure the most significant operations are described: exchange of information with the instructions stack stored at flash memory, data exchange on the RAM for numeric operations, read and write operations of image data, and interface with LCD multi-touch screen.

Figures 2 and 3 describe the complete design of a system-on-programmable-chip (SoPC) [11] for surface characterization using phase shifting interferometry.

4. Results

The solution was coded using C language standard and that gives extra flexibility in terms of platform compatibility. With minor changes in the code, the tests were made on a DELL T7500 workstation with a four-core Intel Xeon E5620 at 2.4GHZ and on the Nios II embedded microprocessor on the Cyclone IV FPGA at 50MHz. Table I shows

convergence time for the BiCGSTAB numeric method on both architectures using generated surfaces.

Architecture	**Image dimensions**			
	64x64	**128x128**	**256x256**	**512x512**
CPU – Intel Xeon	20ms	190ms	2s	15s
FPGA – Nios II	207s	1712s	14926s	117037s

Table 2. Time of convergence comparison between CPU and Nios II.

As shown in table 2, the Intel Xeon CPU performed the phase unwrapping thousands of time faster, from three to four orders of magnitude. The qualitative result is shown in Fig. 4, corresponding to three microlenses samples, first row corresponding to the captured wrapped image; second row, the unwrapped surface in two-dimensions; and third row, surface plotted in 3D.

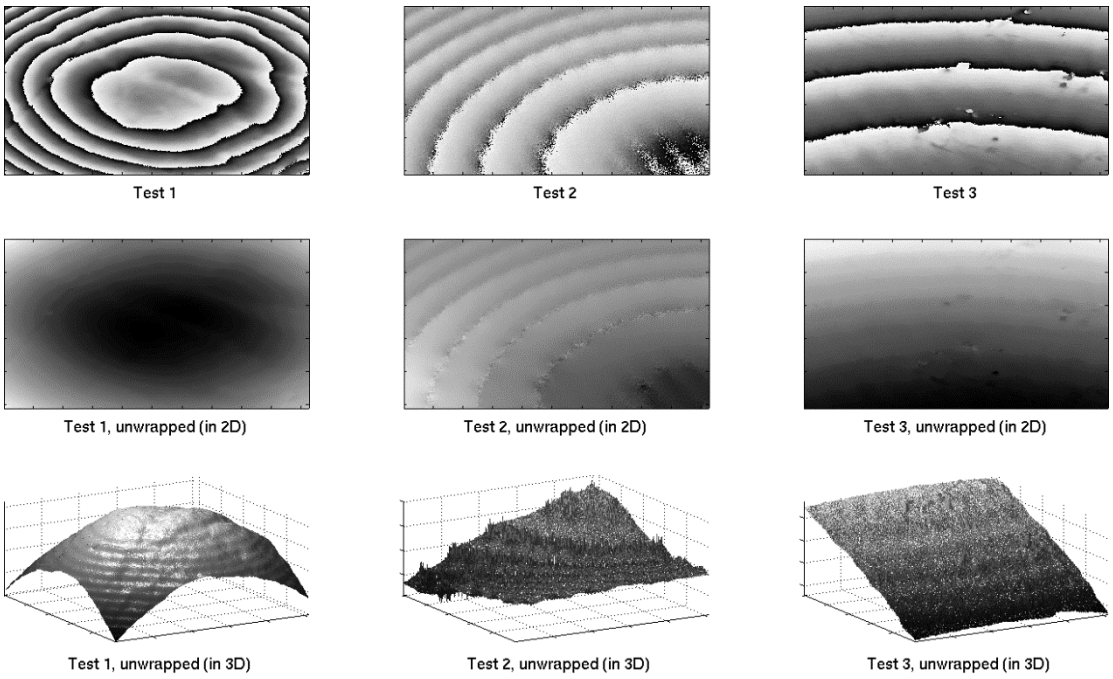

Fig. 4. Unwrapped images.

Test 1 and 3 are successfully unwrapped to the expected result, but test 2 contains "bumps" since the image was scaled to half its original size and had aliasing. In both architectures, Nios II and CPU, the images were unwrapped on the same iteration number and yielded the same residual error.

5. Discussion

As mentioned on the results section, the CPU performs the phase unwrapping approximately four orders of magnitude faster when compared to the Nios II based architecture. This result is expected since the FPGA implementation is limited to the Nios II output, which contains only one 32-bits ALU operating at 50MHz.

Furthermore, the performance is also reduced by the double precision floating point operations required by the numeric method. The Nios II is a 32-bit architecture and all the 64-bits logic is emulated in software, slowing the system overall performance.

In related works, as [12] and [13], the processing of the phase unwrapping is avoided on the FPGA since it would take most logic space, and is discarded as an option given the time it would take to design the linear algebra components needed.

According to the post-synthesis report, an 8% of the total resources of the FPGA logic elements were used, most of them in the Nios II. Therefore, a hardware accelerator for the BiCGSTAB method is proposed as future work in order to reduce the processing time in the Nios II based system.

6. Conclusion

As demonstrated on this paper, it is possible to create a SoPC for bidimensional phase unwrapping applications and reduce the dimensions from a general purpose computer to a DE2-115 board.

The aim of this project is to create a portable system for micrometric surface characterization. On this first iteration, the system was taken from CPU to an FPGA board with embedded microprocessor. Future work includes hardware accelerators and physical synthesis for ASIC manufacturing.

7. Acknowledgements

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8. References

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