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Automated channel emulator based on MEMS switch and improvement of signal transition

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AUTOMATED CHANNEL EMULATOR BASED ON MEMS SWITCH AND IMPROVEMENT OF SIGNAL TRANSITION

by

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ABSTRACT

Channel Emulator, which is widely used in communication system development, is an instrument that emulates the real-world signal propagation environment between transmitter and. To overcome the disadvantages of traditional channel emulator, we propose a novel structure of the automated channel emulator in Section 1, which can be controlled by software and integrated into auto-testing system. MEMS switch, with good RF performance, is used to connect and isolate multiple channels.

In Section 2, we divide the whole channel emulator system into Channel, Support, and Controller Board, and provide detailed design procedures with critical parameters of each board. The well-designed high frequency channel traces are validated by both 2D/3D simulation models and analytical calculations. The automated control logic and driven mechanism are also illustrated by sequence and block diagram.

In Section 3, we perform post-simulation after the completion of PCB layout to check the RF performance of the real PCB board. Then manufacture and assemble the whole system of the automated channel emulator.

In Section 4, we study the discontinuities in channel path in a systematically approach, including: channel trace turns, connector transient tapering, wire-bonding and solder parasitic effects. Analysis, simulations and measurements are performed to provide improvement solutions of signal transition.

Section 5 concludes this thesis work and discuss about the future plan to expand our channel emulator design to differential solution.

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1. INTRODUCTION

1.1. BACKGROUND

Channel Emulator is an instrument that emulates the real-world signal propagation environment between transmitter and receiver in serial link system. It is widely used in communication system development to evaluate the signal transition and response when either the real channel is not available or channel characteristics are varying [1], [2]. As the data propagation speed increases beyond several GBit/s in recent years, channel emulation is becoming increasingly important to ensure the system performance in early R&D, verification and validation work.

The channel loss between transmitter and receiver is a critical element for the receiver test for all electrical multi-gigabit serial interfaces. The channel loss depends primarily on the distance between transmitter and receiver and the electrical medium [3]. To emulate the loss for certain frequencies, the fundamental structure of channel emulator should be consist of several switchable channels with different lengths. Another key element for channel emulator is the frequency range, which determines the range of data speed that can be accurately emulated by this instrument. The maximum working frequency of the modern Channel Emulators on the market varies from 3GHz to 16GHz [3], [4], [5], [6], [7]. With the rapidly increasing data speed of signal in today's industry, designing a channel emulator with larger frequency range is in great demand.

Traditional channel emulators have one pair of connectors as the interface for each internal channel between the transmitter and receiver, so multiple channels with different lengths need multiple pairs of connectors to get accessed out of the channel emulator, see Figure 1.1. There are three main disadvantages of this conventional

emulator design: (1) When people wants to switch from one channel to another, This design requires people manually remove testing cables from one pair of connectors and attach them to another pair. The involving of human activity makes it impossible for this type of channel emulator to be integrated into modern auto-testing system. Thus the testing efficiency will be greatly affected. (2) The connector is very expensive especially for the high precision type, multiple pairs of connectors will increase the overall cost dramatically. (3) The connectors could be gradually worn out or accidentally damaged every time when people remove or attach cables to them. This design requires excessive usage of connectors, thus the life span of the channel emulator would be limited.

Figure 1.1. Traditional Channel Emulator Agilent M8048A [3]

1.2. NOVEL STRUCTURE OF AUTOMATED CHANNEL EMULATOR

To overcome the disadvantages of traditional design of channel emulator and achieve larger frequency range. We focus on building an automated channel emulator which works from DC to 20GHz. Instead of using multiple pairs of connectors for each channel, the novel structure of our designed automated channel emulator includes only one pair of connectors for single-ended communication system (two pairs of connectors

for differential communication system). All of the internal channels are connected to the RF switches and share the connectors as the interface to testing cables. The RF switches can also be controlled by software to select and enable different channels automatically, so our designed automated channel emulator can be easily integrated into Industry Company's auto-testing system. The comparison between traditional channel emulator and automated software controlled channel emulator is shown in Figure 1.2.

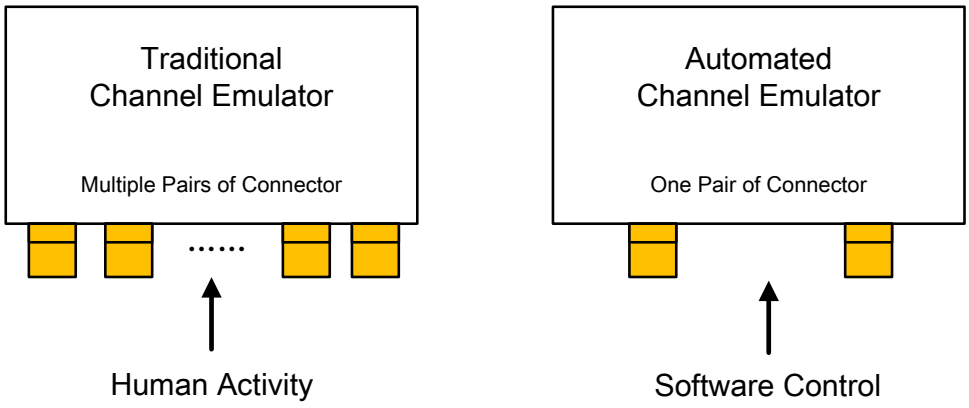
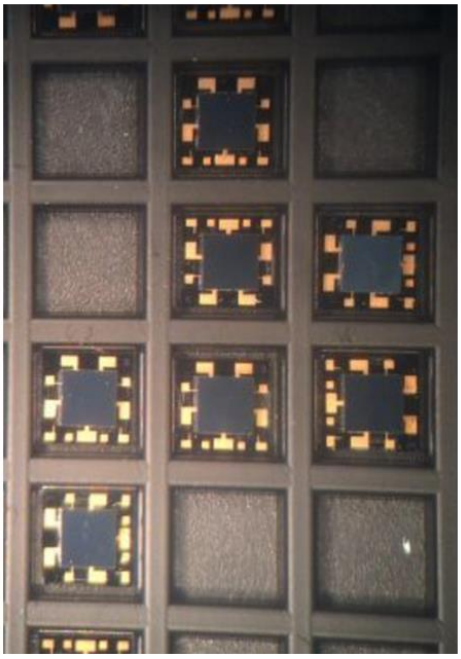
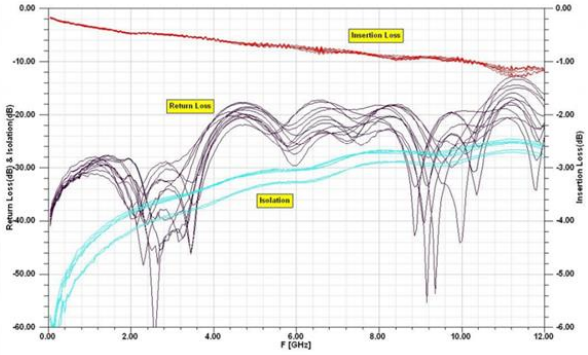


Figure 1.2. Comparison between Two Types of Channel Emulators

A special RF switch, MEMS switch, is used to connect and isolate multiple channels. MEMS, which is short for Micro-Electro-Mechanical Systems, is an evolving technology using miniaturized mechanical and electro-mechanical elements at a sub-millimeter scale. The RF MEMS switch is a specific MEMS designed to operate at radio frequencies [8]. Compared with other RF switches, such as the Solid State Switch which has high insertion loss and narrow frequency range, the MEMS switch provides the

following features: 1) Wide working frequency range; 2) Very high isolation; 3) Very low insertion loss 4) Near-zero power consumption [9]. These features are the most critical advantages for MEMS switch to be used on high frequency channel emulators. Figure 1.3 shows the appearance and specification, Figure 1.4 shows the dimension of the MEMS switch from Radant MEMS Inc.. We can find that: (1) The MEMS switch is extremely small in size, so the channel width cannot be too wide to connect to the MEMS switch. (2) The MEMS switch is only a die without package, so we need to do wire-bonding to reach its pads. (3) The RF performance of MEMS switch is good based on the given specification.





Frequency	Return Loss (dB) (input and output)	Isolation (dB)	Insertion Loss (dB)
50 MHz	-40.0	58.0	0.20
2 GHz	-29.0	38.0	0.43
4 GHz	-21.0	34.0	0.60
6 GHz	-29.0	30.0	0.70
8 GHz	-18.0	27.0	0.90
10 GHz	-19.0	26.0	1.00
12 GHz	-16.0	26.0	1.20

Figure 1.3. Appearance and Specification of Radant MEMS Switch [10]

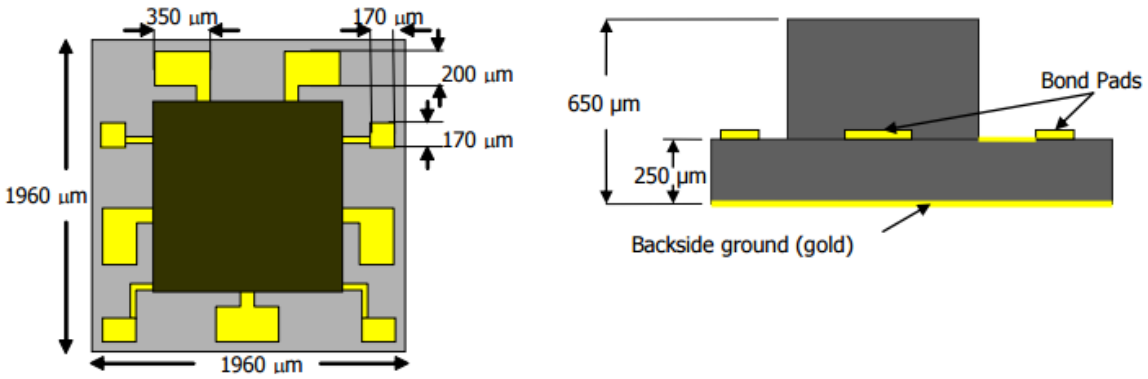


Figure 1.4. Dimension of Radant MEMS Switch [10]

1.3. PRE-MEASUREMENT OF MEMS SWITCH

To validate the RF performance of MEMS switch, we complete pre-measurement on an evaluation board with SP6T MEMS Switch from Radant MEMS Inc. We plan to measure the S-parameter (including S21 and S11) of this evaluation board and compare the results with the insertion and reflection loss from its datasheet. Based on the information, we can get to know the typical performance for the MEMS switch.

Using 20GHz VNA, we connect one of the source port of evaluation board to VNA Port 1 and connect the drain port of evaluation bard to VNA Port 2. Other unused source ports are terminated with 50 Ohm impedance. Even though the MEMS Switch can work up to 20GHz, the evaluation board can only work up to 12GHz due to the imperfect design of transmission line and low quality SMA connectors. The most critical settings of 20GHz VNA is listed below:

- Frequency: 50M ~ 12GHz
- Power: -20dB
- Sweep points: 1601

DC Power supply is 5V. This MEMS switch on the evaluation board is driven by another 5V-to-90V DC-DC voltage booster on a separate board. The setup is shown in Figure 1.5.

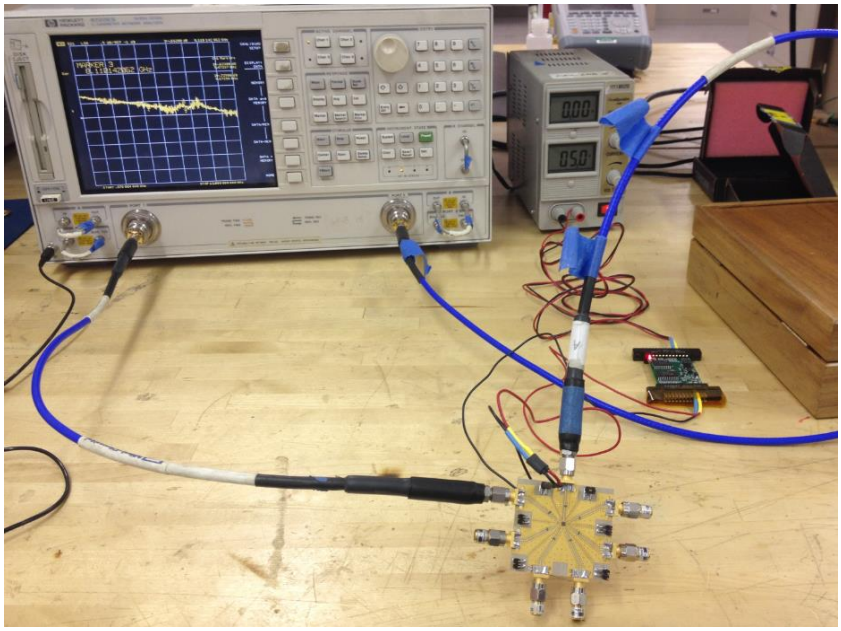


Figure 1.5. Pre-Measurement Setup for MEMS Switch Evaluation Board

The measured S-Parameters are shown in Figure 1.6. The S11 waveforms are generally below -16dB from DC to 12GHz, the maximum value is -15.1dB at 11.12GHz. The S21 waveforms are -0.2dB at 50MHz and -1~-1.2dB at 12GHz. The measurement results are matched very well with the datasheet from Radant MEMS Inc [11], and we can find that the insertion loss is very small and reflection loss is very high from the measured results, so the good RF performance of the MEMS switch can be validated.

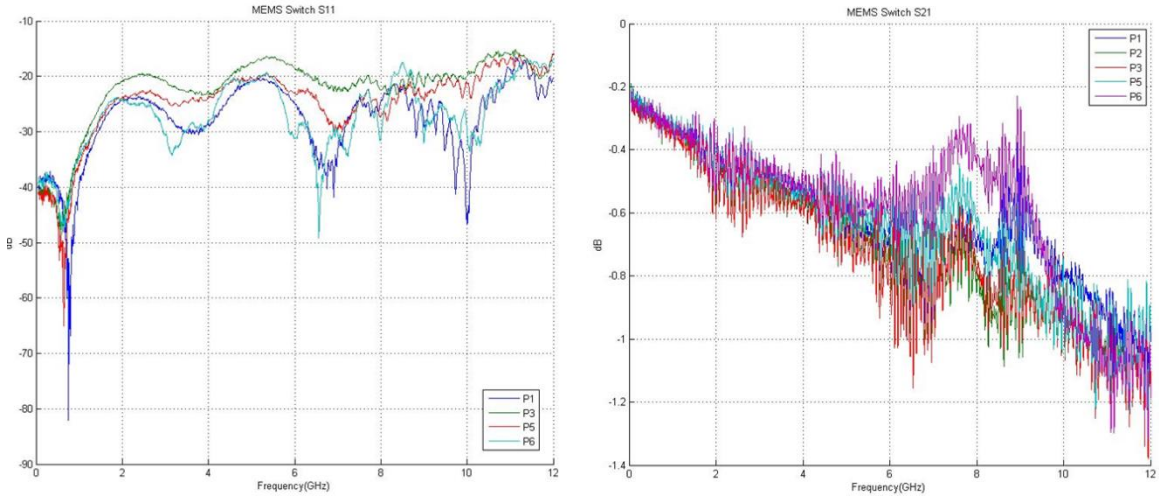


Figure 1.6. S11 (left) and S21 (right) of MEMS Evaluation Board

2. MEMS SWITCH CHANNEL EMULATOR SYSTEM DESIGN

Based on the functionality, we divide the whole channel emulator system into three boards: (1) Channel Board, which contains connectors, well-designed high frequency traces and MEMS switches. (2) Support Board, which is built for mechanical reason to prevent the Channel Board from bending or damaging. It also contains the vertical headers to deliver driven voltage. (3) Controller Board, which has MCU and DC-DC voltage booster that provides controlling mechanism and driven voltage for MEMS switches, see Figure 2.1.

The well-designed high frequency traces on Channel Board have different loss and responses at different frequencies, each trace can form a transmission path between transmitter connector and receiver connector. Channel path can be selected between these well-designed traces by the MEMS switches to emulate different types of channels in real world. A Python script is running on the MCU of Controller Board, which provides a GUI interface and high-level APIs for user interaction and test system integration. The control logic will be translated by MCU into the driven voltage to enable MEMS Switch, the driven voltage will be supplied from Controller Board to the Support Board through the pins of the vertical headers, then delivered to the MEMS Switch on Channel Board.

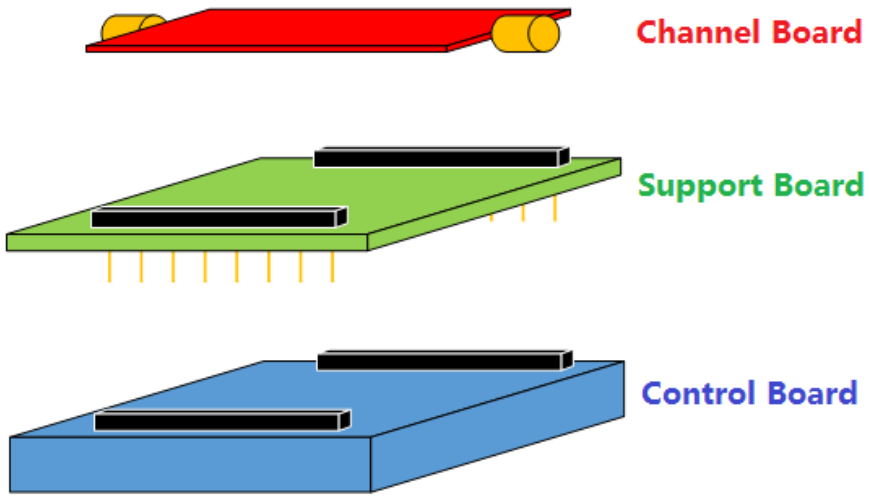


Figure 2.1. Structure of MEMS Switch Channel Emulator

2.1. GENERAL DESIGN OF CHANNEL BOARD

Channel Board consists of three main components: *End-Launch Connector*, *High Frequency Channel Trace* and *Channel Path Switch*, see Table **2.1**. *End-Launch Connector* is the input/output interface of the Channel Board. There is only one pair of connectors on Channel Board, different channel paths are formed by different *High Frequency Channel Traces* with different lengths, and the selection mechanism is controlled by the *Channel Path Switches*. Detailed information is shown below.

- End-Launch Connector: we use high precision 2.40mm connectors from Southwest Microwave, part number is 1492-04A-6.
- High Frequency Channel Trace: we design transmission line structure for the high frequency channel trace, which should maintain 50ohm characteristic impedance from DC to 20GHz.

- Channel Path Switch: we use 6-Channel (SP6T) MEMS switch RMSW260 from Radant MEMS as the channel path switch, which can maintain low insertion loss and high isolation from DC to 20GHz.

Table 2.1. Channel Board Components Table

Component	**Part**	**Note**
End Launch Connector	Southwest Microwave 1492-04A-6 [13]	2.40mm Female, Low Profile
High Frequency Channel Trace	Well-designed Transmission Line	50ohm Characteristic Impedance, Coplanar Waveguide Structure
Channel Path Switch	Radant MEMS RMSW260 [10] and RMSW240 [11]	SP6T or SP4T MEMS Switches, Works Up to 20GHz

From the definition of the components on the Channel Board, it can be concluded that the channel path from transmitter to receiver starts from one *End-Launch Connector*, through several pairs of *Channel Path Switches* and the *High Frequency Channel Traces* between them, then ends at the other *End-Launch Connector*. We define a pair of *Channel Path Switches* and the *High Frequency Channel Traces* connected to this switch pair as one *Channel Block*. Figure 2.2 shows the structure of Non-Cascading Single Block Channel Board. If we use SP6T MEMS switch in the *Channel Block*, there will be 6 High Frequency Channels available to choose for the channel path.

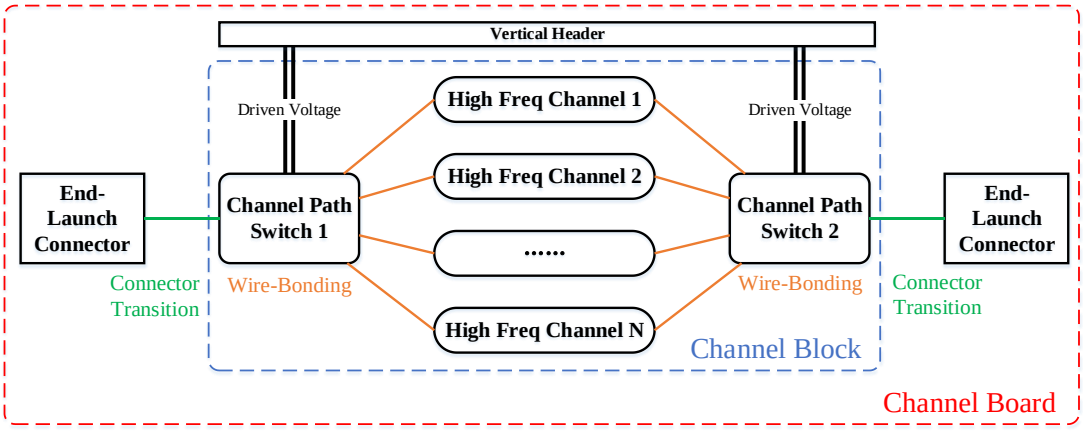


Figure 2.2. Structure of Non-Cascading Single Block Channel Board

To further increase the number of channels as well as variation of channel lengths, we can cascade multiple *Channel Blocks* between two *End-Launch Connectors*. By cascading the *Channel Blocks*, the total channel length will be determined by the selected channel in each *Channel Block*, so the total number of channels will be:

$$N = \sum_{i=1}^{m} N_i, m \geq 1$$

where N is the total channel number, N_i is the channel number in each *Channel Block*, m is the number of cascaded *Channel Blocks*.

Figure **2.3** shows the structure of Cascaded Multi-Blocks Channel Board. If we cascade two *Channel Blocks*, in each *Channel Block* we use SP6T MEMS Switch, we will have 6 channels in each *Channel Block* and the total channel number will be 36. To maximize the variation of channel lengths, the variation of channel's length in *Channel Block 2* should be larger than the maximum difference of channel's length in *Channel Block 1*. Table 2.2 shows one example of the Cascaded Multi-Blocks channel length:

- Maximum difference of channel's length in Channel Block 1 is 25mm (45mm longest minus 20mm shortest)
- Variation of channel's length in Channel Block 2 is 30mm.
- The total channel lengths of two Channel Blocks will be vary from 40mm to 215mm with a fixed 5mm step (36 different lengths in total)

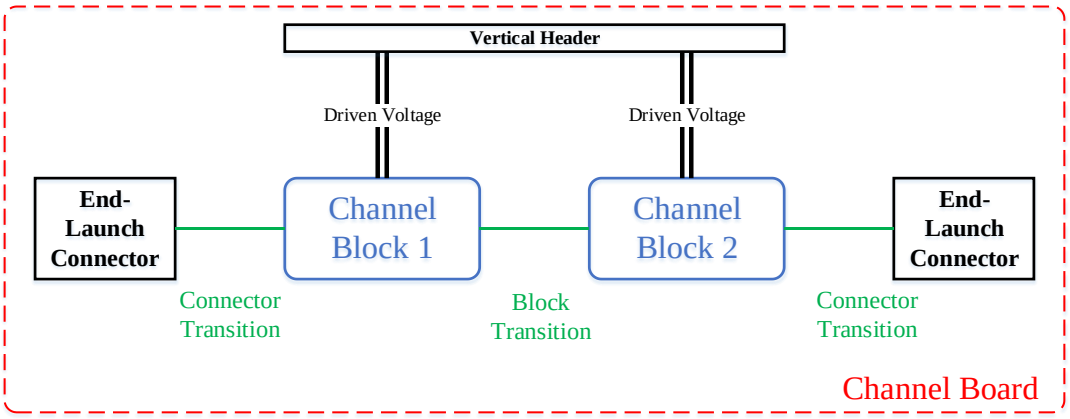


Figure 2.3. Structure of Cascaded Multi-Blocks Channel Board

Table 2.2. Cascaded Multi-Blocks Channel Length Example

Channel Length	Channel Block 1	Channel Block 2
Channel 1	20mm	20mm
Channel 2	25mm	50mm
Channel 3	30mm	80mm
Channel 4	35mm	110mm
Channel 5	40mm	140mm
Channel 6	45mm	170mm

2.2. DESIGN OF HIGH FREQUENCY CHANNEL TRACE

We are designing the high frequency channel trace based on transmission line structure. We need to determine the critical parameters of channel traces based on 2D/3D simulations. For 2D cross-section simulation, we use Q2D and FEMAS, for 3D full wave simulation, we use HFSS and CST. The design procedure is shown in Figure 2.4.

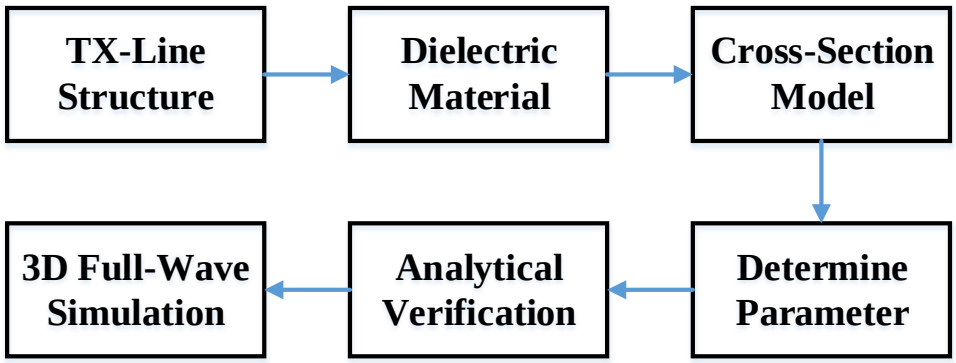


Figure 2.4. Channel Trace Design Procedure

2.2.1. Structure of Channel Trace. As discussed above, the structure of channel trace is a transmission with 50ohm characteristic impedance. To reduce the fabrication cost and difficulty, we choose to design a two-layer board. There are two common types of transmission line structure for two-layer board: Coplanar waveguide and Microstrip. Coplanar waveguide is preferred since it can allow us to narrow the trace almost arbitrarily for a given layer thickness while maintaining 50 ohm impedance.

Coplanar waveguide is a type of electrical transmission line which can be fabricated using the printed circuit board technology, and is used to convey microwave-

frequency signals [14]. Conventional coplanar waveguide (CPW) consists of a single conducting track printed onto a dielectric substrate, together with a pair of return conductors, one to either side of the track. All three conductors are on the same side of the substrate, and hence are coplanar. The return conductors are separated from the central track by a small gap, which has an unvarying width along the length of the line. Away from the central conductor, the return conductors usually extend to an indefinite but large distance, so that each is notionally a semi-infinite plane. Here we are actually using conductor-backed coplanar waveguide (CBCPW) [15]. CBCPW is a common variant of coplanar waveguide which has a ground plane covering the entire back-face of the substrate. The ground-plane serves as a third return conductor (see Figure 2.5).

The important parameters affecting the characteristic impedance includes: dielectric constant, signal trace width, gap spacing between signal trace and adjacent ground, thickness of dielectric, copper thickness, grounding via center-to-center distance, distance between signal trace and grounding via [16], [17], [18].

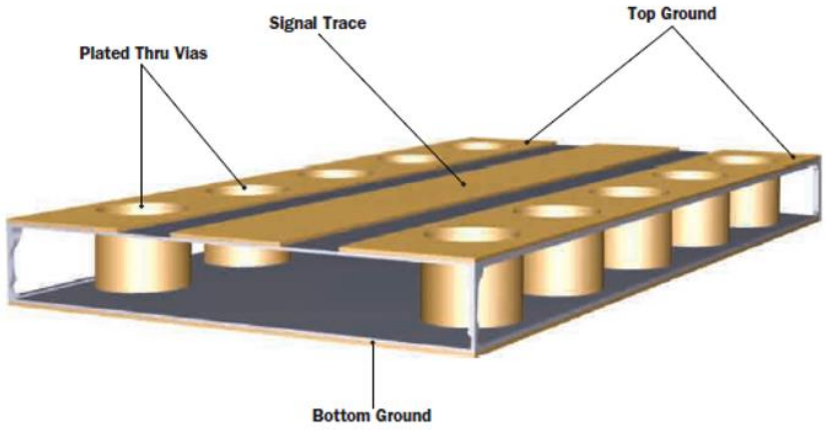


Figure 2.5. Conductor-Backed Coplanar Waveguide (CBCPW) [16]

2.2.2. Dielectric Material of Channel Trace. The dielectric material will affect the characteristic impedance, the per-unit-length loss of channel trace, the manufacture process as well as the overall cost.

Considering the ease of PCB board fabrication, electrical performance and cost, we choose types of dielectric materials for two different Channel Board designs: (1) Rogers 4350B [19] will be used for the low-loss version of Channel Board. (2) FR-4 [20] will be used for the low-cost version of Channel Board. Both materials can be manufactured into an extremely thin board (10mil thickness). Thin PCB board could help us narrow down the width of the signal trace while maintaining 50ohm characteristic impedance, so the channel traces can approach closely to the MEMS switch to reduce the wire-bonding loop. The comparison of the two materials is shown in Table 2.3.

We choose Rogers 4350B as the dielectric for the low-loss version is mainly because of its low-loss property, which allows us to extend the lower boundary of loss level, so we can emulate a wider range of channel loss. We choose FR-4 as the dielectric for the low-cost version is mainly because of its low fabrication cost.

Table 2.3. Parameter Comparison between Rogers 4350B and FR-4

Dielectric Material	Rogers 4350B [19]	FR-4 [20]
Dielectric Constant ε_r	3.66	4.35
Surface Resistivity	$5.7\times10^{9}\Omega$	$10^{8}\Omega$
Dissipation Factor	0.0037	0.014
Flammability	V0	V0
Fabrication Cost	High	Low
RF Performance	Good	Poor

2.2.3. Cross-Section Model of Channel Trace. After determining the structure of channel trace as Conductor-Backed Coplanar Waveguide (CBCPW), and the dielectric material as Rogers 4350B (dielectric constant 3.66) or FR-4 (dielectric constant 4.35), we want to determine the critical parameters of channel trace, including the signal trace width, gap spacing between signal to adjacent ground plane, dielectric thickness, via diameter and position.

We have several constrains in designing the channel trace, which are restricted by the manufacturing capability, the MEMS switch's small dimension. The designing constrains include:

- Signal trace and gap spacing between the signal trace to adjacent ground should be equal or larger than 5mil.
- The total width of signal trace and gap spacing on both sides of signal trace should be smaller than 30 mil.
- The dielectric thickness should be larger than 10mil.
- Via drill diameter should be larger than 8mil, via to via distance (center-to-center distance) should be larger than 30mil.

To find the best parameters to form a 50 Ohm CBCPW transmission line, we use Q2D as the simulation tool to performance cross-section 2D simulations. Figure 2.6 shows the cross-section model for CBCPW in Q2D, which includes the signal trace, top and bottom ground, vias on both sides and dielectric, the parameters defined in cross-section model are shown in Table 2.4.

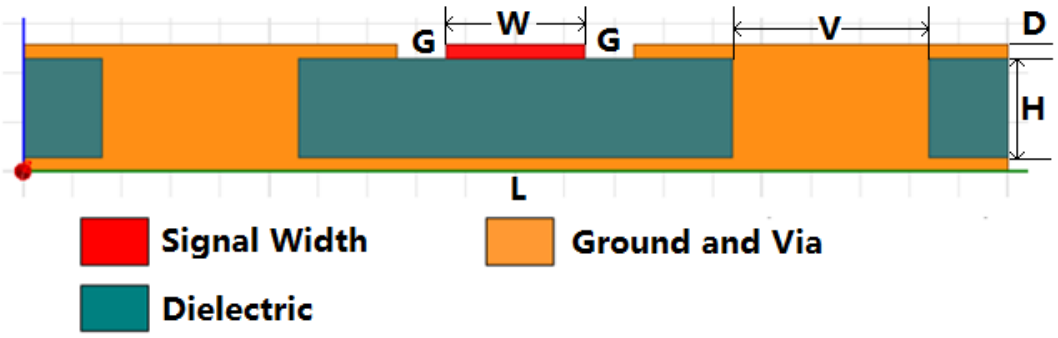


Figure 2.6. Cross-Section Model for CBCPW

Table 2.4. Parameters Defined in Cross-Section Model

Parameter	Definition	Value Range
W	Signal Trace Width	> 8 mil
H	Dielectric Thickness	> 10 mil
G	Gap Spacing Between Signal and GND	> 5 mil
D	Copper Thickness	> 1oz
L	Length of Cross-Section Plan	> 4*(W+2G)
V	Via Diameter	> 8mil

2.2.4. Determine Parameters of Channel Trace. We tried different combinations of dielectric thickness, signal trace width and gap spacing etc. using the cross-section 2D simulation model. The best combination parameters for low-loss version (Rogers 4350B dielectric) and low-cost version (FR-4 dielectric) are shown in Table 2.5. The simulated characteristic impedance based on Q2D cross-section model is shown in Figure 2.7.

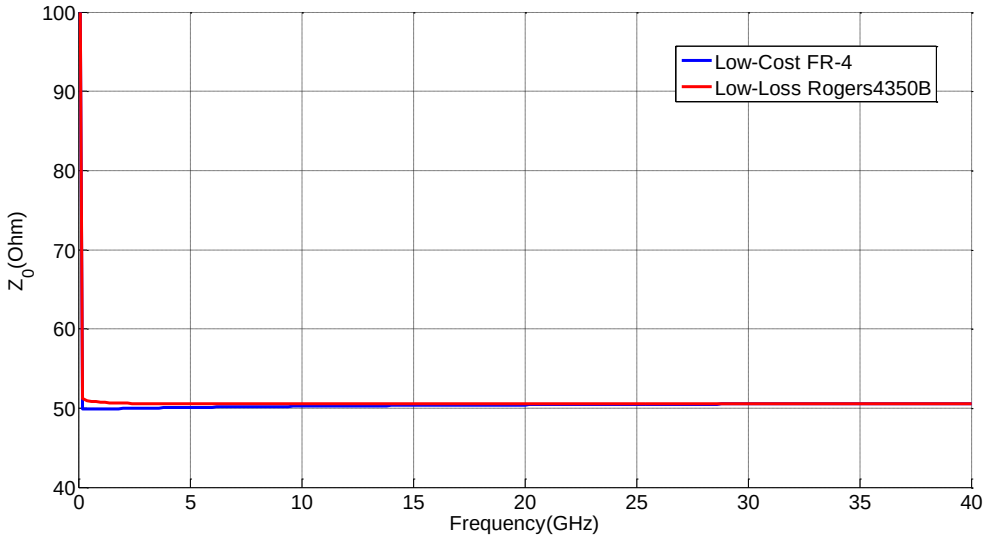


Figure 2.7. 2D Cross-Section Characteristic Impedance Simulation Result

Table 2.5. Best Parameter Combinations of Channel Trace

Parameter	**Low-Loss (Rogers 4350B)**	**Low-Cost (FR-4)**
er	3.66	4.35
W	14 mil (0.356mm)	14 mil (0.356mm)
H	10 mil (0.254mm)	10 mil (0.254mm)
G	5 mil (0.127mm)	7 mil (0.178mm)
D	1oz	1oz
V	20mil (0.508mm)	20mil (0.508mm)

We can find that the characteristic impedance is 50ohm up to 40GHz, which means the designed parameters are suitable. Notice that the characteristic impedance Z_0 is large at very low frequencies and quickly goes down when frequency increases, then it

becomes stable at 50ohm at higher frequencies. To explain the large characteristic impedance at low frequency region, we can start from the fundamental equation:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

At very low frequencies (under 200MHz), the frequency-related terms $j\omega L$ and $j\omega C$ are nearly zero. So the characteristic impedance is mainly formed by the ratio of R and G:

$$Z_0 \approx \sqrt{\frac{R}{G}}, \quad freq < 200MHz$$

The G term, which related to dielectric loss, is very small at low frequencies, so the characteristic impedance Z_0 is large. When the frequency increases, the frequency-related terms $j\omega L$ and $j\omega C$ become dominate, so the characteristic impedance is alternatively formed by the ratio of L and C:

$$Z_0 \approx \sqrt{\frac{j\omega L}{j\omega C}} = \sqrt{\frac{L}{C}}, \quad freq \geq 200MHz$$

The characteristic impedance Z_0 becomes stable at our target value at high frequencies, Based on our experience, the effect of $\frac{R}{G}$ term is ignorable when the frequency is above 200 MHz.

Here we just give an illustration example of how we determine gap spacing width for low-loss channel board (Rogers 4350B dielectric). Suppose we have set the signal trace width as 14mil and dielectric thickness as 10mil. Now we use Q2D ParametricSetup to vary the gap spacing from 3mil to 13mil with 1mil step. 3mil is actually not achievable, we just choose it for illustration purpose. The characteristic impedance vs. gap spacing is

shown in Figure 2.8. From this figure, we can find two facts: 1). the best gap spacing is 5mil, because it will make the characteristic impedance closest to 50 Ohm; 2). Smaller the gap spacing is, more sensitive the characteristic impedance will be, so the low-loss channel board requires manufacturing capability to achieve high fabrication accuracy.

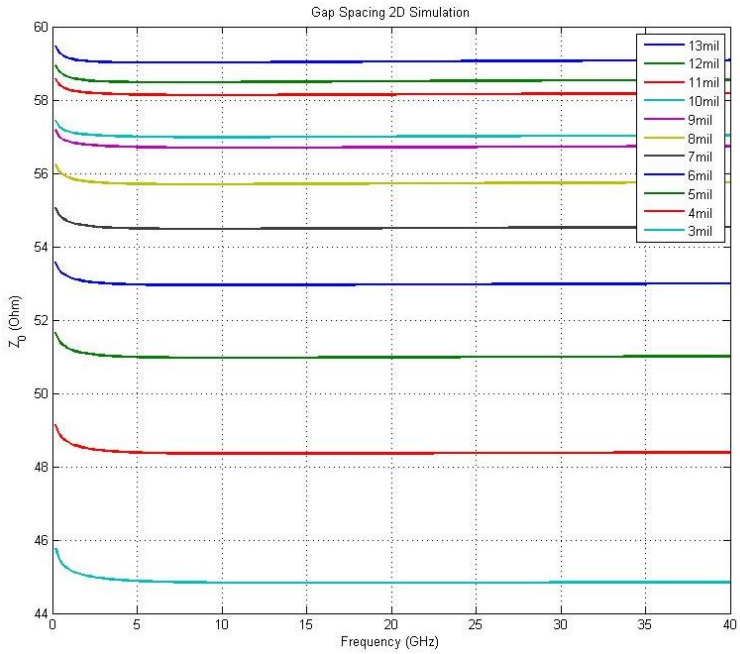


Figure 2.8. Gap Spacing Variation 2D Simulation Results (Low-Loss Board)

2.2.5. Analytical Verification of Channel Trace. We can also use analytical solution to calculate the characteristic impedance based on the parameters determined by the cross-section model of CBCPW. The analytical solution can help us further verify the correctness of the simulation result.

Theoretically speaking, the characteristic impedance and effective dielectric constant of CBCPW are determined by signal trace width s, gap spacing w between signal and ground, dielectric constant ε_r of dielectric and dielectric thickness h, all of the variables are defined in Figure 2.9.

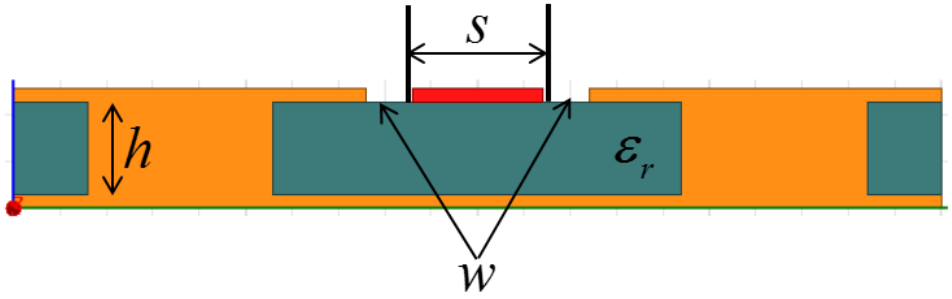


Figure 2.9. Analytical Solution Variable Definition

Firstly we use low-lost version of Channel Board as an example, the low-cost version's analytical solution is similar. We choose the 2D simulation results as the parameters, and the dielectric constant of Rogers 4350B is 3.66.

$$s = 14mil = 0.3556mm$$
$$w = 5mil = 0.127mm$$
$$h = 10mil = 0.254mm$$
$$\varepsilon_r = 3.66$$

The original formulas are in [21]. The formulas use "a" for the track width and "b" for the sum of the track width plus the gaps either side.

$$\begin{cases} a = s = 0.3556 \\ b = s + w = 0.4826 \end{cases}$$

Based on a and b we can calculate four k, k', k_l, k_l' parameters.

$$\begin{cases} k = a/b = 0.7368 \\ k' = \sqrt{1-k^2} = 0.6761 \\ k_l = \dfrac{\tanh\left(\pi a/4h\right)}{\tanh\left(\pi b/4h\right)} = 0.8856 \\ k_l' = \sqrt{1-k_l^2} = 0.4645 \end{cases}$$

The k values calculated above are actually the input for elliptical integrals K. Elliptical integrals is derived by recursive equations which were originally given for use in calculating the inductance of helical coils and are taken from [22].

The first iteration ($n = 0$) is initialized with the following formulas (based on the input value k):

$$\begin{cases} a_0 = 1.0 \\ b_0 = \sqrt{1.0-k^2} \\ c_0 = k \\ K\left(k\right) = \dfrac{\pi}{2a_0} \end{cases}$$

Each successive iteration is then calculated with the following formulas until $c_n = 0$ is within the required accuracy.

$$\begin{cases} a_n = \dfrac{a_{n-1}+b_{n-1}}{2} \\ b_n = \sqrt{a_{n-1}b_{n-1}} \\ c_n = \dfrac{a_{n-1}-b_{n-1}}{2} \\ K\left(k\right) = \dfrac{\pi}{2a_n} \end{cases}$$

For example, if we set the value $k = 0.7368$, the iteration results of elliptical integrals are shown in Table 2.6. The final result $K(k) = 1.8922$. Similarly, we can calculate $K(k')$, $K(k_l)$ and $K(k_l')$ respectively.

Table 2.6. Elliptical Integrals Iteration Result (k=0.7368)

Iteration (n)	a_n	b_n	c_n	$K(k)$ at iteration N=n
0	1	0.6761	0.7368	1.5708
1	0.8380	0.8222	0.1620	1.8744
2	0.8301	0.8301	0.0079	1.8922
3	0.8301	0.8301	1.8798e-05	1.8923
4	0.8301	0.8301	1.0642e-10	1.8923
5	0.8301	0.8301	0	1.8923

The rest elliptical integrals results are shown below:

$$K(k) = 1.8923$$
$$K(k') = 1.8193$$
$$K(k_l) = 2.2229$$
$$K(k_l') = 1.6677$$

Then we can get the effective dielectric constant and characteristic impedance:

$$\varepsilon_{eff} = \frac{1 + \varepsilon_r \dfrac{K(k')}{K(k)} \dfrac{K(k_l)}{K(k_l')}}{1 + \dfrac{K(k')}{K(k)} \dfrac{K(k_l)}{K(k_l')}} = 2.4941$$

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{\frac{K(k)}{K(k')} + \frac{K(k_l)}{K(k_l')}} = 50.2964\Omega$$

We can find that the final characteristic impedance of low-loss channel board derived from analytical solution is 50.2964 ohm, which is very close to our simulation result and our expected value.

Similarly, the characteristic impedance of low-cost channel board derived from analytical solution is 49.7673 ohm, also meets with our expected value. The simplified calculation procedures and results are listed below.

Initial input values:

$s = 14mil = 0.3556mm$
$w = 5mil = 0.178mm$
$h = 10mil = 0.254mm$
$\varepsilon_r = 4.35$

Calculated elliptical integrals results:

$K(k) = 1.8094$
$K(k') = 1.9046$
$K(k_l) = 2.1432$
$K(k_l') = 1.6899$

The effective dielectric constant and characteristic impedance of the low-cost (FR-4 dielectric) channel board:

$\varepsilon_{eff} = 2.9153$
$Z_0 = 49.7673\Omega$

2.2.6. Via-to-Via Distance Estimation. For the Conductor-Backed Coplanar Waveguide (CBCPW) structure, we need to add vias on both sides of the signal trace. So the distance between via and via needs to be estimated based on analysis. If via-to-via distance is small enough, the vias can be regarded as a "cuboid" without discontinuity. However, via-to-via distance cannot be very small due to the limitation of manufacturing process and cost consideration. So we use analytical equations to estimate a proper via-to-via distance.

Even though the expected working frequency is DC to 20GHz, we choose 40GHz as the largest frequency to estimate the needed smallest wavelength. Effective dielectric constant is calculated analytically in above sections, we use $\varepsilon_{eff} = 2.4941$(from low-loss version channel board) in this estimation.

$$f = 40GHz$$

$$v_p = \frac{c}{\sqrt{\varepsilon_{eff}}} = 1.8996 \times 10^8$$

$$\lambda = \frac{v_p}{f} = 4.75mm = 187mil$$

If we look into the transmission line, from the center of via1 to the center of the next via2, there must exist reflections due to the discontinuity of cross-section. The reflected wave may have 90 degree ($\frac{\pi}{2}$) or 180 degree (π) phase difference with the incident wave. If the reflected wave at via1 has the same phase with the incident wave at the same via, we would observe ripples at these frequency points.

Considering the total length of travelling forth and back is two times of the via-to-via distance l, the via-to-via distance should be less than half or quarter of the wavelength, so we have:

$$\begin{cases} l < \dfrac{\lambda}{2} \\ l < \dfrac{\lambda}{4} \end{cases} \Rightarrow l < \frac{\lambda}{4} = 46.75mil$$

We choose $l = 40mil$ for convenience. If $l \geq \frac{\lambda}{4}$, there must exist a wave under the frequency between DC to 40GHz that will generate ripples. However, $l = 40mil$ is small enough compared to a quarter of wavelength, so the vias on both sides of the signal trace can be regarded as a "wall" without discontinuities from the transmission line's perspective, see Figure 2.10.

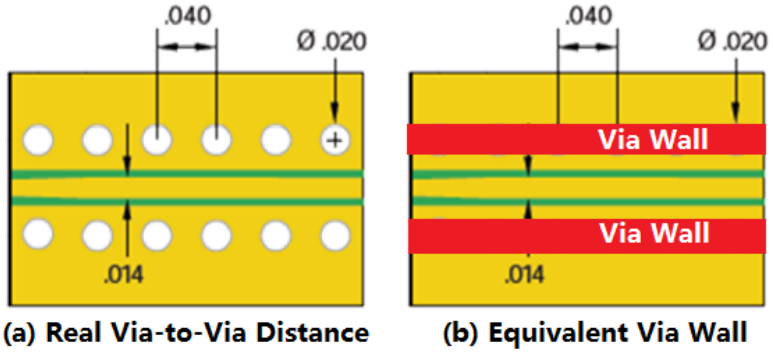


Figure 2.10. Via-toVia Distance Estimation Result

2.2.7. Full Wave Simulation of Channel Trace. After determining the parameters of channel trace from cross-section 2D model, we move on to build 3D full wave model on HFSS and CST to further validate the parameters and characteristic impedance of channel trace structure, also we want to observe the field distribution between signal trace and adjacent ground.

We use the low-loss Channel Board as an example. Signal trace width is 0.3556mm (14mil), gap spacing is 0.127mm (5mil), via diameter is 0.508mm (20mil). The signal trace, top/bottom ground, vias are all copper ($\sigma = 5.8 \times 10^7$), the dielectric is Rogers 4350B ($\varepsilon_r = 3.66$, dielectric loss tangent is 0.004). Since our CBCPW channel trace is designed to work up to 40GHz, so we set the frequency range from 200MHz to 40GHz. Mesh cells are all small enough to give accurate simulation results.

CST simulation setting:

- Boundary: Open boundary except the bottom, bottom plane is electrical
- Excitation: Waveguide port, renormalized to 50 ohm
- Frequency: 200MHz~40GHz, with 200MHz a step
- Accuracy: -60dB

HFSS simulation setting:

- Solution Type: Driven terminal
- Boundary: Radiation air box
- Excitation: Wave port, renormalized to 50 ohm
- Frequency: 200MHz~40GHz, with 200MHz a step

After the 3D full wave simulation, the characteristic impedance simulated by CST model is 50.15 Ohm and in HFSS model is 50.09Ohm, which proves the channel trace parameters are good. Figure 2.11 shows the E-field distribution in CST and HFSS model, Both models show that the E-filed is mainly distributed between the signal trace and two top ground, which agrees with our expectation. The E-fields at the edges of the ports are nearly 0, which means our model port setting is large enough without any truncated effects.

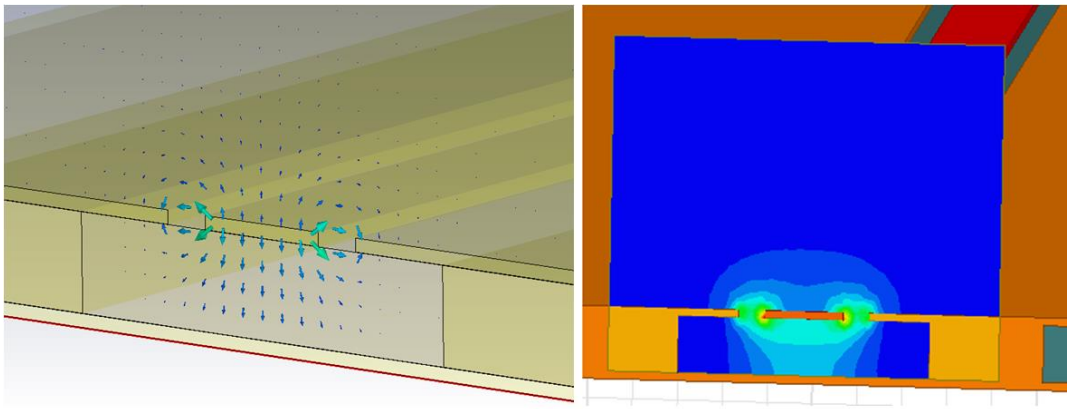


Figure 2.11. E-Field Distribution in CST (left) and HFSS (right) Model

2.3. GENERAL DESIGN OF CONTROLLER BOARD

Controller Board consists of three main components: DC-DC Voltage Booster, Serial to Parallel Converter and MCU, the block diagram is shown in Figure 2.12.

- DC-DC Voltage Booster: Provide high voltage that needed to drive the MEMS switch. We can build a DC-DC voltage booster to convert voltage from 5V to 90V.
- Serial to Parallel Converter: Convert single high voltage input to multiple high voltage outputs so we can drive multiple channels. It can be done by using a Serial to Parallel High Voltage Converter HV513.
- MCU: Run an operating system that can execute Python script. The MCU we choose is STM32F405.

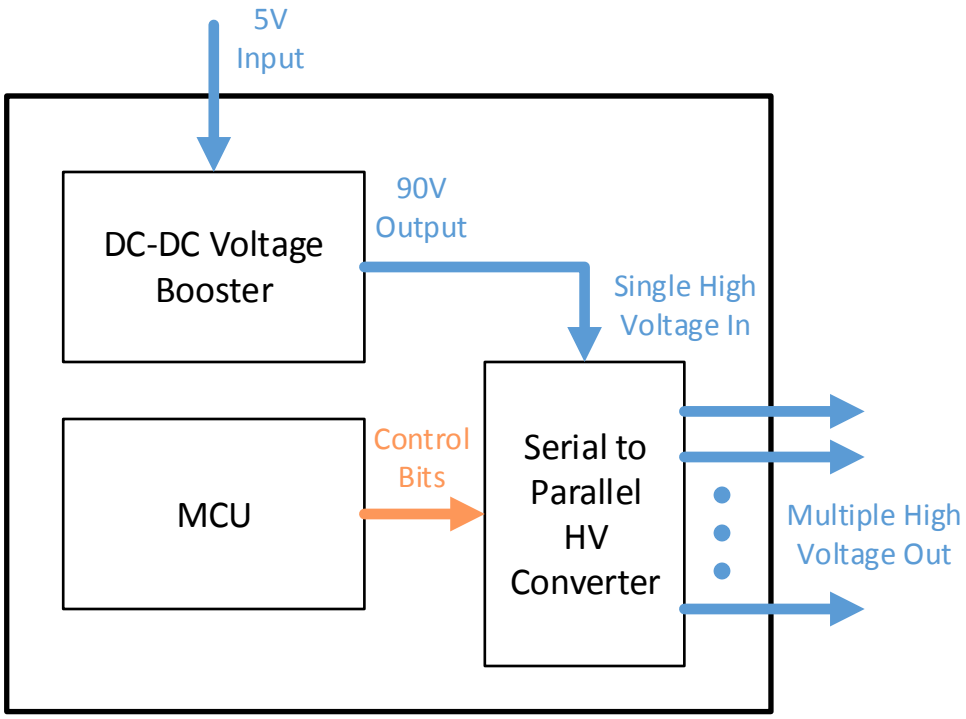


Figure 2.12. Block Diagram of Controller Board

2.3.1. DC-DC Voltage Booster. The driven voltage for MEMS switch is 90V, so we need to design a DC-DC voltage booster to get higher output voltage from input voltage.

The typical circuit diagram of a DC-DC voltage booster is shown in Figure 2.13. In this circuit, in the On-state, the switch S is closed, resulting in an increment in the inductor current; in the Off-state, the switch is open and the only path offered to inductor current is through the diode D, the capacitor C and the load R. This results in transferring the energy accumulated during the On-state into the capacitor. Instead of the switch, we decided to use a fast switching square wave to replace the switch so that we could also get the 90V output with an appropriate duty cycle.

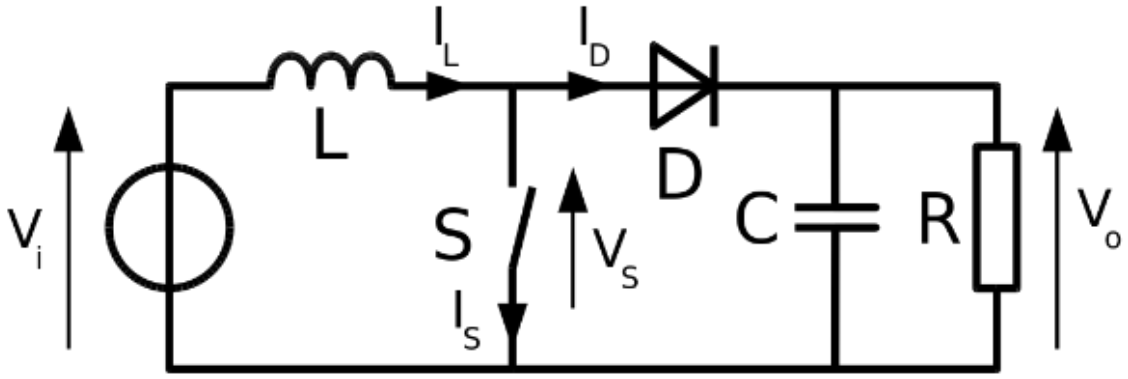


Figure 2.13. Basic Diagram of Voltage Booster [23]

Following the basic principle of voltage booster mechanism, we can find that the basic design of the DC-DC voltage booster is based on a switch turning on and off. We can use a 90V Boost DC/DC Converter LT3482 [24] that has the integrated Schottky Diodes to achieve our goal. The LT3482 from Linear Technology takes a +5V DC input and converts it to a 90V DC output. The output voltage depends on R1, R2 and the internal reference voltage of LT3482, we could adjust the output voltage by changing R1 and R2. The desired output voltage can be calculated as:

$$R_1 = R_2\left(\frac{V_{OUT2}}{V_{REF}} - 1\right)$$

We choose $R_1 = 1M\Omega$, $R_2 = 14K\Omega$, internal reference voltage is fixed to $V_{REF} = 1.235V$, the output voltage can be calculated as:

$$V_{OUT2} = \left(\frac{R_1}{R_2} + 1\right)\cdot V_{REF} = \left(\frac{10^6}{14\times 10^3} + 1\right)\times 1.235 = 89.45V$$

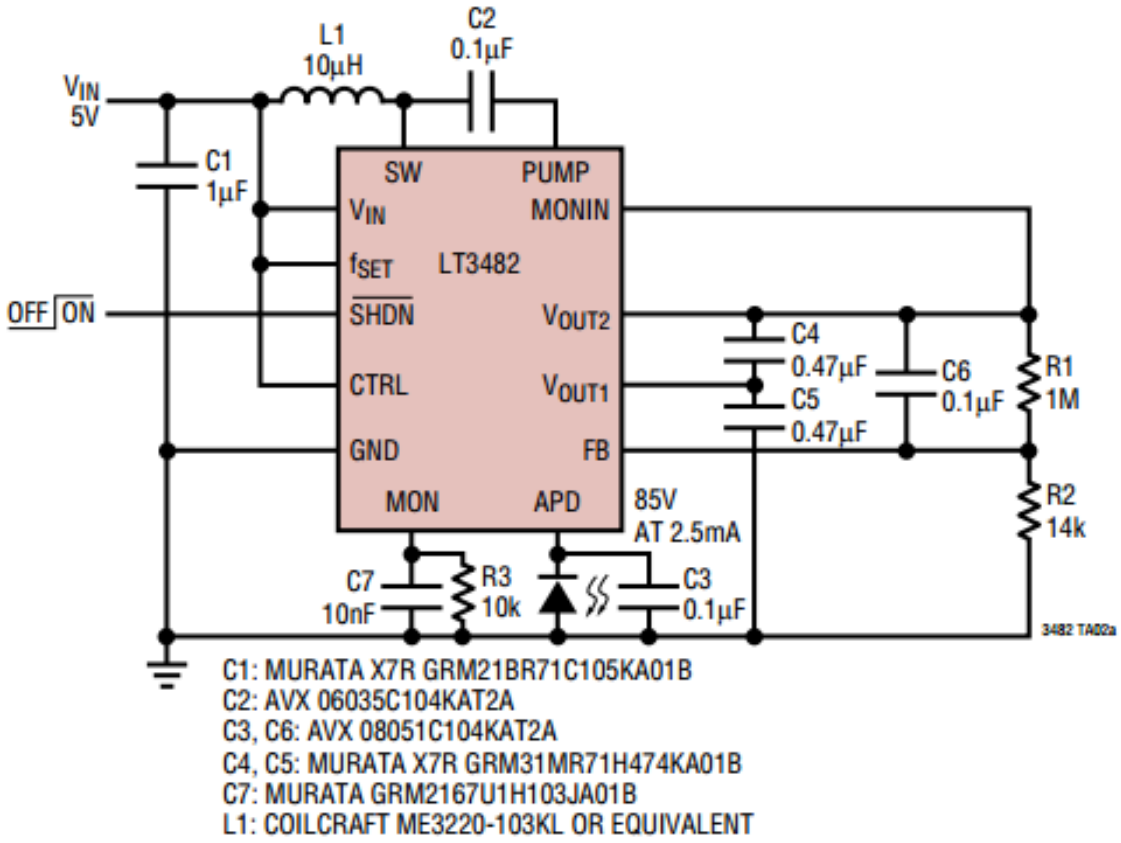


Figure 2.14. Circuit Diagram of 90V Voltage Booster [24]

2.3.2. Serial-to-Parallel Converter. For the Serial to Parallel HV Converter, we choose HV513 [25]. The HV513 is a serial low-voltage to parallel high-voltage converter with 8 high-voltage push-pull outputs. We use this outputs to supply 90V voltage to each MEMS switch so that we could control which channel will be enabled. HV513 consists of an 8-bit shift register, 8 latches, and control logic to perform the polarity select and blanking of the outputs, see Figure 2.15.

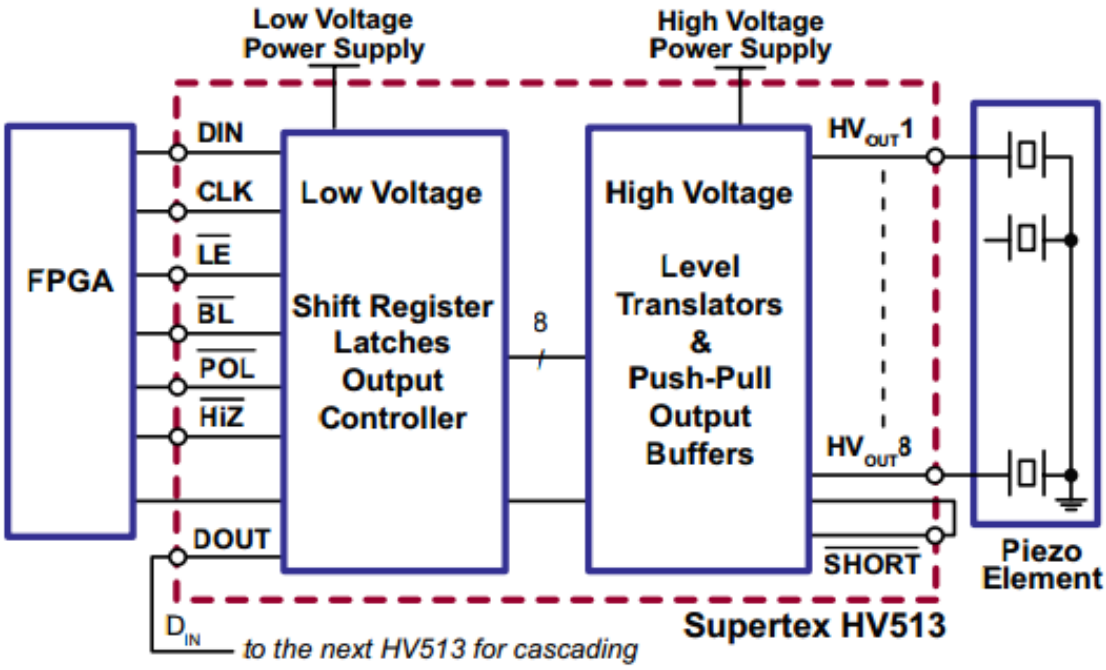


Figure 2.15. Microchip HV513 Circuit Diagram [25]

We only need to drive four pins by GPIOs of MCU. The index of the channel which is enabled is delivered by the serial DIN with synchronized CLK signals. The control logic diagram is shown in Figure 2.15:

- BL (reset output) : GPIO from MCU
- LE (enable latches): GPIO from MCU
- DIN (data in): GPIO from MCU, serial data
- CLK (clock - rise edge): GPIO from MCU
- POL and HI-Z are always high (these two pin have internal pull-up resistors)

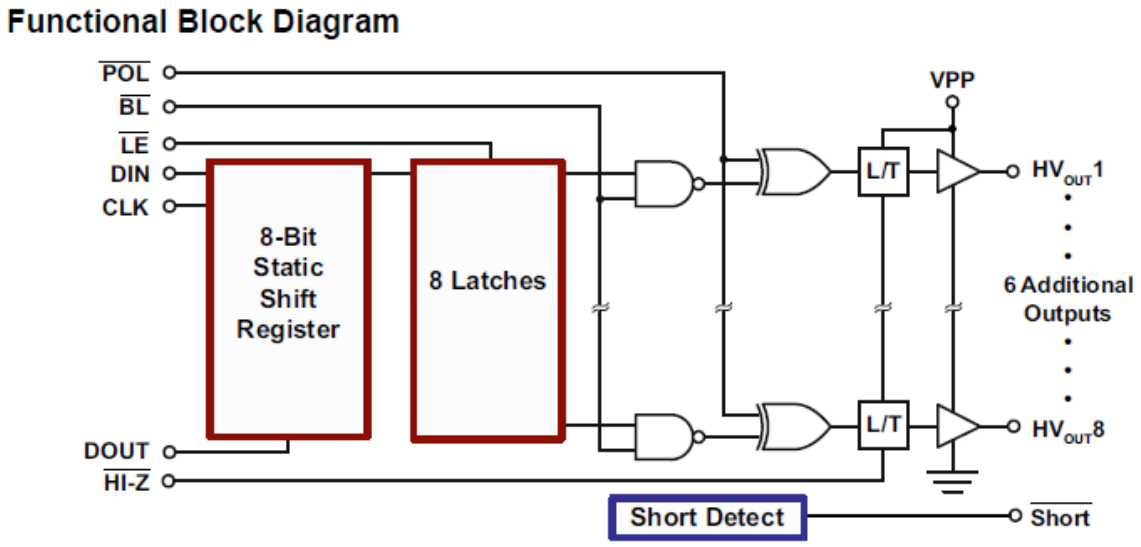


Figure 2.16. Serial to Parallel Converter Control Logic Diagram [25]

2.3.3. MCU with Python. To achieve automated control for our channel emulator, the MCU on control board needs to have the capability to execute the programs. We choose the most widely used programming language in auto-testing systems from industry, Python, to build the software program. A Python script is running on the MCU to determine how to supply driven voltage to MEMS switch and which channel to enable, the control logic is delivered through the MCU's GPIO ports. Since STM32F405 is an ARM chip, we need to build a cross-platform compiler on Linux system to deploy embedded OS to Control Board. The ARM compiler is arm-none-eabi-gcc, after compiling the source code, we can enter DFU boot mode to deploy the operating system.

The control logic sequence can be describe as:

(1) Reset all the outputs to low state and enable latch, so the output voltages of all channels are forced to be low.

(2) Generate clock signal.

(3) At each rise edge of clock signal, load one bit of value (1 or 0) into the latch. If the loaded bit is 1, it means the corresponding channel will turn on. If the loaded bit is 0, the corresponding channel will turn off.

(4) Disable latch to let the loaded bits flow to output. Release the reset pin.

We also complete a simple GUI to provide a more intuitive way for users to switch channels, the GUI is shown in Figure 2.17.

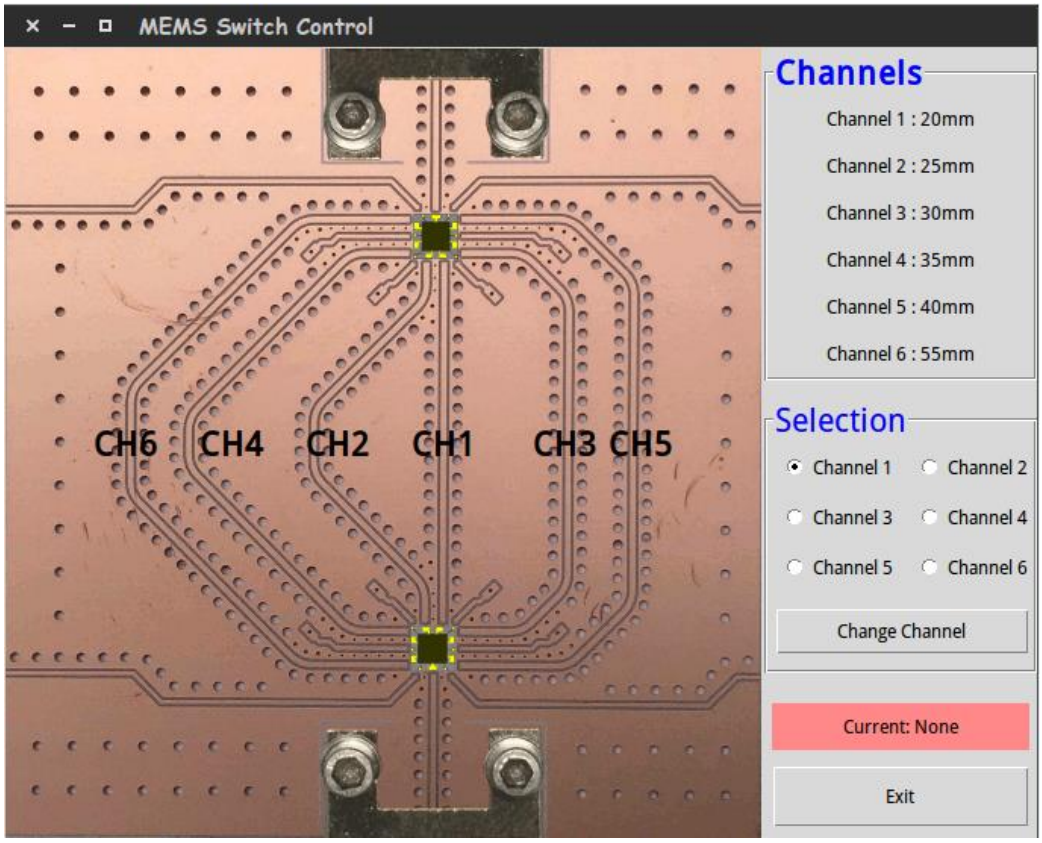


Figure 2.17. GUI of Automated Channel Emulator

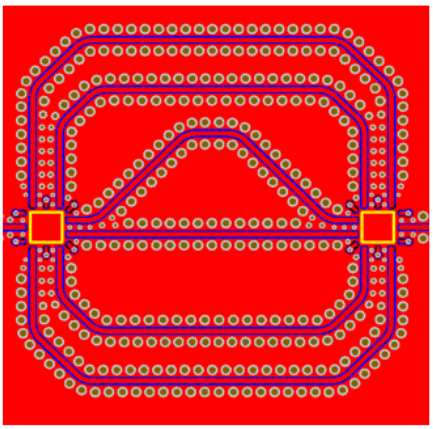
3. POST SIMULATION AND SYSTEM ASSEMBLY

We performance post-simulation after the completion of PCB layout to check the RF performance of channel traces on real PCB board, then after manufacturing PCB boards, we assemble the whole system of the automated channel emulator.

3.1. POST SIMULATION ON CHANNEL TRACE

To better simulate the RF performance of real PCB's channel trace, we export the channel trace from PCB Layout in ODB++ format, then import the PCB structure into CST and assign materials and ports, so the CST model includes the real structures of channel traces. Mesh cells are all small enough to give accurate simulation results.

For the low-loss Channel Board with Rogers 4350 dielectric, we use SP6T MEMS switch to form 6 channels. The channel length and design is in Figure 3.1. After the 3D full wave simulation, we can obtain the S21 of all 6 channels (see Figure 3.2) and calculate the P.U.L (per-unit-length) S21 for each channel trace (see Figure 3.3).



Channel	Length
Channel 1	20mm
Channel 2	25mm
Channel 3	30mm
Channel 4	35mm
Channel 5	40mm
Channel 6	45mm

Figure 3.1. Low-Loss Channel Board Trace Lengths and Design

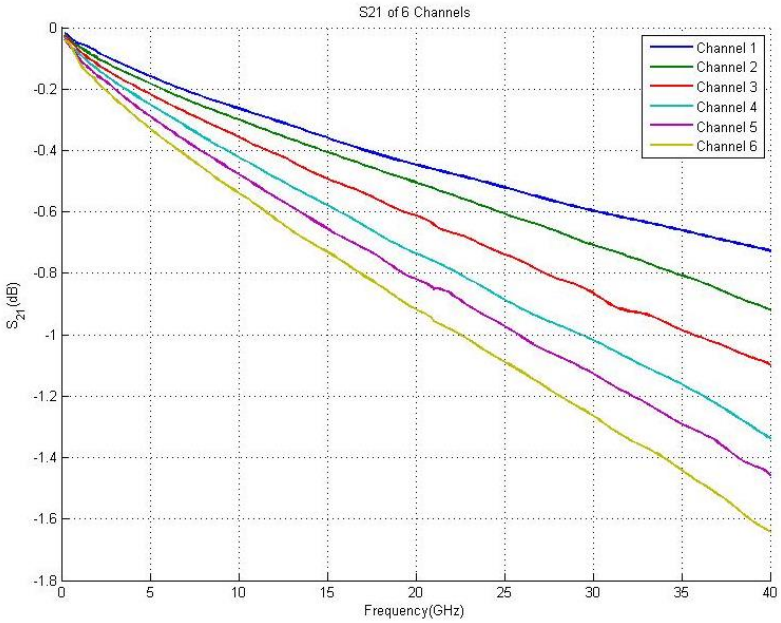


Figure 3.2. Low-Loss Channel Board S21 of All Channels

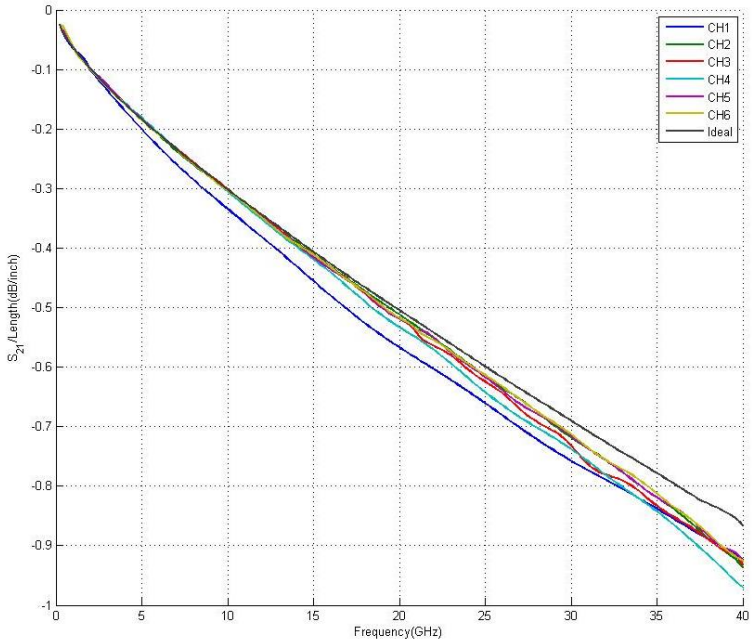
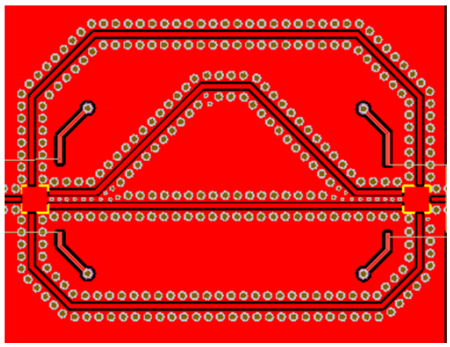


Figure 3.3. Low-Loss Channel Board P.U.L. S21 of All Channels

For the low-cost Channel Board with FR-4 dielectric, we use SP4T MEMS switch to form 4 channels. The channel length and design is in Figure 3.4. After the 3D full wave simulation, we can obtain the S21 of all 4 channels (see Figure 3.5) and calculate the P.U.L (per-unit-length) S21 for each channel trace (see Figure 3.6).



Low-Cost FR-4 Dielectric

Channel	Length
Channel 1	28.743mm
Channel 2	35.893mm
Channel 3	43.043mm
Channel 4	50.194mm

Figure 3.4. Low-Cost Channel Board Trace Lengths and Design

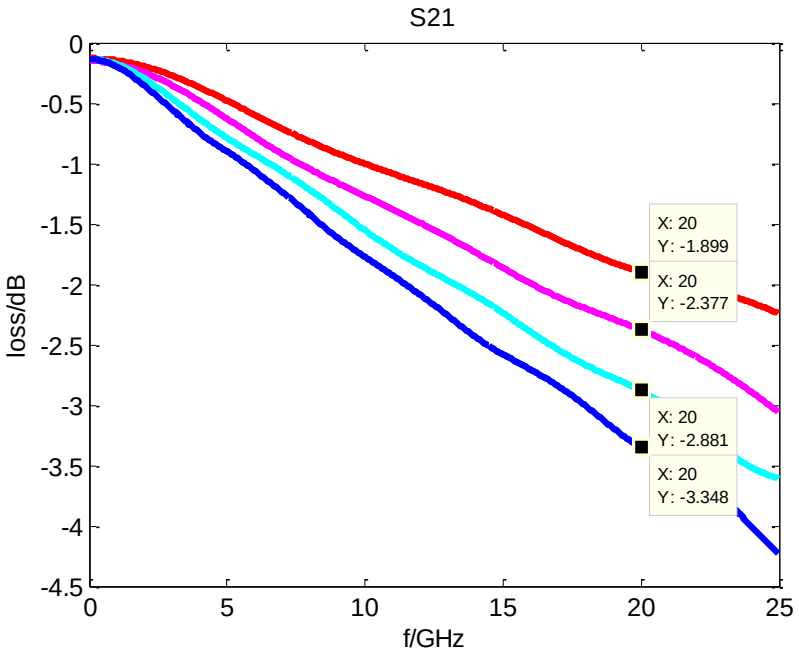


Figure 3.5. Low-Cost Channel Board S21 of All Channels

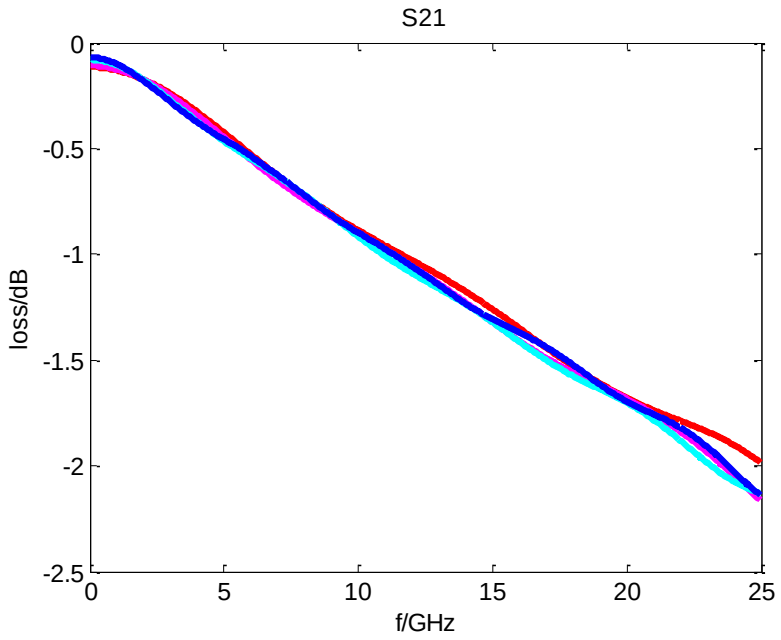


Figure 3.6. Low-Cost Channel Board P.U.L. S21of All Channels

For both low-loss and low-cost channel boards, we can see that the S21 is linearly going down from DC to 20GHz, which means the channel traces are well designed with no multiple reflection and little discontinuity. Each channel has a different level of length corresponding to its length. From the P.U.L. S21 waveforms, we can see that the P.U.L S21 of all the channels are overlapped with each other, which means the per-unit-length of each channel is the same. So it indicates that the channel's loss is only dependent on the length. The low-cost Channel Board has larger P.U.L loss (around -1.7dB/mm @ 20GHz) compared with the low-loss Channel Board (-0.9dB/mm @ 20GHz). This fact also agrees with our expectation, because the low-loss Channel Board uses a low-loss dielectric material Rogers 4350B, however, the fabrication cost of low-loss Channel Board is much higher than low-cost Channel Board.

3.2. SYSTEM JOINT AND ASSEMBLY

We assemble all three boards of the automated channel emulator system, the system joint setup is shown in Figure 3.7. We supply 5V to Controller Board for MCU and DC-DC voltage booster so it can generate 90V driven voltage for the MEMS switch. The testing cables are connected to the end-launch connectors on Channel Board.

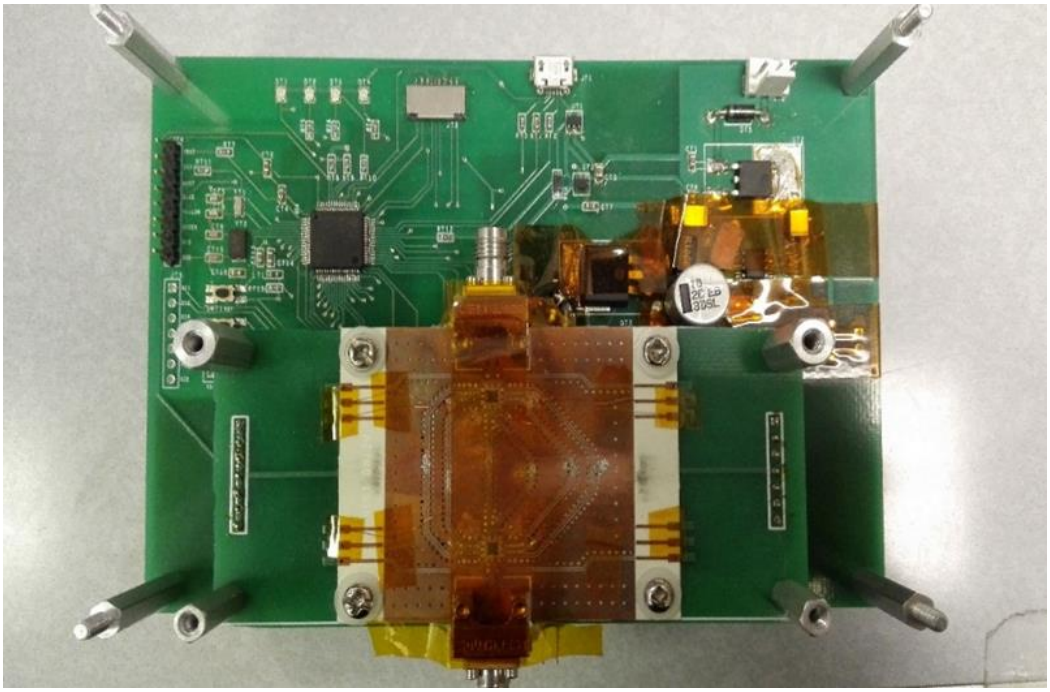


Figure 3.7. Automated Channel Emulator System Joint Setup

4. OPTIMIZATION OF SIGNAL TRANSITION

The overall RF performance of the channel emulator is determined not only by the design quality of high frequency channel trace but also by the design of the transition part. There are four main areas on Channel Board that bring discontinuity and affect the signal transition, including:

- Trace Turns: From the turning and bending of the channel trace. We need to analyze the hidden circuits at trace turns and reduce the parasitic effects.
- Connector Transition: From the end launch connector to the channel trace. We need to compensate the excessive capacitance caused by the inner pin of the connector.
- Wire-Bonding: From the pads on MEMS switch to the channel trace. We need to reduce the excessive inductance caused by the bonding loop.
- Solder Parasitic: From the soldered resistors or capacitors on channel trace. We need to minimize the parasitic effects of the soldering.

In this section, we will analyze the effect of all the discontinuities on the Channel Board and propose solutions to improve signal transition based on simulation and measurement methods.

4.1. OPTIMIZATION OF TRACE TURNS

Since we will route channel traces with different lengths from one MEMS switch to another, there are inevitably turns existing in the longer channel path. Usually the turns distributed in the signal trace are the discontinuity parts of the transmission line, which will cause parasitic inductance and capacitance, as well as additional loss to the whole

channel. We can model this discontinuity as a lumped circuit with shunt capacitance and series inductance. Due to symmetry of the discontinuity, we arrange the L between two shunt capacitance, see Figure 4.1.

Before the current meet the turns, it flows along the two edges due to the skin effect at high frequency .When it comes across the turn, the inner current still flow along the inner edge. However, the outer current would flow through a rounded path with smaller turn angle to achieve the least impedance rather than still follow the outer edge. After it passes the turn, it will spread out to follow as the previous path. Generally say the current path is necked down at the turn, which results in the parasitic inductance.

In addition, the current will be concentrated only on the turn region. The copper signal trace distributed on the out region does not have current flow through and the unused copper still has some voltage potential as a signal trace. This means there is a additional capacitance with respect to the ground and will accumulate excess charge there.

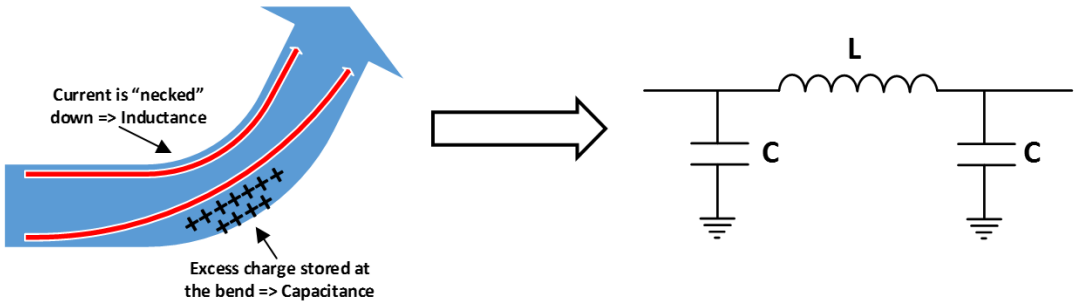


Figure 4.1. Lumped Circuits Model at Trace Turns

The parasitic effects of trace turns are directly related to the turn angle. The more trace is bending at the turns, the larger parasitic inductance and capacitance effect it will be. We use 3D simulation model to check the effects of trace turns and find possible solutions.

Figure 4.2 shows the S21 of four 90-degree turns model, we can find a turning point at about 28GHz. The S21 drops quickly after the turning point, which means the parasitic effect from 90-degree turns causes multiple reflections and un-negligible loss. We the move via closer to trace, via-to-trace's center-to-center distance is reduced from 32mil to 24mil. The S21 above 28GHz improves but the loss turning point is still visible. In Figure 4.3, we choose 45-degree turns instead for a better performance and the simulation results prove our assumption. the S21 from 45-degree model is linearly going down over all the frequencies, which means the simulated channel trace maintains 50 ohm characteristic impedance without multiple reflections or discontinuities.

In conclusion, the optimization solutions for trace turns: (1) Use 45-degree turns instead of 90-degree turns in channel trace (2) Move grounding vias as close to signal trace as possible.

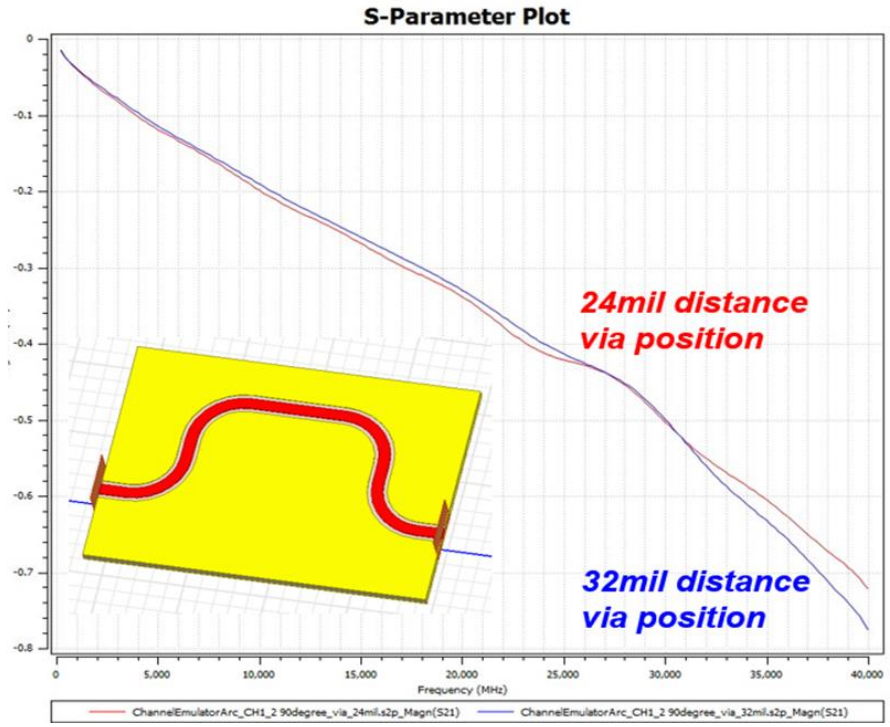


Figure 4.2. Trace Turns Simulation for 90-Degree Turns

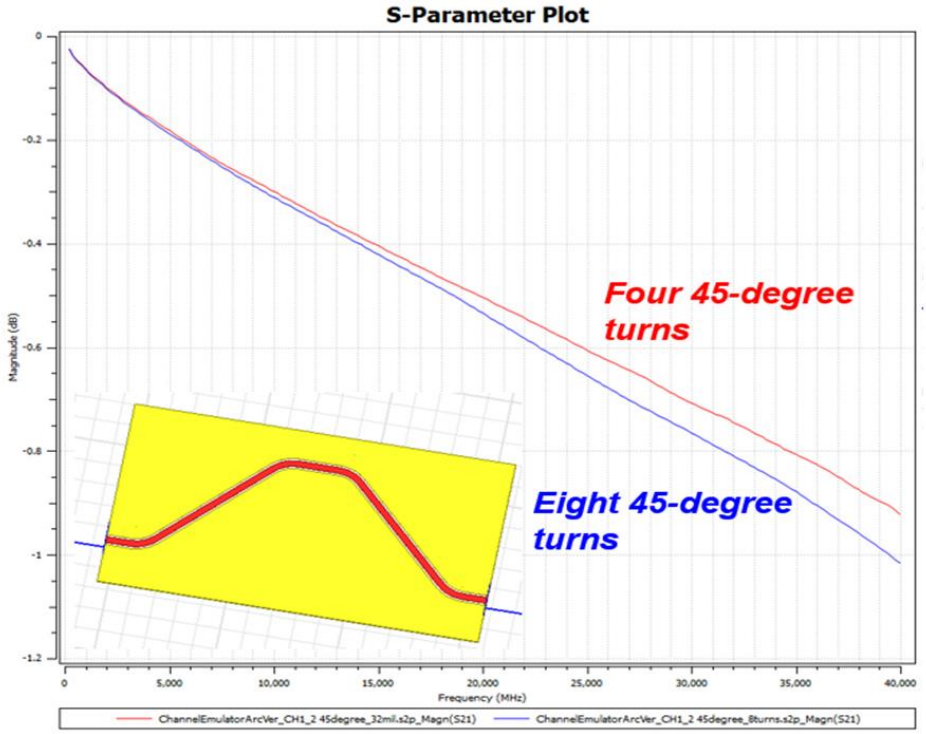


Figure 4.3. Trace Turns Simulation for 45-Degree Turns

4.2. OPTIMIZATION OF CONNECTOR TRANSITION

The end launch connector's inner pin will be landed on the signal trace of the channel, which will bring additional capacitance to the transmission line structure. So the characteristic impedance will decrease at the transient area of end launch connector. To compensate the excessive capacitance brought by the connector's pin, we can taper the signal trace gradually from wide to narrow to achieve smooth transient from channel trace to end launch connector.

Figure 4.4 shows the tapering structure from the channel trace to the end launch connector. We can control two variables in this tapering structure: (1) the tapering length, (2) the final tapered trace width. We can tune these two variables in the end launch transient model to obtain the smallest variation of impedance in the transient area. To better observe the change of characteristic impedance, we can convert the simulated S-Parameters into TDR result [17]. Figure 4.5 shows the effects of different tapering length. We can see without any tapering structure, the characteristic impedance will drop to 48 ohm because of the excessive capacitance. The best tapering length is 0.5~0.6mm to control the characteristic impedance between 49 ohm to 51 ohm.

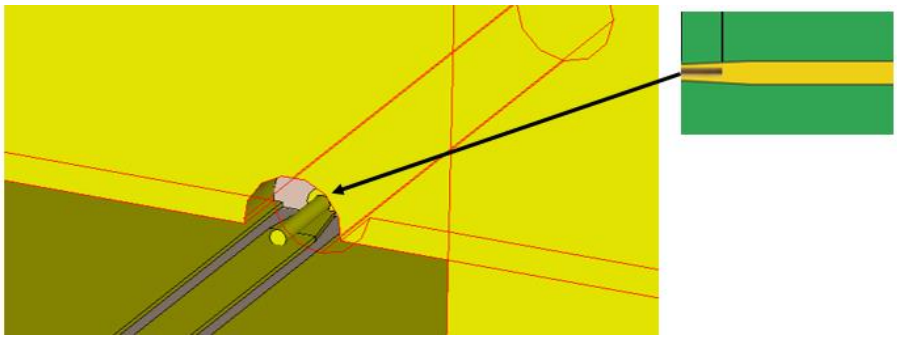


Figure 4.4. Tapering Structure of End Launch Connector Transient Model

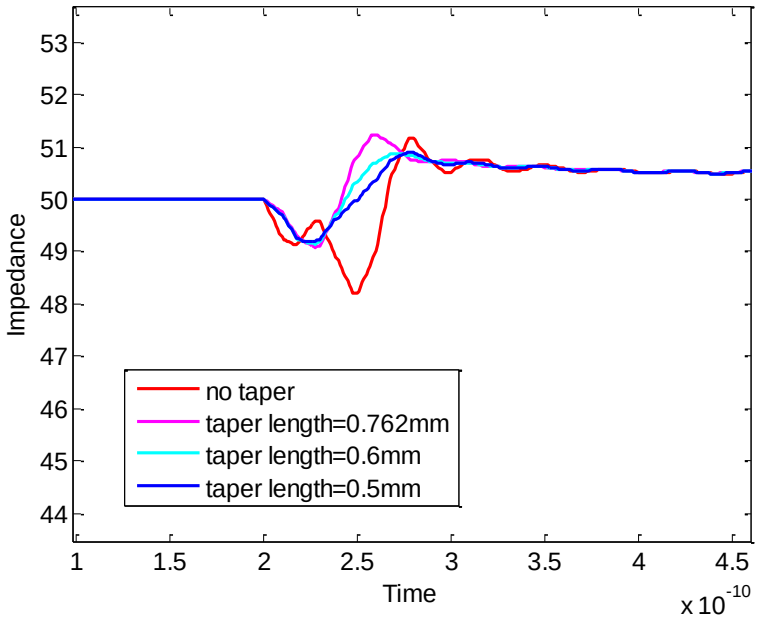


Figure 4.5. TDR of End Launch Connector Transient Model

4.3. OPTIMIZATION OF WIRE-BONDING

The MEMS switch is actually a die without package. We need to attach the die on PCB board and do wire-bonding to connect the MEMS switch pads with signal/gate traces. From Figure 4.6, we can find the bonding wire loop from bond pads to trace, which will bring parasitic inductance.

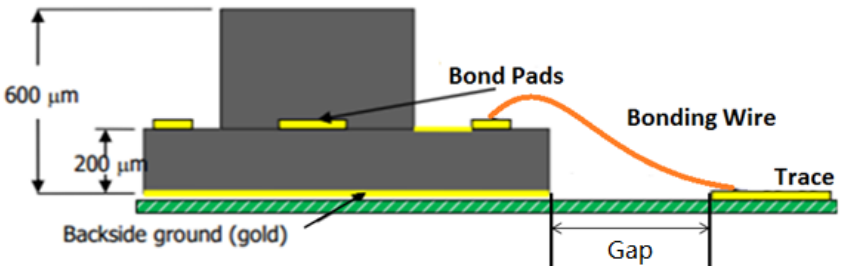


Figure 4.6. Wire-Bonding Structure Side View

To systematically study the parasitic effect of wire-bonding and determine design parameters in manufacturing, we build a simplified wire-bonding model in CST, see Figure 4.7. We build a wire-bonding model and add one waveguide port at one side of the model, we use PEC plane to terminate the other side. The simulated imaginary part of Z11 is shown in Figure 4.8. At 20.035GHz, the imaginary Z11 $\mathrm{Im}(Z_{11})$ is 33.081dBohm. So we can calculate the parasitic inductance of the whole structure is 0.359nH.

$$\mathrm{Im}(Z_{11}) = j\omega L = j2\pi fL = 33.081 dB\Omega$$

$$L = \left|\frac{\mathrm{Im}(Z_{11})}{j2\pi f}\right| = 0.359\,\mathrm{nH}$$

By comparing the relative difference of $\mathrm{Im}(Z_{11})$ among different cases, we can study several parameters affecting the parasitic inductor caused by wire-bonding loop.

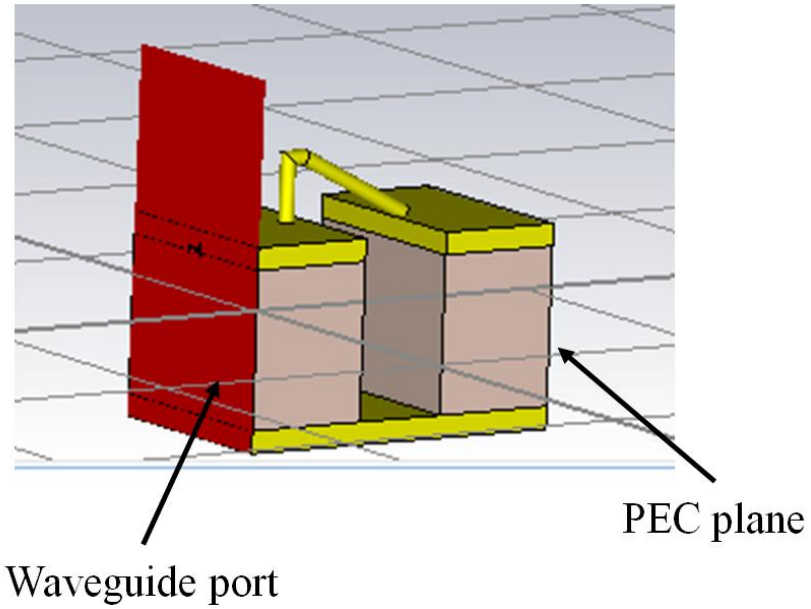


Figure 4.7. Simplified Wire-Bonding Model

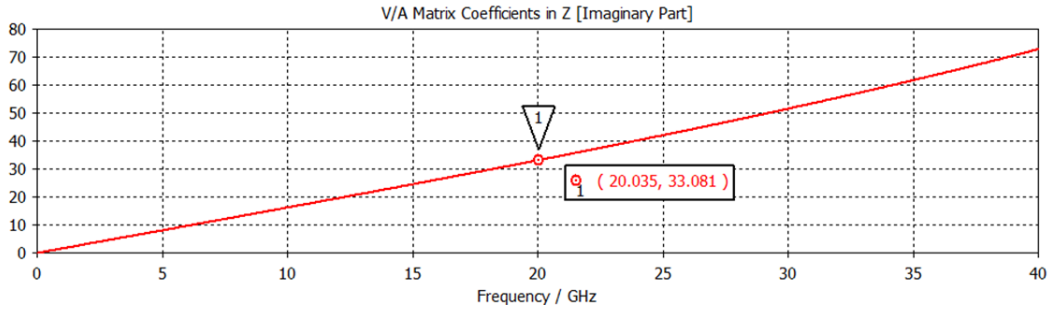


Figure 4.8. Z11 Imaginary Part of Wire-Bonding Model

We investigate four design parameters in wire-bonding: (1) The number of wires, result shown in Table 4.1. (2) The material of bonding wire, result shown in Table 4.2. (3) The diameter of bonding wire, result shown in Table 4.3. (4) The bonding distance from pads to trace, result shown in Table 4.4. Based on the simulated results, we can draw the following conclusion:

- Two wires in wire-bonding has much less parasitic inductance compared with one wire. However, the improvement between three wires and two wires are negligible. So we need to bonding at least two wires in manufacturing process for each MEMS switch pads and channel traces.
- The material of bonding wires has no effect on parasitic effects, so we can choose either copper or gold as the material of wires.
- Larger wire diameter will result in slightly smaller parasitic inductance in wire-bonding, we can choose larger diameter wires if conditions and costs permit during the manufacturing process.

- Bonding distance is another critical parameter that affect the inductance, we want the bonding distance to be as short as 0.1mm to minimize the parasitic effect of wire-bonding.

Table 4.1. Effect by the Number of Wires in Wire-Bonding (20GHz)

Number of Wires	$\mathrm{Im}(Z_{11})$	Inductance
One Wire	33.148	0.362nH
Two Wires	26.962	0.177nH
Three Wires	26.564	0.169nH

Table 4.2. Effect by the Material of Wires in Wire-Bonding (20GHz)

Number of Wires	$\mathrm{Im}(Z_{11})$	Inductance
One Wire Copper	33.144	0.361nH
One Wire Gold	33.148	0.361nH
Two Wires Copper	26.961	0.177nH
Two Wires Gold	26.962	0.177nH

Table 4.3. Effect by the Diameter of Wires in Wire-Bonding (20GHz)

Number of Wires	$\mathrm{Im}(Z_{11})$	Inductance
Diameter = 0.0254mm	26.962	0.177nH
Diameter = 0.0354mm	26.497	0.168nH
Diameter = 0.0760mm	25.001	0.142nH

Table 4.4. Effect by the Bonding Distance in Wire-Bonding (20GHz)

Number of Wires	$\mathrm{Im}(Z_{11})$	Inductance
Distance = 0.3mm	28.698	0.217nH
Distance = 0.15mm	26.962	0.177nH
Distance = 0.1mm	26.119	0.161nH

4.4. OPTIMIZATION OF SOLDER PARASITIC

We need to solder a resistor from signal trace to adjacent ground to provide the DC return path for MEMS switch, the added solder and resistor component will also cause discontinuity to the channel trace. The DUT we use to investigate the solder parasitic is one channel trace board with the same CBCPW structure and dielectric materials, see Figure 4.9.

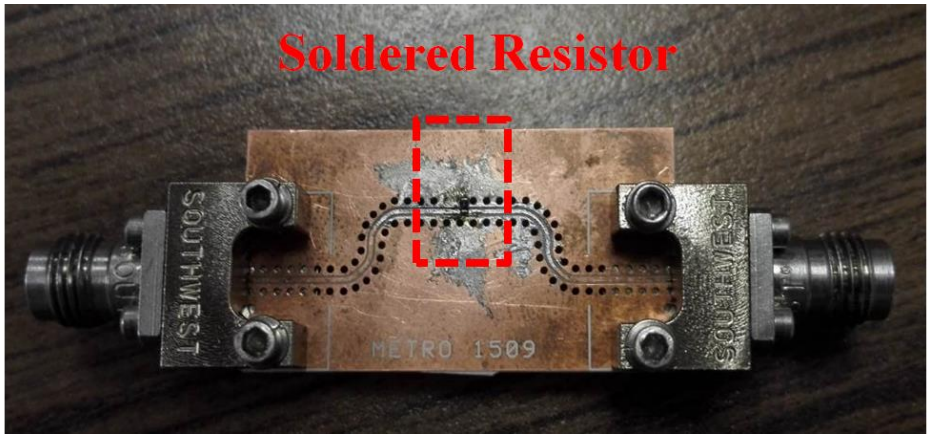


Figure 4.9. DUT to Investigate Solder Parasitic Effect

We study how the parasitic effect will be changed by different solder positions of components. Figure 4.10 shows three solder positions: (1) Normal, resistor is directly soldered to channel trace. (2) Upside Down, since the resistor film is on top layer of the component, we can minimize the loop of the DC return path. (3) Vertical, by solder the resistor vertically we can reduce the contact area to the channel trace. From measured S21 result in Figure 4.10, we find that the Normal and Vertical solder position have similar large parasitic effects (Vertical solder position is also the most difficult one to accomplish), the Upside Down solder position has the smallest parasitic effects.

In addition to solder position, we also try to reduce the package size and remove copper on the bottom ground plane to compensate the added solder on channel trace. Figure 4.12 shows the measured S21 result for different cases. We find that the 0201 package resistor has much less impact on channel trace compared with 0402 package, and the removal of bottom ground copper will also help a little to reduce the solder parasitic.

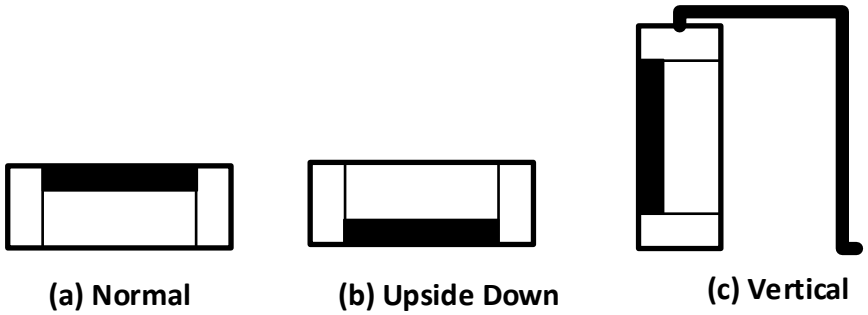


Figure 4.10. Different Solder Positions of Component

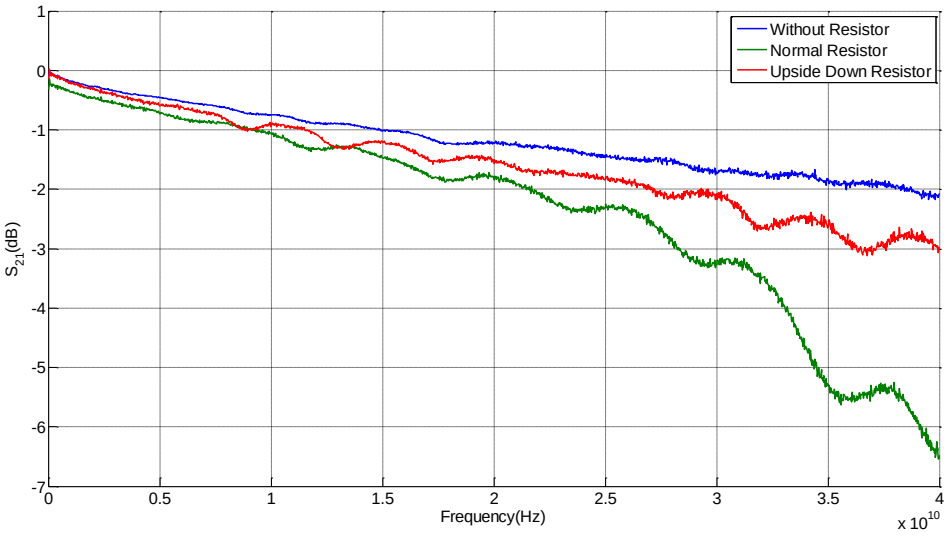


Figure 4.11. Measured S21 of Different Solder Positions

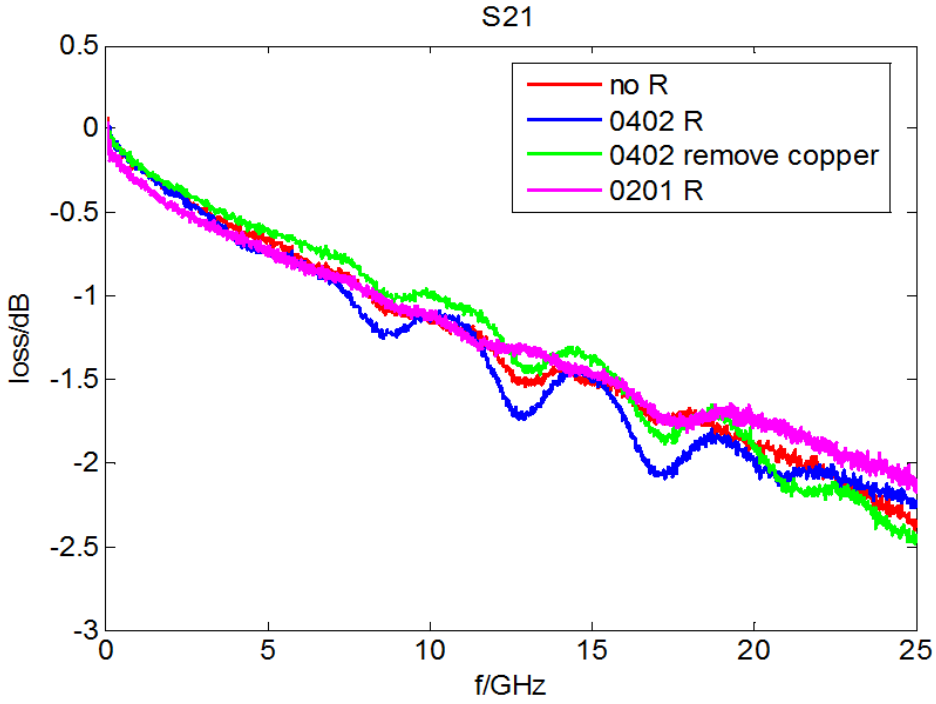


Figure 4.12. Measured S21 of Copper Removal and Package Size

5. CONCLUSION AND FUTURE WORK

This thesis work built an automated channel emulator works up to 20GHz including both high frequency channel part and software logic controller part. The design procedure of transmission line channel is concluded step by step with the validation based on 2D/3D simulation and analytical solutions. In addition, this thesis proposed two different designs of Channel Board, low-loss version and low-cost version, with well-designed parameters for different application scenarios. The discontinuity effects on channel path are studied in a systematically approach from parasitic characterization to simulation verification. Several methods are proposed to improve the signal transition at the discontinuities.

Future work may include the expansion of this automated channel emulator from single-ended solution to differential solution. We could put two identical single-ended channel boards in a back-to-back positions to form an "uncoupled" differential structure. As long as the channel traces are identical with same lengths, the differential trace loss can be emulated from this system.

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VITA

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