DESIGN AND FABRICATION OF A 64-QAM MODULATOR FOR ANALYSIS OF SIGNALS BETWEEN STAGES

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Resumen

Este trabajo propone el diseño de un modulador digital 64-QAM en tarjeta impresa basado en tecnología en chip, la tarjeta desarrollada consta de dos fases de retardo y dos fases de amplificación, el modulador fue desarrollado usando el software PCB Wizard y fueron establecidos puntos de prueba para cada etapa. El diseño desarrollado fue construido a través de una máquina de control numérico por computadora. Los resultados experimentales muestran una mejora significativa en la precisión alcanzada de NMSE de -51 dB. La tarjeta desarrollada ofrece una herramienta de diseño para desarrolladores de hardware donde los

productos de intermodulación puedan ser evaluados, este modulador digital evita inductancias parásitas y capacitancias entre líneas. Los resultados del sistema desarrollado son efectivos para agregar ruido blanco Gaussiano y comprobar los los productos de intermodulación de hasta 3er orden que se pueden agregar, así como el efecto de recrecimiento espectral. El sistema es una herramienta de diseño de hardware capaz de mostrar por etapas los cambios en amplitud y fase que involucra una modulación de tipo QAM.

Palabras Claves: CNC, Diseño, Intermodulación, 64-QAM.

Abstract

This paper proposes the design of a 64-QAM digital modulator on board based on chip technology, the developed board comprises two phase delays and two amplification stages, the modulator was developed using the software PCB Wizard and were established test points for each stage. The developed layout was built through a computer numerical control machine. Experimental results show a significant improvement of the accuracy based on a reached NMSE= -51 dB. The developed board offer a design tool for hardware developers where the intermodulation products can be evaluated, this digital modulator avoid parasitic inductances and capacitances between the lines. The results of the developed system are effective to add white Gaussian noise and probe the intermodulation products up to 3rd order that can be added, as well as the effect of spectral regrowth. The system is a hardware design tool able to show by stages the amplitude and phase changes that involves a 64-QAM modulation.

*Keywords***:** *CNC, Intermodulation, Layout, 64-QAM.*

1. Introduction

With the explosive increase of mobile and portable communications, digital transmission with wide baud rate, the spectral availability has become so scarce. To make possible this global condition is required the use of digital modulation with big transfer schemes such as quadrature amplitude modulation (QAM). The design of the modulation, interleaving, coding, testing and characterization of cable

systems in North America is an important necessity [ANSI/SCTE, 2006], nowadays the main universities in Mexico related to Telecommunications are teaching the main digital concepts solely to explain the interpretation of digital constellations and the obtained performance in a digital link. Unfortunately, the students do not understand the behavior between stages even in the field there is no hardware related to QAM devices where the researchers and students can obtain the signals previous to the antenna in the transmitter.

However, such techniques are more susceptible to noise since a greater number of combinations means that these combinations are closer to each other and therefore the noise signal can be switched more easily. The probability of error in the transmitter chain depends primarily on the noise that is added to the modulated signal over the communication channel. In addition, the designers related to digital schemes requires platforms to properly address and correct the non-desirables effects that QAM system can achieve. For this reason, hardware and system level designers have made special efforts, not only through software [Cárdenas, 2012], but also in hardware implementation [Yan, 2013], [Gnauck, 2011], [Shin, 2003] testing QAM links [Kameda, 2011], [Besnoff, 2015], [Oguma, 2009] or creating sequences for multicarrier applications [Chang, 2010], [Lee, 2016] and QAM structures implemented in FPGA [Vu, 2010].

The authors agree that in order to carry out the feasibility studies of high modulation schemes is required the description in hardware of each stage. In this paper is developed a 64-QAM modulator in board controlled by an open-source electronic prototyping platform programmed in C language. It means that each amplification and phase delay stage is represented into board with the goal of provide a hardware option of QAM analysis for designers, each stage is built through the use of operational amplifiers and digital multiplexers.

This digital modulation technique is mainly used to send data on the downstream channel coaxial cable networks. It is a very efficient technique, supports transmission speeds up to 28 Mbps over a single 6 MHz channel. Although it is susceptible to interference signals, which makes it is not used in the upstream channel because it is very sensitive to the noise.

The main objective of this work is to provide an analysis tool for researchers and students related to telecommunications issues. A further work involves the performance analysis based on bit error rate (BER) compared with the energy per bit to noise power spectral density ratio (EbNo) and a study regarding to antenna coupling, in this case the performance study is not possible because the developed hardware just involves the circuitry and construction between stages.

Additionally, the purpose of this work aims to focus on the development of a 64-QAM modulator where all the test points are perfectly established for signal analysis.

The organization of this correspondence consists of three parts. In the section 2, we state the methodology and the fabrication of the 64-QAM modulator. In the section 3 are described the board performance and the accuracy in terms of normalized mean squared error (NMSE), the section 4 has the main discussion main results and accuracy obtained results the construction of the 64-QAM modulator controlled by FPGA. Finally, in conclusion are summarize the results obtained of the proposed tool.

2. Methods

Employed multilevel schemes as QAM requires a higher signal-to-noise ratio (SNR) than others binary ones under the same bit error rate (BER). Hence the importance of a proper capability for hardware design for these kind of schemes. M-ary QAM is a non-binary memoryless modulation technique in which one of M different symbols is transmitted per time using two orthogonal carriers (in quadrature). In this words are call I and Q signals that are divided by two channels. Each symbol represents a bit stream pack, the M-ary QAM can be represented by equations 1 and 2 [Correa, 2003].

$$s(t) = A_1 \gamma_1(t) + A_2 \gamma_2(t) \qquad (1)$$

$$q = log_2 M \qquad (2)$$

Where $\gamma_1(t) = sqrt(2/Ts)\cos(2\pi f_c t)$ for $0 \leq t \leq Ts$, otherwise $\gamma_1(t) = 0$ and $\gamma_2(t) = -sqrt(2/Ts)\cos(2\pi f_c t)$ for $0 \leq t \leq Ts$, otherwise $\gamma_2(t) = 0$, in which Ts

represents one symbol´s transmission time interval, fc is the carrier frequency and A_1 as wells as A_2 are the orthogonal carrier coefficients.

Considering that n is bigger than q. The n-bits in N sets of q-bits can be grouped, where q is given by equation 1 and N is an integer number. Based on the 64-QAM overview (figure 1) the q bits will travel simultaneously through the channel forming a 64-QAM symbol.

The used signals for the 64-QAM modulator have the same band width reaching a higher efficiency with the signals I(t) and Q(t) that are modulated by two carriers with the same frequency but with a phase delay of 90º, the equation 2 is shows the resulting expression.
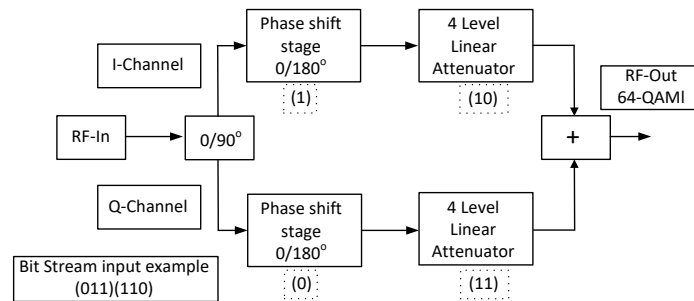
Figure 1 Overview of a typical 64-QAM modulator.

The 64-QAM architecture is based on the direct conversion principle to the RF transmission frequency. Considering the 64-QAM modulator the output signal is based on the RF input frequency [ANSI/SCTE, 2006]. The required frame for 64-QAM is represented in figure 2.
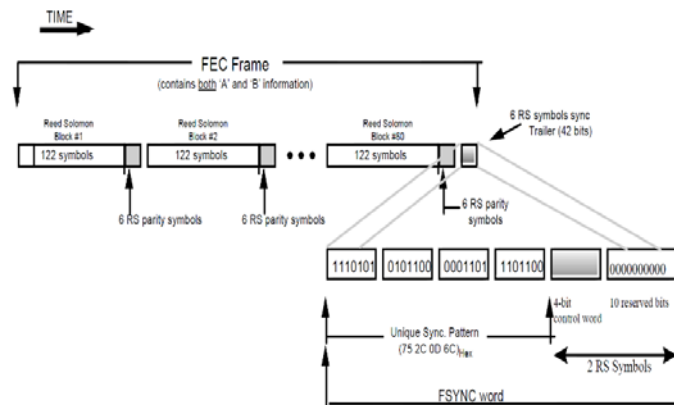

Figure 2 Frame packet format for 64-QAM modulator.

The RF output signal of the 64-QAM modulator can be denoted as s(t) as it is showed in the equation 3.

$$s(t) = I(t)\cos(2\pi f_0 t) + Q(t)\cos(2\pi f_0 t - 90°) = I(t)\cos(2\pi f_0 t) + Q(t)\sin(2\pi f_0 t) \quad (3)$$

Where f_0 represents the carrier frequency of the system. If the digital modulator is properly designed, a 64-QAM receptor should be able to demodulate the *s(t)* signal, adding a local oscillator. In the receptor side, the recovered signal *r_i(t)* is proportional to *s(t)*, an ideal form of *I(t)* is recovered and expressed by the equations 4.

$$I(t) = r_i(t)\cos(2\pi f_0 t)$$
$$= I(t)\cos(2\pi f_0 t) + Q(t)\sin(2\pi f_0 t)\cos(2\pi f_0 t)$$
$$= I(t)\cos(2\pi f_0 t)\cos(2\pi f_0 t) + \sin(2\pi f_0 t)\cos(2\pi f_0 t) \quad (4)$$
$$= I(t)\cos(2\pi f_0 t)^2 + Q(t)\sin(2\pi f_0 t)\cos(2\pi f_0 t)$$

using trigonometric functions, the equation 4 can be expressed as equations 5.

$$I(t) = \frac{1}{2}I(t)\left[1 + \cos(4\pi f_0 t)\right] - \frac{1}{2}Q(t)\left[\sin(4\pi f_0 t)\right]$$
$$= \frac{1}{2}I(t) + \left[\cos(4\pi f_0 t)\right] - Q(t)\left[\sin(4\pi f_0 t)\right] \quad (5)$$

Based on the equations 4 y 5 is designed the circuitry with dual 4-line to 1-line multiplexer that digitally separate the signal between stages, The multiplexers can select 2 bits of data from up to four sources selected by common the bit stream information, in this case the bit 0 and 1 of the 64-QAM symbol represent the address of the circuit, by other hand the bit 3 and 4 are controlling the second amplification stage. This circuit is used to strobe the outputs independently. The design between stages consist of high gain operational amplifiers.

Was used an open-source software for the design, the circuitry in figure 3 was developed in PCB Wizard. Once that the design was completed, and the code was generated using the tool CooperCAM is exported to the CNC machine. In the figure 4 can be seen the design to be exported to the CNC machine.
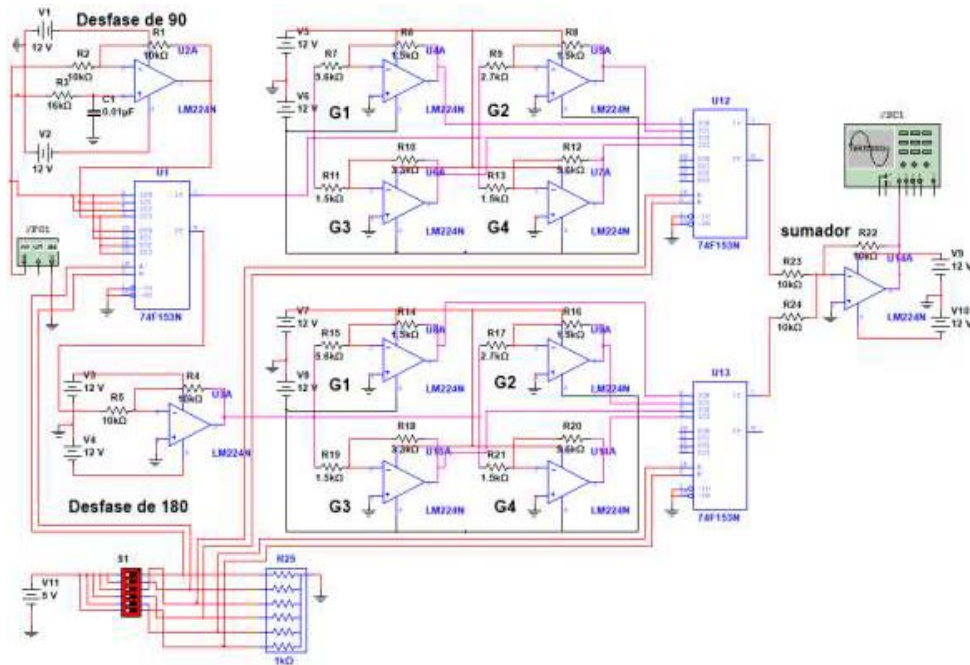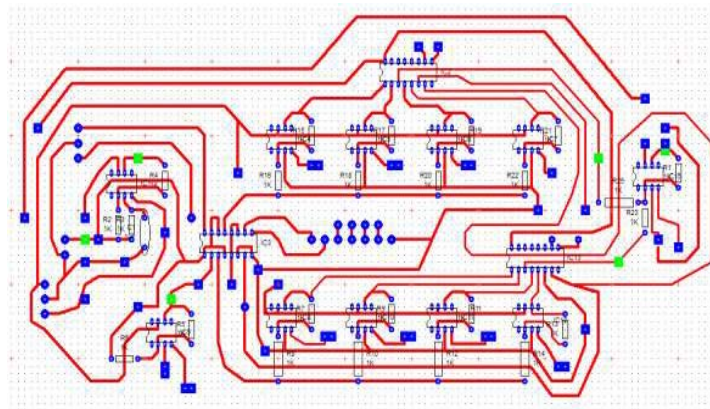
Figure 3 Circuitry of the 64-QAM digital modulator.

Figure 4 Overview of the developed layout.

The spaces between lines are optimized previous to generate the code for the CNC machine, the figure 5 depicts the general distribution of the devices taking into account the operational circuits and digital multiplexers. Should be noted that right angles were avoided in the corners in order to avoid induced antennas included by a poor design.

In the figure 6 is depicted the simulation and the tools that must be used for the drilling and cutting the modulator, the finals details related to time and length are corrected in this stage.
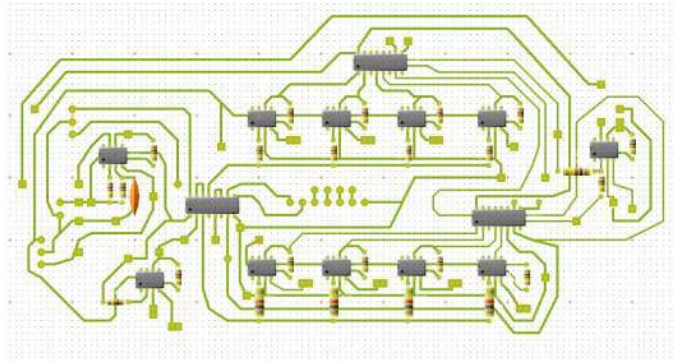
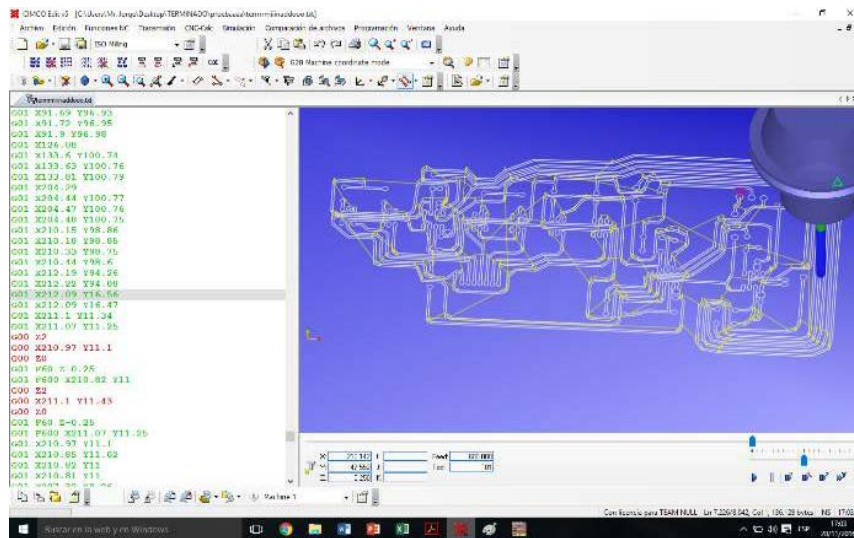Figure 5 Optimization of the developed board.

Figure 6 CIMCO Software of the CNC machine.

The figure 7 shows the generated 64-QAM digital modulator, where the test points were established properly and the parasitic inductances and capacitances between the lines were improved.
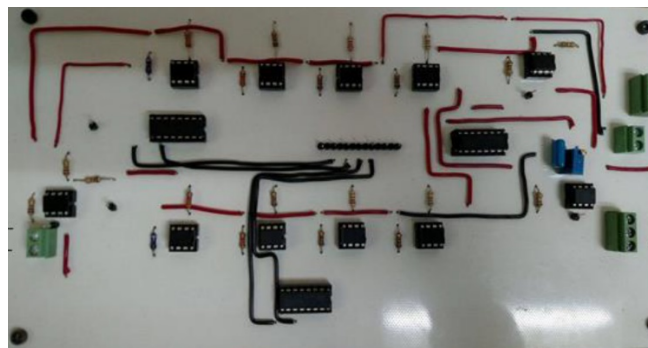

Figure 7 Overview of the developed 64-QAM board.

The figure 8 shows working the 64-QAM modulator, in this case a randomized bit stream was send as information and was packed in symbols (6 bits for 64-QAM), this information was implemented thought the board Arduino Uno taking advantage of the open source platform but other controllers can be adopted to the input port.

Figure 8 Photo of the measurement setup of the 64-QAM modulator.

3. Results

The predicted results based on the equations 4 and 5 were compared with the obtained results of the test bench setup showed in the figure 9. The input data is sent from host computer using Matlab for the result and by other way the data for the board is sent from the Arduino Uno platform, this study integrates a complete high performance for a digital serial stream. The figure 9 shows the signal with a phase offset of 90º in this case: a) represent the model in Matlab and b) the result in the scope for the first stage.

a)   b)
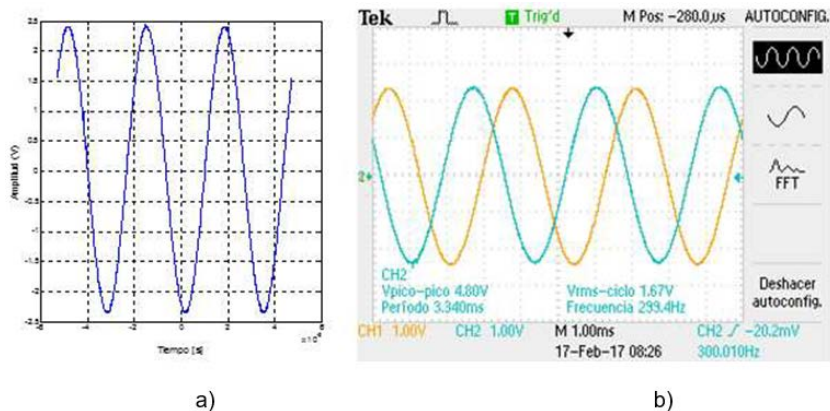
Figure 9 Obtained signal in the first stage with a phase delay of 90º in Matlab and Obtained signal in the scope measured in the Laboratory.

The figure 10 represents the signal with a phase offset of 90º taking into account the bit stream in the input port, in this case the bits numbered as 3 and 6 are controlling the delay stages, a) represent the model in Matlab and b) the result in the scope for the phase delay stages.
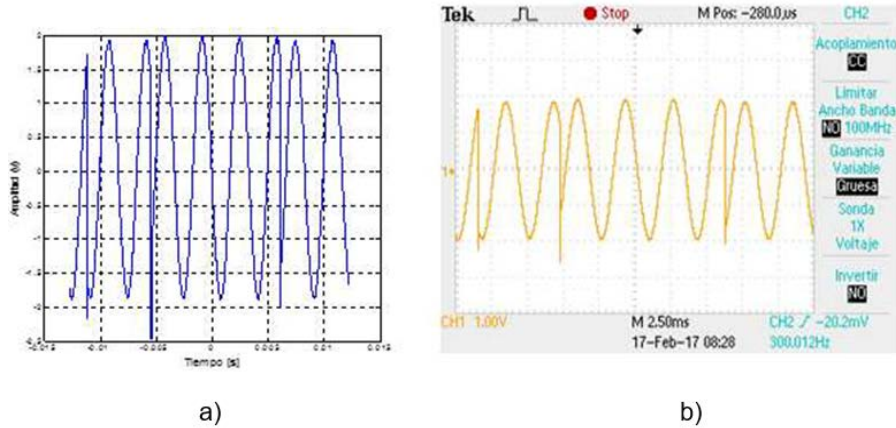

a)   b)

Figure 10 Obtained signal in the first stage with a phase delay of 90º in the two stages in Matlab and Obtained signal in the scope measured in the Laboratory.

The figures 11 and 12 show the amplitude changes after that the phase delay process was implemented, in this case are tested the two amplification stage controlled by four bits, a) represent the obtained model in Matlab and b) the result in the scope after the amplification process involving four amplifiers for each stage.

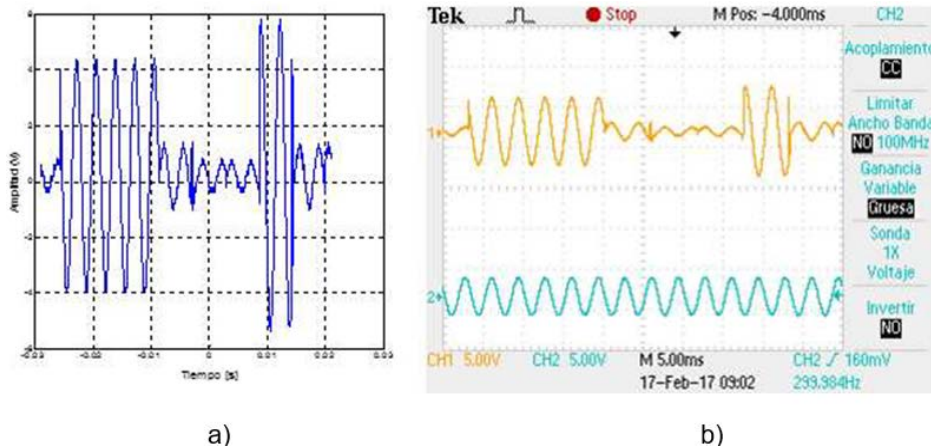a)   b)

Figure 11 Amplified signal previous to the final stage controlled by two bits after the phase delay process for a) Matlab result and Obtained signal in the scope.

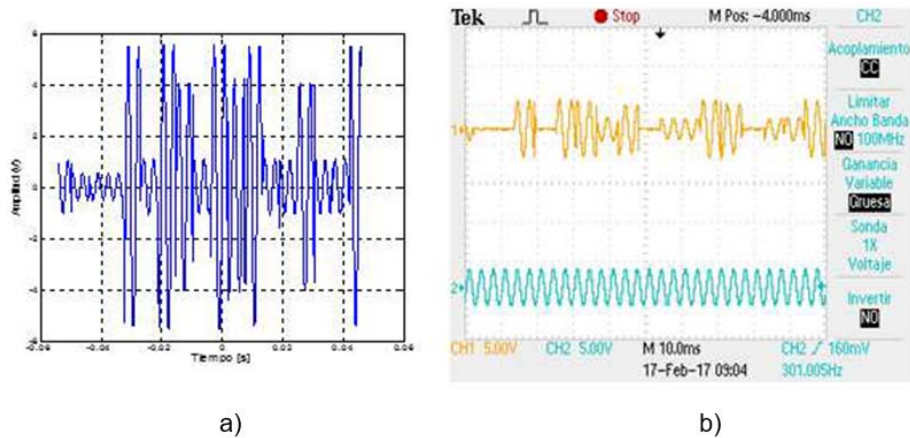a)   b)

Figure 12 Amplified signal of the second stage previous controlled by two bits after the
phase delay process for Matlab result and Obtained signal in the scope.

The used devices allow to work up to 1.3 MHz, the figure 13 shows a general wave
form of a 64-QAM signal, a further woks that include this methodology allow to
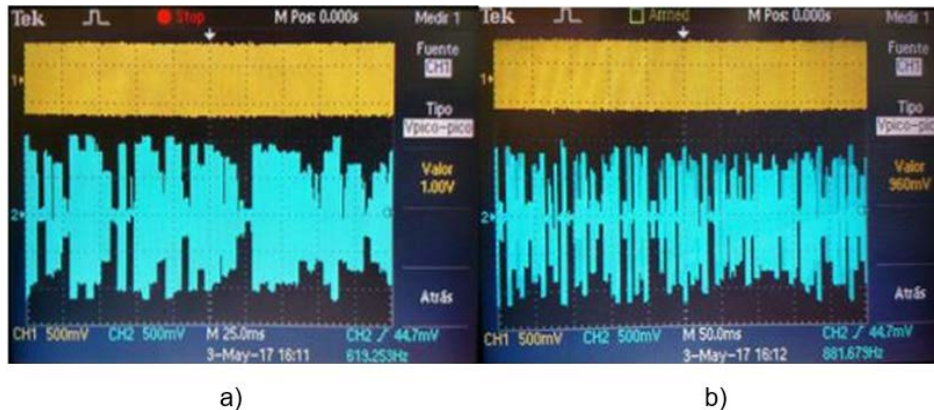emigrate to a higher band in the spectrum.

a)   b)

Figure 13 Two general waveforms of a 64-QAM signal up to 1.3 MHz.

4. Discussion

The hardware developers require the use of flexible platform in order to
understand properly the performance of a digital signal, as in this case the 64-
QAM. Experimental results show firstly in protoboard a result of NMSE= -19.5 dB
that was strongly improved to NMSE= -51 dB with the use of this methodology.
According with the obtained results the objective was reached and is showing with
a high accuracy the signals between stages.

The results modeled in Matlab compared with the general model of a N-QAM system and the measurements done in the laboratory tell us that the board fabricated through CNC machine was properly designed. A lot of knowledge about developing impressed board was gain by the authors.

5. Conclusions

The conclusions are summarized as follows:

- The simulated model and the general performance of the fabricated board had an error or NMSE=-51 dB improving the NMSE=-19.5 dB of a schematic develop in protoboard.

- This work derives in a hardware design tool for analysis of communication links that use 64-QAM.

- The developed tool can be used for academic and research purpose due to the details that comprise each stage.

- The next stage in this study is to measure the spectrum and verify if the spectral regrowth was reduced

- Further work require the use of mounting board an increase the frequency in order to emigrate to VHF and UHF used for ATSC in North America.

- This work contributes with a low cost solution for the national problem of connectivity in Mexico in the analysis stage.

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