Design of Linearity Improved Low Noise Amplifier using Derivative Superposition

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*Abstract–***This paper proposes different implementation of derivative superposition technique to improve the linearity of "Low Noise Amplifier" used in the receiver part of communication system. Derivative superposition is proved to be the promising technique for the improvement of linearity of LNA. This paper introduces the DS techniques in different forms by varying W, L or V_{GS} to achieve higher IIP3. Also the results in the implementations are compared to other existing methods. The proposed scheme just not only provides high IIP3 values but it remains stable for a large variations in V_{GS}, which is not the case with other existing techniques.**

Index Terms– **CMOS, DS, IIP3, LNA.**

I. INTRODUCTION

At present, Wireless communication, plays a very important role in daily life. The unparalleled and unique growth in wireless communication technology, made it mandatory to create an ever-increasing improvement in power consumption, low cost and high performance receiver topologies. Although CMOS is the technology of choice in terms of integration, but has limited capability to handle the interferers, which makes it a poor choice for designing the LNA. On the other hand, low power consumption of this technology made it mandatory to improve linearity of LNA due to the trade-offs exist between power consumption, linearity and gain. [1].

The LNA, a non-linear component, is the first and the most important block in the RF receiver. The linearity performance of the LNA becomes important to suppress the interference, coming with the signal, through antenna [8]. Third-order intermodulation product is the main aspect of consideration for the linearity improvement [1]. To improve the linearity the focus should be on reducing the third order intermodulation product. The input and output relation of any amplifier and IIP3 can be modelled as:

$$Y = g_1 V_{GS} + g_2 V_{GS}^2 + g_3 V_{GS}^3 \text{ and } IIP3$$
$$= \sqrt{\frac{4g_1}{3g_3}} \tag{1}$$

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Different techniques for improvement in IIP3 are already proposed in various literatures. The most common method to improve the IIP3 of any amplifier is to degenerate the source with a resistor or with an inductor. This technique may increase the linearity of the LNA, but with the compromise in gain [2-5]. Moreover, adding a passive component also adds noise in the circuit. Yet another technique is proposed with common source transconductance stage, which requires an additional capacitor (to remove the DC biasing effect in output) in parallel with the gate source intrinsic capacitance [10]. This tends to limit the working frequency of the LNA. Optimal biasing of LNA also provides very high linearity [6]. As shown in figure 1, the amplifier can be biased at the sweet spot where g3 = 0, which results in very high IIP3 in order of 18 to 21 dBm. Optimal Biasing is prone to process variation, which makes the sweet spot unstable. The sweet spot varies frequently and largely with PVT variations, which degrades the linearity performance of the LNA. Some literature also claims the linearity improvement by the technique called 'Current Bleeding' [5]. In this technique an extra transistor is added between the drain of the amplifying transistor pair and supply voltage. This technique is mainly applicable to the differential topology. Moreover, it may increase the gain considerably, but improvement in the linearity is not guaranteed. The paper proposes a simple but effective method of Derivative Superposition (DS), which cancels the third order harmonics in the output and improves the linearity of the amplifier. The concept of DS is presented in the next section.
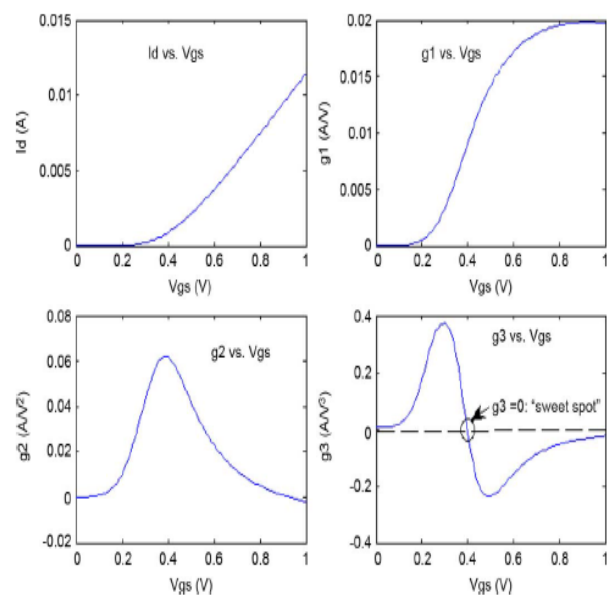

Fig. 1. NMOS Transconductance DC Characteristics

II.   DC THEORY OF DS METHOD

Consider, the MOSFET is biased in saturation. Its output current I_D can be modelled as:

$$I_D = g_1 V_{GS} + g_2 V_{GS}^2 + g_3 V_{GS}^3 \qquad (2)$$

Where, **g_1** represents small-signal gain. g_2 & g_3 represent the strength of corresponding non-linearity. Among all these non-linearity g_3 is of most concern as it controls the 3rd order intermodulation distortion. g_1, g_2 & g_3 are given in (3).

$$g_1 = \frac{\partial I_D}{\partial V_{GS}}, g_2 = \frac{\partial^2 I_D}{\partial V_{GS}^2}, g_3 = \frac{\partial^3 I_D}{\partial V_{GS}^3} \qquad (3)$$

Looking at equation 1, smaller the g3 larger the IIP3 of the amplifier. DS improves the IIP3 by removing the g3 component from the output and makes the amplifier more linear.

The DS technique uses two transistors in parallel as shown in figure 2. One auxiliary transistor (M_A) is biased in weak inversion region or subthreshold region and the main transistor (M_B) is biased in strong inversion region. It can be observed in figure 1 that in subthreshold region the value of g_3 is positive while in strong inversion region the value of g_3 is negative. So, when transistors are connected in parallel, they will add both the g_3 and hence the overall g_3 becomes smaller [7]. The exact cancellation may not be possible, but minimizing the g3 component up to a certain limit is possible. The variation of g3 with respect of input voltage V_{GS} is shown in figure 3. It can be observed that the value of g3 in the output is minimum for the combination of main and auxiliary transistors. The other main observation is that the value is stable for the larger range of V_{GS} variations, which was not the case with optimal biasing.
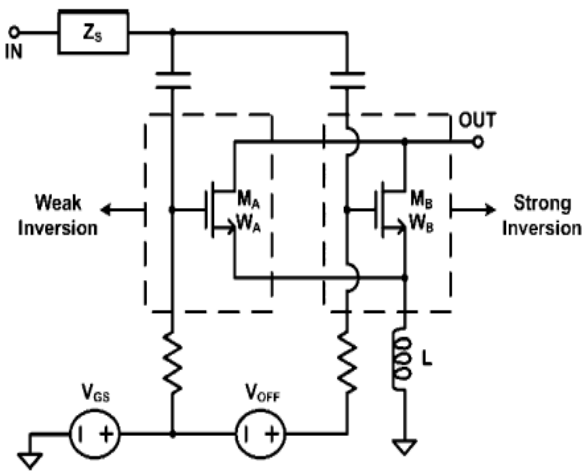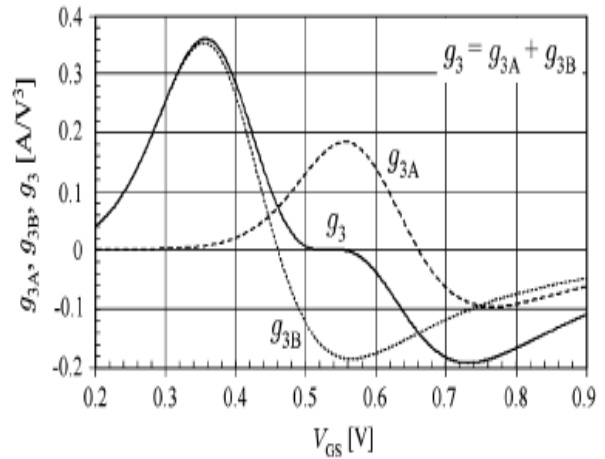

Fig. 2. Derivative Superposition Method

Fig. 3. 3rd Order Non-Linearity Coefficient vs VGS

III.   IMPLEMENTATION OF LNA BASED ON DS

The g3 component is dependent on the third order derivation of the drain current I_D with respect to the input voltage V_{GS}. Moreover, I_D is dependent on the design variables W and L. So, there are three major parameters V_{GS}, W and L those can effect g3 and can be modified easily for any design.

The easiest way to implement DS is to keep the width of auxiliary transistor as that of the main transistor. It is observed that the large transistors give better value of g3 in weak inversion region. So, the width of M_A is kept twice the width of M_B. As the width of the auxiliary transistor changes from W to 2W, the peak in the weak inversion region of the g_3 increases, which when added with the peak of the strong inversion region of main transistor's g3, minimizes the overall g_3. The width of auxiliary transistor can still be increased, but doesn't offer much improvement further. IIP3 can be significantly improved with this method, but stable range for which the value of g3 is minimum is difficult to obtain. To improve the stable minimum range of g3, one more auxiliary transistor with width W can be added to the existing design. Keeping large transistors in parallel with main transistor may improve the linearity of the circuit, but the large size of transistor weakens the performance of the circuit at high frequency. Large transistors also contributes more noise to the circuit.

The other possible improvement is to have two auxiliary transistors with the same width W, as that of the main transistor, but keeping the different bias voltage V_{GS} of both the auxiliary transistors. This method requires multiple voltages to be generated for different biasing, which is difficult to achieve. Auxiliary transistors with different width and different biasing together are also possible, but with very little improvement in linearity and large noise and low frequency of operation.

Yet another design parameter L can be altered to improve the linearity performance of the amplifier. It means that the length of the channel in auxiliary transistor is larger than that of main transistor, but follows the same technology i.e. 180nm. The main advantage of this method over other methods is that it provides a broader range of stable g3 with respect to change in V_{GS}. To further improve the circuit, a source degeneration resistor can be added as shown in the final circuit of figure 4. Once the IM3 components are taken care off, the higher order terms play an important role in deciding the linearity of LNA. The proposed design does not address the higher order nonlinearity.
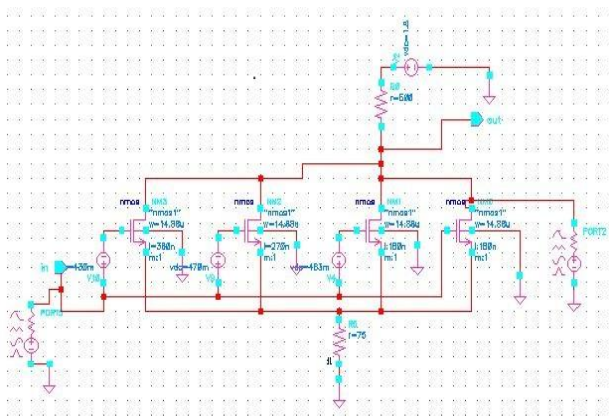

Fig. 5. IIP3 Measurement at -30 dBm Interference Power

Fig. 4. Schematic of Proposed Method

IV.   RESULTS

The Derivative Supper Position technique, which cancels the third order intermodulation products is designed with following specifications.

Table 1.
SPECIFICATION OF LNA

Supply	1.8 V
Power	2.9 mW
Gain	4.6 dB
IIP3	17.74 dBm
IIP2	23.34 dBm
1 dB Compression Point	-2.73 dBm
Frequency of Operation	2.4 Ghz

The maximum value of IIP3 observed is 17.74 dBm at -30dBm of input interference power as shown in figure 5. The voltage range for which the IIP_3 doesn't vary sharply from its peak value is observed to be 60mv in this case. The circuit dissipates 2.9mW power at 1.8V of supply. The results are compared with other reported techniques in Table 2. The maximum IIP3 is not the highest in this case, but it is quite near to the highest achievable IIP3. The added advantage is the large stable range of minimum g3, which is shown in figure 6.
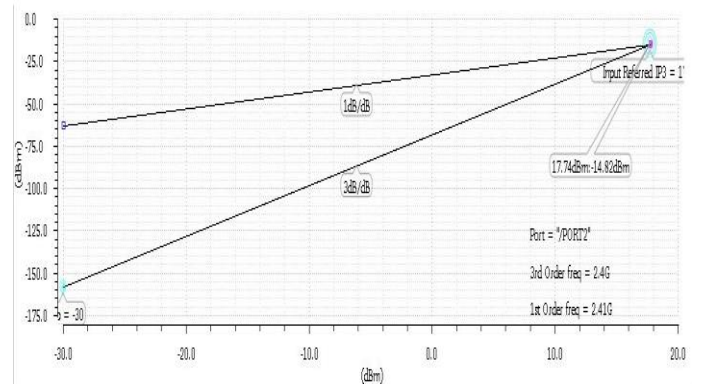

Fig. 6. IIP3 vs. VGS

Table 2.
COMPARISON TABLE

	Single Stage Amplifier (Own Design)	[6]	[7]	[10]	Proposed Work
Supply (V)	1.8	2.7	2.5	1.8	1.8
Technology (μ)	0.18	0.25	0.25	0.18	0.18
Operating Frequency	2.4 GHz	880 MHz	2.2 GHz	5.5 GHz	2.4 GHz
Current (mA)	1.65	2	8	6	1.61
Gain (dB)	9.5	14.6	15.3	10	4.6
IIP3 (dBm)	3.51	10.5	2.7	8.33	17.74
Power (mW)	2.97	5.4	20	10.8	2.9
VGS Range (mV)	NA	20	NA	NA	140

V.   CONCLUSION

High linearity LNA with third order cancellation technique is design in 180nm technology. Source

Degenerated Derivative Super Position method with more than one auxiliary transistors with different channel length is employed to achieve the cancellation of third order intermodulation products. The IIP3 of 17.74 dBm with flat g3 response w.r.t changes in VGS (60mv) is achieved. The implemented design is compared with the reported designs and found better compare to them.

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