Characterization & Comparative Analysis of High Speed CMOS Comparator for Pipelined ADC

Priyesh P. Gandhi, N. M. Devashryaee

***Abstract*—In todays high speed low power era, there is an increasing demand of a High Speed Comparator for ADC, DAC and various other applications in an analog and digital domain. This paper describes and analyzes five different architecture for low power and high speed comparators. In this paper, authors have analyzed and simulated the designs using TSMC 0.35 m CMOS technology with 2.0V for preamplifier based comparator and 1.8V power supply for dynamic comparators. The simulation results allow the circuit designer to fully explore the tradeoffs in comparator design, such as offset voltage, speed, power and area for Pipelined A/D Converters. Prelayout and postlayout simulations are carried out using Eldo SPICE tool and layout using IC Station.**

***Index Terms*—Analog to Digital Converters, CMOS, Comparators, Offset, Propagation Delay**

I. Introduction

THE rapidly growing market of portable electronic systems such as wireless communication devices, consumer electronics or battery-powered medical devices increases the demand for developing lowvoltage and low-power circuit techniques and building blocks [1]. In today's world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high resolution and high speed applications. One such application where low power, high resolution and high speed are required is Analog-to-Digital Converters (ADCs). In the past, pre-amplifier based and differential comparators have been used for ADC architectures. The main drawback of pre-amplifier based comparators is the high constant power consumption. Dynamic comparators are widely used in the high speed ADCs due to its low power consumption and fast speed.

II. Preamplifier Based Comparator

The comparator consists of three stages; the input preamplifier, a positive feedback or decision stage, and an output buffer. Differential amplifier will act as a preamplifier circuit. Higher gain can be obtained if the size of M3 and M4 is larger than the size of M31 and M41[2].Latch stage is also called decision circuit and capable of discriminating mV difference in the logic level. A self biasing differential amplifier is used as the comparator output buffer. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal. Current Mirror is used in the design for providing a constant current over a wide range of voltage [2]-[3].

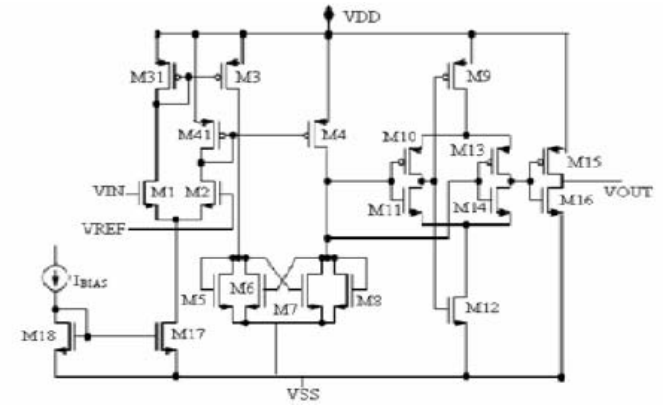

Fig. 1. Preamplifier based Comparator

A. Prelayout Simulation Results

Prelayout simulation is carried out using the ELDO Spice in TSMC 0.35μm technology. This section describes the simulation results of static characteristics and dynamic characteristics of comparator

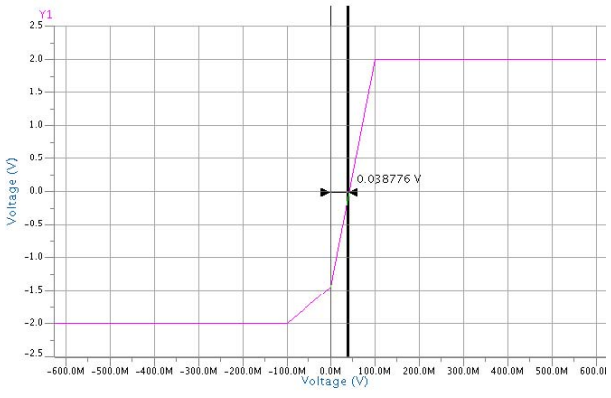

Fig. 2. Offset of Preamplifier based Comparator

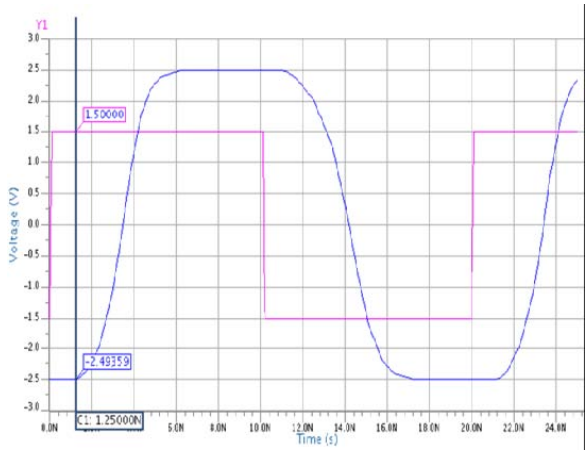

Fig. 3. Propagation Delay Preamplifier based Comparator

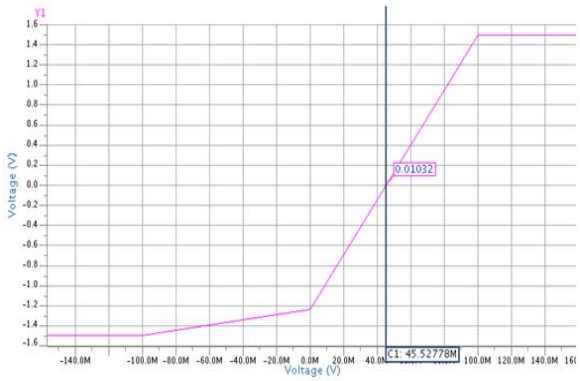

Fig. 6. Offset of Preamplifier based Comparator

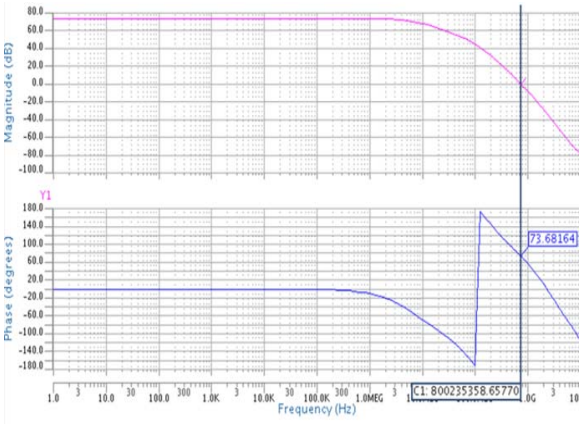

Fig. 4. Frequency Response of Preamplifier based Comparator

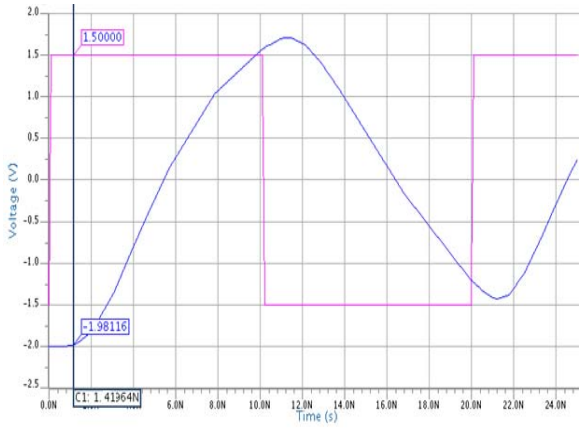

Fig. 7. Propagation Delay Preamplifier based Comparator

B. Layout and Postlayout Simulation Results

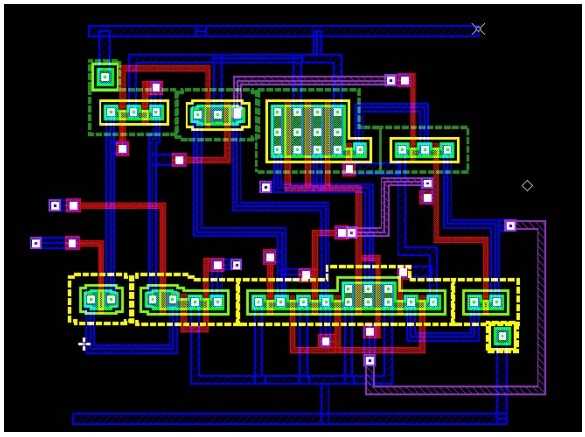

Fig. 5. Layout of Preamplifier based Comparator

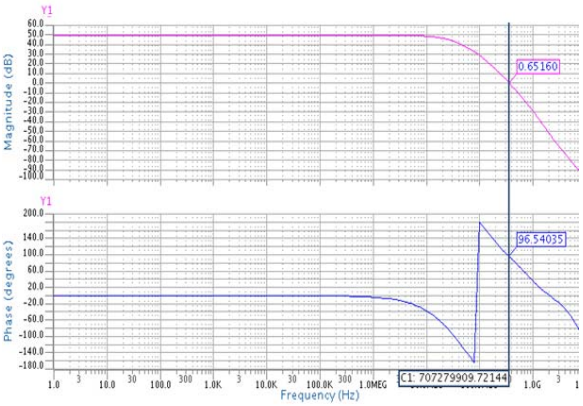

Fig. 8. Frequency Response of Preamplifier based Comparator

III. Differential Comparator

A fully differential typical dynamic comparator is shown in Fig. 9 [4]. The comparator consists of two cross coupled differential pairs with inverter latch at the top. Comparison is made based on the inverter currents, which are related to the inputs, when the clk goes high [4], [5]. The transistors

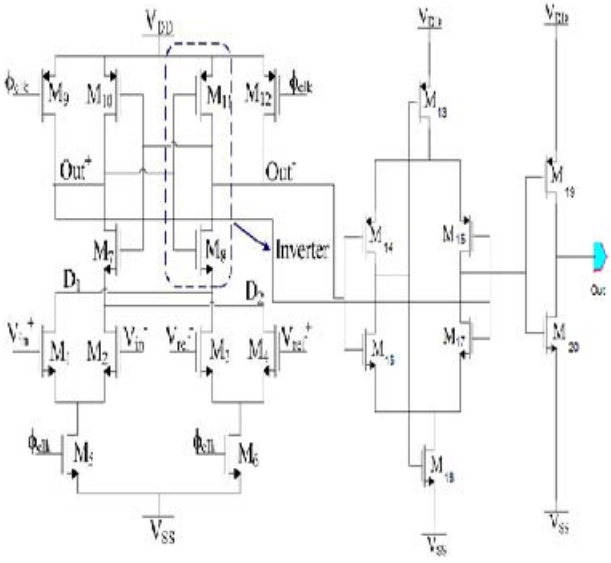

Fig. 9. Differential Dynamic Comparator

connected to the input and reference $(M1M4)$ are in the triode region and act like voltage controlled resistors. If no mismatch is present the comparator changes its output when the conductances of the left and right input branches are equal $gL = gR$. By denoting $WA = W4$ and W5 and $WB = W2 = W3$ the input voltage where the comparator changes the state is

$$V_{in+} - V_{in-} = \frac{W_B}{W_A}(V_{ref+} - V_{ref-}) \tag{1}$$

The transconductance of the transistors $M1M4$ operating in the linear region can be approximately written

$$g_{m1,2,3,4} = \mu_0 C_{ox} \frac{W_{1,2,3,4}}{L} V_{ds1,2,3,4} \tag{2}$$

A. Prelayout Simulation Results

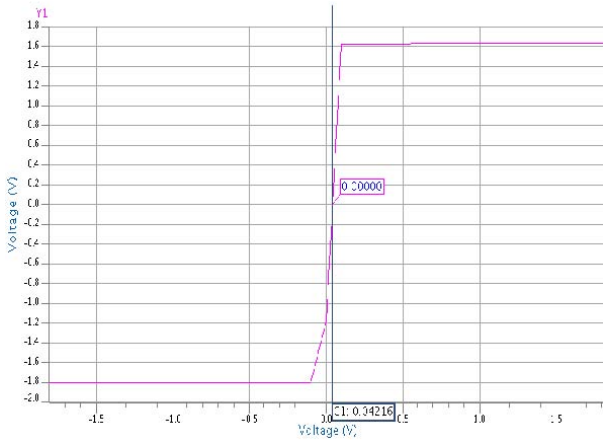

Fig. 10. Offset of Differential Comparator

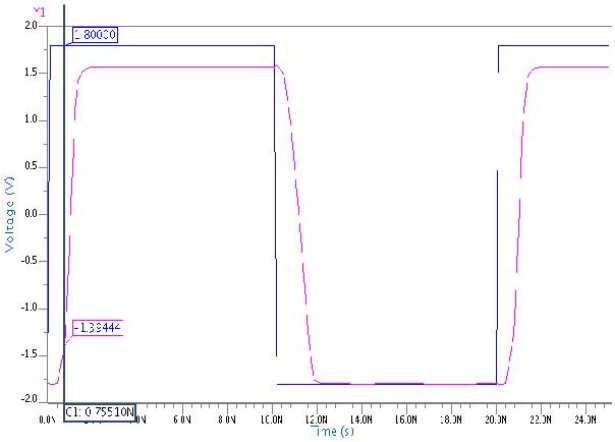

Fig. 11. Transient Response (Propagation Delay) of Differential Comparator

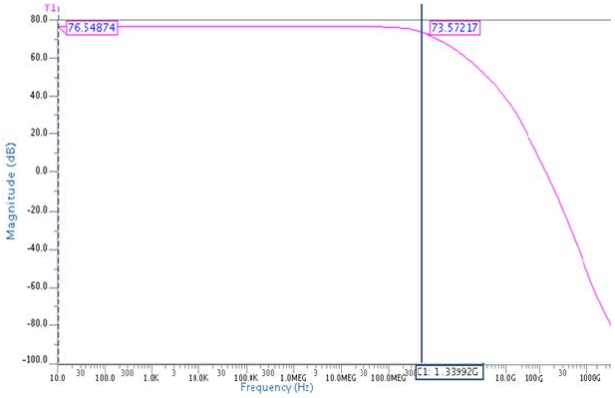

Fig. 12. Frequency Response (Gain) of Differential Comparator

B. Layout and Postlayout Simulation Results

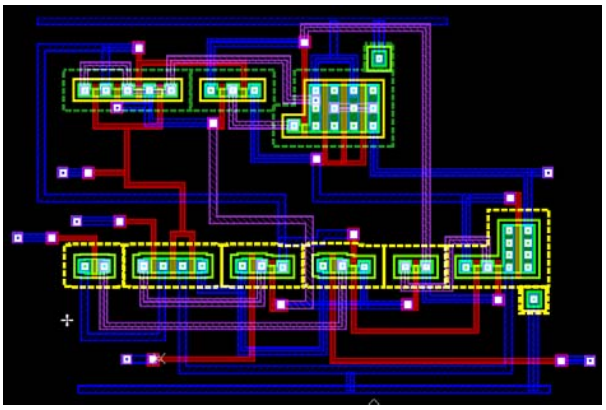

Fig. 13. Layout of Differential Comparator

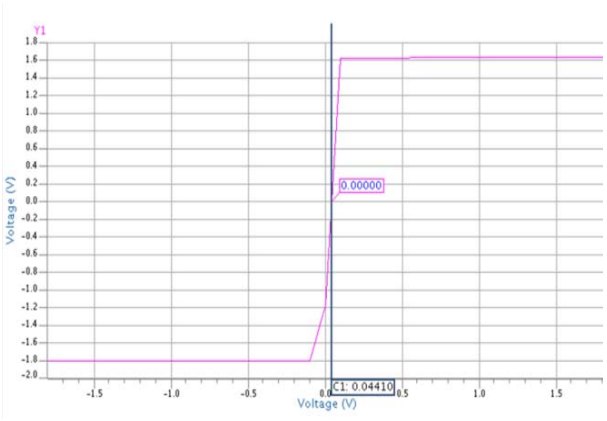

Fig. 14. Offset of Differential Comparator

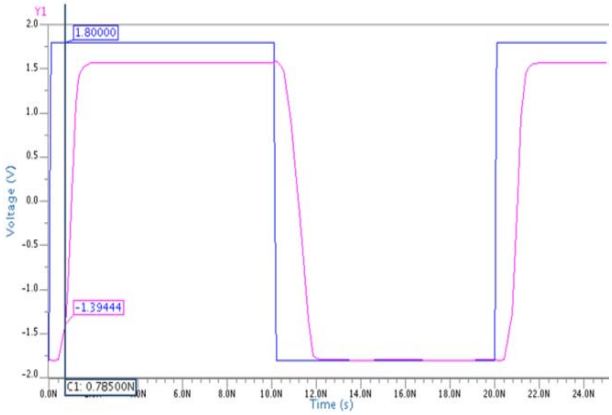

Fig. 15. Transient Response (Propagation Delay) of Differential Comparator

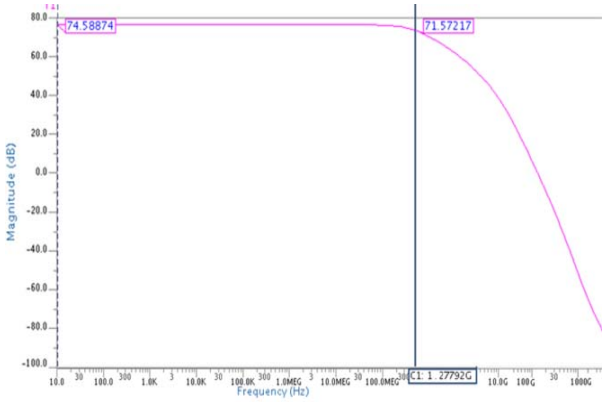

Fig. 16. Frequency Response (Gain) of Differential Comparator

IV. Dynamic Comparator

A dynamic comparator is present in this section which addresses the problems in the differential comparator as shown in Fig. 17 [6]. The first modification is related to the tail current clock signal. Instead of using the same clock as that for the top switches, which goes from V_{ss} to VDD, a same phase restricted voltage swing clock (ϕclk,B) has been used, i.e. ϕclk,B high is less than VDD. V_{in+} and V_{ref+} (and V_{in-} and V_{ref-}) are combined in one differential pair as compared to V_{in+} and V_{in-} (and V_{ref+} and V_{ref-})[6],[7].

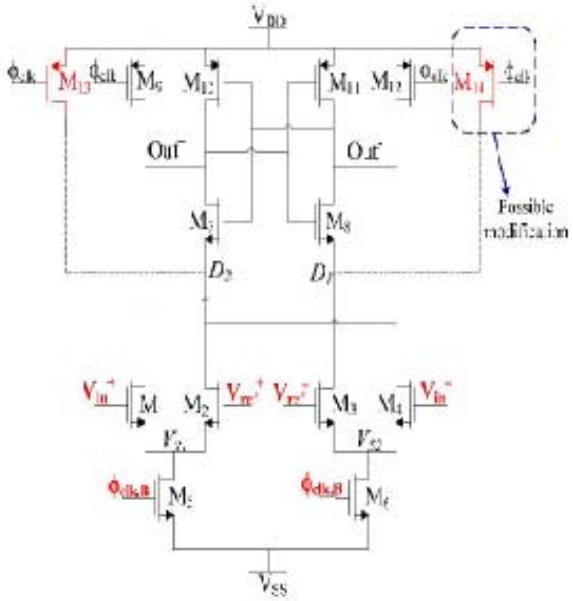

Fig. 17. Dynamic Comparator

A. Prelayout Simulation Results

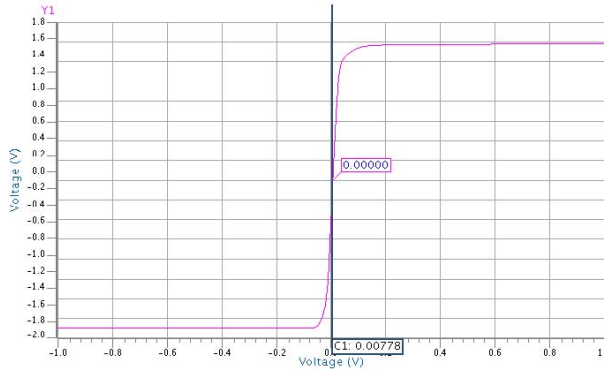

Fig. 18. Offset of Dynamic Comparator

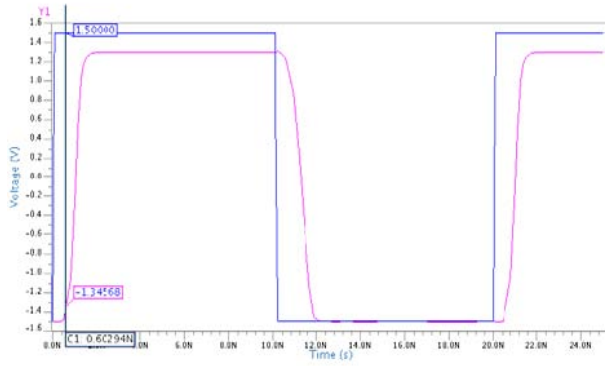

Fig. 19. Transient Response (Propagation Delay) of Dynamic Comparator

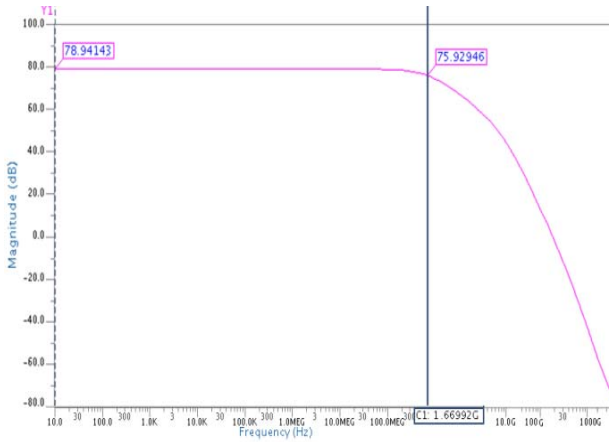

Fig. 20. Frequency Response (Gain) of Dynamic Comparator.

B. Layout and Postlayout Simulation Results

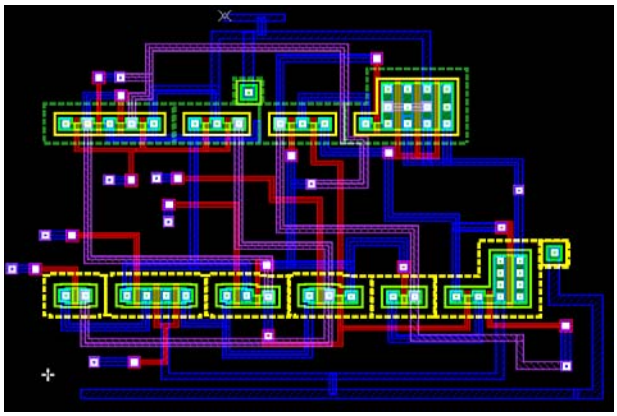

Fig. 21. Layout of Dynamic Comparator

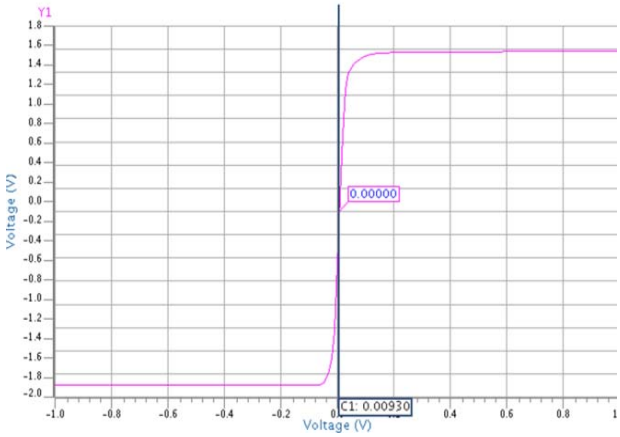

Fig. 22. Offset of Dynamic Comparator

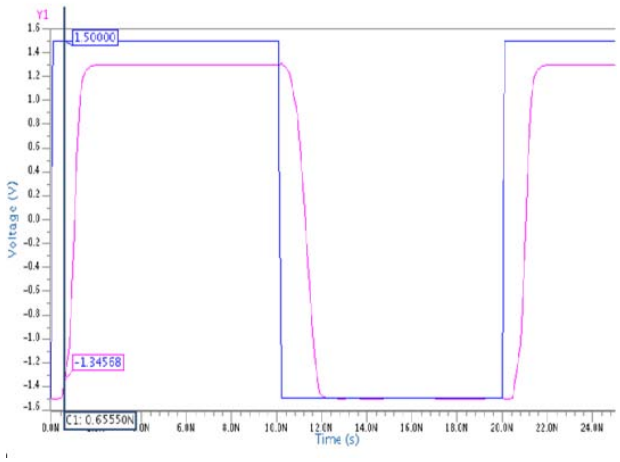

Fig. 23. Transient Response (Propagation Delay) of Dynamic Comparator

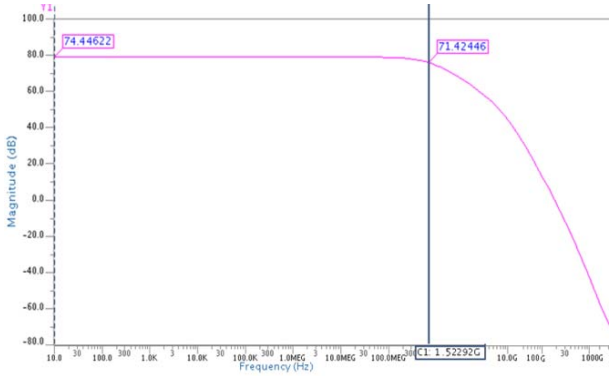

Fig. 24. Frequency Response (Gain) of Dynamic Comparator.

A. Prelayout Simulation Results

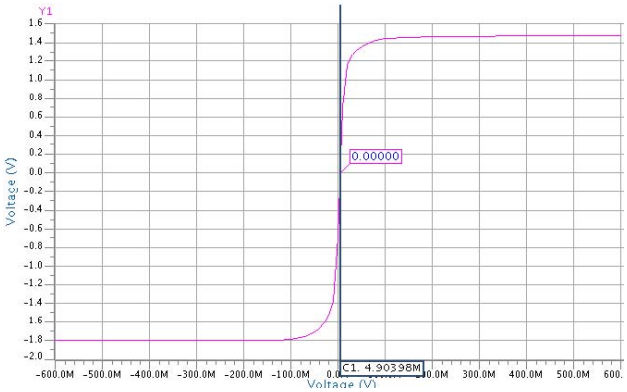

Fig. 26. Offset of Dynamic Comparator using Positive F/B

V. Dynamic Comparator using Postive F/B

Dynamic comparator using positive feedback is shown in Fig. 25. The hysteresis can also be accomplished by using internal positive feedback [8]. In this circuit there are two paths of feedback. The first is current-series feedback through the commonsource node of transistors M1 and M4. This feedback path is negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors M9 and M11. This path of feedback is positive. If the positive-feedback factor is less than the negative-feedback factor, then the overall feedback will be negative and no hysteresis will result [8],[9]. If the positive-feedback factor becomes greater, the overall feedback will be positive, which will give rise to hysteresis in the voltage-transfer curve. As long as the ratio $\frac{\beta_{M9}}{\beta_{M8}}$ is less than one, there is no hysteresis in the transfer function. When this ratio is greater than one, hysteresis will result.

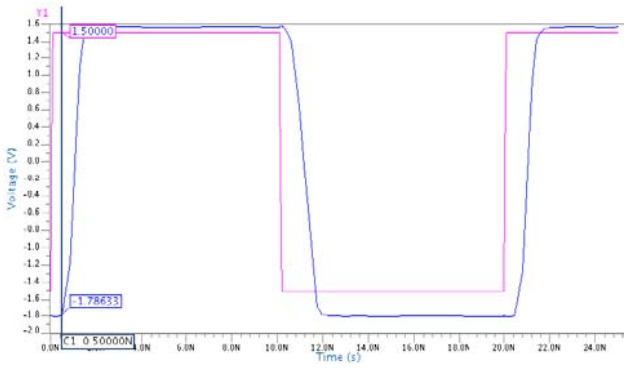

Fig. 27. Transient Response of Dynamic Comparator using positive F/B.

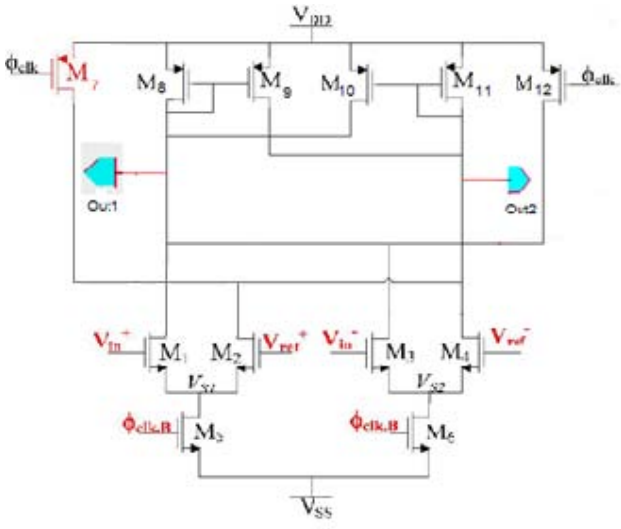

Fig. 25. Dynamic Comparator using Positive F/B

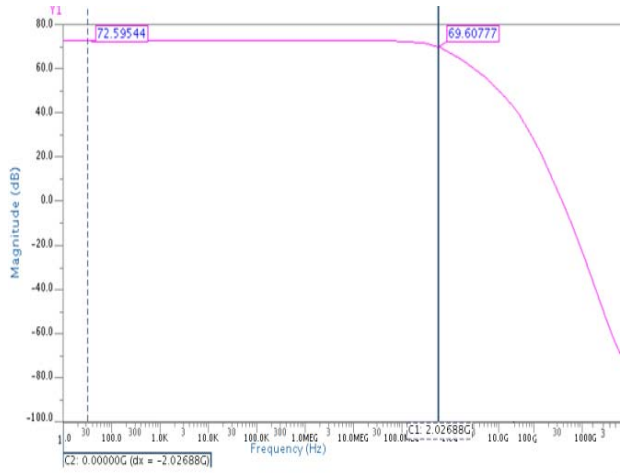

Fig. 28. Frequency Response (Gain) of Dynamic Comparator using Positive F/B

B. Layout and Postlayout Simulation Results

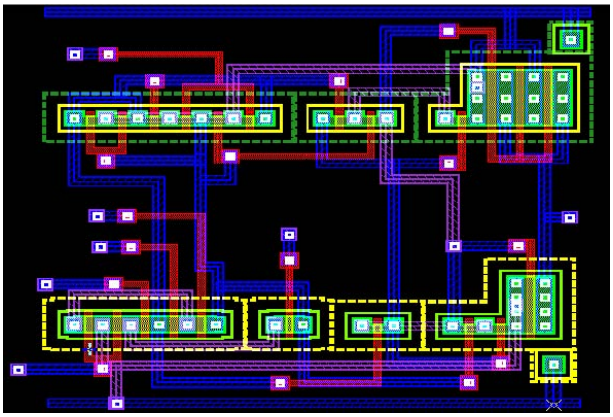

Fig. 29. Layout of Dynamic Comparator using Positive F/B

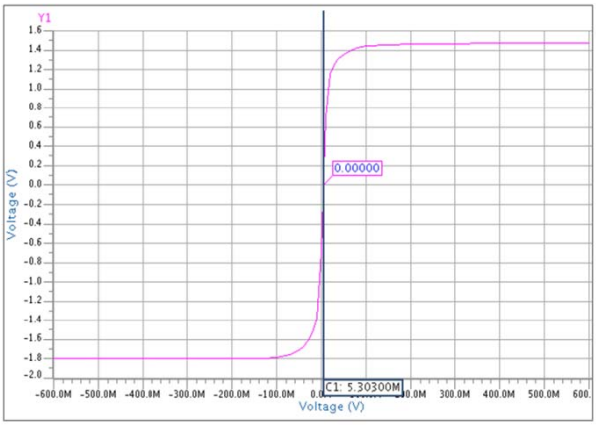

Fig. 30. Offset of Dynamic Comparator using Positive F/B

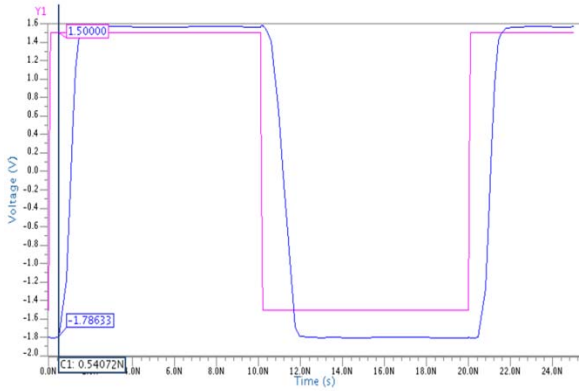

Fig. 31. Transient Response of Dynamic Comparator using positive F/B

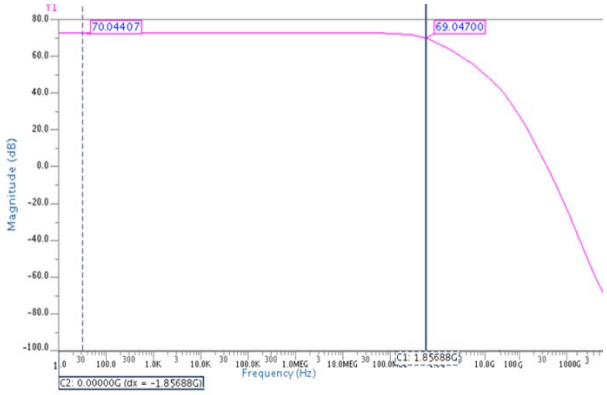

Fig. 32. Frequency Response (Gain) of Dynamic Comparator using Positive F/B

VI. DYNAMIC COMPARATOR USING POSITIVE F/B & PMOS SWITCH

The Dynamic Comparator using Positive F/B & pMOS Switch design is shown in Fig-33 is similar as Dynamic Comparator using Positive F/B shown in Fig.-25 of accept two pMOS Switches are connected to the clock and these two pMOS switches draws more current .So mismatches are reduced . After simulation the offset voltage is 1.40 mV

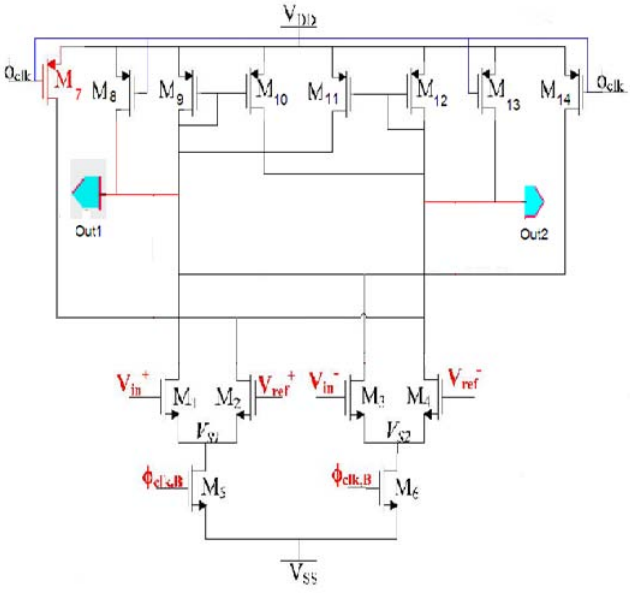

Fig. 33. Dynamic Comparator using Positive F/B & pMOS Switch

A. Prelayout Simulation Results

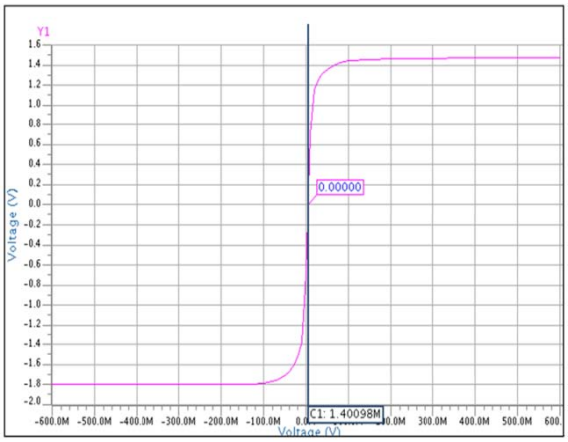

Fig. 34. Offset of Dynamic Comparator using Positive F/B & PMOS Switch

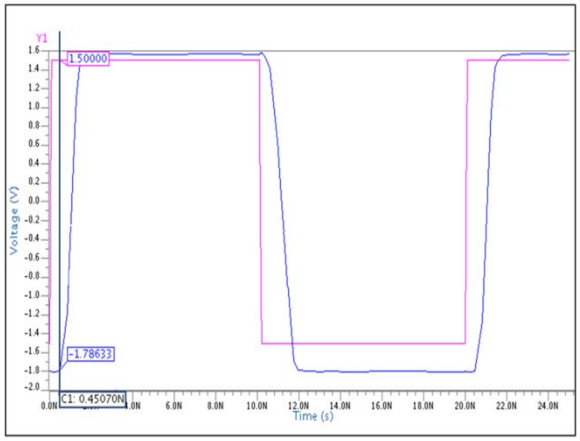

Fig. 35. Transient Response of Dynamic Comparator using positive F/B & pMOS Switch

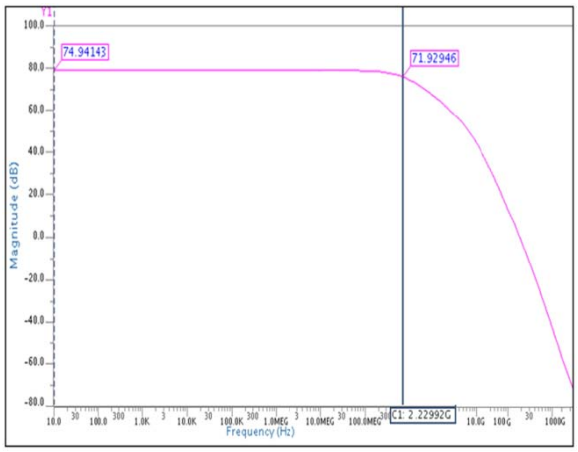

Fig. 36. Frequency Response (Gain) of Dynamic Comparator using Positive F/B & pMOS Switch

B. Layout and Postlayout Simulation Results

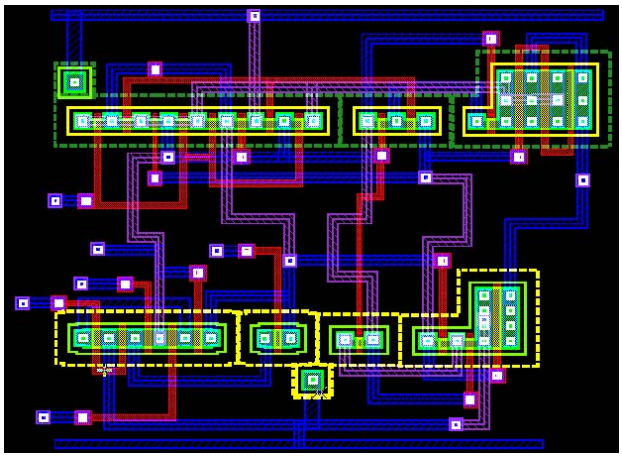

Fig. 37. Layout of Dynamic Comparator using Positive F/B & pMOS Switch

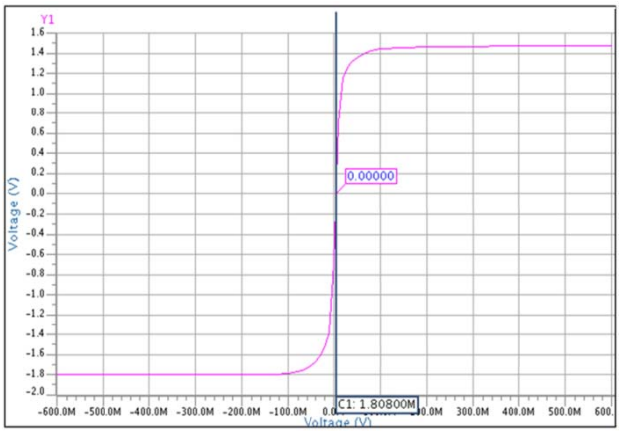

Fig. 38. Offset of Dynamic Comparator using Positive F/B & PMOS Switch

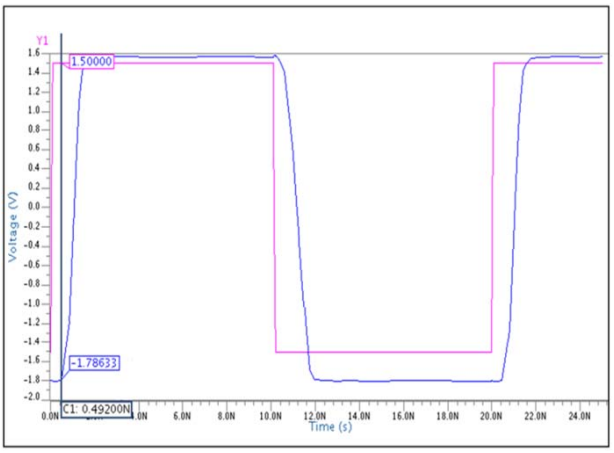

Fig. 39. Transient Response of Dynamic Comparator using positive F/B & pMOS Switch

Sr.No.	Type of Comparator	Offset(mV)	Delay(ns)	Speed	Gain(dB)	Power Dissipation(mW)
1.	Preamplifier Based Comparator	38.77	1.25	800MHz	75	2.3
2.	Differential Comparator	42.67	0.75	1.33GHz	76.54	1.87
3.	Dynamic Comparator	7.78	0.60	1.66 GHz	78.94	2.57
4.	Dynamic Comparator Using Positive F/B	4.90	0.5	2.00	72.59	1.97
5.	Dynamic Comparator Using Positive F/B & pMOS Switch	1.40	0.45	2.22	74.94	2.37

TABLE I
CHARACTERIZATION & COMPARATIVE ANALYSIS OF HIGH SPEED CMOS COMPARATOR: PRELAYOUT SIMULATION RESULTS

Sr.No.	Type of Comparator	Offset(mV)	Delay(ns)	Speed	Gain(dB)	Power Dissipation(mW)	Area(μm^2)
1.	Preamplifier Based Comparator	45.52mV	1.4	714MHz	49	3.41	31,312
2.	Differential Comparator	44.10mV	0.78	1.28GHz	74.58	3.65	37,591
3.	Dynamic Comparator	9.30mV	0.65	1.52GHz	74.44	3.97	39,390
4.	Dynamic Comparator Using Positive F/B	5.30	0.54	1.85	70.04	2.48	22,400
5.	Dynamic Comparator Using Positive F/B & pMOS Switch	1.80	0.49	2.02	71.44	2.93	27,024

TABLE II
CHARACTERIZATION & COMPARATIVE ANALYSIS OF HIGH SPEED CMOS COMPARATOR: POSTLAYOUT SIMULATION RESULTS

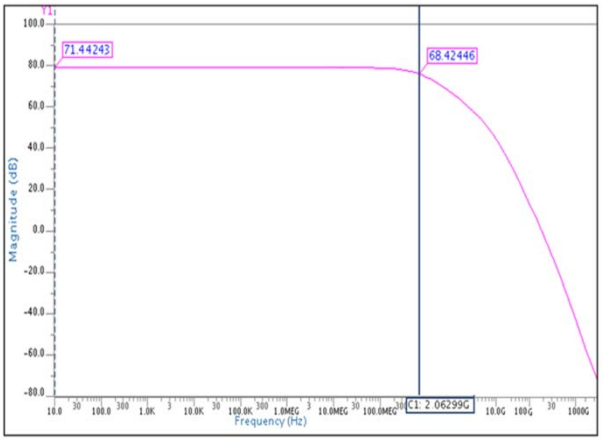

Fig. 40. Frequency Response (Gain) of Dynamic Comparator using Positive F/B & pMOS Switch

VII. CHARACTERIZATION & COMPARATIVE ANALYSIS

The pre-layout and post-layout simulations are carried out using ELDO Spice and Layout is done using IC-Station Tool from Mentor Graphics. Following Table-I and Table-II shows the comparative analysis of the different architectures of the CMOS Comparator Design which is presented in this thesis.The comparator is characterized in terms of the offset, propagation delay, gain, power dissipation and area. The simulation results allow the circuit designer to fully explore the tradeoffs in comparator design, such as offset voltage, speed, power and area for Pipelined A/D Converters. In the past, Preamplifier Based and Differential Comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the high constant power consumption.Dynamic comparators are widely used in the high speed ADCs due to its low power consumption and High speed. As shown in Table-I and II Dynamic Comparator has low offset, high speed and low power consumption as compared to the Preamplifier Based Comparator and Differential Comparator. By adding Feedback as shown in Fig-27 the Dynamic Compactor which is presented here can be realized for the flash and pipelined A/D Converters because of the less offset, high speed, low power consumption and less area.

VIII. CONCLUSION

The comparators are simulated in TSMC 0.35m standard digital CMOS process. Results are tabulated in Table I and II. We have observed that the dynamic comparator can be realized for the flash and pipelined ADC because it shows low offset, high speed, high gain and low power dissipation compared to preamplifier based comparator and differential comparator. Further by decreasing the number of transistors and scaling of each transistor, less area, low power dissipation and high speed can be achieved.

REFERENCES

[1] Jun He, Sanyi Zhan, Degang Chen, Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators IEEE Transation on Ciruits ans Systems-I: Regular Papers, Vol. 56, No. 5, May 2009.

[2] R. Jacob, Baker, Harry W. Li and David E. Boyce, CMOS-Circuit, Design, Layout and Simulation."

[3] Philips E. Allen, Douglas R. Holberg , CMOS Analog Circuit Design.

[4] L. Sumanen, M. Waltari, K. Halonen, "A Mismatch Insensitive CMOS Dynamic Comparator for Pipeline A/D Converters IEEE ICECS, vol.1, pp. 32-35, Dec. 2000.

[5] L. Sumanen, M. Waltari, V. Hakkarainen, K. Halonen, "CMOS Dynamic Comparators for Pipeline A/D Converters," IEEE ISCAS, vol.5, pp. 157-160, May 2002.

[6] T. W. Matthews, P. L. Heedley, "A Simulation Method for Accurately Determining DC and Dynamic Offset in Comparators," IEEE MWSCAS, pp. 1815-1818, Aug. 2005.

[7] Vipul Katyal, Randall L. Geiger and Degang J. Chen, A New Low Offset Dynamic Comparator for High Resolution High Speed ADC Application, Semiconductor Research Corporations Student Symposium 2006.

[8] J. Millmand and C. C. Halkies. Integrated Electronics: Analog and Digital Circuits and Systems. McGraw Hill, New York, 1972.

[9] A. S. Sedra and K. C. Smith. Microelectronics Circuits. 4th Edition, Oxford University Press, 1998.

[10] S.Sheikbaei S. Mirabbasi and A. Ivanov. A 0.35 m CMOS Comparator Circuit for High- Speed ADC Applications. IEEE International Symposium on Circuit and Systems, vol. 39,pp. 6134-6137, May 2005.

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