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PCB access impedances extraction method of in-situ integrated circuit

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Abstract

This article describes an extraction technique of input and output impedances of integrated circuits (ICs) implemented onto the printed circuit boards (PCBs). The feasibility of the technique is illustrated with a proof-of-concept (POC) constituted by two ICs operating in a typically transmitter-receiver (Tx-Rx) circuit. The POC system is assumed composed of three different blocks of emitter signal source, load and interconnect passive network. This latter one is assumed defined by its chain matrix known from its electrical and physical characteristics. The proposed impedance extraction method is elaborated from the given signals at the transmitter output and receiver input. The terminal access impedances are formulated in function of the parameters of the interconnect system chain matrix. The feasibility of the method is checked with a passive circuit constituted by transmission lines driven by a voltage source with RL-series network internal impedance and loaded at the output by the RC-parallel network. Good correlation between the access impedance reference and calculated is found.

1. Introduction

To meet the public and industrial challenging demand, modern electronic printed circuit boards (PCBs) must operate in a critical condition of confined space under higher data speed and higher frequency [1-3]. Nowadays, the high-density interconnect (HDI) [4] design is adopted as the main technological solution against this technological constraint. The technology and the PCB reliability become a major issue during the design phase [5]. The electrical interconnect network becomes outstandingly complex with respect to the increase of integration density [6-7]. The interconnect impact as signal integrity (SI), power distribution, signal distortion and signal delay must be taken into account [8-10]. Moreover, significant electromagnetic compatibility (EMC) and electromagnetic interference (EMI) issues are encountered by the PCB designers and manufacturers [11-12].

Therefore, further progress on design methodology is reported in order to overcome the PCB HDI constraints [13]. New insight on the interconnect model must be developed [14]. Despite the developed design methodologies, a lot of improvement is required for understanding the different electrical and electromagnetic effects generated by the HDI structures. Improvements in term of analysis and design are necessary to predict the electrical network efficiency [15]. To face up this technical issue, interconnect complexity reduction was proposed [16]. PCB layout design was reported [17]. Moreover, the design technique enabling constant cost reduction processing was developed [18]. So far, different steps of interconnect modeling of planar PCB have been proposed [19-22]. In addition to the lumped circuit approach, more accurate modeling from symmetrical [19-20], asymmetrical [21] and interbranch coupled [22] effects on PCB signal distribution has been achieved.

Despite the development of interconnects modeling, the mismatch effect between the localized components as integrated circuits (ICs) cannot also be neglected on the PCB SI performances [23-24]. It was found that the in-situ IC mismatch effect remains a main breakthrough of electronic PCB users. To analyze this effect, the matched access impedances constitute the key elements for the electronic system and PCB efficiency. The nets input and output impedances may become a challenging task when the electronic system as printed circuit board (PCB) is in operation mode. The diagnosis analysis can be validated with the appropriate measurement methodology [25-29]. This analysis chain is required for the ending step of PCB layout guidelines. Pin point signal testing constitutes one of the efficient techniques for the PCB diagnosis [25]. Different test techniques have been deployed for controlled impedance circuits [26]. However, the existing techniques are expensive and time-consuming to meet the board level testability requirement [27-28]. Few test techniques are, so far, available to assessing the PCB integrated component characteristics as impedance assessments. The in-circuit test (ICT) technique which enables to characterize one component independently to the others was suggested to address this issue [29]. But the technique must be accompanied by the suitable post-processing method. Such technique can be envisaged for characterizing the PCBs access impedances.

In the frame of the EDDEMA project funded by EURIPIDES² EUREKA program, we are dealing with the analysis of transmitter-receiver (Tx-Rx) electronic circuit. In other words, it acts as a multilayer PCB SI linked to the in-situ PCB mismatch problem. Figure 1 illustrates the configuration of the multilayer PCB [30-31]. This mismatch problem can be solved with the access impedance characterization.

For this reason, the present paper purposes to initiate an extraction method of the access impedances of the electronic system signal transmission chain. The method is based on the consideration of typically transmitter-receiver (Tx-Rx) system diagram.

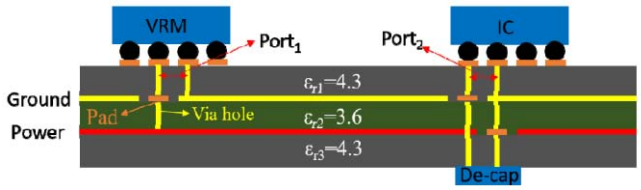

Figure 1: Tx-Rx circuit implemented on multilayer interconnect PCB [30-31].

The system is mainly assumed composed of a transmitter block which contains the voltage signal source, the receiver block and the interconnection system. Based on the considered system chain matrix [19-21], the relations between the input/output voltages and currents are established. Then, the access impedance assessment relations are calculated.

2. Description of impedance extraction methodology

The present section describes the analytical steps of the impedance extraction method under study. After the definition of the system problem, the equivalent chain matrix is elaborated. Then, the access impedances in function of the given test signals are expressed. It is worth to mention that the proposed access impedance extraction method can be applied only to linear time-invariant (LTI) system.

2.1. Statement of the system analysis problem

Fig. 2 introduces the diagram of the Tx-Rx circuit configuration under consideration. This diagram is mainly composed of two integrated circuits (ICs). IC_1 is assumed as the driven source. It generates the input signal propagating along the considered network. IC_2 is considered the receiver circuit which behaves as an output load. The main unknowns of this problem are the output impedance Z_1 of IC_1 and input impedance Z_2 of IC_2.

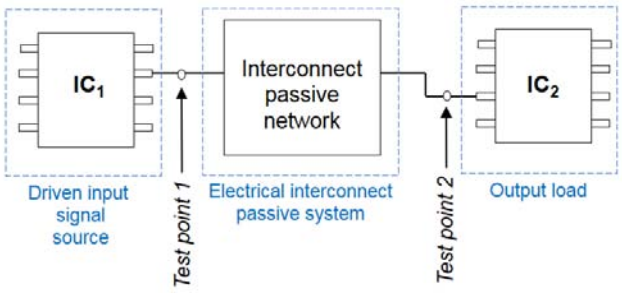

Figure 2: ICs based circuit under study.

However, the electrical interconnect network is considered as perfectly known with given physical and electrical parameters. To solve the problem, we can start with the time-dependent signals $v_1(t)$ and $v_2(t)$ from test points 1 and 2. Then, the circuit model of the structure will be described in the next section in order to establish the analytical expression of the voltage transfer function.

2.2. Electrical circuit description of the problem

The electrical equivalent circuit representation is needed for elaborating the proposed access impedance under investigation. To do this, let us consider the cascaded block diagrams shown in Fig. 3. It consists of three different blocks. The input signal source and output load blocks are combined via the interconnect passive network constituted by interconnect circuit.

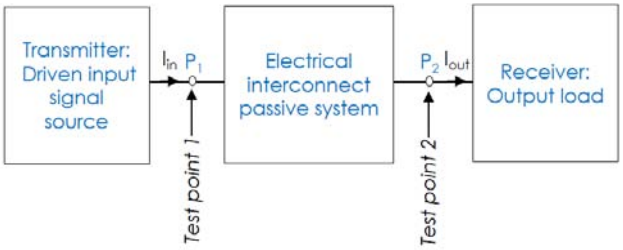

Fig. 3: Diagram of the Tx-Rx system.

The transmitter generates the voltage source signal Vin with output impedance Z_1. The receiver represents the output load denoted Z_2. The intermediate system is a two-port electrical network. The posed-problem for the system consists in determining Z_1 and Z_2 knowing the test point signals $V_1(P_1)$ and $V_2(P_2)$. The interconnect network is assumed as a known system based on the electrical and physical given parameters. To solve this problem, let us establish the analytical equation between the test point voltages and the proposed system access impedances.

2.3. Equivalent chain matrix of the circuit under study

Acting as a two-port electrical system, the intermediate interconnect network can be represented as a two-dimension chain matrix:

$$[T(s)] = \begin{bmatrix} T_{11}(s) & T_{12}(s) \\ T_{21}(s) & T_{22}(s) \end{bmatrix}, \quad (1)$$

with s is the Laplace variable. Therefore, the diagram introduced in Fig. 3 can be represented by the circuit shown in Fig. 4. According to the circuit and system theory, the access voltages and currents of a two-port system can be linked by the chain matrix with the following relation:

$$\begin{bmatrix} V_{P_1}(s) \\ I_{in}(s) \end{bmatrix} = [T(s)] \times \begin{bmatrix} V_{P_2}(s) \\ I_{out}(s) \end{bmatrix}. \quad (2)$$

The chain matrix enables to establish a relation between the access voltages and currents at any stage of the circuit.

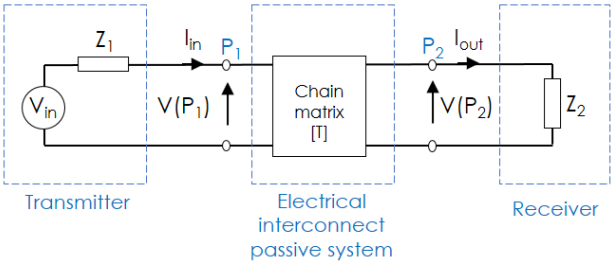

Figure 4: Electrical circuit equivalent to the diagram introduced in Fig. 3.

First, the voltage transfer function (VTF) between $V(P_2)$ and $V(P_1)$ can be obtained with the total chain matrix:

$$[T_t(s)]=\begin{bmatrix} T_{t_{11}}(s) & T_{t_{12}}(s) \\ T_{t_{21}}(s) & T_{t_{22}}(s) \end{bmatrix}=\begin{bmatrix} T_{11}(s) & T_{12}(s) \\ T_{21}(s) & T_{22}(s) \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \dfrac{1}{Z_2(s)} & 1 \end{bmatrix}$$

$$\Rightarrow [T_t(s)]=\begin{bmatrix} T_{11}(s)+\dfrac{T_{12}(s)}{Z_2(s)} & T_{12}(s) \\ T_{21}(s)+\dfrac{T_{22}(s)}{Z_2(s)} & T_{22}(s) \end{bmatrix} \quad (3)$$

According to the circuit theory [19-22], the voltage transfer function (VTF) is equal to the first element of the total transfer matrix:

$$VTF(s)=\frac{V_{P_2}(s)}{V_{P_1}(s)}=\frac{1}{T_{t_{11}}(s)} \quad (4)$$

By considering the transfer matrix expressed in (3), the expected VTF can be written as:

$$\frac{V_{P_2}(s)}{V_{P_1}(s)}=\frac{1}{T_{t_{11}}(s)}=\frac{Z_2(s)}{T_{12}(s)+Z_2(s)T_{11}(s)} \quad (5)$$

This circuit approach leads to the determination of the input and output impedances.

2.4. Formulations of the access impedance extraction

The proposed impedance extraction can be performed in two steps. First, we can extract the output impedance and then input one.

2.4.1. Output impedance extraction formulation

Knowing the voltages $V(P_2)$ and $V(P_1)$, the output load impedance can be determined by inverting equation (5). Therefore, the output load input impedance can be formulated as:

$$Z_2(s)=\frac{T_{12}(s)V_{P_2}(s)}{V_{P_1}(s)-T_{11}(s)V_{P_2}(s)} \quad (6)$$

It can be pointed out that:

- We have the short-circuit effect $Z_2(s)=0$ under the condition:

$$T_{12}(s)=0 \quad (7)$$

- We have a high impedance effect $Z_2(s)=\infty$ under the condition:

$$V_{P_1}(s)-T_{11}(s)V_{P_2}(s)=0 \quad (8)$$

2.4.2. Input impedance extraction

The equivalent diagram of the system seen from the input plane P_1 can be represented as shown in Fig. 4. The global equivalent impedance is defined by:

$$Z_{in}(s)=\frac{T_{11}(s)Z_2(s)+T_{12}(s)}{T_{21}(s)Z_2(s)+T_{22}(s)} \quad (9)$$

Generally, this input impedance behaves as a first-order network constituted by elementary components resistance R, inductance L and capacitance C for most electronic system technology.

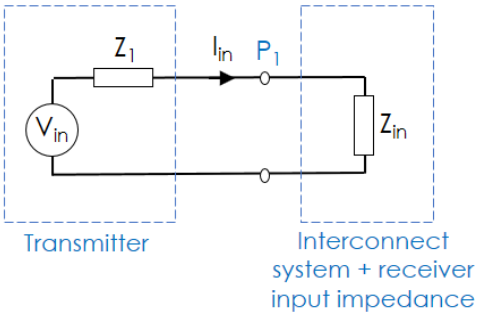

Figure 5: Reduced circuit equivalent to the system shown in Fig. 4.

2.5. Equivalent network topology

The topologies of the input and output impedances can be identified based on the linear passive circuit theory. There are different ways to estimate the RLC parameters. They can be estimated for example based on the analysis of the impedance real and imaginary parts. Then, the expected parameters can be represented by the average values. Another way can be also the extremal frequencies impedance behavioral analysis. With this analysis, one can follow the identification approach of RL-series, RC-series, RL-parallel and RC-parallel networks addressed in Table 1. This first order network configuration depends on the manufacturing technology of the electronic system under investigation.
Based on the system theory frequency analysis, we have to consider the angular frequency ω whose $s=j\omega$ is the Laplace variable.

Table 1: First order impedance and admittance configurations.

Configuration	Description	Equivalent impedance
Series	RL-series	$Z(s)=R+L\cdot s$ (10)
	RC-series	$Z(s)=R+1/(C\cdot s)$ (11)
Parallel	RL-parallel	$Z(s)=R\cdot L\cdot s/(R+L\cdot s)$ (12)
	RC-parallel	$Z(s)=R/(1+R\cdot C\cdot s)$ (13)
Configuration	**Description**	**Equivalent admittance**
Series	RL-series	$Y(s)=1/(R+L\cdot s)$ (14)
	RC-series	$Y(s)=C\cdot s/(1+R\cdot C\cdot s)$ (15)
Parallel	RL-parallel	$Y(s)=1/R+1/(L\cdot s)$ (16)
	RC-parallel	$Y(s)=1/R+C\cdot s$ (17)

Table 2: First order impedance extreme frequency behaviors.

Behavior	VLF	VHF
RL-series	$Z(\omega\approx 0)=R$ (18)	$\lvert Z(\omega\approx\infty)\rvert/\omega=L$ (19)
RC-series	$\omega\lvert Z(\omega\approx 0)\rvert=1/C$ (20)	$Z(\omega\approx\infty)=R$ (21)
RL-parallel	$\omega\lvert Y(\omega\approx 0)\rvert=1/L$ (22)	$Z(\omega\approx\infty)=R$ (23)
RC-parallel	$Z(\omega\approx 0)=R$ (24)	$\omega\lvert Y(\omega\approx\infty)\rvert=C$ (25)

The passive component identification can be performed based on the equivalent impedance behaviors at very low frequencies (VLF) and very high frequencies (VHF) which are defined analytically by $\omega\approx 0$ and $\omega\approx\infty$ respectively. Accordingly, we have the formulations indicated in Table 2.

3. Methodology of the interface equivalent circuit identification

Knowing that the proposed access impedance extraction is based on the input and output signal processing, it can be assumed that the input circuit should be constituted by a voltage source in combination to the output impedance of the driving circuit.

3.1. Transmitter voltage source identification

The input current can be calculated from the Ohm's law applied to this global impedance:

$$Z_{in}(s)=\frac{V_{P_1}(s)}{I_{in}(s)} \quad \Rightarrow \quad I_{in}(s)=\frac{V_{P_1}(s)}{Z_{in}(s)}. \tag{26}$$

Finally, the transmitter main voltage source can be determined from the first Kirchhoff's law:

$$V_{in}(s)=V_{P_1}(s)+Z_1(s)I_{in}(s)=\left[Z_1(s)+Z_{in}(s)\right]I_{in}(s). \tag{27}$$

3.2. Workflow about the proposed impedance extraction method

The proposed impedance extraction method can be summarized in the following steps:

- Step 1: Identification of the system constituting blocks: transmitter, receiver and interconnect passive network.
- Step 2: Modelling or measurement of the interconnect passive network and conversion into chain matrix $[T(s)]$.
- Step 3: Measurement of the test point voltages $v_{P_1}(t)$ and $v_{P_1}(t)$. Calculations of the FFT can be performed with the expressions:

$$V_{P_1}(j\omega)=FFT\left[v_{P_1}(t)\right], \tag{28}$$

and

$$V_{P_2}(j\omega)=FFT\left[v_{P_2}(t)\right]. \tag{29}$$

- Step 4: Calculation of the output load Z_2.
- Step 5: Identification of the input impedance Z_1.

- Step 6: Identification of the input voltage source $V_{in}(s)$. Calculation of the time-domain input signal can be performed with the following expression:

$$v_{in}(t) = IFFT\left[V_{in}(j\omega)\right]. \quad (30)$$

To check the relevance of the proposed impedance extraction method, numerical application with an example of LTI circuit is described in the next section.

4. Application example

The present section introduces an application example of the proposed access impedance extraction method. An example of an electronic circuit network with arbitrary parameters is considered. The application was simulated data with the transient input signal. The test point signals were exploited to estimate the access impedances.

4.1. Description of the structure POC

Fig. 6 describes the test circuit schematic defined with arbitrarily chosen parameters.

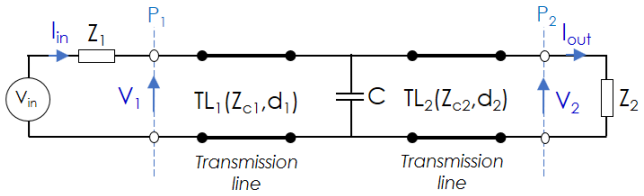

Figure 6: Considered application circuit.

Table 3 addresses the parameters of the proof-of-concept circuit. It consists of two pieces of different transmission lines TL_1 and TL_2. They present characteristic impedances Z_{c1} and Z_{c2}, and physical lengths d_1 and d_2 respectively. They are separated by a parallel capacitor C. The input load impedance Z_1 is constituted by an RL-series network (R_1, L_1) and the output impedance Z_2 is a parallel RC-parallel network (R_2, C_2).

Table 3: Parameters of the POC circuit.

Elements	Parameter	Value
TL_1	Z_{c1}	48 Ω
	d_1	50 mm
TL_2	Z_{c2}	53 Ω
	d_2	40 mm
Intermediate capacitor	C	22 pF
Considered input parameter	R_1	15 Ω
	L_1	8 nH
Considered output parameter	R_2	1 kΩ
	C_2	10 pF

As numerical testing, this circuit was simulated in a transient regime with the square wave pulse input signal with duration T=20 ns along the time window T_{max}=5T.

4.2. Operating signal analysis

The input data considered for the developed method is plotted in Fig. 7. It is represented by transient signals generated at the points P_1 and P_2. The frequency spectrums of the proposed circuit from DC to 1 GHz are displayed in Fig. 8. As introduced in the previous section, these spectrum data serve to the extraction of the access impedances of the system under study.

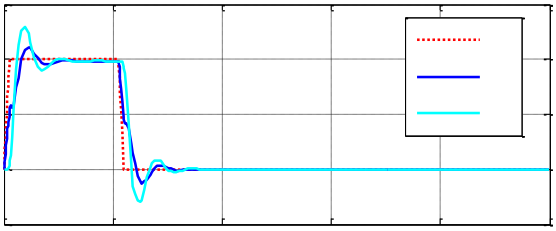

Figure 7: Transient plots of signals v_{P1} and v_{P2}.

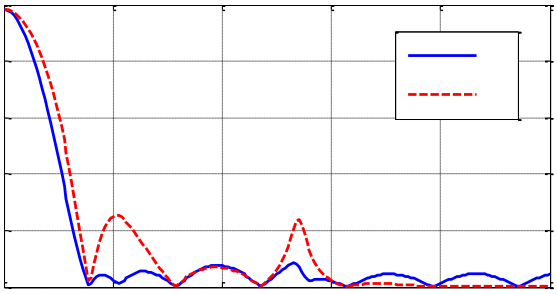

Figure 8: Spectrums of signals V_{P1} and V_{P2}.

4.3. Extracted impedances from the proposed method

After the application of the proposed impedance extraction method, we obtain the results described in the present paragraph. First, the interconnect network equivalent chain matrix elements are plotted in Fig. 9. It can be pointed out that the transmitted voltage and current respectively related to T_{11} and T_{22} from this chain matrix present transmission zero around 0.26 GHz. The transfer impedance related to T_{21} is lower than -20 dBΩ. The magnitude of the calculated output impedance Z_2 is plotted in the bottom of Fig. 10. It can be understood that it presents an RL-series network impedance behavior. The constituting resistance R_2 is extracted from the real part of Z_2. And the constituting inductance L_2 is defined from the imaginary part. The corresponding results are plotted in the bottom of Fig. 10.
Moreover, Figs. 11 displays the spectrum of the input impedance magnitude Z_{in} (in the top) and the overall circuit input current I_{in} (in the bottom). As seen in the top of Fig. 11, the input impedance Z_{in} behaves as a resistance at VLF below 50 MHz. It means that this input impedance can be roughly approximately equal to the input resistance $Z_{in} \approx 15.77\ \Omega \approx R_1$. The inductance parameters can be calculated by considering the frequency point where the input current presents significant value. For example, by taking the higher

frequency where the inductive effect dominates the resistive one. Following this approach, the estimated input inductance is L_1=7.45 nH.

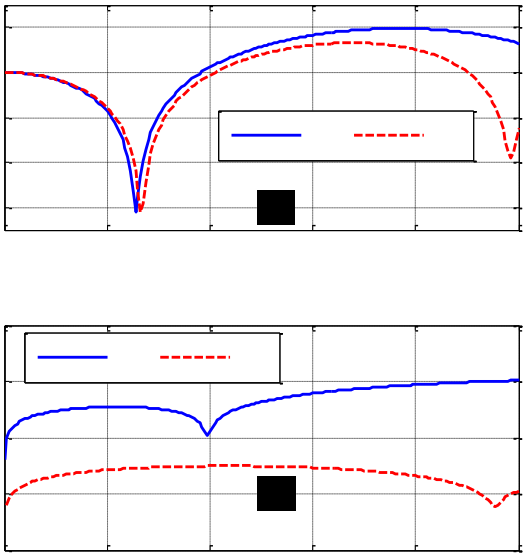

Figure 9: Transfer matrix elements: (a) T_{11} and T_{22}, and (b) T_{12} and T_{21}.

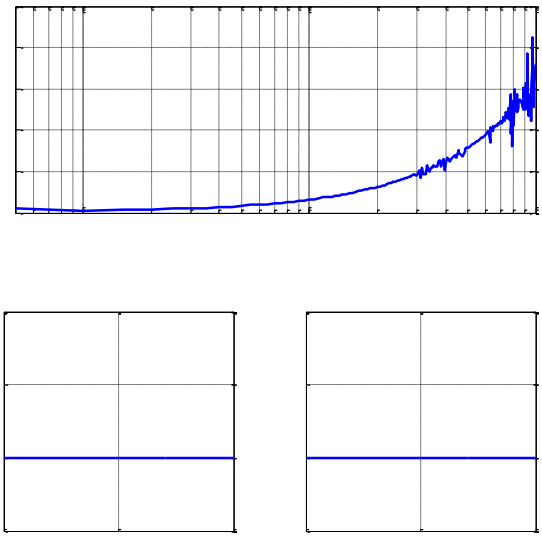

Figure 10: Spectrums of Y_2 in top, and the extracted resistance R_2 and capacitor C_2 in bottom.

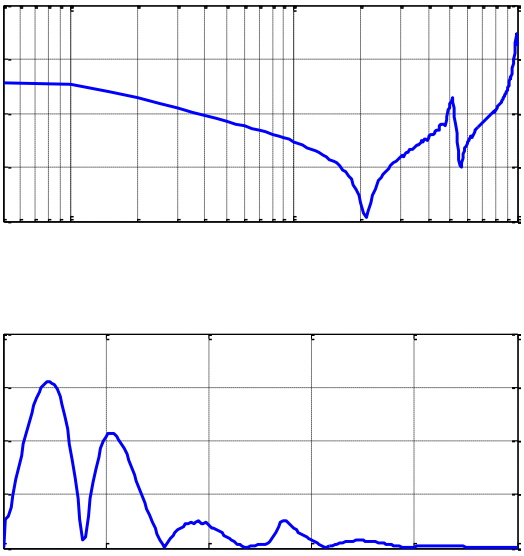

Figure 11: Spectrums of the input impedance Z_{in} and current I_{in}.

4.4. Advantages and limits of the proposed method

The proposed impedance extraction method presents the following advantages:

- The proposed modeling computation speed for 451 samples is of about tens milliseconds compared to more than ten minutes with HFSS® software by using a PC equipped a single-core processor Intel® CoreTM i3-3120M CPU @ 2.50 GHz and 8 GB physical RAM with 64-bits Windows 7.
- The ability to consider any type of passive equivalent access circuits,
- The possibility to be applied to complex PCBs,
- The possibility to be applied in both time- and frequency-domain,
- The fast computation time,
- The adaptability to different electrical and electronic systems,
- And the non-dependence of the signal measured at the test points to the other parts of the circuit.

Nevertheless, its drawbacks are:

- Limited to only linear input and output access circuits and cannot be applied to the nonlinear interface,
- Limited to the bandwidth of the test probes,
- And sensitive to the numerical inaccuracies especially when the choice of the RLC circuit identification is made around the resonance frequencies.

Table 4 addresses a comparative performance of different methods and techniques [25, 26, 27, 29, 32] available in the literature

Table 4: Comparison of advantages and drawbacks of method/technique performances available in the literature.

Description	Advantages	Drawbacks
Diagnosys PinPoint II R [25]	- Test and fault-find electronic circuits quickly and reliably - Passive and dynamic digital in-circuit functional test	- Test setup preparation - Bandwidth limitation
Controlled Impedance Test [26]	- Adaptability to complex PCBs - Absolute accuracy of the measurement	Factors influencing measurement repeatability: - Test fixtures - Operator - Test probes - Test cables - Test equipment - External influences
Board-Level Design for Testability [27]	- Board-level and schematic design considerations - Possibility of device selection and identification - Considerations for memory cluster testing - Considerations of power supply loading	- Experimental setup complexity - Measurement accuracies
In Circuit Test (ICT) [29]	- Possibility to gain access to the circuit nodes on a board - Possibility to measure the performance of the components regardless of the other components connected to them - Adaptability to complex PCB - Possibility to undertake a very comprehensive form of PCB test, ensuring that the circuit has been manufactured correctly and has a very high chance of performing to its specification	- Fixtures expensive: As the fixtures are mechanical and require general and wiring assembly for each printed circuit board, they can be a costly item. - Fixtures difficult to update: As the fixture is a fixed mechanical item, with the probes or "nails" mechanically fixed, any updates to the board changing the position of the contact points can be costly to change. - Test access becoming more difficult: With the size of boards becoming ever smaller, access to nodes becomes increasingly difficult. In an ideal system, special contact points should be provided, but because of the constraints caused by miniaturization, these contacts are rarely available. Some nodes may not even have accessible contact points. This makes ICT difficult and reduces the fault coverage obtainable. - Back-driving: One problem that concerned people, especially some years ago was that of back driving. When performing a test some nodes have to be held at a certain level. This meant forcing the output of possibly a digital integrated circuit to an alternative state purely by applying a voltage to over-ride the output level. This naturally put a strain on the output circuitry of the chip. It is generally assumed that this can be done for a very short period of time - sufficient to undertake the test - without any long-term damage to the chip. However,

		with the geometries in ICs shrinking, this is likely to become more problematical.
HFSS® ANSYS [32]	- Adapted to the influence of the 3D design parameters - Possibility to predict the high frequency effects	- Time for pre-processing design - Difficulties to consider the lumped component parameter variations - Difficulties to be adapted to low frequencies

5. Conclusion

An extraction method of in-situ ICs implemented on operating PCB is introduced. The proposed method is practically limited to the LTI system. The method is applied to an example of an electronic chain composed of transmitter, receiver and interconnects network blocks. The extraction method principle is described. During the calculation, the interconnect network must be preliminarily defined and can be modeled as a chain matrix. The analytical formulas enabling to calculate the impedances in function of the test signals are established.

To validate the proposed method an example of circuit with RL-series source impedance and RC-parallel load is considered. As expected, calculated impedances from transient test signals well correlated to the initial values are obtained.

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