MEMS based monolithic Phased array using 3-bit Switched-line Phase Shifter

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Abstract

This article details the design of an electronically scanning phased array antenna with proposed fabrication process steps. Structure is based upon RF micro-electromechanical system (MEMS) technology. Capacitive type shunt switches have been implemented here to cater high frequency operation. The architecture, which is deigned at 30 GHz, consists of 3-bit (11.25º, 22.5º & 45º) integrated Switched-line phase shifter and a linearly polarized microstrip patch antenna. Detailed design tricks of the K_a-band phase shifter is outlined here. The whole design is targeted for future monolithic integration. So, the substrate of choice is High Resistive Silicon (ρ > 8kΩ-cm, tan δ =0.01 and ϵ_r =11.8). The overall circuit occupies an cross-sectional area of 20 × 5 mm^2. The simulated results show that the phase shifter can provide nearly 11.25º/22.5º/45º phase shifts and their combinations at the expense of 1dB average insertion loss at 30 GHz for eight combinations. Practical fabrication process flow using surface micromachining is proposed here. Critical dimensions of the phased array structure is governed by the deign rules of the standard CMOS/MEMS foundry.

Index terms –MEMS, Phase shifter, Phased array, CPW-MS transition.

1. Introduction

Since the last decade, people have witnessed the tremendous potential of **M**icro **E**lectro **M**echanical **S**ystems (MEMS) technology in almost every aspect of engineering field. Starting from mechanical or environmental (physical) sensor to space usage, MEMS has spread its wings everywhere even in biological application, too. Day by day it is becoming popular because of its unique features. In RF/microwave domain also, MEMS is coming up with its promising characteristics. Bulky devices or circuit elements of now-a-days are on the verge of replacement with MEMS devices because of its tiny size, light weight, low insertion loss, negligible power loss and above all linear characteristics [1-3]. In addition to above features, worldwide this booming technology is growing exponentially in modern communication field as it offers an easy means to design reconfigurable devices for realizing multiband system.

One of the important building blocks of the air-borne RF module is 'Phased Array Antenna' for defense/ civilian application in satellite or RADAR system. Electronic scanning technology is evolved in modern era to eradicate bulky mechanical scanning components [4]. Traditional ferrite-based phase-shifter system is going to be replaced by its immediate challenger i.e MEMS based phase shifter.

'Phased array' is the backbone of electronic scanning array (ESA) system. It consists of multiple stationary radiating elements fed with signals with different phase-shifts at different instants [4][5]. Usually, till date, antenna elements, phase shifter component and feed network are designed and manufactured separately on different substrates and then integrated finally with hybrid connections. It not only increases the circuit size and packaging costs but also invites parasitic effects and extra losses associated at higher frequencies[6][7].

To alleviate these issues, there is a need to realize all system components on the same platform of a single substrate, forming a monolithic version of phased array, which is possible with the enabling MEMS technology.

This paper presents the detailed design of a monolithic electronically scanning array using RF-MEMS technology. The centre frequency of the design is 30 GHz. Operational bandwidth is 2 GHz around this centre frequency. It employs 3-bit Switched-line MEMS based phase shifter, which is easy to fabricate and package as compared to its other counterparts. This phase-shifter are used to obtain eight combinations of progressive phase-shifts in the excitations of radiating patch antenna to steer the beam. Capacitive type shunt switches are employed in phase shifter as switching elements. Standard 675 ± 15 µm thick High resistive silicon wafer is used as a monolithic substrate.

Section II demonstrates the configuration of the electronic scanning array, while Section III presents design of phase-shifter and antenna; Section IV provides proposed fabrication steps, which is followed by conclusion in Section V.

2. Phased Array architecture

The proposed architecture consists of 3-bit integrated digital phase shifter and a radiating element. The same structure

can be repeated N-times to realize N-element phased array antenna along with its corporate feeding network. The operating frequency is selected as 30 ± 1 GHz. Whole design is based on 675 ± 15 μm thick high resistive silicon (ρ > 8kΩ-cm, tan δ =0.01 and ϵ_r=11.8).substrate. Total size of the system is approximated by 20 × 5 mm^2. The layout of the system is shown in Fig.1. The phase shifter structure is implemented using CB-CPW (Conductor backed Co-planar waveguide) whereas the antenna is designed by microstrip(MS) line. So, optimized CPW-MS transitions are desired at the input and output ports of the phase shifter. Tapered live (or signal) line is the key feature of this transition structure for mode matching in a smoother way. Dynamic range in terms of operation bandwidth is decided significantly with this tapering structure. Here, inset-fed microstrip patch is chosen as a radiating element. With the proper actuation of the RF–MEMS switches, the signal is routed either through reference or delay arm of the phase-shifter bits. Thus, 3-bit phase shifter is designed to provide progressive phase-shifts at 11.25º/22.5º/45º and their combinations at 30 GHz. Total eight combinations (000 to 111) are possible for scanning the antenna beam. Table-I shows the truth of the scanning angle obtained with alteration of states of integrated phase-shifter.

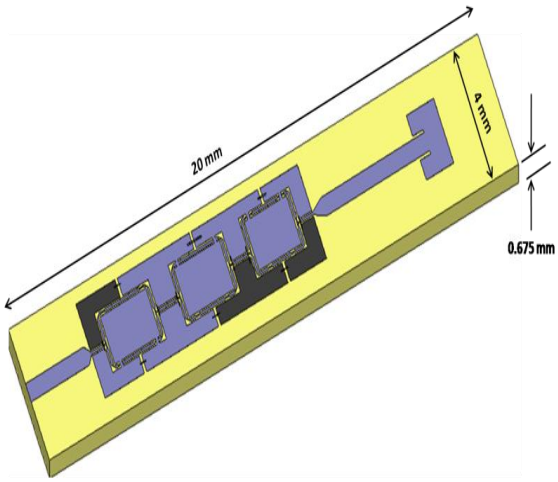


Figure 1: Geometry of the Phased-array system

Table I: Truth table for 3-bit integrated phase shifter

State			Scanning Angle
0	0	0	Reference
0	0	1	45º
0	1	0	22.5º
0	1	1	67.5º
1	0	0	11.25º
1	0	1	56.25º

3. Design and Analysis

The phased-array system comprises of phase shifter and patch antenna. Detailed design of individual circuit elements are described here below.

3.1 Phase Shifter

Till date most of the phase-shifters used in commercial or strategic applications are based on either Ferrite or semiconductor devices such as FET or p-i-n diode switches. Bulky ferrite based designs are preferred where low insertion loss (~ 1dB) and slow switching speed (~150 μs) are desired [8][9]. Whereas, semiconductor switches come up with very low DC power consumption, but it show significant RF losses (4-6 dB @12-18 GHz) [10]. In context with the above discussions, MEMS technology offers very low insertion loss, negligible power consumption, light weight and almost linear characteristics [1]. So, current trend in research is going on to develop various components of RF T/R module with radio frequency MEMS enabling technology. There can be n improvement of 6-8 dB in the insertion loss of RADAR system by utilizing MEMS technology. For this, even one of the amplifier stages can be removed, reducing both DC power consumption and production cost of the system [7].

The present work details about the application of RF-MEMS technology to construct a capacitive type shunt switch structure, followed by phase shifter architecture. Switched-line topology has been chosen here for its ease of design and reduced fabrication complexity [11]. It has two arms viz., reference and delay arm. Input RF signal is routed either of the arm by changing the state of the shunt switches placed at quarter-wavelength apart from the T-junction as shown in Fig.2. CB-CPW configuration is implemented here to realize the system. The electrical length of the reference arm is set as 270º to avoid unwanted resonance in the OFF state of the switches. The required phase shift of the individual bit is governed by Eqn.(1), where $l_2=(l_1+\Delta L)$, β is phase constant(rad/m).

$$\Delta\phi = \phi_2 - \phi_1 = \beta (l_2 - l_1) \qquad (1)$$

To design an N bit switched line phase shifter, each bit is designed separately and cascaded in succession. Switched line phase shifter is also known as true time delay as t=dφ/dw, φ is proportional to w, and t is a constant over bandwidth.

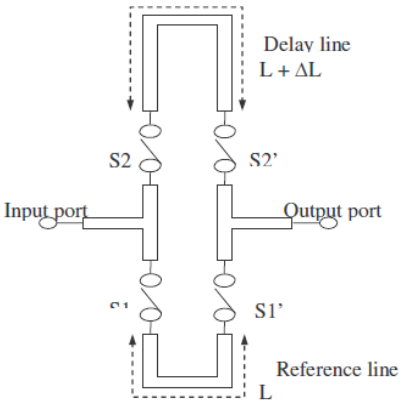


Figure 2: Geometry of the switched-line phase shifter

Typical parameters chosen for individual bit of the phase shifter is summarized in Table-II.

Table-II: Typical design dimensions for phase shifter

Symbol	Parameter	Selected Value
f_c	Centre Frequency	30 GHz
Z_o	Characteristic Impedance	50 Ω
ε_r	Dielectric constant	11.8 for Silicon
h	Substrate thickness	270 µm
Selected Dimensions		
W	Width of the centre conductor CPW line	80 µm
G	Gap between centre conductor & ground plane of CPW	46 µm
t	Thickness of the membrane	1 µm
w	Width of the membrane	100 µm
l	Length of the membrane	272 µm
g_0	Initial gap between the switch and CPW	2.5 µm

Design philosophy adopted in phase shifter is explained in the following subsections.

3.1.1 Bit Design

The bit design starts with building the layout as shown in Fig.3 using the values shown in Table-II. The main design constraints in the bit design of the phase-shifter are position and the number of switches, height of the membrane, Tx-line impedance(CPW dimensions), discontinuity in Tee-junctions or bends and bias line induced parasitic. To tackle all these criticalities of designing, numerous parameters are optimized viz., reference/delay line lengths, tapering in the t-line, T-junction widths/lengths, ground plane widths in FG-CPW(Finite Ground CPW) configurations, notch in ground plane, air-bridge size & numbers and slot in the ground plane.

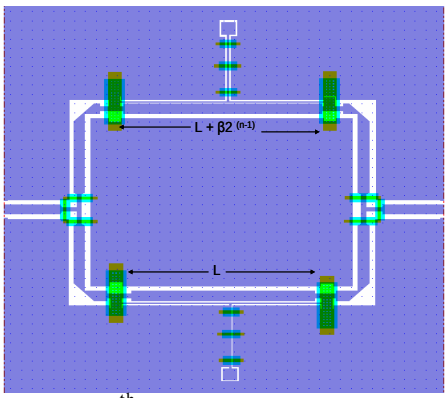


Figure 3: n^{th} bit layout of the phase shifter

3.1.2 Air-bridge Optimization

To facilitate the DC biasing of the RF switch, splitting in CPW ground –plane is often employed. But, this splitting introduces extra discontinuity in the structure and also causes coupled slot wave propagation. Two ground planes may not see same potential at the same time, which may support odd-mode propagation, unpredictable at higher frequencies. To eliminate these problems, air-bridges are incorporated between two grounds. Increasing the number of bridges not only enhances the fabrication complexity (especially stiction), but also affects the RF performance (insertion phase) significantly. Table-III shows the optimization results for number of air-bridges. It clearly depicts that, in a splitted ground CPW structure three numbers of air-bridges are sufficient to compensate all parasitic effects. Further this number can be reduced by providing a thin slit for continuation in RF ground, as shown in Fig.4. Here, all the analysis has been carried out with 150 µm long & 20 µm wide air bridges. Simulation shows that a change in RF ground width of 20 µm can affect a change in insertion phase of ~ 1°.

Table III: Comparative study of the effect of number of the air-bridges on RF performance

Type of Structure		S_{11}(dB)	S_{21}(dB)	Phase(S_{21})
Basic CPW structure		-26.48	-0.169	-92.28
Splitted ground	Single air-bridge	-17.40	-0.273	-96.63
	Two air bridges	-21.29	-0.206	-93.72
	Three air bridges	-25.01	-0.183	-92.28

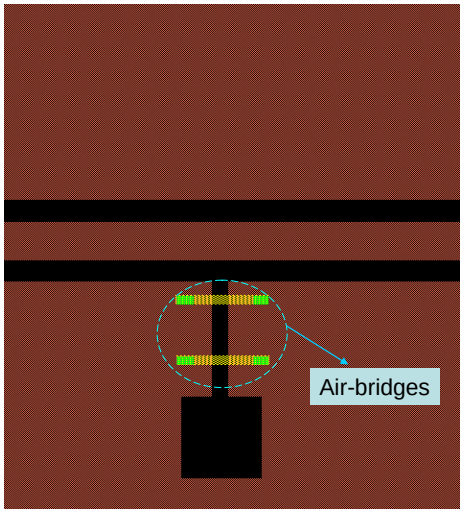
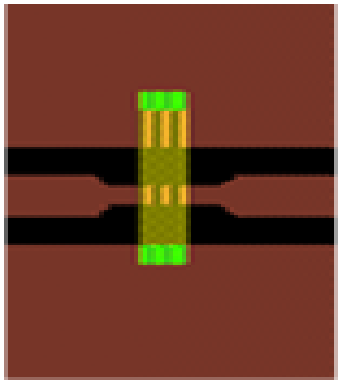


Figure 4: Reduction technique of no. of air bridges.

3.1.3 *T-matching*

Switch insertion introduces extra capacitance and degrades the RF performance of the CPW line. Due to the low height of the membrane layer, a significant additional capacitance is present between the inner conductor of the CPW and the short-circuited anchored strip. This modifies the characteristic impedance of the line and the effective dielectric constant in the bridged region. By tapering the t-line beneath the membrane, the degradation in return loss is minimized leaving marginal phase deviation, which can be taken care in the T-matching. Basically, two short high-impedance sections of t-lines before and after the bridge are introduced, which behave as series inductors and provide an excellent match at the desired frequency [2]. Fig.5 shows the layout of the T-match circuit along with its equivalent diagram.



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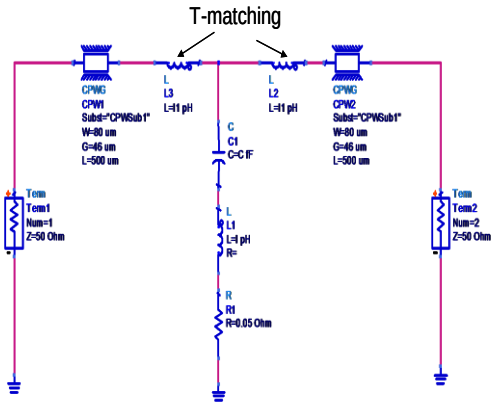


(b)

Figure 5: Layout for the T-match circuit (a) and equivalent circuit (b).

Table-IV shows the parametric study of the inductive matching by varying the length and the width of the tapering in the live line of the CPW. Fig.6 shows a comparative study between a switch inserted simple CPW structure and a structure with inductive matching. The T-matching enhances the return loss performance by around 20 dB in Ka-band, leaving the insertion loss behaviour more or less same.

Table-IV: Parametric study of the T-match circuit

Tapering Length(μm)	Tapering width (μm)	L(pH)
100	34	39
120		36.91
150		41.85
200		49.93
Tapering Width(μm)	Tapering Length (μm)	L(pH)
30	120	14.37
32		13.05
34		36.91
38		32.32

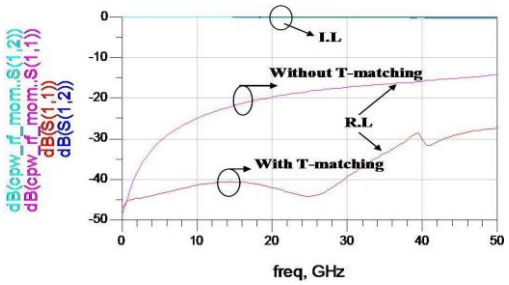


Figure 6: Improvement of RF performance by T-match circuit

3.1.4 *Notch Incorporation*

The design of bits with higher weightage (90° & 180°) is quite difficult, as the line lengths give resonance & change the RF-performance. Therefore, notches are introduced (to increase inductance) at the membrane ends to compensate the parasitic. Fig.7 shows a notch introduced RF switch structure. A detailed simulation is carried out in K_a-band by varying the width and length of the notch structure, shown in Fig.8. It depicts that, changing the length of notch much affect in RF performance rather than its width change.

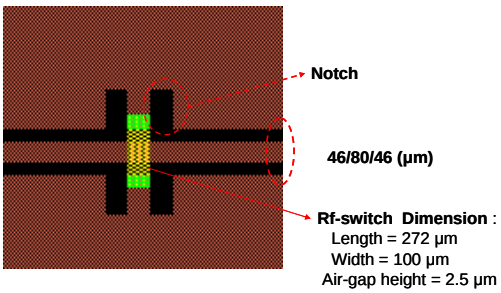
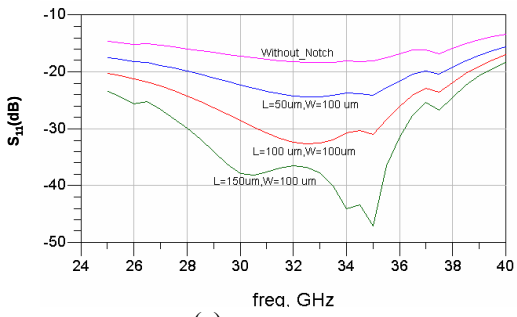


Figure 7: Notch introduced capacitive type shunt RF-switch structure



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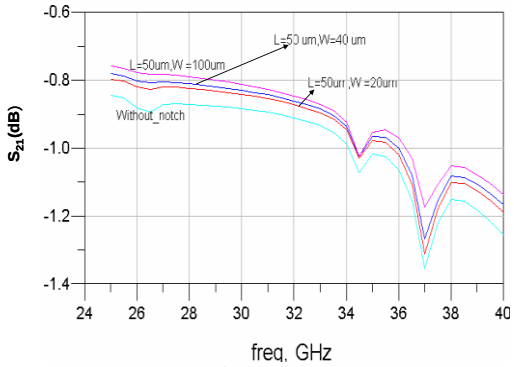


(b)

Figure 8: (a) Return loss performance with fixed width/variable length notches (b) Insertion loss variation with fixed width/variable length notches

Ground notching can also be incorporated beneath the membrane to facilitate the DC biasing arrangement of switches, as shown in Fig.9. Here, notches not only improve the loss parameters as per the above discussion, but also allow to employ bigger size actuation pad beneath the shunt switch, which results in reduction of pull-down voltage.

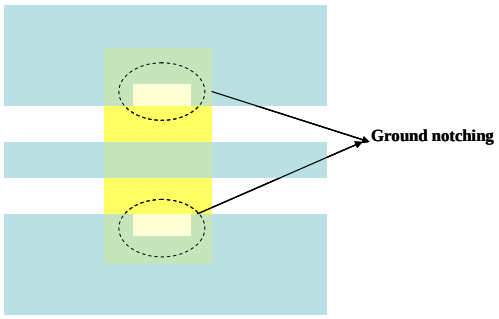


Figure 9: Layout of RF-switch with notched CPWground

3.1.5 CLR model

The modeling of phase-shifter starts with the equivalent circuit of RF switch. The MEMS switches, embedded in the switched-line phase shifters, are doubly anchored capacitive shunt devices. When the membrane is in the UP position (OFF state of the switch), the parallel plate capacitance between the metal membrane and the bottom electrode, C_{off}, is small and the switch behaves as an open circuit. Hence, the signal transmission through the switch takes place with low insertion loss. Alternatively, when the membrane is in the down position (ON state of the switch), the capacitance between the metal membrane and the bottom electrode, C_{on}, is large and the switch behaves as a short circuit. For the phase shifter, one can either close of the switches to get the desired phase delay.

The switch is modelled by two short sections of t-line and a lumped CLR model of the bridge with a variable capacitor (C_{off} / C_{on}) [2]. The model parameters of the shunt switch using the physical dimensions, given in Table-V are shown in Table-VI. Using the CLR model of the RF switch, a single bit phase-shifter can be modelled. The switches are placed λ_g /4 apart from the input/output T-junction to cancel the parasitic.

Table-V: Physical parameters of the designed switch

Parameters	Values
Length L (μm)	272
Width w(μm)	100
Height g(μm)	2.5
Membrane	Gold(0.5 μm)

Table-VI: Model parameters of switch

Parameters	Values
Up-state capacitance C_{off}	28.506 fF
Down-state capacitance, C_{on}	3.318 pF
Inductance	7.622 pH
Resistance	0.05 Ω
FOM(C_{on} / C_{off})	116.4

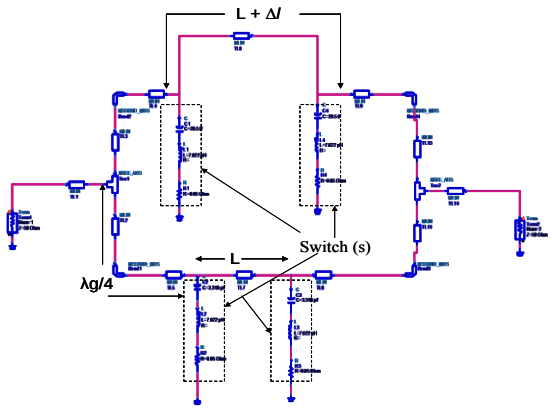


Figure 10: Equivalent ckt. of the single bit phase shifter

3.1.6 EM simulation of the individual bit

Electromagnetic simulation of the individual phase-shifter bits is summarized below in Table-VII. It depicts that the proposed structure offers maximum insertion loss of 0.3 dB and minimum return loss of 14 dB at 30 GHz. The

individual bits are integrated properly to have a 3-bit digital RF phase shifter. Matching becomes the prime concern in this kind of cascading process, as two or more live lines are running parallel at close vicinity to each other at a very high frequency. Mutual coupling becomes a major issue in this context. T-junction matching plays an important role to determine the overall impedance profile of the structure. Further, the bifurcation of the DC as well as RF ground plane introduces some extra discontinuity and hence parasitic. Proper placement of the air-bridge structures can mitigate this to some greater extent. The layout of the integrated structure is shown in Fig.11 below.

Table-VII: Summarized performance of the individual phase shifter bits

Bit	Reference Arm		Delay Arm	
	Return loss (dB)	Insertion loss (dB)	Return loss (dB)	Insertion loss (dB)
11.25°	-13.73	-0.295	-20.85	-0.290
22.5°	-14.26	-0.189	-15.74	-0.179
45°	-23.25	-0.035	-25.69	-0.04

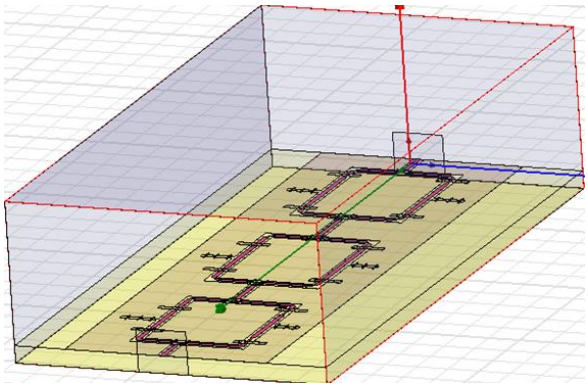


Figure 11: Schematic of the 3-bit integrated phase-shifter structure built in HFSS.

In practice, this kind of MEMS based structure can't be utilized in a working system without a sealed environment or packaging enclosure. Designing such enclosure needs expertise in that field with the knowledge of parasitic inductance, capacitance ,all these parameters. Separate exercise should be done to have a proper packaged device at Ka-band. Initial work on that have been accomplished by introducing a metallic shield placed at quarter-wavelength (at centre frequency) apart from the DUT(Device Under Test) block. Eigen-mode simulations are carried out to predict the signature of package resonances with the introduction of various structural elements, like-DC feed thrus, Input/output cable ports, etc. Table-VIII depicts the results of the integration after placing the structure in a metallic enclosure.

Table-VIII: Effect of metallic enclosure on the phase-shifter structure

Freq. band (GHz)	f_0 (GHz)	Without metallic shielding		With metallic shielding	
		R.L(dB)	I.L(dB)	R.L(dB)	I.L(dB)
28-32	30	-13.02	-0.8	-12.2	-0.9

3.2 Patch Antenna

The electronic eye of the proposed phased-array system is its main radiator i.e patch antenna. In practical system, to meet the customer specifications for high gain always it is recommended to use array of such antenna structures. Depending upon the design criteria corporate feed or series feeding arrangement is chosen tactfully. At higher frequencies, this feeding arrangement itself acts as a spurious radiator. In the present case, to avoid this kind of intricacy only single patch radiator is used. Our main motive is to show the phase scanning methodology with the implementation of MEMS based 3-bit integrated Phase shifter.

Patch antenna is designed using the classical equations [12]. Silicon is of prime choice for design considering the monolithic integration point of view. Inset-fed patch antenna is considered for the proposed work. Aluminium is used as metallization layer. The detailed dimension (in 'mm') of the antenna is shown in Fig.12 and the simulated performance is depicted in Fig.13. Table-IX summarizes the computed antenna performance at a glance.

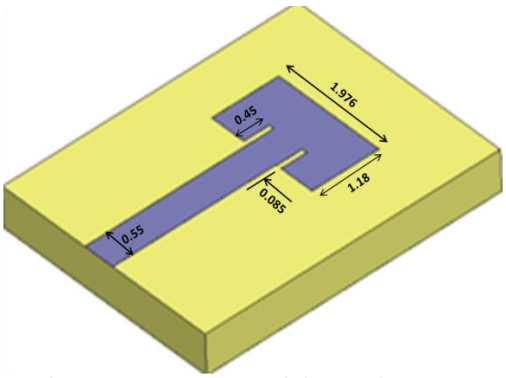
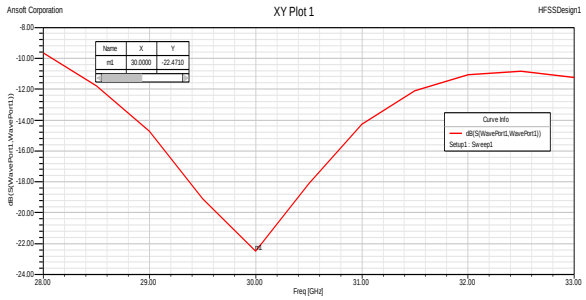


Figure 12: Geometry of the patch antenna

Table-IX: Computed Antenna Parameters

Parameters	Values
Return Loss @ 30 GHz	22.47 dB
Peak Gain	1.27 dBi
Peak Directivity	1.5 dBi
Radiation Efficiency	100 %
FBR(Front-to-Back ratio)	10.62 dB



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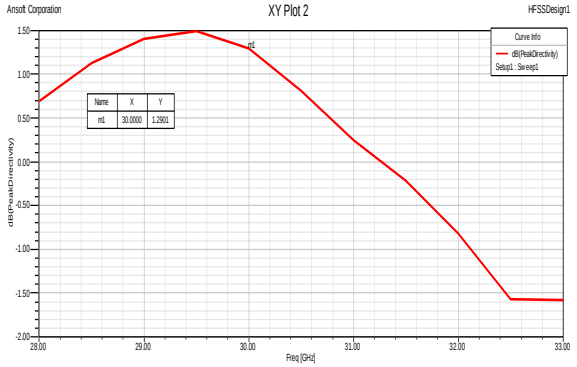

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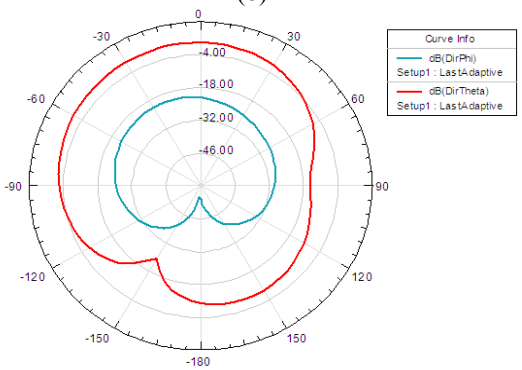


(c)

Figure 13 : Simulated (a) return loss (b) Peak directivity and (c) far-field radiation pattern of the patch antenna

3.3 Phased-array system

The final integration of the system is accomplished with extra care taken at the junction of the two differently matched passive networks viz. Phase-shifter and patch antenna. Phase-shifter is the heart of this system and antenna acts as an electronic eye for this. The whole scanning resolution depends on the phase-shifter operation.

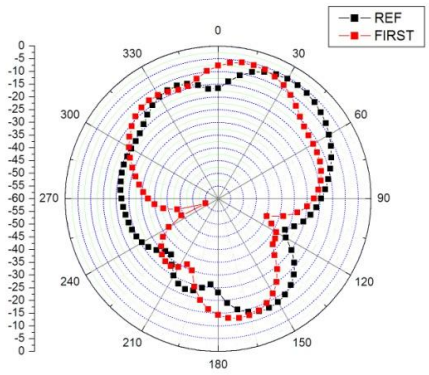
Phase-shifter is designed on conductor-back co-planar waveguide (CB-CPW) whereas the patch radiator is implemented by microstrip (MS) transmission line. At the juncture of these two different kinds of planar transmission lines, suitable transition structures are made to match the impedance profile of these two lines. This MS-CPW transition should radiate minimally at Ka-band. Tapering structure is used for smooth transition of these Tx-lines. After that, the placement of the patch radiator is also important to get rid of its SLL(Side-Lobe -Level). Optimization is carried out in this regard to achieve the maximum radiation efficiency of the system.

Finally to demonstrate the scanning array mechanism, 3-bit integrated phase-shifter structure is implemented, as shown in Fig.11. The concerned phase-shifter is of digital type (ON/OFF) there will be total eight (000 to 111) numbers of states as explained in Table-I. Here, state '0' refers to the signal passing through the reference arm and the state '1' signifies the propagation of the signal via delay arm. In this way, total eight numbers of phase scanning combinations can be obtained with this structure.

The overall antenna performance is shown in summarized in Table-X. The scanning process(rotation of antenna beam pattern) is clearly noticed in the far-field radiation pattern of the antenna system, as shown in Fig.14.

Table-X: Overall performance of the phased-array antenna

Parameters	Values
Return Loss @ 30 GHz	18.5 dB
Peak Gain	1.27 dBi
Peak Directivity	2.23 dBi
Radiation Efficiency	81 %
FBR(Front-to-Back ratio)	27 dB



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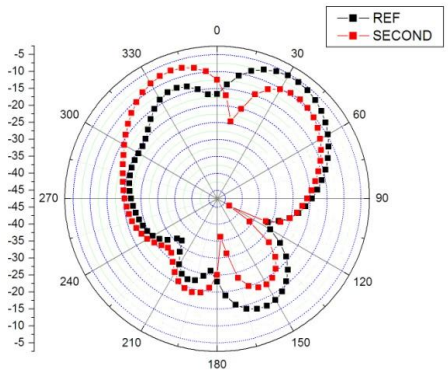

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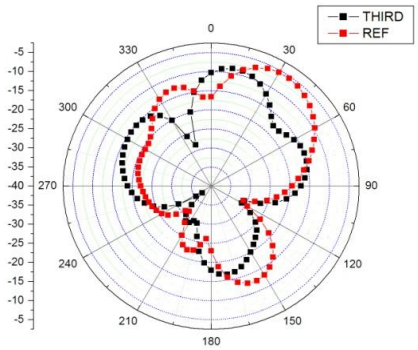

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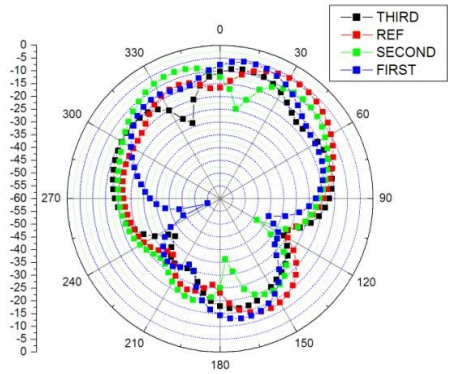


(d)

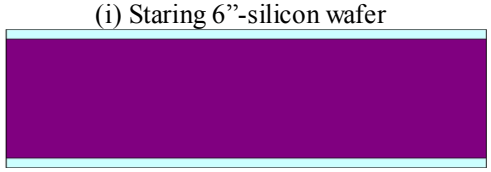
Figure 14: Scanning of the antenna beam with respect to (a) 1st bit (b) 2nd bit (c) 3rd bit (d) composite effect

4. Fabrication of the Phased Array

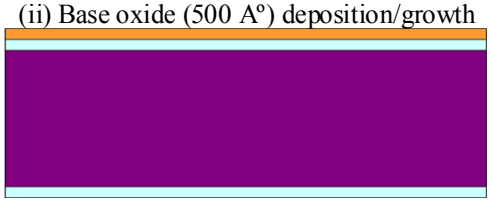
This section illustrates the proposed process flow for the fabrication of final phased array antenna. All the process steps are set according to the standard CMOS/MEMS foundry specifications. Pictorially it has been shown in Fig.15.

The fabrication process of the phased-array starts with the double-side polished (DSP) p-type <100> oriented 6"-diameter 675 µm thick-high resistivity (ρ >8kΩ-cm) silicon wafer. Actual process is initiated after a thorough chemical cleaning of wafers to remove all organic as well inorganic contaminations. Base oxidation of 500 Aº is grown on the furnace at the both side of the wafer as a buffer layer is followed by PECVD nitride deposition (1500 Aº). This oxide/nitride (O/N) stack is basically used to nullify the stress profile associated with the base wafer subsequently after several process steps applied in situ for realizing the actual device. Aluminium (10,000 Aº) with 4% Cu and 0.5% Silicon is sputtered at the front-side of the wafer to make the signal and ground lines of the CPW line and microstrip live line. After that, 1200-1500 Aº thin PECVD nitride is deposited followed by nitride lithography/masking and etching to make a dielectric pad above the actuation plates of the RF-MEMS switch structures. Metal is etched thereafter using RF plasma to form the phase shifter structure and patch antenna. A thick(2.5-3 µm) silane based PECVD type doped oxide(BPSG) is deposited at the front-side followed by two stage planarization methods using back etch process. This oxide layer acts as a sacrificial layer for surface micromachining process adopted for RF-switch realization. A tapered MESA type profile is made for smooth step-size at the both anchor portions of the switch and air-bride structures followed by lift-off lithography and E-beam evaporation of Cr/Au (300Aº/10,100Aº) layer at the both sides of the wafer. Bottom metallization layer acts as a common ground for patch antenna and CB-CPW based phased-shifter architecture, whereas front side chrome-gold layer is used as a free-hanging membrane structures for switches and air bridges. Finally, the whole wafer is cut into small pieces and these pieces are processed in HF-based solutions for surface micromachining of MEMS structures. Immediately after this wet process the free-hanging micro-machined phased array structures are dipped into IPA and then dried in critical point dryer(CPD) machine with liquid CO_2 at 31º C to remove all in-situ inbuilt stresses and stiction problem associated with this wet-based chemistry.

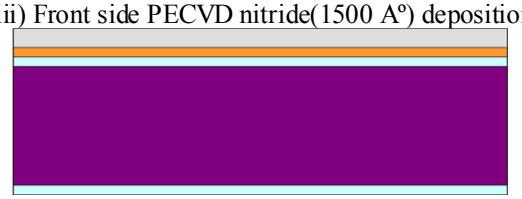
(i) Staring 6"-silicon wafer



(ii) Base oxide (500 Aº) deposition/growth

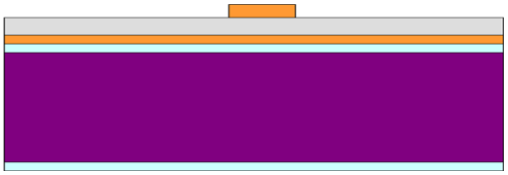


(iii) Front side PECVD nitride(1500 Aº) deposition

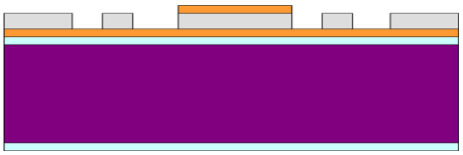


(iv) Aluminium sputtering (1 µm)

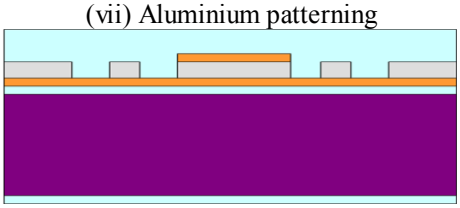
(v) PECVD nitride deposition(1500 Aº)



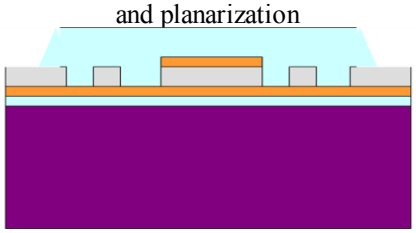
(vi) Nitride patterning



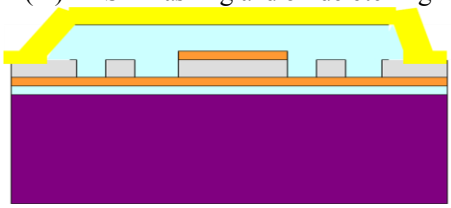
(vii) Aluminium patterning



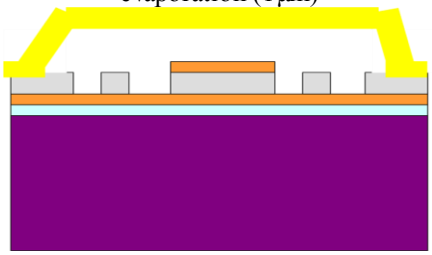
(viii) 2.5 μm-thick sacrificial oxide (BPSG) deposition and planarization



(ix)MESA masking and oxide etching



(x)Lift-off lithography followed by Cr/Gold E-beam evaporation (1 μm)



(xi) Lift-off process followed by sacrificial oxide etching

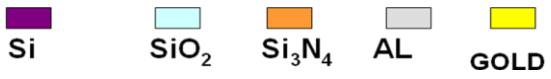


Figure 15: Proposed process flow for phased array fabrication

5. Conclusion

In this article, design of monolithic MEMS based Phased-array system is elaborated. Individual building block design is explained along with its governing mathematical equations. FEM based 3D EM-solver HFSS suite is used to analyze the final design. Before that, MoM based 2.5D simulator ADS Momentum is used to create various layout of the circuits. Electrical equivalent model is also proposed with this work. This will help to understand the basic principle of operations of this complicated system. Three-bit integrated switched-line phased-shifter is used here as a backbone of the whole system. It basically determines the eight numbers of states of operation for the scanning beam. The beam pattern of the scanning system will be oriented accordingly. The resolution of the scanning is inversely proportional to the number of bits in the phase-shifter structure. But, the complexity of the system increases exponentially with the number of bits. So, there is trade-off between these two. Due to non-availability of the fabrication lab inside our N.I.T-Durgapur, the circuit can't be realized practically. But, this system can be fabricated from any standard CMOS/MEMS foundry as all the critical dimensions of the design is kept as per the standard design rules in the industry/R&D lab.

References

[1] G. M. Rebeiz, *RF MEMS Theory, Design, and Technology*, Hoboken,NJ: Wiley, 2003.

[2] B. R. Norvell, R. J. Hancock, J. K. Smith, M. I. Pugh, S. W. Theis, and J. Kviakofsky, Micro electro mechanical switch (MEMS) technology applied to electronically scanned arrays for space based radar, *Proc.Aerosp. Conf.*, pp. 239–2471999.

[3] K.Topalli, O.A. Civi, S.Demir, S.Koc and T.Akin, A monolithic phased array using 3-bit distributed RF MEMS phase shifters, *IEEE Transactions on MTT* 56(2): 270-277,2008.

[4] R. J. Mailloux, *Phased Array Antenna Handbook*. Norwood, MA: Artech House, 1994.

[5] D. Parker and D. C. Zimmermann, Phased arrays—Part II: Implementations,applications, and future trends, *IEEE Trans. MTT*-50(3),pp. 688–698, 2002.

[6] K. Van Caekenberghe, T. Vaha-Heikkila, G. Rebeiz, and K. Sarabandi, Ka-band MEMS TTD passive electronically scanned array (ESA), *IEEE Antennas Propag. Symp. Dig.*, pp. 513–516, 2006.

[7] K. Topalli, M. Unlu, O. A. Civi, S. Demir, S. Koc, and T. Akin, A monolithic phased array using 3-bit DMTL RF MEMS phase shifters, *IEEE Antennas Propag. Symp. Dig.*, pp. 517–520, 2006.

[8] W. E. Hord, C. R. Boyd, Jr., and D. Diaz, A new type of fast switching dual-mode ferrite phase shifter, *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. II, pp. 985–988, 1987.

[9] C. R. Boyd, An accurate analog ferrite phase shifter, *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 104–105, 1971.

[10] V. Sokolov, J. J. Geddes, A. Contolatis, P. E. Bauhahn, and C. Chao, A Ka-band GaAs monolithic phase shifter, *IEEE Trans. Microw. Theory Tech.*, 31(12), pp. 1077–1083,1983.

[11] S.Koul and B.Bhat, *Microwave and Millimeter Wave Phase Shifters: Semiconductor and Delay Line Phase Shifters*, Artech House Publishers,1992.

[12] C.A.Balanis, *Antenna Theory: Analysis and Design*, New York: Harper and Row, 1997.