Integrated Millimeter-Wave Antennas for On-Chip Communication

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Abstract

This paper introduces the design and analysis of circularly polarized (CP) and dual-polarized on-chip microstrip antennas for wireless communication at 60 GHz. The CP on-chip antenna consists of a circular aluminum patch with two overlapped circular slots fed by the transmission line. The radiation characteristics of the CP have been analyzed using the finite integration technique and finite element method based electromagnetic solvers. The CP antenna introduces left-hand circular polarization and employs as on-chip transmitter. A design of dual-polarized on-chip microstrip antenna at 60 GHz is investigated and is employed as on-chip receiver. The dual ports of the dual polarized antenna are designed with high isolation between them in order to be used as a two on-chip receivers. The radiation characteristics of the dual-port antenna have been calculated. The effect of the separation distance between the CP-antenna and the dual-polarized antenna on the same chip has been investigated. The performance parameters like the reflection coefficient, transmission coefficient, and the transmission gain of the two antennas at different separation distances have been introduced.

1. Introduction

Recently, there is a special interest in the short range communication applications in the 60-GHz band [1]. A variety of applications such as uncompressed high definition video streaming, mobile distributed computing, wireless gaming, internet access, and wireless personal area networks falls into the 60 GHz band communications interest [2]. This frequency band is characterized by high attenuation of atmospheric oxygen of 10–15 dB/km in a bandwidth of about 7 GHz centered at 60 GHz [3]. A multi-Gbps wireless connectivity can be realized for short distances between electronic devices for this communication [4]. The data rate increases to 40–100 times faster than current technologies. Integration of the antenna-on-chip with different communication circuits introduces low fabrication cost due to the elimination of cost associated with materials required for off-chip (external) antennas [5]. Moreover, the antenna matching circuits will be eliminated as the 50 Ohm boundary is no longer needed.

The antenna integration, on-chip allows one step fabrication for the solid wireless system.

Complementary metal–oxide semiconductor (CMOS) is an effective technology because its high-frequency performance has been improved through scaling [6]. A typical 0.18 μm CMOS-technology consists of 6-8 metal layers embedded in silicon oxide layers is introduced in [7]. The top metal layer is utilized to fabricate the on-chip antennas, while the bottom metal layer is applied as a ground shield for reducing the losses [6]. However, the CMOS substrate is characterized by low resistivity and high permittivity; hence, antenna on-chip performance is poor in terms of gain, radiation efficiency and front-to-back ratio (FBR). Different antennas have been integrated in CMOS systems such as dipoles, dielectric resonator antennas, and microstrip antennas in the literature [8-10]. The antenna radiation characteristics are improved by using on-chip ground where the bottom metal layer is used as a ground shield for reducing the losses from low resistivity silicon substrate. An on-chip antenna has also been employed as a transformer in radio frequency identification systems (RFIDs) [11]. A single chip transceiver with on-chip antennas can provide a wireless communication link for sensor network. On-chip antennas can be employed for wireless data communication between different chips to minimize the pin counts, reducing the form factor, packaging costs, and signal delays [12]. Two-dipole pairs have been investigated for chip to chip communication in [13]. Circularly polarized (CP) antennas are desirable in wireless communication to minimize the path loss between the transmitter and receiver antennas and freedom of their orientation. A 60 GHz artificial magnetic conductor based CP on-chip antenna has been designed and fabricated using standard 0.18 μm six metal-layer CMOS technology in [14].

In this paper, the connection between CP on-chip antenna and dual-polarized on-chip antenna integrated for a 60-GHz CMOS single-chip transceiver is designed and analyzed. The radiation characteristics of on-chip antennas are investigated. The CP on-chip antenna is used as a transmitter, while dual-polarized on-chip antenna with dual feed transmission lines is used as a receiver for two

different circuits on the same chip. The effect of the separation distance between the CP- and dual-polarized on-chip antennas on the radiation characteristics of the two antennas have been investigated. The HFSS finite element method (FEM) [15] and the CST Microwave studio finite integration technique (FIT) [16] -based on 3-D full-wave electromagnetic solvers are used for the simulation in this paper.

2. Numerical results

2.1. Circularly-polarized circular microstrip on-chip patch antenna

A schematic of the proposed CMOS on-chip CP-microstrip antenna is shown in Fig.1a. The antenna consists of circular patch printed on the CMOS substrate six-layer structure. The circular microstrip antenna dimensions are designed for dominant mode TM11 at 60 GHz applications. The resonance frequency is given by [17]

$$f_{11} = \frac{c}{2\pi R_e \sqrt{\varepsilon_{re}}} x'_{11} \qquad where \ x'_{11} = 1.842 \qquad (1)$$

where R_e is the effective patch radius due to the fringing effect, and ε_{re} is the effective relative dielectric constant of the substrate. A fine tuning for the patch dimensions is used to adjust the resonance frequency. The circular patch is made from aluminium with thickness 1 μm, radius R=0.68 mm and two overlapped identical circular slots with radius R_s=0.115 mm and center to center separation C=74 μm are cut out from the patch. A microstrip transmission line is used for feeding the patch. The transmission line consists of two sections for impedance transformation and has dimensions L_t=0.2 mm, L_f=0.435 mm, w_t=10 μm and w_f=30 μm. The microstrip patch antenna and the transmission line are on the top metal layer in the CMOS structure. A silicon oxide substrate with ε_r=4, length L_s=2.4 mm, width w_s=2.2 mm, and thickness h_d of 22 μm is placed under the circular patch. The first metal layer in the CMOS structure is used as on-chip ground under the silicon oxide layer. The silicon chip substrate with ε_r=11.9 and σ=10 S/m and thickness h_s of 300 μm is placed beneath the ground plane.
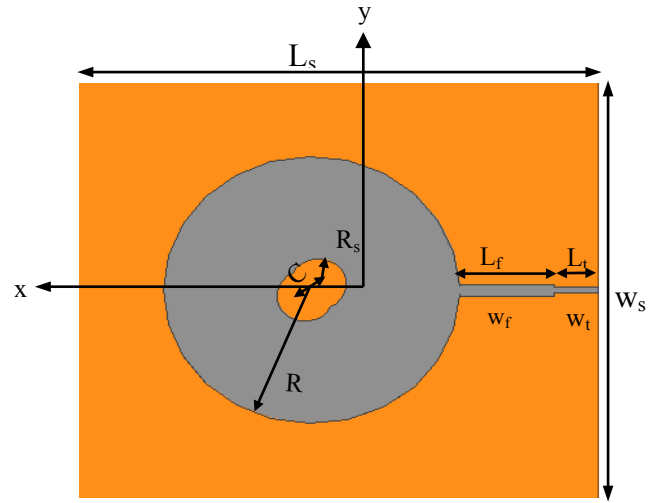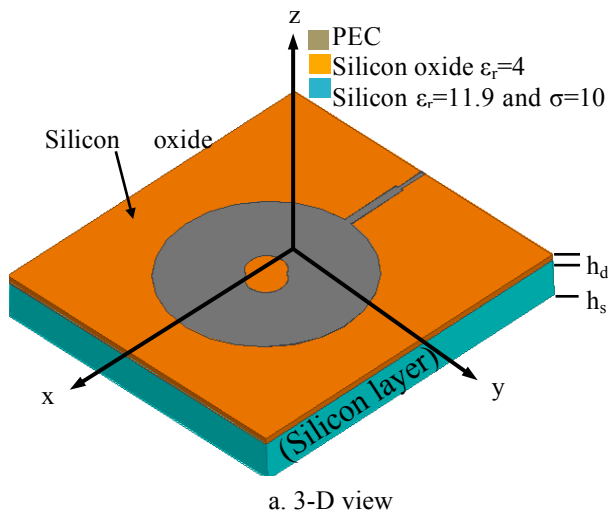

a. 3-D view

b. Top view

Fig.1. The configuration of the CP microstrip on-chip patch antenna with L_s=2.4 mm, W_s=2.2 mm, h_s =300 μm, h_d=22 μm, R=0.6825 mm, R_s=0.115 mm, L_f=0.435 mm, L_t=0.2 mm, w_f=30 μm, w_t=10 μm, and C=74 μm.

The variation of the reflection coefficient versus frequency for the CP on-chip antenna is shown in Fig. 2a. The antenna structure is simulated using the FIT and its results are compared with that obtained using the FEM. Good agreement between results is obtained. The antenna introduces impedance matching bandwidth of 2.85 GHz. The surface current distribution on the CP-microstrip antenna is shown in Fig. 2b. The surface current has its maximum amplitude around the feeding transmission line and around the circular slots. The two overlapped circular slots exhibit an electrically asymmetrical structure which induces two modes (TM10, and TM01) that have equal amplitudes and a 90° phase difference. The current flows in the clockwise direction results in left-handed circular polarization mode. The variations of antenna gain and radiation efficiency versus frequency for the CP-antenna are shown in Fig. 3a. A maximum gain of 0.3 dBi at 60 GHz is obtained with variation within 1.4 dB over the entire frequency band (55-65 GHz). The radiation efficiency of the antenna is within 25 % at 60 GHz. The variation of the radiation efficiency versus the silicon oxide thickness is shown in Fig. 3b. As the silicon oxide layer thickness is increased, the radiation efficiency is increased. The axial ratio variation versus frequency at the broadside direction is shown in Fig. 3c. Again, good agreement between the FEM and FIT results is depicted. The antenna introduces circular polarization properties at 60 GHz with an axial ratio of 1.9 dB and axial ratio bandwidth of 600 MHz (6%). The circular polarization radiation pattern components E_L (left-hand) and E_R (right-hand) at 60 GHz in x-z and y-z planes are shown in Fig. 4. The antenna introduces left-hand circular polarization with front-to-back ratio (FBR) of

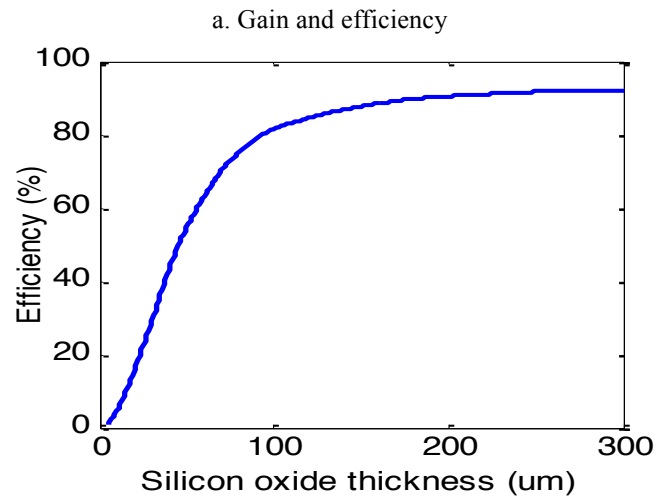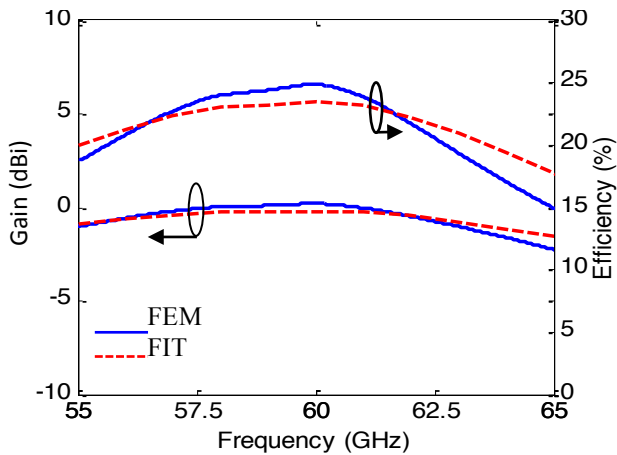26/27.5 dB in the two planes with co-/cross-polarization of 31.9/33.8 dB at θ=0.
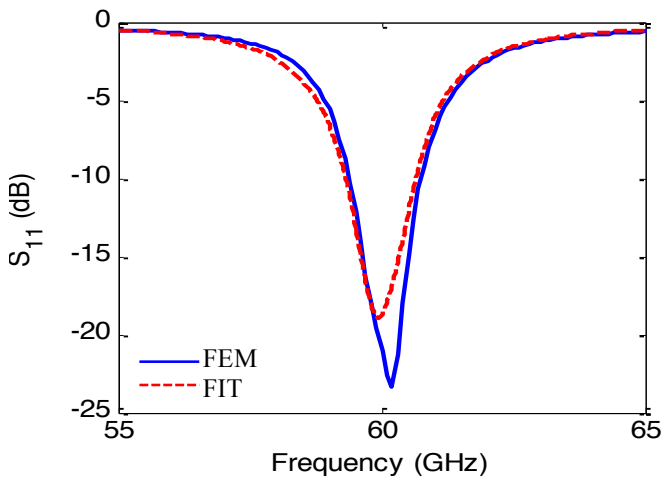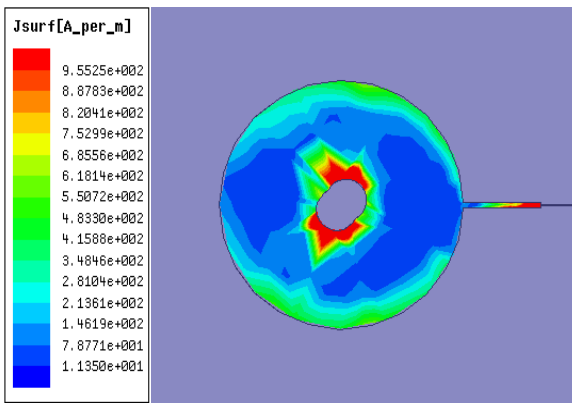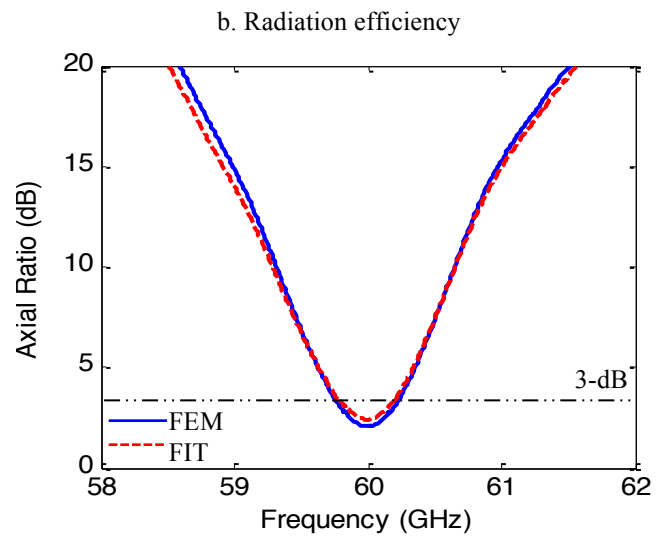

a.   Return loss (dB)

b.   Surface current

Fig. 2 a. The variation of return loss versus frequency of CP microstrip patch on-chip antenna. b. The surface current distribution on the CP microstrip patch on-chip antenna at 60 GHz.
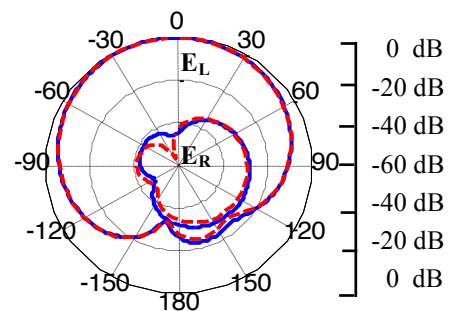

a. Gain and efficiency

b. Radiation efficiency

c.   Axial ratio

Fig. 3 a. The variations of the gain and radiation efficiency versus frequency of CP microstrip patch on-chip antenna. b. The variation of the radiation efficiency versus the silicon oxide thickness. c. The variation of the axial ratio versus frequency for CP microstrip patch on-chip antenna.
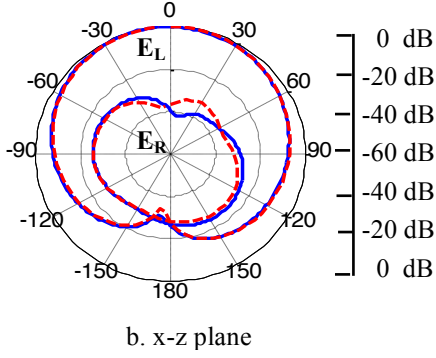

a. y-z plane

b. x-z plane

Fig. 4. The circular polarization radiation patterns of the CP on-chip antenna in x-z and y-z planes at 60 GHz.

2.2. Dual-polarized square microstrip patch on-chip antenna

The geometry of the dual-polarized square microstrip patch on-chip antenna with detailed dimensions is shown in Fig. 5. The square patch is printed on a silicon oxide substrate of thickness h_d=22 μm with aluminium ground plane. The resonance frequency for the fundamental mode TM_{10} is given by [17]

$$f_{10} = \frac{c}{2\pi L_{pe}\sqrt{\varepsilon_{re}}} \qquad (2)$$

where L_{pe} is the effective patch length due to the fringing effect. The square patch has side-length L_p=1.2 mm. Two orthogonal microstrip transmission lines are used to feed the square patch for dual-polarization. Each transmission line consists of two sections for impedance transformation and has dimensions L_t=0.2 mm, L_f=0. 435 mm, w_t=10 μm and w_f=30 μm. The two transmission lines are symmetrically oriented about the edge center of the square patch to excite two orthogonal modes. The same silicon oxide and silicon substrates in section A is used for dual-polarization on-chip antenna.
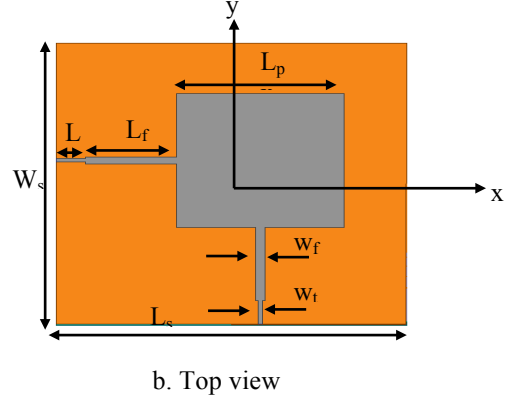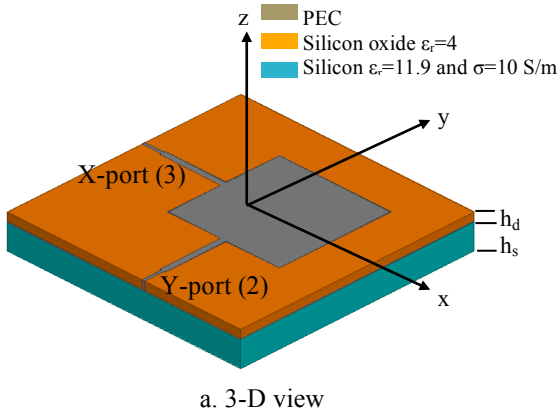

a. 3-D view

b. Top view

Fig. 5. The configuration of the dual-polarized microstrip patch on-chip antenna with L_s=2.4 mm, W_s=2.4 mm, h_s=300 μm, h_d=22 μm, L_p=1.2 mm, L_f=0.435 mm, L_t=0.2 mm, w_f=30 μm, and w_t=10 μm.

The variations of the reflection coefficients (S_{22} and S_{33}) and the isolation (S_{32}) for both the X-port (in x-axis direction) and Y-port (in y-axis direction) versus frequency are presented in Fig. 6a. The same reflection coefficient variation versus frequency is obtained for both the X- and Y- ports due to the symmetry in the patch and the transmission line position on the antenna. The resonance frequency is 60 GHz with impedance matching bandwidth of 1.120 GHz. Good isolation between the two ports is obtained and it is close to -25.4 dB at 60 GHz and below this value over the whole frequency band. The variations of antenna gain and radiation efficiency versus frequency for the dual-ports are shown in Fig. 6b. Both the X-port and Y-port introduce maximum gain of 0.7 dBi and radiation efficiency of 25% at 60 GHz. The simulated surface current distributions on the dual- polarized microstrip patch on-chip antenna for the both the X-port and Y- port at 60 GHz are shown in Fig. 7. For the X-port, the surface current distribution has its maximum value along the x-directed. For the Y-port, the surface current distribution has its maximum value on the y-directed. Identical surface current distribution, but with cross-polarization is obtained for both the X- and Y-ports. The radiation patterns for the X- and Y-ports at 60 GHz in different planes are shown in Fig. 8. The FBR is 29/28 dB and the co-/cross-polar level of 33/33 dB for the X-/Y-port in the x-z plane. The FBR is 30/29dB and the co-/cross-polar level of 34/32 dB for the X-/Y-port in the y-z plane. In order to investigate the effect of the CMOS six-metal layers structure on the radiation characteristics of the on-chip antenna, the metal layers are inserted with the dual-polarized antenna as shown in Fig. 9a. The six-metal layers are surrounding the patch to investigate its effect on the antenna radiation characteristics. The variation of the reflection coefficient versus frequency for the dual-polarized antenna is shown in Fig.9b. A slight shift in the resonance frequency of about 0.5 GHz with nearly the same matching bandwidth due to the presence of the six-metal layers. This shift can mainly take into account during the antenna design by adjusting the patch dimensions.
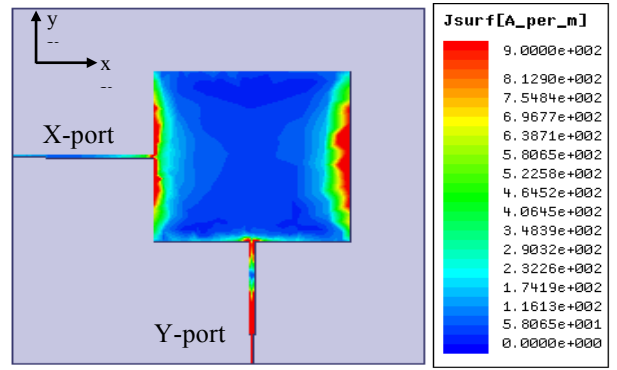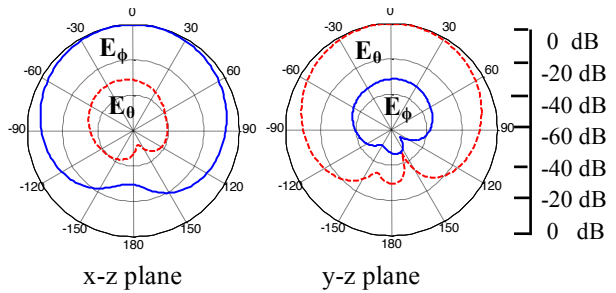
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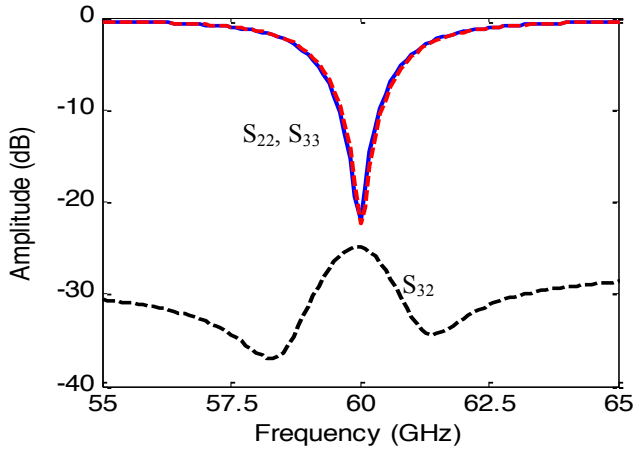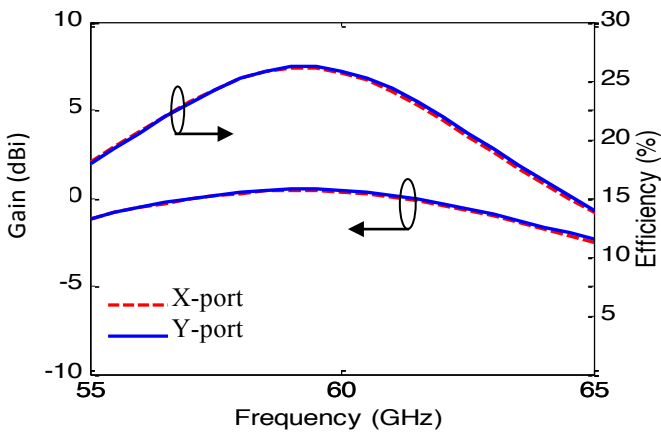
a. S-parameters

b. Gain and efficiency

Fig.6 a. The variation of the S-parameters versus frequency for the dual-polarized microstrip patch on-chip antenna. b. The variation of gain and radiation efficiency versus frequency for the dual-polarized microstrip patch on-chip antenna.
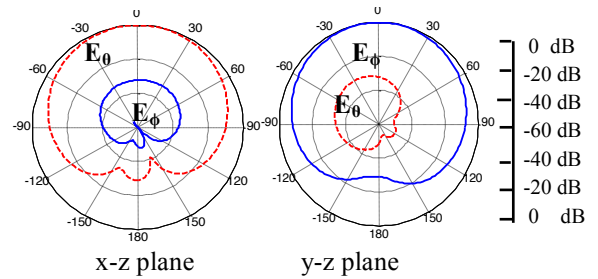

a. X-port excitation

b. Y-port excitation

Fig. 7. The surface current distribution on the dual-polarized microstrip patch on-chip antenna for both the X-port and Y-port at 60 GHz.

x-z plane   y-z plane
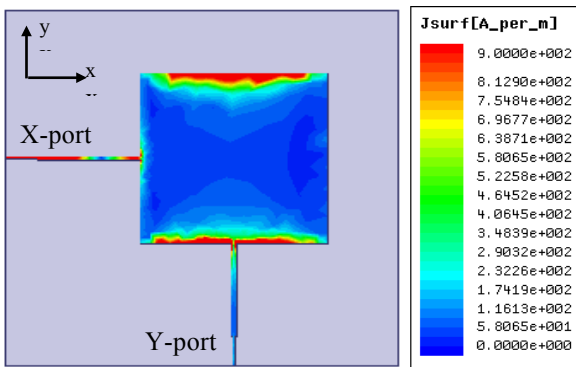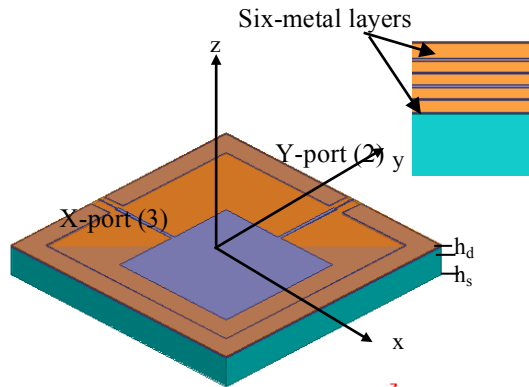
a. X-port excitation
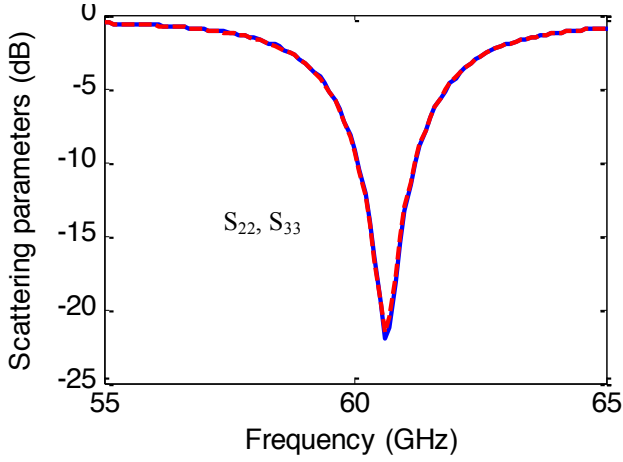

x-z plane   y-z plane

b. Y-port excitation.

Fig. 8. The radiation patterns of the dual-polarized microstrip patch on-chip antenna for both the X-port and Y-port at 60 GHz in different planes.


a. 3-D geometry

b. S-parameters

Fig.9 a. The geometry of the dual-polarized microstrip on-chip patch antenna with six-metal layers. b. The variation of the S-parameters versus frequency for the dual-polarized microstrip patch on-chip antenna in the presence of the six-metal layers.

## 2.3. Circular polarized and dual polarized antennas on the same chip:

For multi-chip wireless communications, both the CP-microstrip and dual-polarized microstrip patch on-chip antennas are placed face-to-face with a separation distance D between their edges, as shown in Fig. 10a. The CP-microstrip patch on-chip antenna is applied as a transmitting antenna and the dual-polarized microstrip patch on-chip antenna is applied as a receiving antenna. The power transmission gain (Gi) between the transmitting and the receiving antenna, is defined by

$$G_i = \frac{|s_{i1}|^2}{(1-|s_{11}|^2)(1-|s_{ii}|^2)} \qquad , i = 2,3 \qquad (3)$$

Due to the high isolation between the X- and Y-port of the dual-polarized antenna, the two ports can be considered as a two separate receiving antennas. The CP-microstrip patch on-chip antenna is considered as a transmitting antenna and each port of the dual-polarized antenna is considered as a receiving antenna.
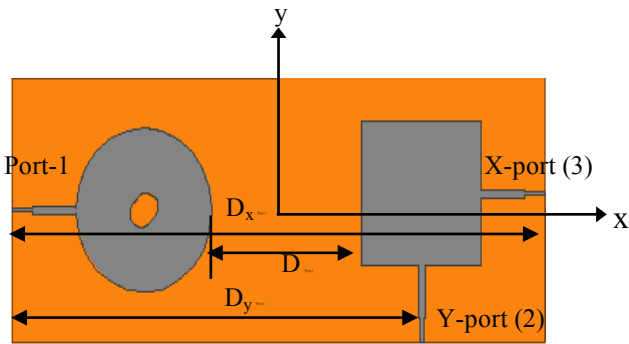

a. 2-D view
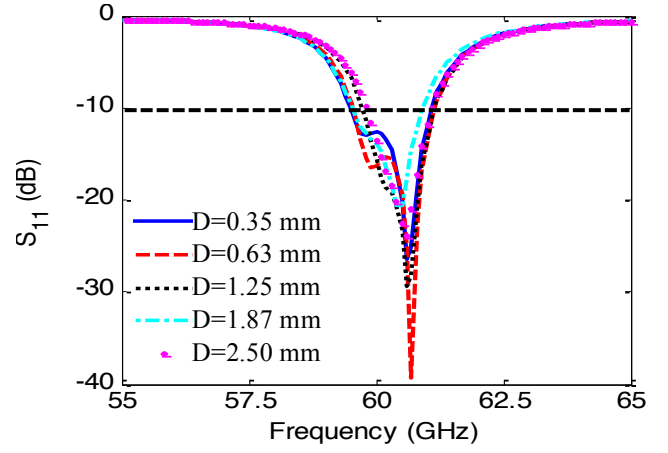
b. Reflection coefficient (dB)

Fig. 10a. The detailed arrangement of the CP microstrip and the dual-polarized microstrip patch on-chip antenna with separation distance D. b. The variation of the reflection coefficient of the CP-microstrip patch on-chip antenna in the presence of the dual- polarized on-chip antenna versus frequency for different separation distance D.

The variations of the reflection coefficient of the CP-microstrip patch on-chip antenna in the presence of the dual-polarized antenna versus frequency for different separation distance D are shown in Fig. 10b. The impedance matching bandwidth is varied between 2 GHz for D=0.5 mm and 2.4 GHz for D=2.5 mm with nearly the same resonant frequency. The variations of the transmission coefficient between the CP-microstrip patch on-chip antenna (port-1), X-port (3) and Y-port (2) versus frequency for different separation distance D are shown in Fig. 11. For the each separation distance D_x (D_x=D+3.8 mm) and D_y (D_y=D+2.6 mm), the transmission coefficient has its maximum value near the resonance frequency of the antennas for both X-and Y-port. As the distance increased the transmission coefficient decreased due to the broadside radiation of the X- and Y- port. For D=1.5 mm the transmission coefficient is -32 dB for the X-port and -35 dB for the Y-port.
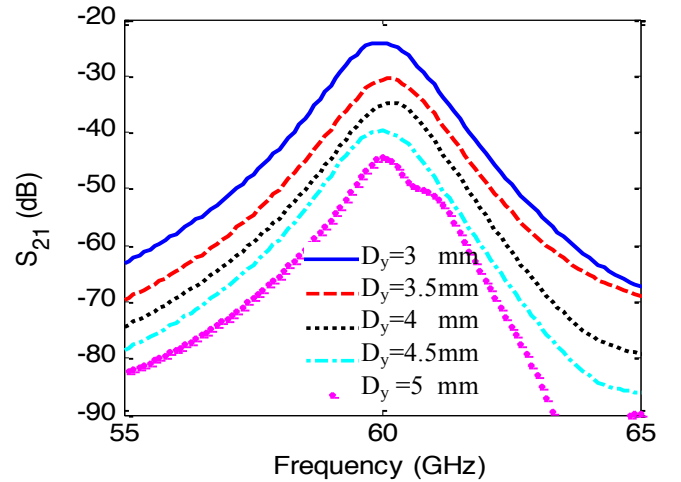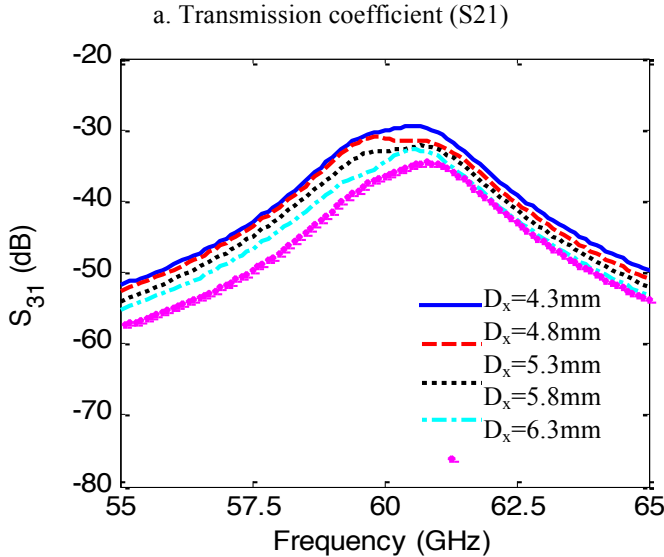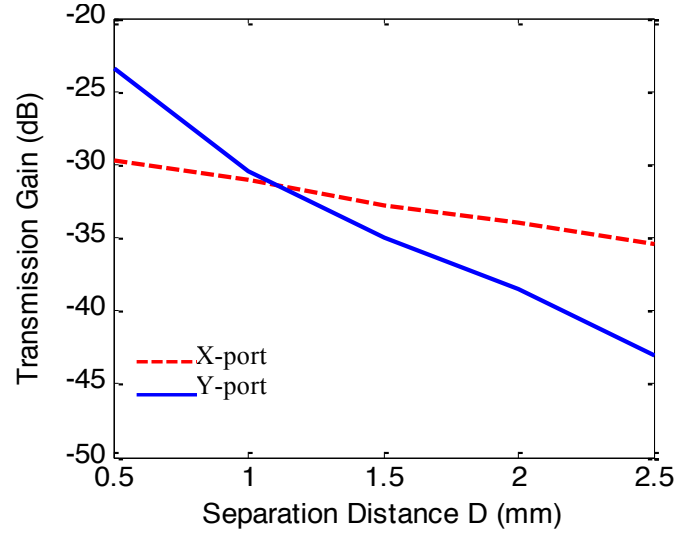
b. Transmission coefficient (S31)

Fig. 11. The transmission coefficient between the CP-microstrip patch on-chip antenna (port 1) and the dual-polarized microstrip patch on-chip antenna (Y-port (2) and X-port (3)) versus frequency for different separation distance D.
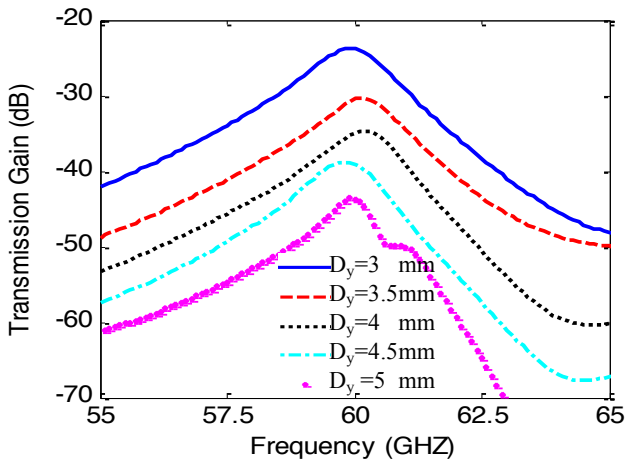

b. Transmission gain versus distance

Fig. 12. The transmission gain versus frequency and the transmission gain versus separation distance between the CP-microstrip on-chip antenna (port 1) and the dual-polarized on-chip antenna (Y-port (2) and X-port (3)) versus separation distance D at 60 GHz.

The variation of the transmission gain between the two antennas versus frequency at different separation distance D for the X- and Y-port is shown in Fig. 12a. For both the X- and Y-port, the transmission gain is decreased with increasing the separation distance between the antennas as shown in Fig. 12b. The transmission gain and transmission coefficient decreasing rate for the Y-port is faster than that for the X-port due to their positions relative to the CP-antenna. The transmission gain varies from -23.5 dB to -43 dB for the Y-port while it varies from -29.5 dB to -35.5 dB for the X-port. The radiation efficiency variation versus separation distance at 60 GHz is nearly the same of about 25 % dominate for both ports at different separation distances.

3. CONCLUSION

The paper introduces two different designs for on-chip microstrip antennas for wireless data transmission at 60 GHz applications. The first proposed design is a circularly polarized circular microstrip patch on–chip antenna with two overlapped circular slots fed by microstrip transmission line using the 0.18 μm CMOS technology. The antenna introduces an impedance matching bandwidth of 2.85 GHz centered at 60 GHz. The antenna gives left-hand circular polarization with axial ratio bandwidth of 600 MHz (6%). Maximum gain of 0.3 dB and radiation efficiency of 25 % at 60 GHz are obtained. The second proposed on-chip antenna is a dual-port square patch with dual feeding transmission lines at two orthogonal edges of the patch for 60 GHz applications. Good isolation between the two ports is obtained (about -25.4 dB at 60 GHz). Both the X-port and Y-port introduces a maximum gain of 0.7 dB and radiation efficiency of 25% at 60 GHz due to the symmetry in the antenna configuration. The CP-microstrip patch on-chip antenna is considered as a transmitting antenna and each port of the dual-polarized antenna is considered as a receiving antenna. The impedance matching bandwidth is varied between 2 GHz for D=0.5 mm and 2.4 GHz for D=1 mm with nearly the same resonant frequency. As the distance is increased the transmission coefficients between the CP-microstrip on-chip antenna (port-1) and the X-(port-3) and Y-(port-2) ports are decreased.

a. Transmission gain versus frequency

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