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Simulation of III-V Material Based Steep Slope Tunnel FET for RF Harvester Application

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Abstract

Due to the limitation of Sub-threshold Swing (SS) of 60 mV/dec in CMOS, alternately Tunnel FETs (TFETs) are more attractive in recent years since it has high energy efficiency and better switching performance even at a reduced voltage level. Because it has the benefits of Band to Band Tunneling (BTBT) behavior of operating mechanism and achieved a steep slope characteristic of less than 60 mV/dec. Despite these merits due to the band to band tunneling, the conventional Silicon based TFET is suffered from very low and limited ON-state current due to indirect and large energy gap feature. In the indirect band gap, the conservation of momentum occurs only when the absorption and emission of a photon are required which makes the absorption coefficient lower and limits the flow of electron. To address this problem, in this paper, a Hetero-Junction Tunnel FET (HTFET) devices employing with different lower bandgap materials (InAs/GaSb and InGaAs/InP) are designed by using Silvaco TCAD device simulator. The overall DC and analog/RF performance of HTFET devices are being extracted and investigated suitable for RF energy harvesting applications. The InAs/GaSb HTFET has shown a superior in characteristics by achieving a higher ON-state current of 2.3 mA/μm at V_{gs} = 1V, OFF current leakage of 4.18 x 10^{-11} A/μm, SS of 22.18 mV/dec and cut-off frequency range from MHz to GHz in operation. Under very low ambient RF level or sub-milliwatt (< 0 dBm) level conditions, the conventional CMOS based rectifier in RF harvester shows very poor performance and probably fails to convert RF signal into DC output voltage. This is due to the SS limitation of 60 mV/dec. Hence, HTFET based RF harvester is proposed and implemented in the circuit level by using the Keysight ADS software. The result indicates that a two-stage Dickson voltage multiplier design using InAs/GaSb HTFET can able to produce a DC output of 1.9 V, 1.6 μA @ 0 to -10 dBm, maximum efficiency of 59 % @ -14 dBm, operating frequency of 850 MHz at 10 kΩ loads with a sensitivity of 0 to -25 dBm.

Keywords: tunnel FET, band to band tunneling (BTBT), sub-threshold Swing (SS), RF harvester

1. Introduction

In recent decades, the continuous downscaling of CMOS creates a fundamental performance limitation such as short channel effects, high power dissipation due to leakage currents, low Ion/Ioff current ratio and sub-threshold Slope (SS of ≥ 60 mV/dec) at room temperature [1-2]. This is due to the phenomenon of drift-diffusion injection carrier mechanism in current MOSFETs. Hence the research is being carried out to find a new alternate device. Recently Tunnel FET has attracted huge attention and a most promising device for ultra-low power analog and digital circuits because it offers very low leakage current, low power dissipation, the steep sub-threshold slope of (less than 60 mV/dec) and fits best into the low standby power region [3-5]. TFETs are highly immune to short channel effects due to the band to band tunneling behavior of

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injection carrier mechanism on the source side as well as the scaling of gate length is possible along with the tunneling barrier width of less than 5nm. Moreover, TFET is independent of thermal factor kT/q not likely in MOSFETs. Silicon-based TFET is highly preferred since it can be easily fabricated and manipulate because of the existing CMOS technology supports it. However, the performance of Si-TFET is very poor in terms of ON-state current compared to MOSFETs due to indirect and large energy gap [6-7] and it fails to achieve the required current for the advanced technology nodes [8].

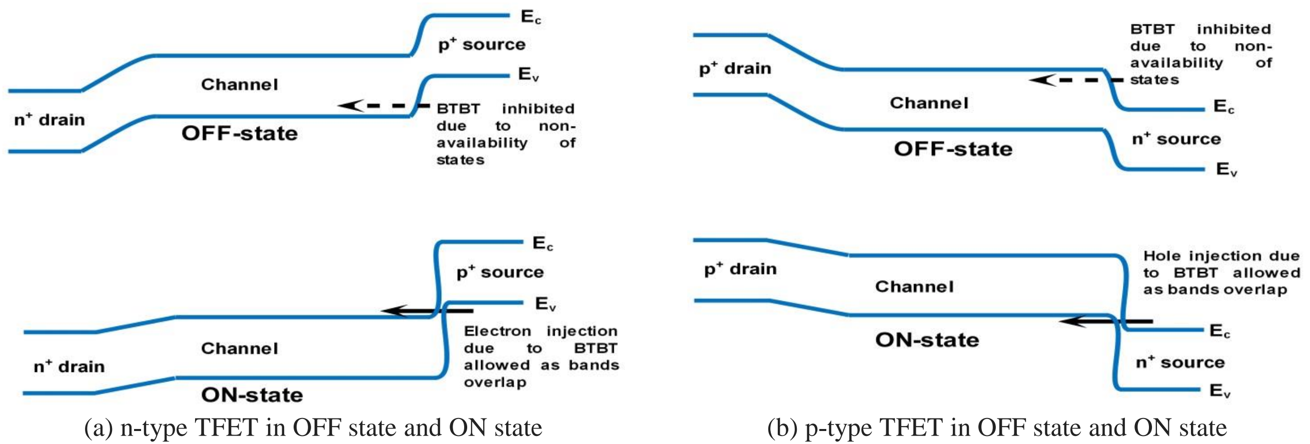
To overcome the above problem, recently a number of techniques were proposed by the researchers in their work by using high-k gate dielectric [9], gate stacking [10], strain engineering [11], and by using lower band gap material [12]. In order to accomplish a large on-drive current in TFET, small bandgap materials are desirable. Germanium (Ge) is also similar to Si, which is more CMOS compatible. It has been attracted by most of the researchers because of the very small gap of 0.67 eV compared to Si. However, it can increase the current mobility but it suffers from large leakage current [13]. Some of the research works have included the hetero-junction of both Si and Ge for attaining higher ON state current [14]. Next, to the Si and Ge, small band gap with low energy mass and higher tunneling probability properties of III-V compound materials are preferred [15]. By combining the metallic group III from the periodic table and the non-metallic group V from the periodic table, III-V compound material is formed. The application of III-V materials such as InAs, GaSb, InGaAs, AlGaSb, GaAsSb etc., are quite promising to be used for designing the TFET in recent days [16]. There are some simulation studies were performed by the researchers to find the physical insights of TFET and optimize the device design for enhancing the performances [17-18]. However, still, there are challenging remains in the III-V semiconductor-based TFET to achieve a very good steep sub-threshold slope and analog characteristics suitable for ultra-low power applications. Hence in this work, a TCAD simulation study of hetero-junction and different low band gap materials of InAs/GaSb and InGaAs/InP based TFETs are investigated. Since the effective tunneling mass of III-V materials is small compared to tunneling mass of Si. To enhance the electro-static control of drain currents through the gate electrode, a double gate structure is employed in both the TFETs. The III-V material based TFETs considered in this work are simulated in Silvaco TCAD and their performances are analyzed in terms of output dc characteristics and analog/RF parameters. Finally, an ultra-low power RF energy harvester application is chosen for implementing our HTFET.

2. Device Structure and Simulation Setup

TFET is a three terminal device similar in structure to MOSFET. The n-type TFET consists of P+ doped acting as a source, an intrinsic channel of I, and N+ doped region acting as a drain terminal. The height of the channel barrier height is controlled by the electrostatic control of the gate terminal voltage like same in MOS transistor. The operating mechanism of TFET is unique and different from MOSFET. The basic operating mechanism of TFET is based on Band-To-Band Tunneling (BTBT). BTBT involves tunneling of carriers from the valence band into the conduction band through the forbidden band gap or vice versa. Band diagrams of an n-type TFET are shown in Fig. 1(a) in the OFF-state and in the ON-state. When the gate voltage is close to zero, the TFET is in the OFF-state. The conduction band in the channel lies above the valence band in the source. As a result, BTBT is inhibited and the TFET is in the OFF-state with extremely low drain current. When the gate voltage is increased, the gate voltage modulates the carrier density below the gate and the conduction band in the channel is pushed down. When a sufficiently high voltage is applied to the gate, there is band bending at the source such that the valence band in the source and the conduction band in the channel get aligned, as shown in Fig. 1(a). As a result, the electrons in the valence band of source terminal can tunnel into the conduction band of the channel. The electrons that tunnel into the channel are swept to the drain terminal by the positive bias of the drain. The band diagrams of a p-type TFET in OFF-state and ON-state are shown in Fig. 1(b).

The principle of operation of a p-type TFET is like the n-type TFET. When the gate voltage is close to zero, the TFET is in the OFF-state. The conduction band in the source lies above the valence band in the channel. As a result, BTBT is

blocked and the TFET is in the OFF-state. When a sufficiently large negative voltage is applied to the gate, the valence band in the channel is pushed above the conduction band of the source as shown in Fig. 1(b). As a result, holes are injected into the channel, which is subsequently swept to the drain terminal by the negative bias of the drain. The high energy carriers distributed in the Fermi-Dirac tail are rejected by the band gap in the source and hence it cannot contribute to the movement process [19]. It is fundamentally the lower temperature of carriers involved in the transportation process through tunneling window which results in a steep slope SS of less than 60 mV/dec. The tunneling probability of electrons across the potential barrier in the source-channel TFET junction is analytically solved by WKB (Wentzel Kramers Brillouin) approximation [20] as

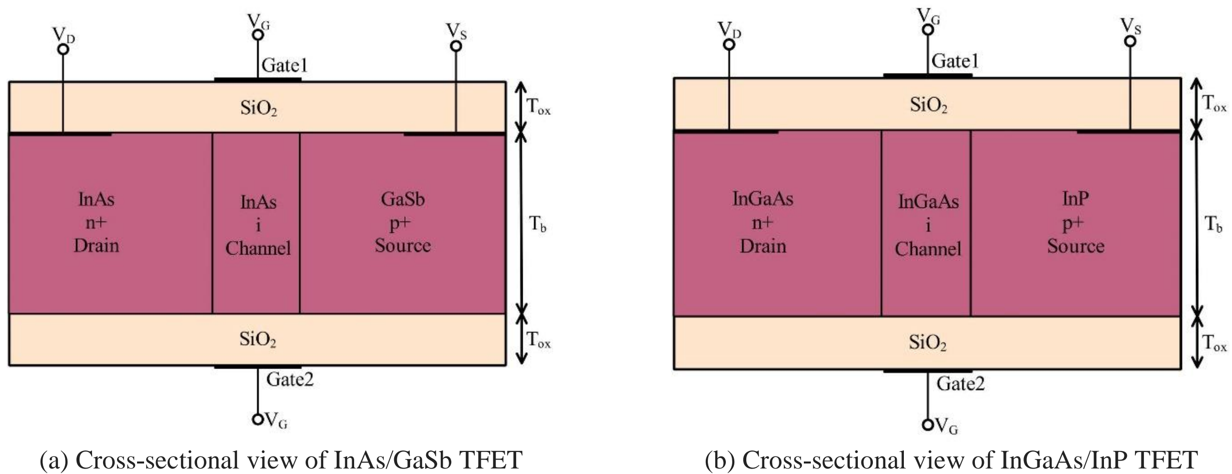


(a) n-type TFET in OFF state and ON state (b) p-type TFET in OFF state and ON state

Fig. 1 BTBT Operation of n-type TFET and p-type TFET

$$I_D \propto T\left(b2b\right) \approx \exp\left(\frac{-4\sqrt{2m^*}E_g^3}{3eh\left(E_g+\Delta\varphi\right)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}\right) \tag{1}$$

where m* and E_g is the carrier effective mass and energy band gap of material, Δφ stands for energy range where tunneling is taking place, e is the charge of electron and h is Planck’s constant. ε_{ox} and ε_{si} is the dielectric of oxide and body substrate respectively. t_{ox} and t_{si} is the thickness of oxide and body substrate respectively.



(a) Cross-sectional view of InAs/GaSb TFET (b) Cross-sectional view of InGaAs/InP TFET

Fig. 2 The cross-sectional view of III-V material based HTFET devices

The tunneling probability of electrons is directly proportional to the flow of drain current. By referring the Eq. (1), it can be clearly understood that the material having low effective mass m* and energy band gap E_g can improve the tunneling probability which leads to increase in the drain current. The schematic of n-type III-V based TFET devices (a) InAs/GaSb TFET (b) InGaAs/InP TFET considered in this work are shown in Fig. 2(a) and (b). Table 1 shows the material parameters and the values used in this simulation work. There we can observe the III-V materials effective mass and energy band gap

values are lower than the conventional Si. The reduced effective mass value of holes and electrons has the advantage of an increase in tunneling the barrier. The high mobility and direct band gap feature of III-V materials can also improve the tunneling current.

Table 1 Material Parameters used in the simulation

Parameters	InAs	GaSb	InGaAs	InP
Effective mass of electron tunneling (m_e)	0.023	0.042	0.043	0.08
Effective mass of hole tunneling (m_h)	0.4	0.4	0.052	0.012
Mobility of electron (cm^2/V.s)	33000	5000	12000	5400
Mobility of Hole (cm^2/V.s)	400	850	300	200
Energy Band Gap E_g (eV)	0.36	0.72	0.75	1.35
Permittivity	15.15	15.7	13.9	12.5

A common double gate electrode structure is chosen in this work because it gives better electrostatic control on the channel of the device. The combined effect features of material engineering will reduce the energy barrier at source-channel junction leads to improve the BTBT rate and SS. III-V materials of 10nm body thickness and gate oxide material of SiO2 with a dielectric value of ε=3.9 is chosen for this study. The device design parameters used in the TCAD simulations are shown in Table 2.

Table 2 Device design parameters used in the simulation

Parameters	Value
SiO_2 layer thickness (T_{ox})	1.5 nm
Body Thickness (T_b)	10 nm
Source length (L_s)	50 nm
Gate length (L_g)	20 nm
Drain length (L_d)	50 nm
Source, Channel & drain doping	$1x10^{22}$ atoms/cm^{-3}, $1x10^{16}$ atoms/cm^{-3} & $1x10^{19}$ atoms/cm^{-3}
Gate 1 & Gate 2 metal work function	4.5 eV (Chromium)

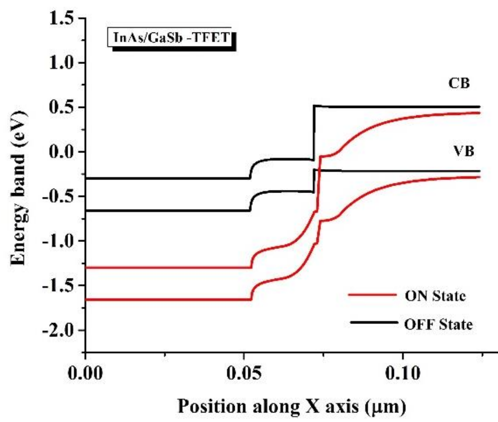
To do an extensive simulation of III-V TFET devices, Silvaco 2D Atlas device simulator is used in this work [21]. The non-local band to band tunneling model is employed in this simulation for modeling the tunneling process accurately as well as considering the spatial variation of energy band. To introduce the trap-to-band phonon-assisted tunneling in our device, trap assisted model is considered. The tunneling probability across the junction is calculated by using the Wentzel-Kramers-Brillouin (WKB) method. Shockley-Read-Hall (SRH) generation and recombination model is adopted to include the effect of carrier recombination and account the leakage currents. To account the transfer of electrons and holes in the simulation, the drift-diffusion transport model is considered. To incorporate the temperature dependent carrier mobility, Lombardi Constant Voltage Temperature (CVT) mobility is used [22]. Since the body thickness of our simulated III-V TFET devices is more than 5nm, here the quantum transport model and Band Gap Narrowing (BGN) is not considered in our work [23].

3. TCAD Simulation Results and Discussion

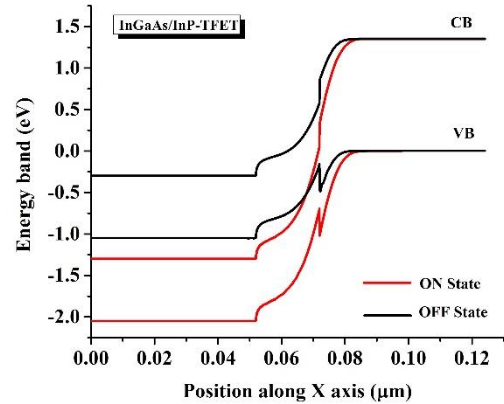
3.1. DC performance analysis

To clearly understand the BTBT behavior of HTFET, an energy band diagram is the best one to observe in which how the tunneling width is getting reduced can be seen. The Fig. 3(a) and (b) show the Valence Band (VB) and Conduction Band (CB) energies of the devices considered in this work under the condition of both OFF (Vgs= 0V & Vds= 1V) and ON (Vgs= 1V & Vds= 1V) states. The differences in the channel bandgap position relative to the energy levels of the source and drain facilitate the tunneling mechanism as observed from the energy band diagrams. It is noticed that in OFF state; both the III-V HTFET device has high tunneling width distance between valence and conduction band due to the large potential barrier exists. Therefore, the tunneling probability of electrons moving from VB of the source to CB of the channel is very low. However, in ON state under positive gate bias, the CB and VB of the channel are approaching to get aligned with CB and VB of drain causes the tunneling width distance is reduced. Therefore, it provides a less potential barrier and more tunneling

probability of electrons moving from VB of the source to CB of the channel is taken place. However, it is observed that InAs/GaSb HTFET has closer alignment of energy gap on source-channel junction when compared to InGaAs/InP TFET. Since the energy band gap values of InAs and GaAs values are very less compared to InGaAs and InP values which can be referred to in Table 1.

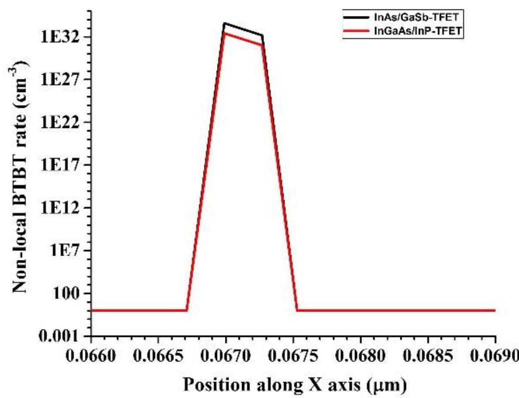


(a) Energy band diagram of InAs/GaSb TFET

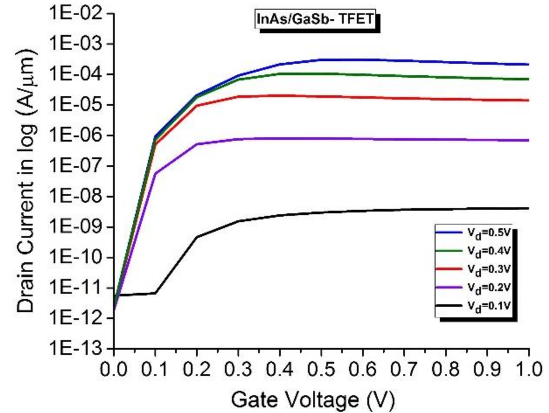


(b) Energy band diagram of InGaAs/InP TFET

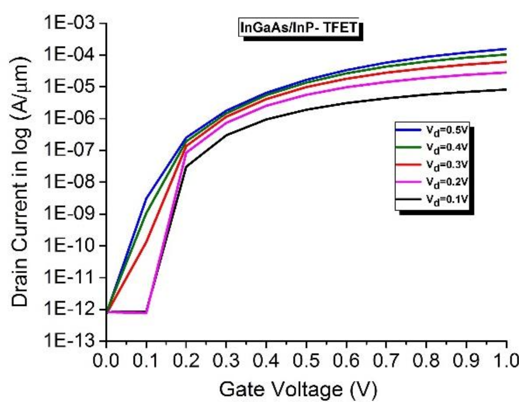
Fig. 3 Energy band diagram of III-V material based HTFET devices



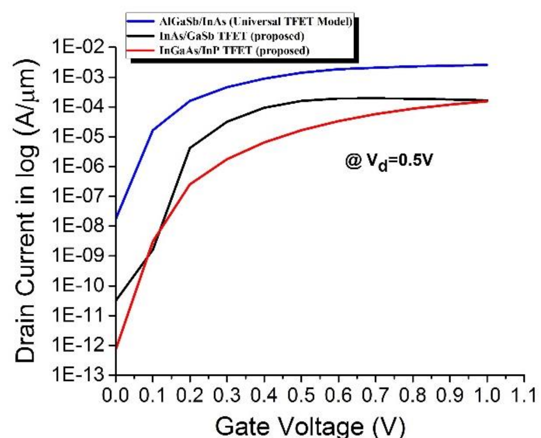
(a) BTBT rate of InAs/GaSb & InGaAs/InP TFET



(b) Drain current characteristics of InAs/GaSb TFET



(c) Drain current characteristics of InGaAs/InP TFET



(d) Calibration of HTFET devices with Universal

Fig. 4 BTBT rate and Drain current characteristics of III-V TFET devices

Due to the impact of low energy band gap III-V materials in the design, there will be an increase in the Band to Band Tunneling (BTBT) rate on the source channel interface during the ON state. The InAs/GaSb HTFET has achieved a maximum BTBT rate of 3.79 x 1033 electrons/cm-3 along the length of the source-channel junction. Similarly, the InGaAs/InP TFET has also achieved a maximum BTBT rate of 2.51 x 1032 electrons/cm-3 which is comparatively less as

shown in Fig. 4(a). The high BTBT rate involves in the source channel interface leads to the flow of high ON state drain current. The drain current transfer characteristics of both the HTFET at different Vds values are shown in Fig. 4(b) and (c). There it can be seen that an ON-drive current of 1.59 x 10-4 A/µm and 1.65 x 10-5 A/µm achieved by both the devices InAs/GaSb and InGaAs/InP TFET at Vgs =0.5V & Vds= 0.5V respectively. Both the HTFET devices are comparatively giving very good drain current characteristics and it is calibrated with Universal TFET model as observed in Fig. 4(d). It is preferred that our simulated III-V devices curves are more or less try to achieve the same as Universal TFET characteristics. The Universal TFET model is available in nano-hub website [24] in which double gate AlGaSb/InAs is considered in this work as a calibrated model. The InAs/GaSb TFET achieved a maximum current value is 2.3 mA/µm at Vgs = Vds= 1V which is comparatively greater than InGaAs/InP TFET. The OFF current values can be extracted from Id-Vgs characteristics of a particular device and it is very important to be considered at ultra-low power applications. The obtained OFF-state current value of InGaAs/InP TFET is very low of 8.66 x 10-13 A/µm when compared with InAs/GaSb TFET of 4.18 x 10-11 A/µm. The InGaAs/InP combination forms a staggered band alignment which creates a high depletion region or big tunneling barrier at the source-channel interface and makes the OFF-state current becomes lower. In the case of InAs/GaSb HTFET, although it has shown an improvement in high ON state current it shows a high OFF state current comparative than InGaAs/InP HTFET due to the formation of a broken gap. A very low value of device OFF current indicates that standby power consumption to be very low when it is used in analog and digital circuits.

The point sub-threshold slope is calculated by taking the maximum slope of the log Id versus Vgs curve. The calculated values are 22.18 and 21.11 mV/dec respectively. The average SS of the simulated device is calculated by using the Eq. (2).

$$SS = \frac{V_t - V_{off}}{LogI_{vt} - LogI_{off}} \tag{2}$$

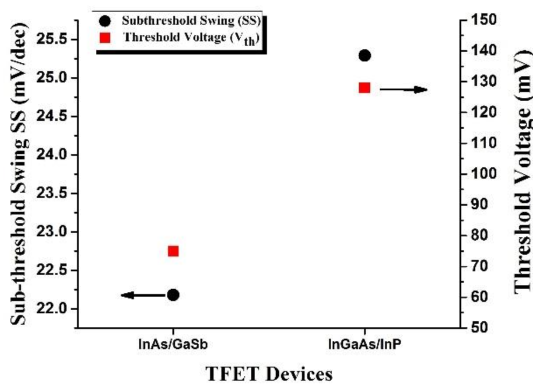
The calculated SS values of InAs/GaSb HTFET and InGaAs/InP HTFET are 22.18 and 25.29 mV/dec respectively. It is noted that very low SS achieved by III-V TFET device indicates a very steeper slope characteristic. Hence it is expected that a higher I_{on}/I_{off} ratio can be obtained even at a very low supply voltage of less than 0.5 V. The HTFET devices achieve a higher I_{on}/I_{off} ratio of 10^9. Hence, it can be a promising device for a reduced dynamic power dissipation of digital circuits. Due to the very steep SS and very low OFF-state leakage current of HTFET, it will lead to having a low threshold or turn-on voltage. The calculated threshold voltage value of simulated HTFET devices is 75 mV and 128 mV respectively. The calculated SS and threshold voltage values for simulated III-V TFET devices are shown in Fig. 5(a). The SS achievement of less than 60 mV/dec achieved by the simulated III-V TFET devices indicates that its switching speed is very high which is very essential in the case of ultra-low power and energy efficient applications. In addition to that, OFF state leakage and the threshold voltage parameter trade-offs can be relaxed because of the tunneling operating mechanism. The achievement of low threshold voltage indicates that the device sensitivity can be increased. From the DC analysis response of simulated III-V TFET devices, it is observed to be suitable for ultra-low power applications.

3.2. Analog/Radio Frequency (RF) performance analysis

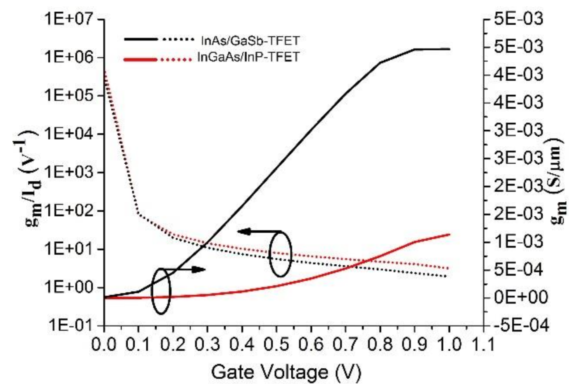
Analyzing the analog/RF response of the TFET device is very essential when it is utilized at the circuit level. It can be analyzed through no. of parameters such as Transconductance (gm), Transconductance to the current ratio (gm/Id), Gate to drain capacitance (Cgd), Unity gain cut-off frequency (fT) and Gain Bandwidth Product (GBP). Transconductance (gm) plays a vital role in the design of analog circuits such as Operational Transconductance Amplifier (OTA) and Operational Amplifiers (OP-Amp). Transconductance (gm) parameter signifies the amplification provided by the device. It is directly proportional to the gain of the circuit. It also affects bandwidth, noise performance, and offsets. The Transconductance (gm) is calculated by the Eq. (3).

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \tag{3}$$

The value of g_m with the variation of $V_{gs,}$ at V_{ds} = 1V for the HTFET devices are shown in Fig. 5(b). As per the Eq. (3), the value of g_m is directly depended on the exponential increase in the value of the drain current (I_d). The simulated InAs/GaSb HTFET device has a good exponential increase in I_d with the variation of V_{gs} characteristics, and then it achieves a higher g_m value of 1.65 x10^{-3} (S/μm). The higher value of g_m provided by the HTFET devices which mean it can be a suitable choice for analog amplification circuits. In the same Fig. 5(b) (refer dotted line), the variation of Transconductance to the current ratio (g_m/I_d) with the increase in V_{gs} is also shown. It is referred to as a governing factor for the net transconductance generation efficiency of a device. It represents the efficiency of the device to convert the bias current into transconductance. This parameter is strongly related to analog performance (i.e) higher the g_m/I_d value ensures the better amplification per unit drain current. In the low sub-threshold region of V_{gs} less than 0. 1V, both the HTEFT devices provide a very high g_m/I_d of around 5 x 10^5 (V^{-1}). As the V_{gs} increases further, the g_m/I_d value of both the HTEFT gets degrades very faster. Hence it is very difficult to provide the linear output to the circuit's level. However, it can be most suitable for the design of ultra-low power analog circuit applications. It is noted that simulated III-V HTFET devices are having non-linearity problem and there is a lack of noise performance analysis, which may be considered as future work. Then only the prediction of analog performance would be complete.



(a) SS and Threshold voltage value of simulated TFET

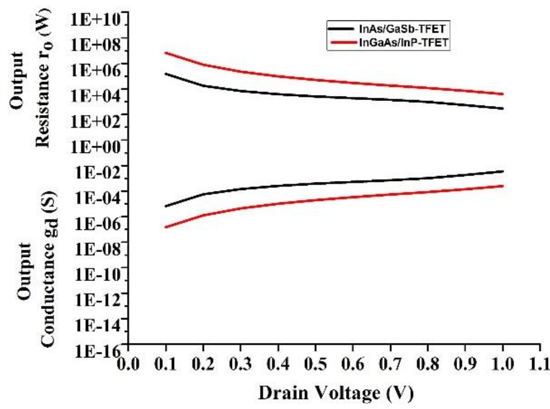


(b) Transconductance (gm) value of simulated TFET

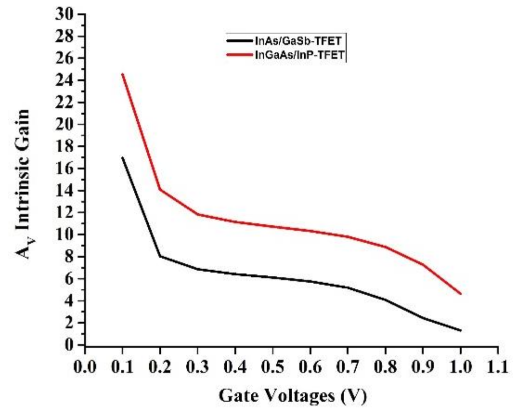
Fig. 5 SS, Threshold voltage and Transconductance (gm) value of simulated III-V TFETs

The variation of output conductance (g_d) with V_{ds} for III-V TFET devices at V_{gs} = 1V are shown in Fig. 6(a). It is observed that at a lower value of $V_{ds,}$ the drain control decreases and the drain current rises non-linearly. As a result, it provides a small increase in the output conductance (g_d) until a certain V_{ds} voltage of 0.5V. After that, it enters into the saturation region. This minimum value of g_d is obtained due to Drain Induced Barrier Lowering (DIBL) and channel length modulation, so the current is constant in the saturation region. In the same time, at a reduced gate voltage of V_{gs}, there is a sufficient drain control at a lower value of V_{ds}. Hence it can be predicted that the III-V HTFET simulated devices have more advantages in producing high gains at low power supply because the g_d decreases at a lower value of V_{gs} and V_{ds}. However, at under low $V_{gs,}$ the output resistance (r_0) of HTFET shows larger since there is no PN junction formed on the drain side. It can be clearly observed from (r_0) curve in Fig. 6(a) which is exactly the inverse of g_d. It is calculated that InAs/GaSb TFET and InGaAs/InP TFET obtains a minimum DIBL value of 135.6 mV/V and 44.4 mV/V respectively. It can be employed to achieve a higher value of intrinsic gain A_v by

$$A_v = \frac{g_m}{g_d} = g_m . r_o \tag{4}$$



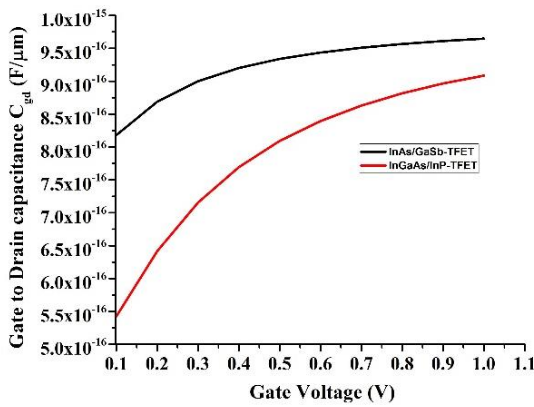
(a) Variation of gd and r0 as a function of drain voltage at Vgs = 1V



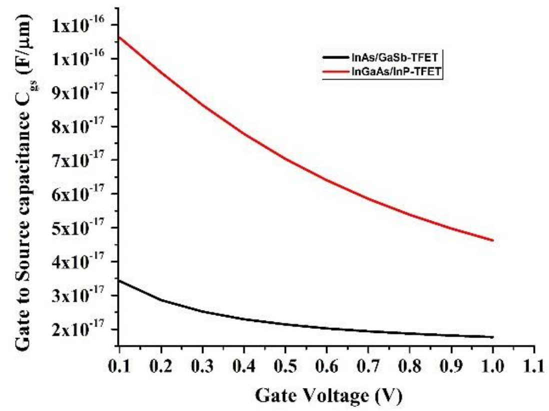
(b) Intrinsic gain of simulated device at Vds=1V

Fig. 6 Output conductance (gd), Output resistance (r0), and Intrinsic gain of simulated III-V TFET devices

The Fig. 6(b) shows the Intrinsic gain of the simulated device with respect to the gate to source voltage at V_{ds}=1V in which InGaAs/InP TFET has achieved a higher gain compare to InAs/GaSb TFET. Since the output conductance (g_d) and output resistance (r_0) values are very low values over the variation of the gate voltage as referred to in Fig. 6(a). The proposed InGaAs/InP TFET can provide a high intrinsic gain A_v of 24.5 at a gate voltage of 0.1 V.



(a) Gate to drain capacitance (Cgd) values



(b) Gate to source capacitance (Cgs) values

Fig. 7 Gate to drain capacitance (Cgd) and Gate to source capacitance (Cgs) values of III-V TFETs at Vds=1V

Among the analog parameters, C_{gd} plays an effective role in determining high-frequency responses. As lower the value of C_{gd}, there is better control of gate over the channel, to achieve higher RF performance by reducing the parasitic effect. Fig. 7(a) shows the variation of C_{gd} for the TFET devices considered. It is noted that InAs/GaSb TFET device has possessed a very low C_{gd} value of 9.57 x 10^{-16} F/µm and InGaAs/InP TFET possess a C_{gd} value of 9.09 x 10^{-16} F/µm with little difference in range. This is due to the lower energy band gap III-V materials and high mobility of electron features incorporated in the design. The reduced value of C_{gd} means it has a better gate controlling over the channel. Due to the increase in electron concentration at the source-channel interface, it will reduce the C_{gs} value. The Fig. 7(b) shows the variation of C_{gd} for the TFET devices considered in this work. The combined effect of the lower value of C_{gs} and C_{gd} will determine the other high-frequency parameters. The key parameters of high-frequency performance are evaluated by unity gain cut-off frequency (f_T) and gain bandwidth product GBP. The f_T and GBP are computed by using the formulas shown in Eqs. (5) and (6).

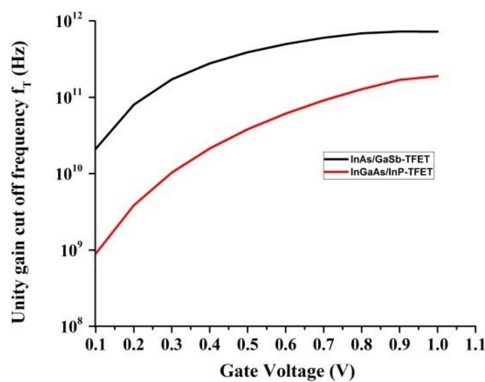
$$f_T = \frac{g_m}{2\pi\left(C_{gd} + C_{gs}\right)} \tag{5}$$

$$GBP = \frac{g_m}{2\pi\left(C_{gd}\right)} \tag{6}$$

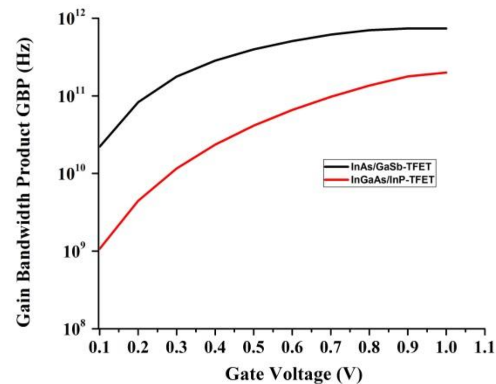
F_T is the transient frequency where the current gain of the device becomes unity and GBP is the measure of the device performance in high-frequency ranges calculated at DC gain of 10. InAs/GaSb TFET has very good f_T response and achieves a higher frequency value (in GHz range) at lower V_{gs} as shown in Fig. 8(a). This is due to the combined effect of the higher value of g_m at smaller V_{gs} and the reduced value of $C_{gs} + C_{gd}$. Similarly, it is noticed that GBP value for InAs/GaSb TFET is a significantly higher range in frequency compared to the InGaAs/InP device due to the effect of lower $C_{gd\ as}$ shown in Fig. 8(b). Thus, the simulated hetero-junction InAs/GaSb and InGaAs/InP TFET devices will be suitable for high radio frequency circuit and ultra-low power applications. The summary of simulated III-V material based TFET results are tabulated in Table 3. It is observed that both the simulated TFETs are achieved a very good DC and analog characteristics at very low gate voltages.

Table 3 Summary of TCAD simulation results of III-V TFETs

Parameters	InAs/GaSb	InGaAs/InP
SS avg	22.18 mV/dec	25.29 mV/dec
BTBT Rate	3.79×10^{33} electrons/cm^{-3}	2.51×10^{32} electrons/cm^{-3}
I_{on} (@V_{gs}=0.5V)	1.59×10^{-4} A/μm	1.65×10^{-5} A/μm
I_{off}	4.18×10^{-11} A/μm	8.66×10^{-13} A/μm
I_{on}/I_{off} ratio	10^9	10^6
Threshold voltage (V_{th})	75 mV	128 mV
DIBL	135 mV/V	44.5 mV/V
Transconductance (g_m) @V_{gs}=0.1	1.13×10^{-4} S/μm	3.66×10^{-6} S/μm
Output conductance (g_d) @V_{gs}=0.1V	6.69×10^{-6} S/μm	1.49×10^{-7} S/μm
Intrinsic gain (A_v) @V_{gs}=0.1V	17	24.5
Gate to drain Capacitance (C_{gd}) @V_{gs}=0.1V	8.18×10^{-16} F/μm	5.42×10^{-16} F/μm
Gate to source Capacitance (C_{gs}) @V_{gs}=0.1V	3.43×10^{-17} F/μm	1.06×10^{-16} F/μm
Cut-off frequency (f_T)	2.12×10^{10} Hz	8.97×10^{8} Hz
Gain band width product (GBP)	2.21×10^{10} Hz	1.07×10^{9} Hz



(a) Cut-off frequency fT values of simulated TFETs



(b) Gain band width product (GBP) of simulated TFETs

Fig. 8 Cut-off frequency (fT) and gain band width product (GBP) variation with gate to source voltage at Vds = 1V

4. TFET Modeling for RF rectifier

It has been referred from Table 3 that compared to InGaAs/InP TFET, the simulation results of InAs/GaSb TFET shows that excellent linear current onset at the very low gate and drain voltages of 0.1 to 0.5V. It also noted that Radio Frequency (RF) response of it is in the range from MHz to GHz while referring the Cut-off frequency fT characteristics. It enables the

above TFET could be a suitable device for ultra-low power RF applications. Nowadays, RF energy harvesting circuits using a rectifying antenna (rectenna) are getting more attention and it may be a viable solution for powering ultra-low power sensors. Currently, the RF rectifier in the rectenna circuit is facing a major challenge that under very low ambient RF level condition, it shows very poor performance and probably fails to convert RF signal into a required dc output voltage. This is due to the subthreshold voltage limits or weak sensitivity of the rectifying device used in the rectifier [26]. Hence, our simulated III-V TFET has the potential for supporting this RF rectifier circuit due to very steep slope characteristics and superior performance at very low voltages [27]. To illustrate this potential, a lookup table based Verilog-A TFET model has been employed for circuit simulations. The schematic of Verilog-A transistor model is shown in Fig. 9. The lookup table is generated by extracting the model parameters based on TCAD simulations running at fine step drain-source voltage bias Vds and gate-source voltage bias Vgs range from 0 to 50 mV. This lookup table model consists of two-dimensional tables having the transfer characteristics Ids (Vds, Vgs), gate-source capacitance Cgs (Vds, Vgs), and gate-drain capacitances Cgd (Vds, Vgs) values. The device transient characteristics are obtained through charge models. The drain and source terminal charge (Qgs, Qgd) can be calculated by using Cgs and Cgd from lookup tables.

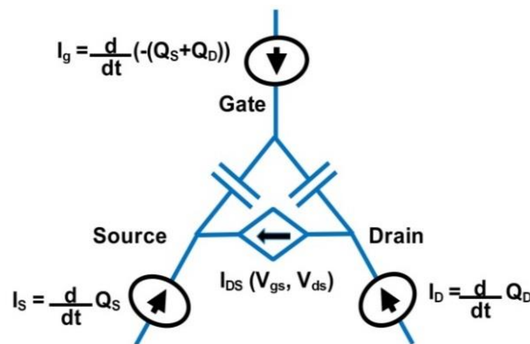
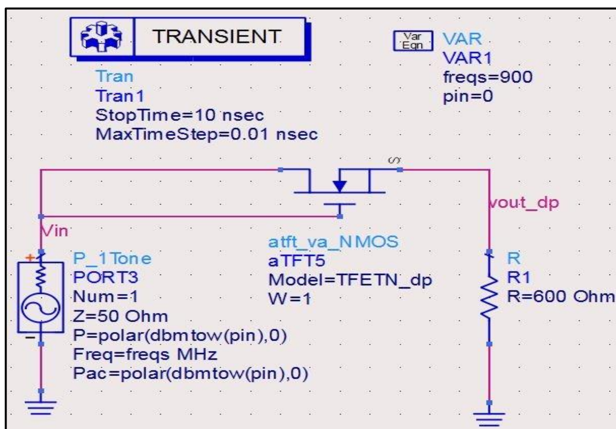
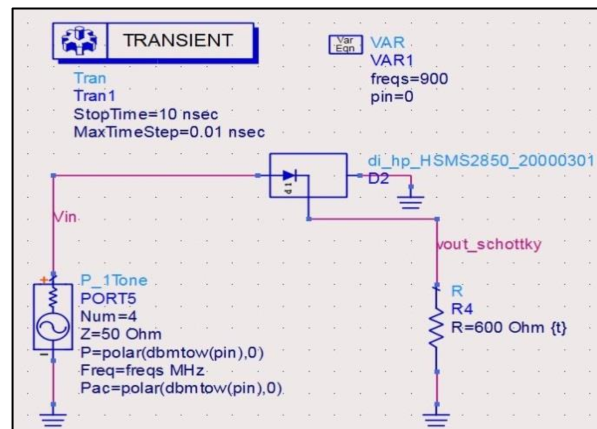


Fig. 9 Verilog-A TFET model Schematic

A simple half wave RF rectifier is designed by using Verilog A simulated III-V TFETs and Avago HSMS 2850 Schottky diode. The circuit consists of an RF power source input of 0 dBm at a frequency of 900 MHz is shown in Fig. 10. The RF rectifier circuit is simulated by using Advanced Design System (ADS) software which is a commercial tool for RF designers.



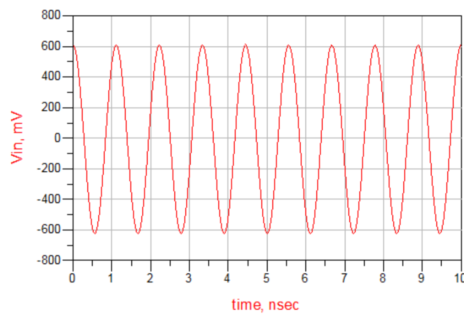
(a) Half wave RF rectifier using InAs/GaSb TFET



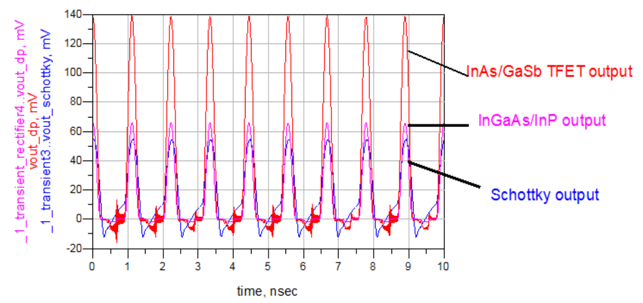
(b) Half wave RF rectifier using HSMS 2850 RF Schottky diode

Fig. 10 Schematic of Half-wave RF rectifier using Verilog-A InAs/GaSb TFET & HSMS 2850 RF schotky diode

The transistor can be operated as a diode by connecting a gate and drain terminal. Then, by doing a transient analysis of time around 10 ns, the simulated input and output waveforms of both circuits are shown in Fig. 11. The half-wave rectified dc output voltage of around 139 mV is obtained using InAs/GaSb, 63 mV by InGaAs/InP TFET and 58 mV obtained using HSMS 2850 schottky diode. The result shows that our simulated InAs/GaSb TFET is having potential opportunities for low power RF energy harvester applications.



(a) RF Input wave form at 900 MHz & 0 dBm

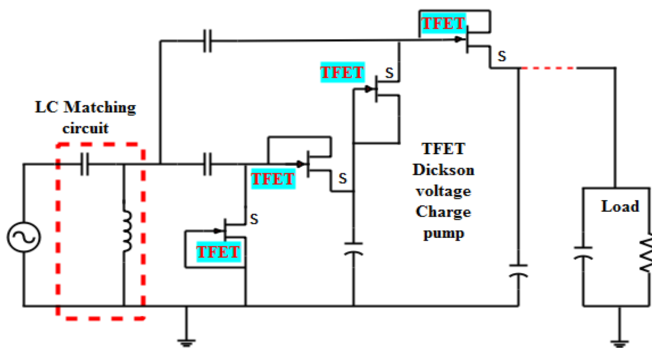


(b) Rectified output voltage of HTFETs & HSMS 2850

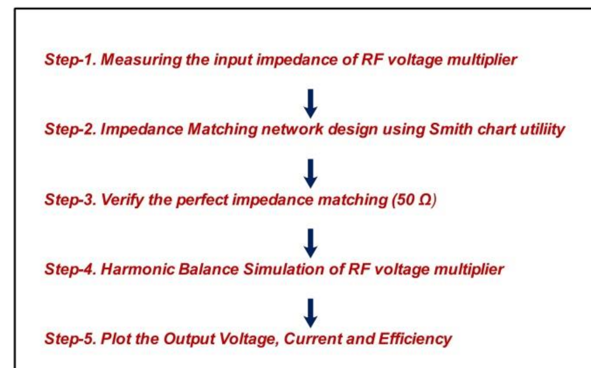
Fig. 11 Simulated Input and Output waveforms of Half-wave RF rectifier using Verilog-A HTFETs & HSMS 2850

4.1. Implementation of simulated HTFETs in RF Harvester Circuit

The general block diagram of RF energy harvester is shown in Fig. 12(a). It consists of receiving antenna as a source, impedance matching, and charge pump/voltage multiplier circuit. It is very challengeable to design when the harvester deals with very low RF power levels of less than 0 dBm available in the environment.



(a) Block diagram of RF energy harvester



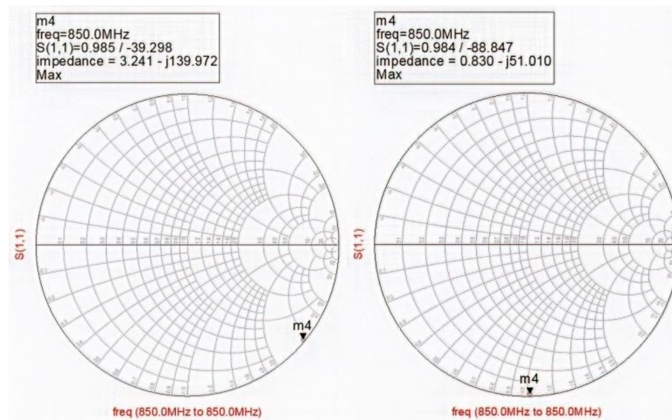
(b) Procedure to design TFET based RF Harvester

Fig. 12 General block diagram and the steps followed to design TFET based RF Harvester

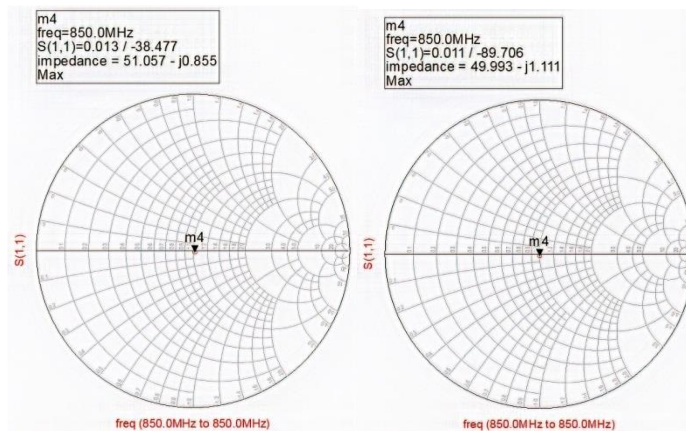
To design the RF harvester circuit, the design procedures to be followed exactly for efficient conversion of RF to DC output voltage. The steps involved in the Tunnel FET based RF harvester design using ADS software is shown in Fig. 12(b). Before going to the design steps, it was verified in the previous section that InAs/GaSb and InGaAs/InP TFETs can be modeled and operated as a diode in high-frequency input. In this work, the harvester operating frequency is set at 850 MHz for all the simulations because in most of the GSM mobile towers in Malaysia are sending the RF signal at this range only. The voltage multiplier is also known as the "charge pump" which is widely used in most of the Energy harvesting ICs. In this work, voltage multiplier made of Dickson topology connection is used for an improved DC output voltage. A two-stage TFET based Dickson voltage multiplier is proposed for minimizing the circuit size. The first stage of Dickson voltage multiplier is functioning as a rectifier only. To measure the input impedance of two-stage voltage multiplier, a port terminal impedance of 50 Ω is connected in both input and output of it. The S parameter simulator tool available in ADS software is used to find the input impedance value of it. By running an S parameter simulation at 850 MHz frequency, the input impedance value of two-stage voltage multiplier can be measured from the reflection coefficient S11 parameter which is shown in Fig. 13(a). The obtained values are 3.2-j140Ω and 0.83-j51Ω for InAs/GaSb and InGaAs/InP TFET based voltage multiplier circuits respectively. While measuring the input impedance value, we have considered the width of T1 = 40 um and T2 = 80 um.

In the second step, in order to transfer maximum power from receiving antenna source to voltage multiplier circuit, an LC impedance matching network is inserted in between antenna and voltage multiplier. Smith chart utility is one of the most practical and intuitive design tools which is available in ADS software, used to determine the impedance matching values.

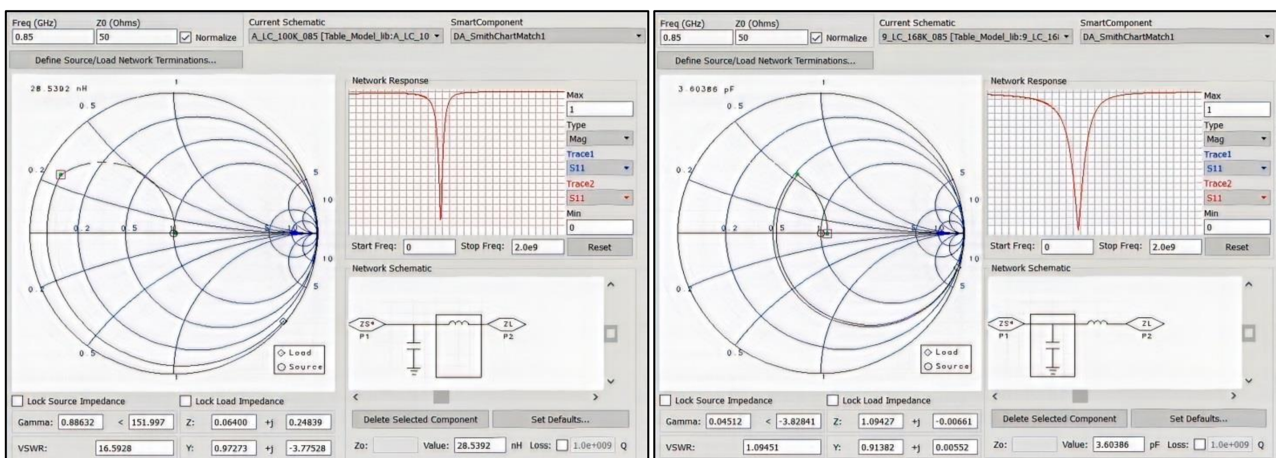
The obtained input impedance value of the voltage multiplier circuit from the first step is added into the smith chart tool as load impedance Z_{load}. The standard antenna impedance of 50 Ω is entered as source impedance Z_{source} on the smith chart. The schematic of the smith chart tool used in our design is shown in Fig. 13(c). The impedance matching values obtained by using smith chart for InAs/GaSb TFET based voltage multiplier are L= 28.53nH and C= 14.14pF. Similarly, we have obtained the impedance matching values for InGaAs/InP TFET based voltage multiplier circuits are L= 79.26nH and C= 3.60pF. It is necessary to verify that the whole RF harvester circuit impedance value should be around 50 Ω in the third step. This ensures that maximum power has been transferred from source to load. To verify it, again we need to measure the input impedance of the voltage multiplier with the addition of calculated LC matching elements between the source and load. It has been observed from Fig. 13(b) that the measured input impedance value with the inclusion of LC matching networks are 51.057-j0.855Ω and 49.99-j1.11Ω for InAs/GaSb and InGaAs/InP TFET based harvester circuits respectively.



(a) Measured input impedance value of InAs/GaSb and InGaAs/InP TFET based harvester circuit

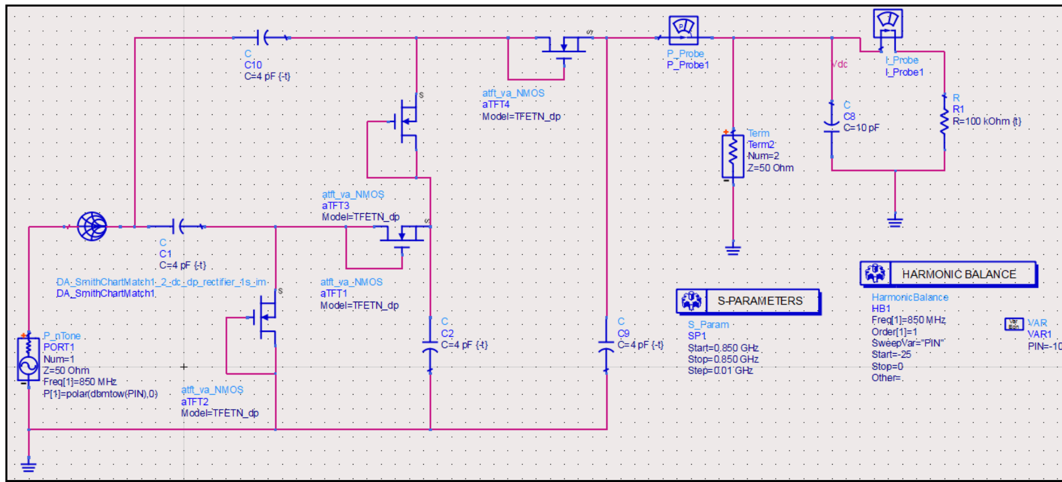


(b) Measured input impedance value of InAs/GaSb and InGaAs/InP TFET based harvester circuit with LC matching

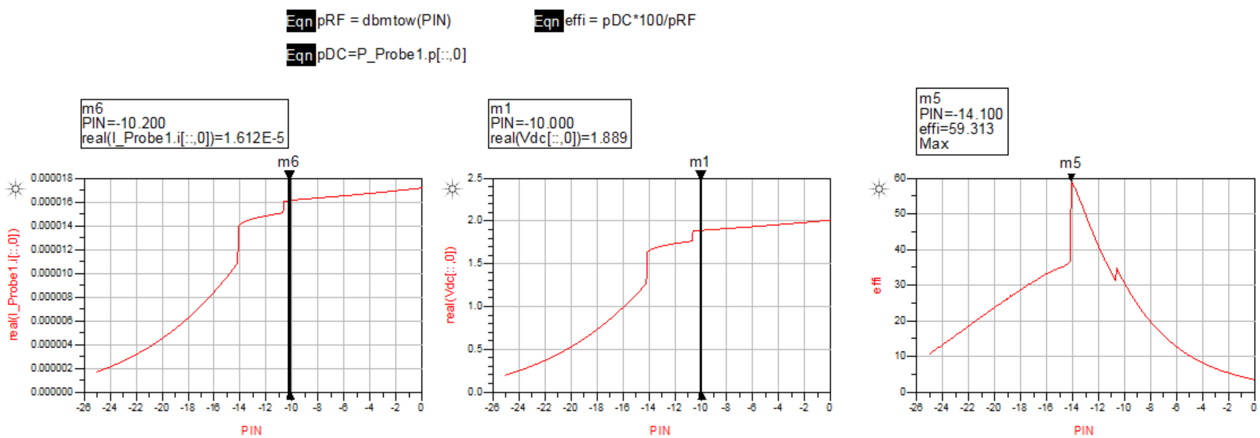


(c) Smith chart utility tool used to find LC matching values for InAs/GaSb and InGaAs/InP TFET based harvester circuit

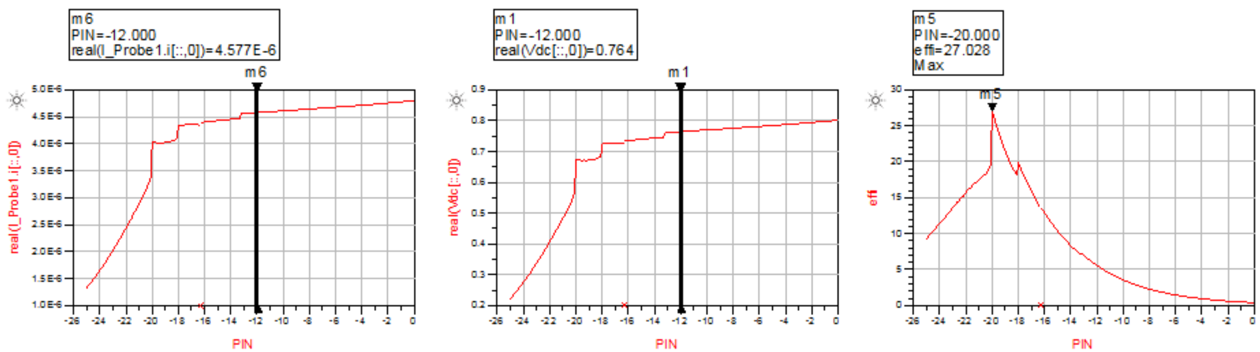
Fig. 13 Measured input impedance and smith chart tools used in the TFET based RF Harvester design



(a) Measured input impedance value of InAs/GaSb and InGaAs/InP TFET based harvester circuit



(b) Output results of current, voltage and efficiency of InAs/GaSb TFET based harvester circuit



(c) Output results of current, voltage and efficiency of InGaAs/InP TFET based harvester circuit

Fig. 14 Schematic design and DC output results of TFET based RF Harvester

Harmonic Balance (HB) simulation is a frequency domain analysis technique for simulating non-linear circuits and systems. It is most suitable for simulating analog, RF and microwave circuits since these circuits are handled mainly with frequency domain. HB simulation calculates the magnitude and phase of electrical parameters voltages or currents at many harmonically related frequencies for each fundamental signal under consideration on the non-linear circuit. It is an iterative method and obtains the steady-state solutions that can be approximated to satisfactory accuracy by means of finite Fourier series. Finally, the above HB simulation technique is applied in our RF harvester design for getting the DC output results. A single tone power source of 850 MHz is considered as an antenna source in this work. The ADS schematic design of TFET based harvester is shown in Fig. 14(a). By running HB simulations at 850 MHz, from 0 dBm to -25 dBm, the DC output results are obtained. As we have already discussed in the previous session that InAs/GaSb TFET has superior characteristics,

it can able to produce an output voltage of 1.9 V, a current of 16.1 μA @ 0 to -10 dBm which is shown in the Fig. 14(b). It can generate the maximum efficiency of 59 % @ -14 dBm at 100 kΩ loads with a sensitivity of -25 dBm. The comparative RF harvester simulation results are summarized in Table 4. Similarly, the InGaAs/InP TFET based RF harvester design generates the maximum efficiency of 27% @ -20dBm, 168 kΩ load with output voltage and current of 0.7 V and 4.5 μA @ 0 to -12dBm. The performance of InGaAs/InP TFET in RF harvester circuit is weak compared to InAs/GaSb TFET due to the formation of staggered band alignment design.

Table 4 Comparative summary of RF harvester simulation results using III-V TFETs

Reference/ Parameter	[28]	[29]	This Work	
Fabrication	0.18 μm CMOS	40nm CMOS	20nm InAs/GaSb HTFET	20nm InGaAs/InP HTFET
Device V_{th}	(EVC)	0.45V	0.075	0.128
Matching Network	LC Matching Network	LC Matching Network	LC Matching Network	LC Matching Network
Rectifier Topology	2-T Drive	Full wave Dickson	Dickson topology	Dickson topology
RF Frequency	145 MHZ	900 MHZ	850 MHZ	850 MHZ
RF input power/voltage	-18dBm	0.4 to 0.55 V	-25dBm to 0 dBm	-25dBm to 0 dBm
Output DC voltage	1 V	1.34 V	1.9 V, 16.1μA @ 0 to-10dBm	0.7V, 4.5μA @ 0 to -12dBm
PCE	25.87% @ -18dBm, 0.5μA	50% @ 12μA	59% @ -14 dBm, 100 kΩ load	27% @ -20 dBm, 168 kΩ load
Sensitivity	-22.5 dBm	0.39V	-25 dBm	-25 dBm
No. of stages	4	7	2	2

Then, in step II, the effect of the type of the carried cargo on the probability of theft was simulated. For this purpose, 10,000 transport cases, identical for each of the 12 types of cargo, were created. Based on the received data, it was possible to compare the impact of the cargo type on the probability of theft.

In step III, the costs of loss were calculated based on the appropriate algorithms. For variant I - a carriage without cargo monitoring systems and for variant II - a carriage with cargo monitoring systems, the cost of loss was calculated from Eq. (1).

5. Conclusions

In this paper, two different III-V material InAs/GaSb & InGaAs/InP based hetero-junction TFET has been designed and simulated by using Silvaco 2D Atlas simulator. The designed TFET devices have been investigated in terms of DC and analog/RF performance Figure of Merits (FOMs). It has been observed that InAs/GaSb HTFET has shown better performance in terms of SS, drain current, gate to drain capacitance and frequency compared to InGaAs/InP HTFET, due to the formation of broken gap alignment. To implement the above HTFETs in circuit-level simulation, a look-up table based Verilog A TFET model has been created. A two-stage Dickson voltage multiplier based RF harvester made of Verilog A HTFETs has designed and studied. The Harmonic Balance simulation of InAs/GaSb TFET based RF harvester operates at 850 MHz provides the DC output voltage of 1.9 V, output current of 16.1 ”μA @ 0 to -10 dBm. It can generate the maximum efficiency of 59 % @ -14 dBm at 100 kΩ loads with a sensitivity of -25 dBm. Hence based upon this simulation study, InAs/GaSb III-V material based TFET could be a future device for ultra-low power RF harvester circuits.

Conflicts of Interest

The authors declare no conflict of interest.

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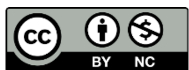

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