Design Feasibility and Prospect of High-Performance Sub-50-nm-Channel Silicon-on-Insulator Single-Gate SOI MOSFET

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Abstract

This paper describes advanced results of our evaluation of the minimum channel length (L_{min}). For the first time, we have added the constraint of subthreshold swing to that of threshold voltage, which has already been proposed. The L_{min} definition that includes the subthreshold swing constraint successfully yields a design guideline for low standby power applications, while the L_{min} definition based on the threshold voltage constraint does the same for high-speed applications. In contrast to previous predictions, simulation results indicate that the planar single-gate SOI MOSFET promises better performance, clearing the ITRS roadmap until at least 2007 for low standby power applications.

Index terms: SOI MOSFET, planar, single gate, minimum channel, ITRS road map, high speed, low standby power

1. Introduction

The aggressive down-scaling of MOSFET's is being continuously pushed in order to realize advanced applications that will better conform with social demands. However, contemporary down-scaling raises various issues that must be addressed, such as short-channel effects[1], significant gate leakage[2], and various parasitic drawbacks, including inevitable large gate fringing capacitance[3]. In an attempt to overcome most of these difficulties, attention is being focused on the SOI MOSFET[4]. The SOI MOSFET can reduce source and drain parasitic capacitances since it replaces the semiconductor-depletion region with a low-k insulator[5]. In addition, the SOI MOSFET has significant benefits such as low-power consumption, low-threshold voltage, steep subthreshold swing, and radiation hardness[4].

The recent ITRS roadmap[6] describes that conventional planar single-gate (SG) SOI MOSFET technology cannot be applied to device generation beyond the 50-nm node, but we note that the technical discussion of this issue is still at the drawing-board stage. One of the authors (Omura) has already studied whether or not the sub-50-nm-channel SG SOI MOSFET is promising with regard to future applications[7, 8]; this research has predicted that 20-nm-channel SG SOI MOSFETs will indeed support high-speed applications[7]. The previous papers introduced an SG SOI MOSFET design guideline that was based on a model of minimum

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channel length (L_{min})[7], but support for various applications was not addressed comprehensively. The previous model for L_{min} was constructed on the basis of the results of many simulations conducted from the viewpoint of high-end applications. However, we should reconsider the latest guidance because a low-standby power design guideline is urgently needed for many portable applications.

In this paper, we propose an advanced design guideline for sub-50-nm-channel planar SG SOI MOSFET's. For the first time, we have taken into account the lateral diffusion length of source and drain diffusion (L_{ld}), because it plays a significant role in suppressing the short-channel effect[9]. We used a 2-D device simulator (*Synopsis-DESSIS*[10]) with a hydrodynamic transport model. We propose new models for minimum channel length from the viewpoint of subthreshold swing control-in other words, low-standby power designs. In addition, we address the problem of how to design high-performance sub-50-nm channel SG SOI MOSFET's that have low-standby power consumption. Intrinsic delay time and power-delay product are also discussed, using many simulation results. It is demonstrated that, in contrast to previous predictions, sub-50-nm channel SG SOI MOSFET's retain their attraction for many applications.

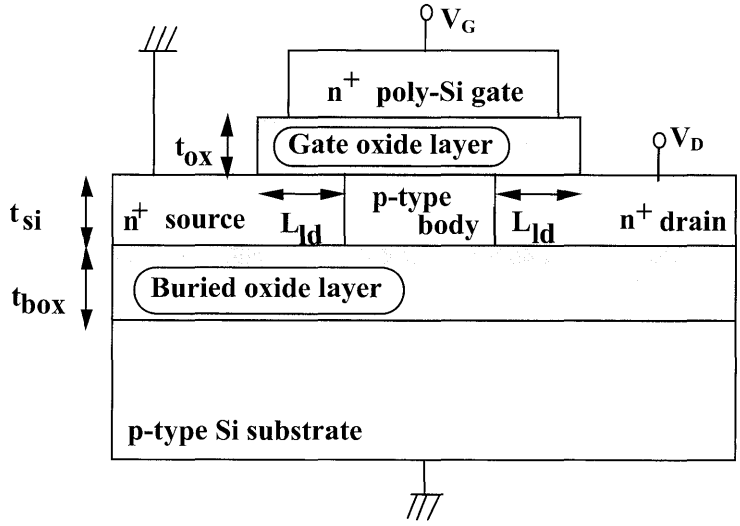

Fig. 1 Schematic device structure assumed.

Table 1. Device parameters assumed in the simulations.

Device parameters	Values [unit]
Gate oxide thickness, t_{ox}	2 - 5 [nm]
SOI layer thickness, t_{si}	5 - 30 [nm]
Buried oxide layer thickness, t_{box}	10 - 100 [nm]
SOI doping concentration, N_A	$3x10^{15}$ - $1x10^{18}$ [cm^{-3}]
Lateral diffusion length, L_{ld}	5 - 30 [nm]
Substrate doping concentration, N_{sub}	$3x10^{17}$ [cm^{-3}]
Source/drain doping concentration, $N_{S/D}$	$4x10^{20}$ [cm^{-3}]
Gate poly-Si doping concentration, $N_{S/D}$	$4x10^{20}$ [cm^{-3}]

2. DEVICE STRUCTURE AND SIMULATIONS

The device structure assumed here is the fully-depleted (FD) SG n-channel SOI MOSFET shown in Fig.1. Device parameter values are given in Table 1. In the simulations, the channel length (L) is changed from 10 nm to 200 nm, the gate oxide thickness (t_{ox}) from 2 nm[11] to 5 nm, the buried oxide thickness (t_{BOX}) from 10 nm to 100 nm[12], the SOI doping (N_A) from $3\text{x}10^{15}$ cm^{-3} to $1\text{x}10^{18}$ cm^{-3}, and the lateral diffusion length (L_{ld}) from 5 nm to 30 nm. We assumed that the minimum value of SOI layer thickness is 5 nm, which obviates the need to consider distinct quantum-mechanical effects. A hydrodynamic transport model is assumed in the simulations. We did not consider sub-2-nm-thick gate oxide (or EOT), because the SOI MOSFET has a design margin in terms of suppressing short-channel effects[11]. It is assumed, for simplicity's sake, that the lateral out-diffusion of impurities from the source and drain region is Gaussian. All device characteristics were calculated at the drain voltage (V_D) of 1V. We extracted threshold voltage (V_{th}) and sub-threshold swing (S) from the simulation results; the threshold voltage is defined as the gate voltage at which the drain current is $(W/L)10^{-7}$ A. The minimum channel length (L_{min}) means effective channel length in this paper.

The minimum channel length (L_{min}) was extracted in the following two ways.

(i) *Extract-A* :

L_{min} is defined as the channel length at which the threshold voltage of the device is lower by 0.1V than that of a long-channel device (L=200nm). This approach was proposed by Kawamoto et al.[7].

(ii) *Extract-B* :

L_{min} is defined as the channel length at which the subthreshold swing is lower than a certain value.

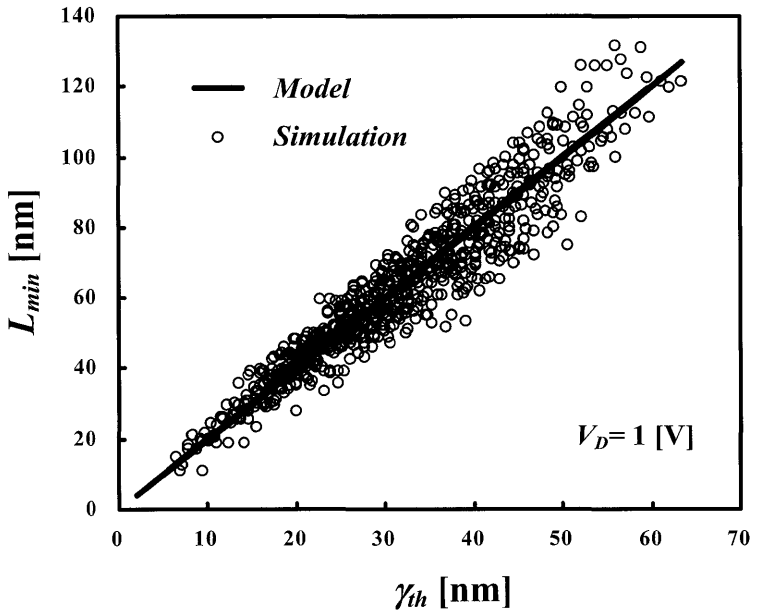

Fig. 2 L_{min} dependence on γ_{th} at V_D= 1 V using *Extract-A* (ΔV_{th}= 0.1 V). Solid line/symbols denote the model/simulation results.

3. PROPOSED MODEL FOR MINIMUM CHANNEL LENGTH

3.1 Minimum channel length model constructed using Extract-A

αWe investigated the L_{min} dependence on individual device parameters. Since the previous model[7] used a complex function of device parameters, we tried to simplify the model. We obtained the following new expressions:

$$\gamma_{th} = \beta_{th} \cdot I_n\left(\frac{N_A}{\alpha}\right) + 3.8 \cdot t_{ox} + 1.3 \cdot t_{si} + 0.13 \cdot t_{box} - 0.46 \cdot L_{ld} + \sigma_{th}, \quad (1)$$

$$L_{min} = 2 \cdot \gamma_{th}, \quad (2)$$

where γ_{th} and L_{min} are given in nm units, and we assume that α= 1 cm^{-3}, β_{th} = 1.3 nm, δ_{th} = -46 nm. N_A is in units of cm^{-3}. The other device parameters are given in nm units. The curve produced by Eq. (2) is shown in Fig. 2, where the simulation results are also plotted for comparison. We can see there is a good agreement between the simulation results and the model curve (Eq. (2)). Thus a model equation (2) can yield the design guideline for device construction. In contradiction to the previous prediction[7], it should be noted that we can realize a 10-nm channel SG SOI MOSFET by optimizing the device parameters. The performance that can be realized using *Extract-A* will be discussed later in detail.

Table 2. Constant values used in the model.

Constants	Values
P_1	2.91x10^{-2} [nm]
P_2	3.59x19^{-2} [dec/mV]
P_3	-1.65x10^{-1} [dec/mV]
P_4	-1.00x10^{-4} [(dec/mV)^2]
P_5	2.14x10^{-2} [dec/mV]
P_6	-3.76x10^{-2} [dec/mV]
P_7	1.00x10^{-4} [(dec/mV)^2]
P_8	-3.01x10^{-2} [dec/mV]
P_9	-8.08x10^{-1} [dec/mV]

3.2 Minimum channel length model constructed using *Extract-B*

In the present paper, we consider how low-standby power LSI's can be designed. Since the low-standby power operation of these devices is primarily conditioned by subthreshold swing, we must determine the maximal swing value (S_{max}) so that the low-standby power performance can be reproduced. For the engineers' convenience, we derived the following useful expression for L_{min}.

$$\gamma_s = C_{NA} \cdot I_n\left(\frac{N_A}{\alpha}\right) + C_{tox} \cdot t_{ox} + C_{tsi} \cdot t_{si} + C_{tbox} \cdot t_{box} + C_{Lld} \cdot L_{ld} + C_\delta, \quad (3)$$

$$L_{min} = 2 \cdot \gamma_S, \quad (4)$$

where $\alpha = 1$ [cm^{-3}] *and* C_{NA}, C_{tox}, C_{tsi}, C_{tBOX},, C_{Lld} and C_{δ} are parameters depending on the maximal S value (S_{max}) allowed in the device design. These parameters are given by

$$C_{NA} = P_1 \cdot \exp(P_2 \cdot S_{max}) , \quad (5\,a)$$
$$C_{tox} = P_3 \cdot S_{max} + 18.5 , \quad (5\,b)$$
$$C_{tsi} = P_6 \cdot S_{max} + 4.89 , \quad (5\,c)$$
$$C_{tbox} = P_4 \cdot S_{max}^{\ 2} + P_5 \cdot S_{max} - 9.19 \times 10^{-1} , \quad (5\,d)$$
$$C_{Lld} = P_7 \cdot S_{max}^{\ 2} + P_8 \cdot S_{max} + 1.02 , \quad (5\,e)$$
$$C_{\delta} = P_9 \cdot S_{max} + 46.1 , \quad (5\,f)$$

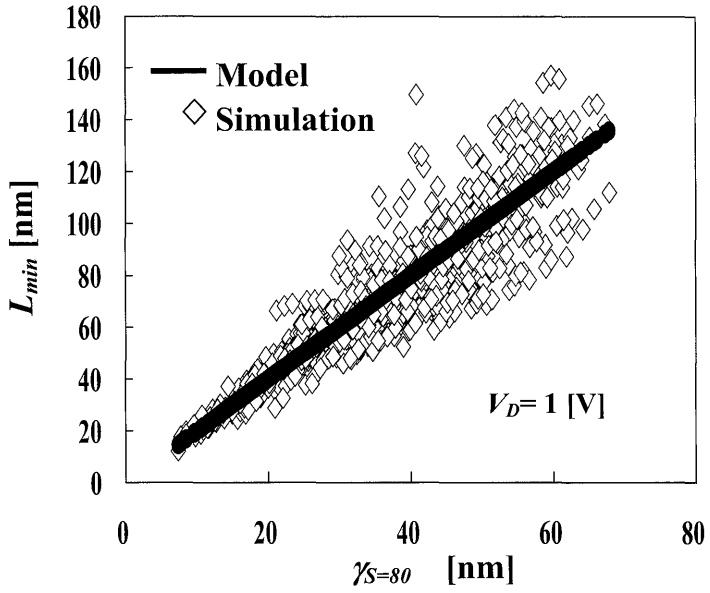

Fig. 3 L_{min} dependence on γ_{th} at V_D= 1 V using *Extract-B* (S_{max}= 80 mV/dec). Solid line/symbols denote the model/simulation results.

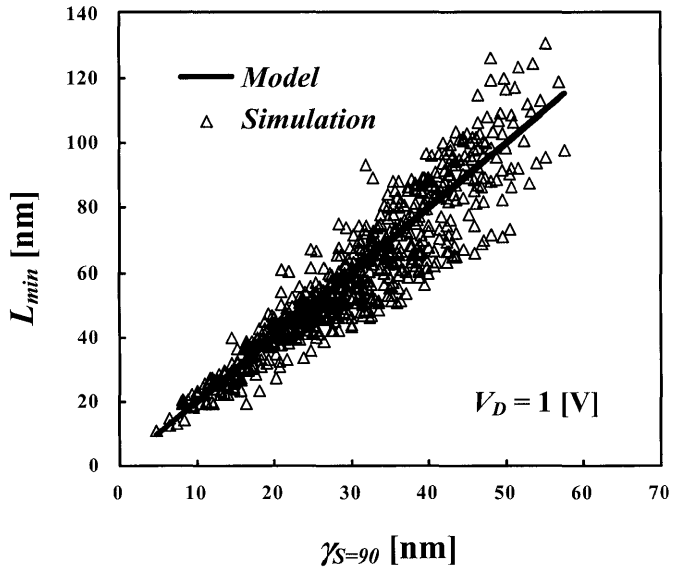

Fig. 4 L_{min} dependence on γ_{th} at V_D= 1 V using *Extract-B* (S_{max}= 90 mV/dec). Solid line/symbols denote the model/simulation results.

where P_1 to P_9 are constants (see Table 2).

The dependency of L_{min} on γ_S for various S_{max} values is shown in Figs. 3 and 4. It can be seen that model equations (3) to (5) successfully reproduce the simulation results. It should be noted that we can realize a 20-nm channel SG SOI MOSFET with S_{max}= 80 mV/dec for low-standby power applications by optimizing the device parameters. In a similar manner, a 10-nm channel SG SOI MOSFET with S_{max} = 90 mV/dec can also be realized. These results are the first confirmation of this level of design optimization.

4. PERFORMANCE PROSPECTS OF SCALED SOI MOSFETs

We statistically analyzed L_{min} dependencies of drive current (I_{on}), intrinsic delay time (τ), standby leakage current (I_{off}) and delay-time (τ)-power dissipation (P_D) product (τP_D) in order to examine the performance prospect of SG SOI MOSFETs with minimum channel length (L_{min}). A comparison of simulation results with the 2003 ITRS roadmap[13] yields a couple of new findings on the potential of the SG SOI MOSFET. In all figures, we assumed V_D = 1 V, V_G = 1 V and V_{th} = 0.1 V or 0.3 V.

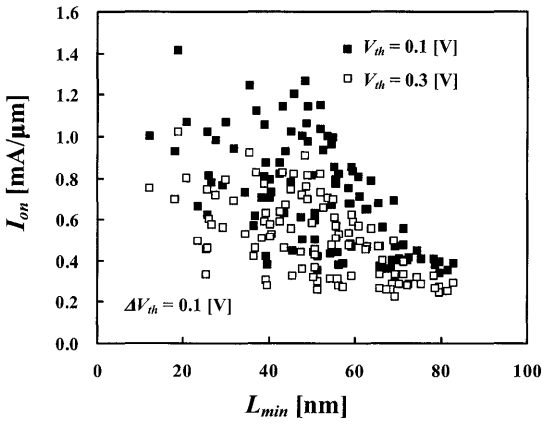

Fig. 5 Drive current (I_{on}) dependence on L_{min} at V_D= 1 V using *Extract-A* (Δ V_{th}= 0.1 V) for various threshold voltages.

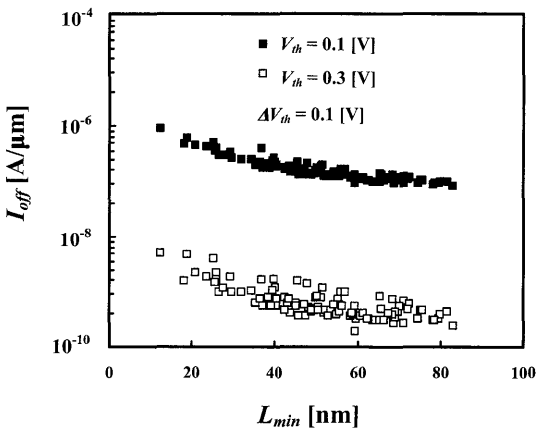

Fig. 6 Standby leakage current (I_{off}) dependence on L_{min} at V_D= 1 V using *Extract-A* (ΔV_{th}= 0.1 V) for various threshold voltages.

4.1 Dynamic operation characteristics of scaled SG SOI MOSFETs

In this section, we consider the impact of *Extract-A* on L_{min} control with regard to a comprehensive performance analysis of scaled SG SOI MOSFETs. First we show on-current (I_{on}) in Fig. 5 and off-leakage current (I_{off}) in Fig. 6 as functions of L_{min}. In Fig. 5, as expected, I_{on} increases as L_{min} decreases. It can be seen that there are many ways (many device parameter choices) to realize the maximal I_d when a certain L_{min} value is assumed. On the other hand, it should also be noted that the distribution of I_{on} values for V_{th} = 0.1 V and that of I_{on} values for V_{th} = 0.3 V overlap widely, which suggests that intrinsic delay times of devices with V_{th} = 0.1 V or 0.3 V are almost identical. In Fig. 6, as expected, it is seen that I_{off} depends strongly on V_{th}. We can extract the following empirical equation from Fig. 6.

$$I_{off} = I_L 10^{Vth/SS} Lmin^{\sigma th}, \quad (6)$$

where I_L is the constant value of leakage current, SS is the subthreshold swing, and parameter σ_{th} = -6/5 and -7/5 for V_{th} = 0.1 and 0.3 [V], respectively. From the viewpoint of estimating the standby power dissipation, we should note that the L_{min} dependence of I_{off} is steeper than first expected.

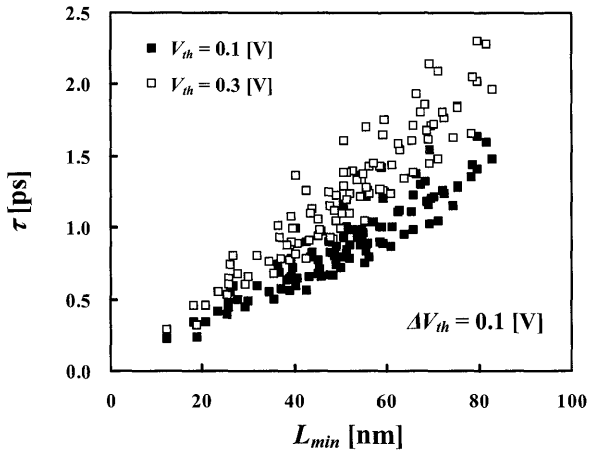

Fig. 7 Intrinsic delay time (τ) dependence on L_{min} at V_D= 1 V using *Extract-A* (ΔV_{th}= 0.1 V) for various threshold voltages.

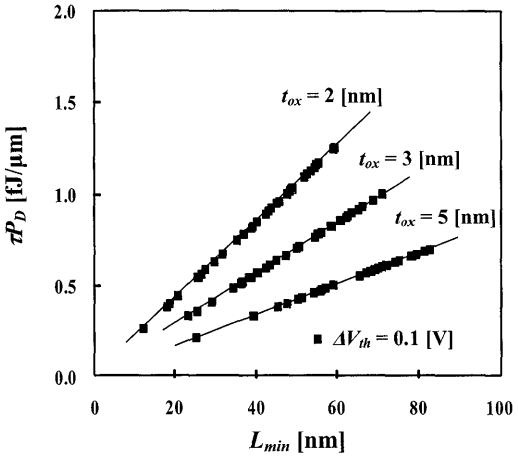

Fig. 8 Dissipation-power-delay time product (τP_D) dependence on L_{min} at V_D= 1 V using *Extract-A* (ΔV_{th}= 0.1 V) for the threshold voltage of 0.3 V.

Fig.7 shows the intrinsic delay time (τ) dependence on L_{min} at V_D = 1 V, where $\tau = C_G V_G / I_{on}$ and C_G is the physical gate oxide capacitance. From Fig. 7, we can see that, because of the increase in I_{on}, τ decreases as L_{min} decreases, and that the requirement of small τ is not always satisfied simply by tuning the threshold voltage. Since, in practice, scaled SOI MOSFETs have a relatively large fringe capacitance and overlap capacitance, we should reconsider the practical usefulness of τ calculated simply from simulation results.

The dissipation power-delay product (τP_D) is often used in estimating the power efficiency of a device. We show the dependence of τP_D on L_{min} at V_D = 1 V in Fig. 8 using data extracted from simulation results following *Extract-A*; τP_D is normalized by channel width. τP_D is proportional to L_{min}, and inversely proportional to t_{ox}. This is because τP_D is expressed by $C_G V_G^2$ in the present consideration. Curves show that τP_D decreases as t_{ox} increases because the total charge required in switching decreases with increase in t_{ox}, while τ itself increases because I_{on} decreases.

Now, we will discuss the performance prospects of scaled SG SOI MOSFETs on the basis of the simulation results shown above. Simulated parameters are compared to the ITRS roadmap 2003[13] (see Figs. 9 and 10); physical L_{gate} is equal to L_{min} +2L_{ld} +2 nm; and threshold voltage is made to match the roadmap value by adjusting the work function of the gate electrode (see Table 3). V_G and V_D are assumed to be 1.0 V in the simulations, while they range from 1.0 V to 1.1 V in the 2003 ITRS roadmap. Simulated values and roadmap requirements for I_{on} and I_{off} are compared in Fig. 9. '*Simulation-A*' shows values for the case of t_{ox}= 2 nm (SiO_2) and '*Simulation-B*' shows values for the case of EOT= 1 nm. Simulated I_{on} values for EOT= 2 nm are lower than the roadmap requirement, while simulated

Table 3. Possible device parameters for each technology node (Figs. 9 and 10).

Tech. node	L_{min} [nm]	t_{si} [nm]	N_A [cm-3]	t_{ox} [nm]	t_{box} [nm]	L_{ld} [nm]
A	30	5	$3x10^{17}$	2	10	10
B	26	5	$3x10^{15}$	2	100	30
C	24	5	$3x10^{15}$	3	50	30
D	21	10	$3x10^{15}$	2	10	30
E	18	5	$3x10^{17}$	2	10	30

I_{off} satisfies the roadmap requirement to 2007. Lower values of simulated I_{on} result from a thicker gate SiO_2 film (2 nm)[11]. Of course, sub-2-nm-thick EOT (effective oxide thickness) is possible when a high-k material is employed[14]. We investigated the impact of EOT on device performance and evaluated the performance (I_{on}) of the device with an EOT of 1 nm (high-k insulator with a permittivity of 15.6 ε_0[15]) as compared with that with an EOT of 2 nm (2-nm-thick SiO_2 film). Simulation results of I_{on} for EOT of 1 nm are denoted by the broken line with closed squares in Fig. 9. They almost satisfy the ITRS roadmap requirement. As a result,

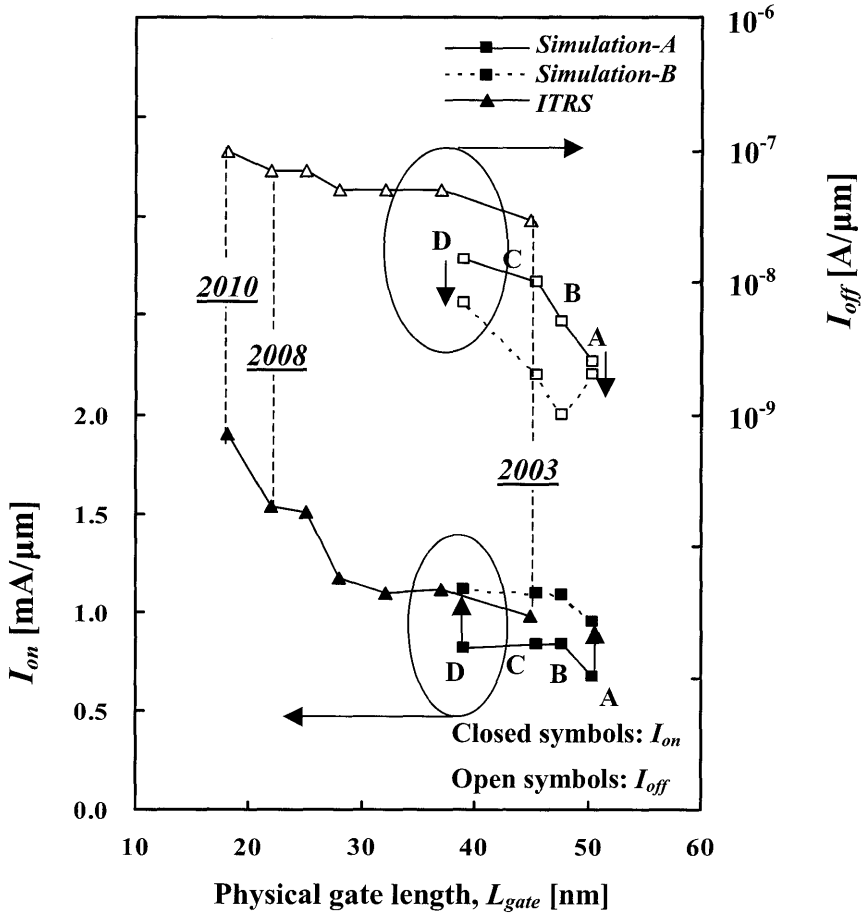

Fig. 9 Comparison of simulated I_{on} and I_{off} values with the 2003 ITRS roadmap 2003 using *Extract-A*. This illustration shows a potential of single-gate SOI MOSFET. In addition, simulated I_{on} and I_{off} values for assuming a high-k gate insulator are also shown. '*Simulation-A*' : t_{ox}= 2 nm and '*Smulation-B*' : EOT= 1 nm.

it is suggested that the condition of EOT < 2 nm is more or less appropriate without making any changes in other device parameters. In contrast to I_{on}, the I_{off} is drastically improved by using a high-k gate insulator, because the subthreshold swing is sharpened. It is expected that the I_{off} values will satisfy the roadmap requirement until at least 2010.

Simulated values and roadmap requirements of τ and τP_D are compared in Fig. 10. All simulated values of τ more or less match the roadmap requirements, but simulated values of τP_D are much lower than the roadmap requirements. Thus we identified possible device parameters for high performance (HP) applications. Table 3 shows the extracted device parameters for each technology node shown in Figs. 9 and 10. It should be noted that a large L_{ld} value ranging from 10 nm to 30 nm is required – much larger than first expected. As shown in Table 3, a very thin SOI layer of 5 nm is required in realizing HP applications, for the short-channel effects must be sufficiently suppressed. In addition, fairly thin buried oxide layer, ranging from 10 nm to sub-100 nm, is assumed in the simulations. This suggests that a thinner gate EOT is required, for the 2003 ITRS roadmap assumes a 100-nm-thick buried oxide layer[13]. However, the present practical requirement is not satisfied with the use of a high-k gate insulator if we need a higher I_{on}. As shown in Fig. 10, the high-k insulator used for the

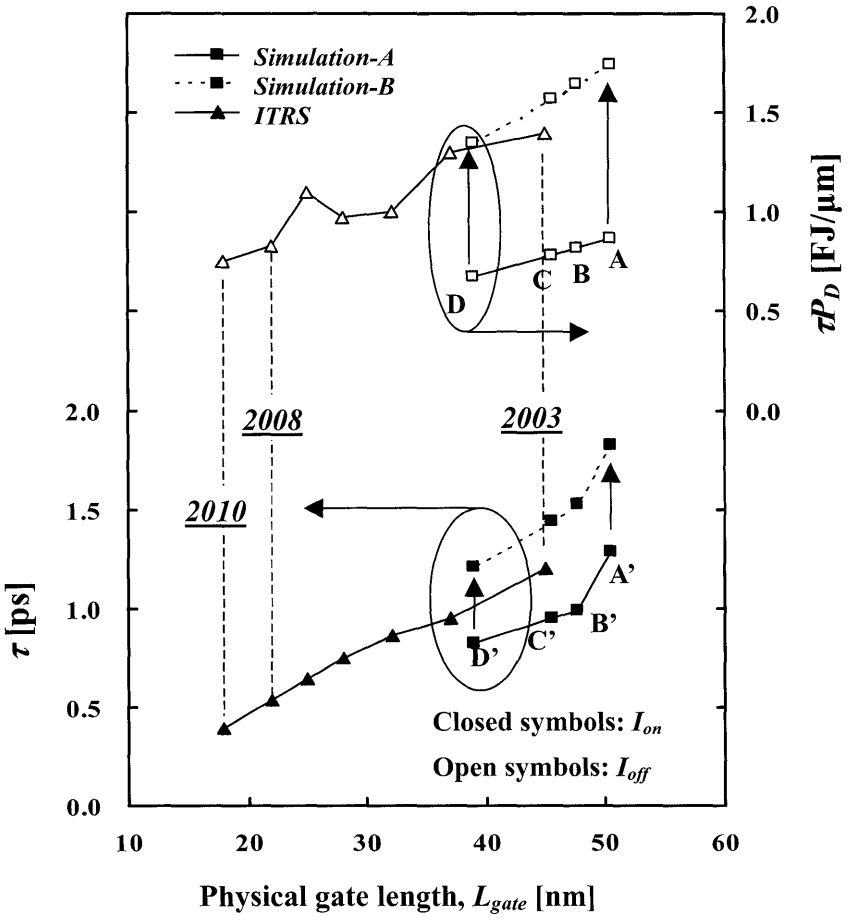

Fig. 10 Comparison of simulated τ and τP_D values with 2003 ITRS roadmap using *Extract-A*. This illustration shows the potential of the single-gate SOI MOSFET. Simulated τ and τP_D values assuming a high-k gate insulator are also shown.

Table 4. Possible device parameters for each technology node (Figs. 9 and 10).

Tech. node	L_{gate} [nm]	t_{si} [nm]	N_A [cm-3]	t_{ox} [nm]	t_{box} [nm]	L_{ld} [nm]	WF[eV]
A	52	5	$3x10^{17}$	2	10	20	5.2
B	45	5	$3x10^{17}$	2	20	20	5.2
C	39	10	$3x10^{15}$	2	50	20	5.3
D	32	5	$3x10^{15}$	2	20	20	5.2

gate insulator does not contribute to the high-speed shift because it enhances the contribution of the inversion layer capacitance, hindering improvement in I_{on} and causing degradation in τ. In order to improve the switching speed, we have to introduce an underlapped source and drain structure: this maximizes I_{on} and minimizes the fringing capacitance[16].

We can see from Fig. 10 that the SG SOI MOSFET still has the potential to support HP and low operation power (LOP) applications. However, strained-Si-on-insulator (sSOI)[17] or germanium-on-insulator (GOI)[18] will be required after the limits of the silicon-based SG SOI MOSFET are reached.

4.2 Trade-off and optimization of standby power consumption and dynamic operation

In the previous section, we discussed the design feasibility of scaled SG SOI MOSFETs using *Extract-A*. It was demonstrated that *Extract-A* makes it possible to design devices for HP applications. In this section, we will discuss the simulation results obtained by *Extract-B*; we illustrate on-current (I_{on}) in Fig. 11 and off-leakage current (I_{off}) in Fig. 12 as functions of L_{min}. In Fig. 11, as expected, I_{on} increases as L_{min} decreases regardless of the S_{max} value. It can be seen that there are many ways (many device parameter choices) by which to realize the maximal I_{on} when a certain L_{min} value is assumed; the threshold voltage is also a parameter to

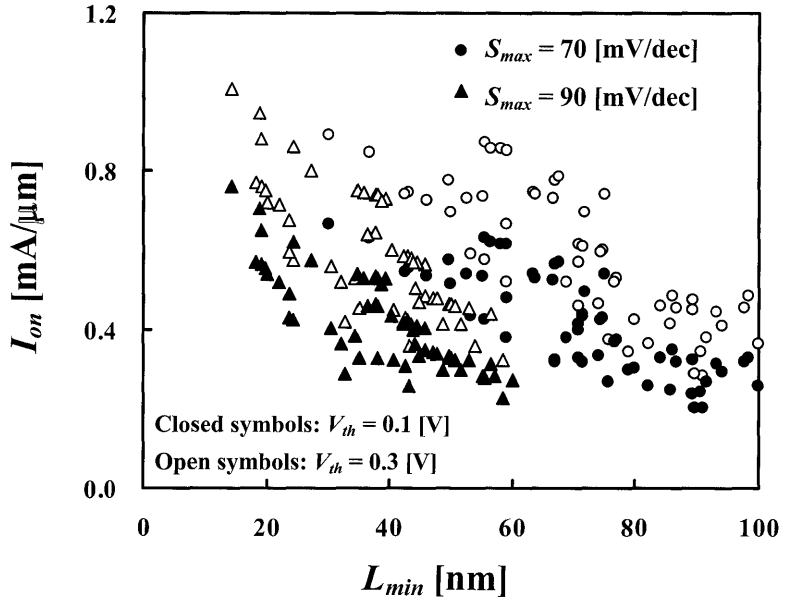

Fig. 11 Drive current (I_{on}) dependence on L_{mi} at V_D= 1 V using *Extract-B* (S_{max} = 70 and 90 mV/dec) for various threshold voltages.

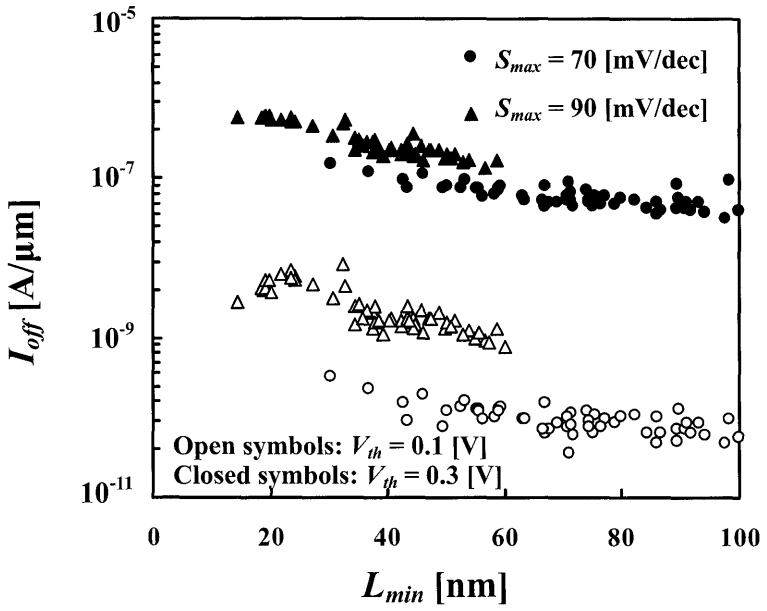

Fig. 12 Standby leakage current (I_{off}) dependence on L_{min} at V_D= 1 V using *Extract-B* (S_{max} = 70 and 90 mV/dec) for various threshold voltages.

be assumed. It should also be noted that, in contrast to *Extract-A*, the distribution of I_{on} values for S_{max}= 70 mV/dec and that of I_{on} values for S_{max}= 90 mV/dec do not significantly overlap (see Fig. 5), which suggests that the intrinsic delay times of devices with S_{max}= 70 mV/dec differ from those with 90 mV/dec. In Fig. 12, it is seen that, as expected, I_{off} depends strongly on both S_{max} and V_{th}. We can extract the following empirical equation from Fig. 12:

$$I_{off} = I_L 10^{-Vth/SS} L_{min}^{ss}, \quad (7)$$

where we assume parameter σ_S= -1.0 and -6/5 for V_{th}= 0.1 and 0.3 V, respectively, and S= 70 mV/dec. On the other hand, σ_S= -6/5 and -7/5 for V_{th}= 0.1 and 0.3 V, respectively, and S= 90 mV/dec. We should note that a small swing value makes the standby leakage current relatively insensitive to L_{min}.

Fig. 13 shows the intrinsic delay time (τ) dependence on L_{min} at V_D = 1 V with parameters of V_{th} and S_{max}. From Fig. 13, we can see that τ decreases as L_{min} decreases because of the increase in I_{on}, and that the requirement of small τ is not always satisfied if we restrict ourselves to merely tuning the threshold voltage as mentioned previously.

The dissipation power-delay product (τP_D) is often used in estimating the power efficiency of a device. We show the τP_D dependence on L_{min} at V_D = 1 V in Fig. 14 using data extracted from simulation results obtained using *Extract-B*. τP_D is normalized by channel width and is proportional to L_{min}, while being inversely proportional to t_{ox}. This is because τP_D is expressed by $C_G V_G^2$ in the present analysis. Curves show that τP_D decreases as t_{ox} increases because the total charge required in switching decreases as t_{ox} increases, while τ itself increases because I_{on} decreases. The salient point is that a large S_{max} value yields a small τP_d value.

We shall now discuss the performance prospect of scaled SG SOI MOSFET on the basis of simulation results shown above using (*Extract-B*). Simulated parameters are compared to

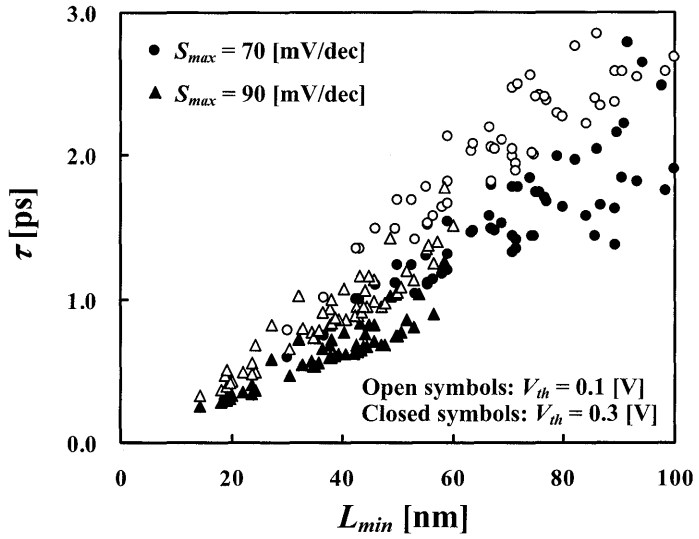

Fig. 13 Intrinsic delay time (τ) dependence on L_{min} at V_D= 1 V using *Extract-B* (S_{max} = 70 and 90 mV/dec) for various threshold voltages.

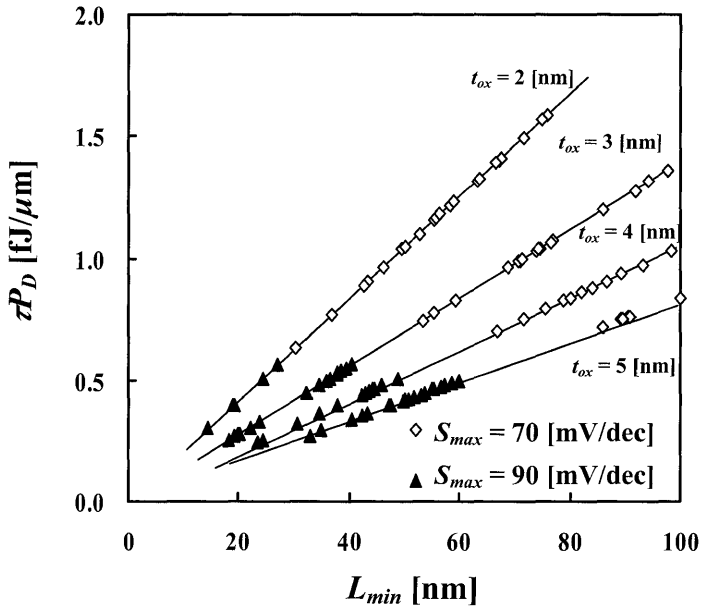

Fig. 14 Delay-time-dissipation-power product (τP_D) dependence on L_{min} at V_D= 1V using *Extract-B* (S_{max} = 70 and 90 mV/dec) for a threshold voltage of 0.3 V.

the ITRS roadmap 2003 (see Figs. 15 and 16); physical L_{gate} is equal to L_{min} +2L_{ld}+2 nm and threshold voltage is made to match the roadmap value by adjusting the work function of the gate electrode. Figures 15 and 16 were generated by assuming S_{max}= 70 mV/dec. V_G and V_D are both assumed to be 1.0 V in the simulations, while they range from 1.0 V to 1.2 V in the 2003 ITRS roadmap. The simulated values and roadmap requirements for I_{on} and I_{off} are compared in Fig. 15; all simulated I_{on} values are lower than the roadmap requirement after

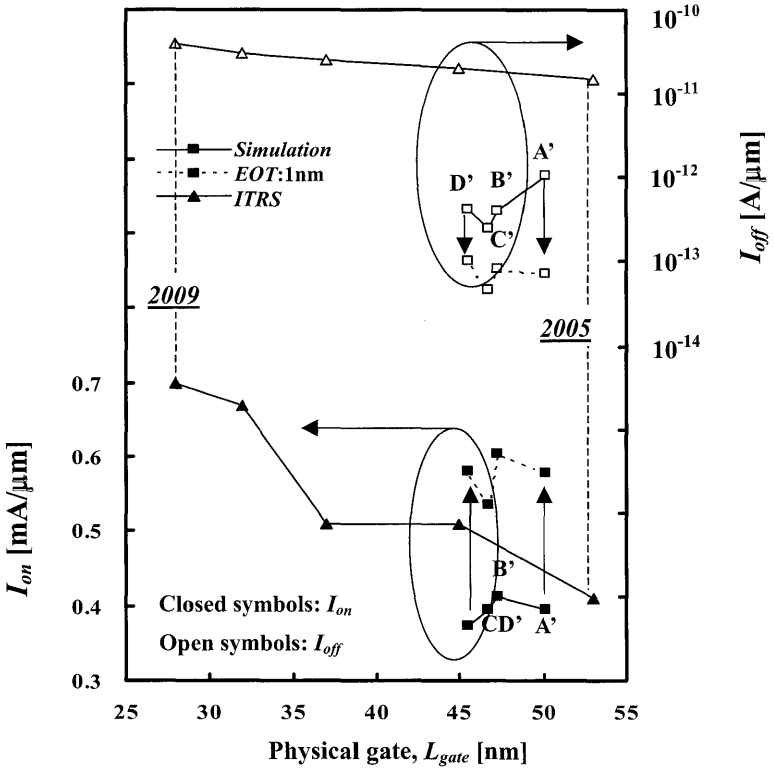

Fig. 15 Comparison of simulated I_{on} and I_{off} values with the 2003 ITRS roadmap 2003 using *Extract-B* (S_{max}= 80 mV/dec.). This viewgraph shows the potential of the single-gate SOI MOSFET. Simulated I_{on} and I_{off} values assuming high-k gate insulator are also shown.

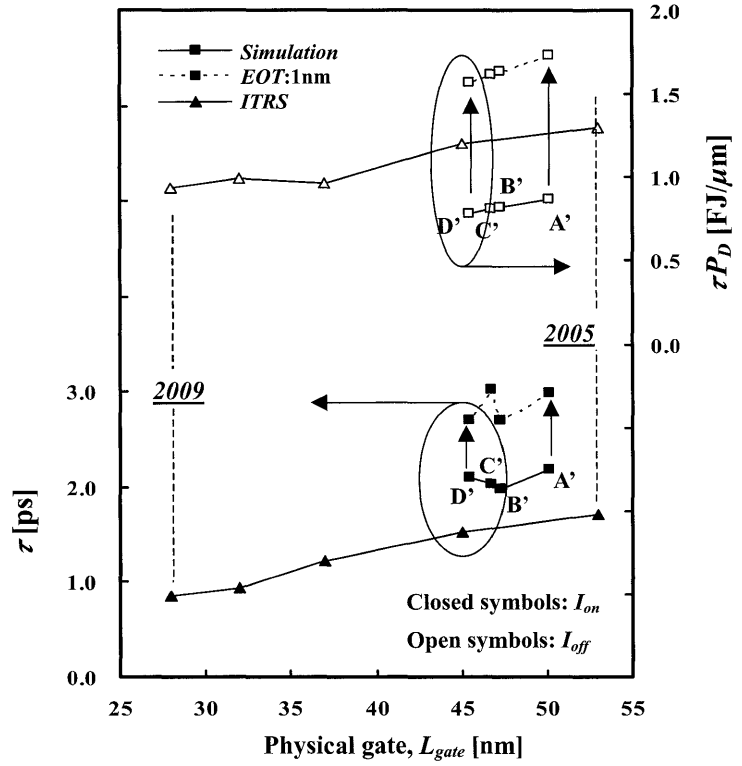

Fig. 16 Comparison of simulated τ and τP_D values with the 2003 ITRS roadmap using *Extract-B* (S_{max}= 80 mV/dec.). This illustration shows the potential of a single-gate SOI MOSFET. In addition, simulated τ and τP_D values assuming a high-k gate insulator are also shown.

2005, while simulated I_{off} satisfies the roadmap requirement until at least 2009. Lower values of simulated I_{on} result from a thicker gate SiO_2 film (2 nm)[11]; of course, sub-2-nm-thick EOT (effective oxide thickness) is possible when a high-k material is employed[14]. The potential for using a high-k gate insulator with a permittivity of 15.6 ε_0[15] is examined in Fig. 15, where simulation results for I_{on} are denoted by the broken line. The high-k insulator contributes to the increase in I_{on}; and I_{on} values for devices with the high-k insulator match the roadmap requirement, which is different from the result seen in Fig. 9. In addition, I_{off} is considerably improved by use of the high-k gate insulator because the subthreshold swing is sharpened. I_{off} values satisfy the roadmap requirement until at least 2009.

Simulated values and roadmap requirements of τ and τP_D are compared in Fig. 16. All simulated values of τ are greater than the roadmap requirements, while all simulated values of τP_D are much lower than the roadmap requirements. Accordingly, we extracted possible device parameters for low-standby power (LSTP) applications. Table 4 lists the extracted device parameters for each technology node shown in Figs. 15 and 16. It should be noted that a larger-than-expected L_{id} value of 20 nm is required, and we should reconsider the source-drain engineering in order to minimize the switching time[16]. Because the short-channel effects must be sufficiently suppressed, a very thin SOI layer of 5 nm is required to realize LSTP applications. A moderately-thin buried oxide layer ranging from 10 nm to 50 nm is assumed in the simulations. Use of the high-k gate insulator allows a thicker buried oxide layer, which would match the roadmap requirement. When a thin buried oxide layer (sub-100 nm) is not allowed for reasons of ESD protection and other issues, a double-buried-insulator substrate[19] should be used. The double-buried insulator substrate has high potential with regard to robust circuit applications although the substrate would be more expensive than the present SOI substrate with a single buried insulator.

5. CONCLUSION

This paper considered an advanced methodology to extract the minimum channel length. A new approach to determining the minimum channel length has been proposed that is based on a specific restriction of subthreshold swing value. A comprehensive design guideline for scaled SG SOI MOSFETs was derived from the viewpoint of high-speed operation and low-power consumption or low standby power consumption. Simulations suggest that the SG SOI MOSFET can achieve a minimum channel length of about 10 nm when a threshold voltage roll-off restriction (ΔV_{th}= 0.1 V) is assumed (*Extract-A*). In addition, we find that the SG SOI MOSFET can achieve minimum channel lengths of about 30 nm, 20 nm or 10 nm when the maximal subthreshold swing value is restricted to 70 mV/dec, 80 mV/dec, or 90 mV/dec, respectively (*Extract-B*).

When *Extract-A* is used in SG SOI MOSFET scaling, it has been demonstrated that it affords us a design guideline for high-performance devices. Simulated results strongly suggest that the SG SOI MOSFET can offer adequate high-speed performance until 2009 if device parameters are set appropriately. However, in practice, the ITRS roadmap requires a 100-nm-thick buried oxide layer. This limits the design window: a sub-1-nm-thick EOT and/or a sub-5-nm-thick SOI layer must be applied to the device.

Extract-B was shown to yield a design guideline for low standby power devices. Simulation

results strongly suggest that the SG SOI MOSFET can offer adequate low-standby power performance beyond 2009 if the appropriate device parameters are set. The ITRS roadmap requiring a 100-nm-thick buried oxide layer limits the design window and requires non-ideal optimization of device parameters. In this case, the use of a high-k gate insulator is a possible solution.

We have shown that the thickness of the buried oxide layer significantly restricts SG SOI MOSFET scaling, and so must be considered as a future issue in terms of SOI devices and substrate technology.

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