# The Potential and the Drawbacks of Underlap Single-Gate Ultrathin SOI MOSFET

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## Abstract

This paper describes the performance prospect of underlapped single-gate ultra-thin (USU) SOI MOSFET with a low-*k* or high-*k* gate dielectric from the viewpoint of both digital and analog applications. Increase in underlap length suppresses the threshold voltage variation as well as suppression of short-channel effects. In addition, the thickness of the SOI layer directly impacts the maximization of drive current (i. e., minimization of intrinsic delay time). Since the fringe capacitance is reduced in introduction of underlap region, effective gate capacitance is also reduced, while voltage gain of the device rises. Since apparent rise of cut-off frequency stems from the reduction of voltage gain, advancement of analog performance is inherently limited.

Use of a high-*k* gate dielectric basically reduces the gate-induced drain leakage (*GIDL*) current, while short-channel effects are degraded. In the case of very high dielectric constant, however, a very high electric-field region appearing far from the gate edge becomes a new source of high *GIDL* current. So, optimization of the dielectric constant of the gate insulator is required.

**Key words:** MOSFET, silicon-on-insulator, underlap gate, GIDL, analog, high-k insulator

## 1. Introduction

The short-channel effects of the sub-30-nm SOI MOSFET appear to limit the performance improvements possible with simple down-scaling. It is thought, however, that multiple-gate SOI MOSFET, such as SOI FinFET[1] and triple-gate (TG) SOI MOSFET[2], will make a technical breakthrough possible. However, it is already understood that a simple fin structure does not give a desirable solution of SOI FinFET or TG SOI MOSFET[3], which suggests that optimization of device parameters or the proposal of an advanced device structure is needed for practical applications.

On the other hand, an SOI device with a source/drain (S/D) away from the gate edge (so-called 'underlap') is interesting because the short-channel effects can be suppressed through the relaxation effect of the drain-induced field[4, 5]. It has been predicted recently[6] that underlapped single-gate ultra-thin (USU) SOI MOSFET may offer the sharp subthreshold swing (*SS*) and short intrinsic delay time ( $\tau$ ) that we would expect from a sub-50-nm channel

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device, although USU device parameters will have to be well tempered[7]. In addition, high-$k$ gate material must be introduced to advance the USU device performance in future. However, impact of the use of a high-$k$ gate dielectric has not yet been extensively discussed. In modern applications of MOSFETs, the RF performance of USU devices is simultaneously required because fast AD/DA transformation is necessary in circuitry. For this reason, analog performance should also be discussed.

In this paper, we will discuss fundamental d. c. and a. c. characteristics of USU SOI MOSFET and the impact of use of high-$k$ gate dielectric on the d. c. and switching characteristics of the USU SOI MOSFET with a view to optimizing the device structure by tuning device parameters, such as the underlap length ($L_{no}$). We will address the trade-off of d. c. and a. c. characteristics and how to optimize the device performance.

## 2. Simulations

We used the device simulator *DESSIS*[8] for the hydrodynamic transport model. Device structures assumed are shown in Fig. 1; (a) conventional USU device (device *A*), (b) USU device with a high-$k$ gate dielectric (device *B*)[9], and (c) USU device with a stacked gate dielectric (device *C*). Equivalent oxide thickness (*EOT*) of the gate dielectric was fixed at 2 nm, and the buried-oxide layer (*BOX*) thickness ($t_{box}$) is 100 nm. Four different values of $L_{no}$ and their doping profiles were considered, as shown in Fig. 2. When the peak position of the doping concentration in the S/D region is away from the gate edge, $L_{no}$ increases. The physical gate length (70 nm) and the metallurgical channel length ($L_{met}$=30 nm) hold invariant when $L_{no}$ increases; i. e., the overlap length is 20 nm. Here, we don't use the word "effective channel length", because the "effective channel length" is significantly modulated with the gate voltage. Since the electron density of the low-doped "underlapped region" beneath the gate electrode is a strong function of the gate voltage, the effective channel length increases with the gate voltage. This mechanism is well known in the lightly-doped drain (*LDD*) MOSFET[10]. The body doping concentration ($N_A$) is $3.0\times10^{15}$cm$^{-3}$, and the peak of S/D doping concentration ($N_D$)

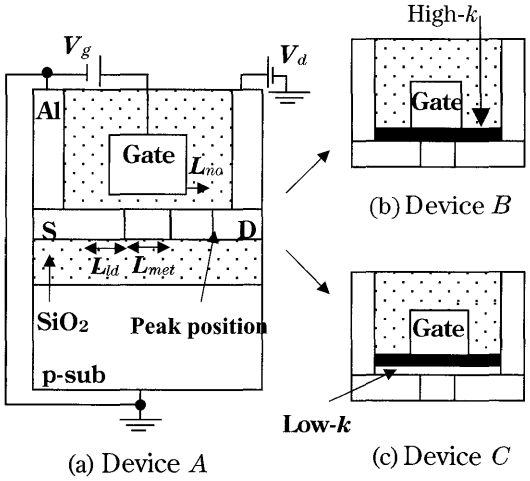


Fig. 1 Schematic view of USU SOI MOSFET assumed in simulations. $L_{ld}$ is the distance from the doping peak to the junction.

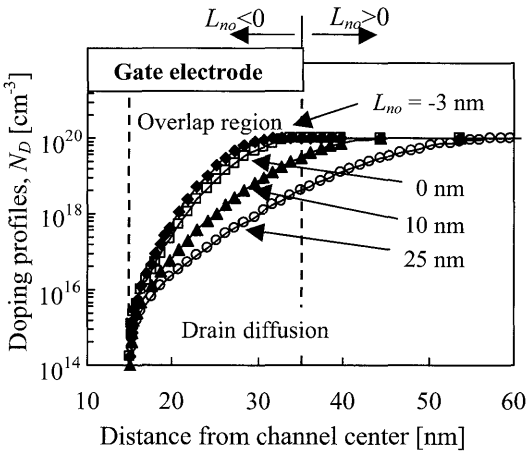


Fig. 2 Drain diffusion profiles. Drain and source diffusions are symmetric.

**Table 1.** Device parameters assumed.

| Parameters | Values | Units |
|---|---|---|
| Gate length, $L_g$ | 70 | nm |
| Metallurgical channel length, $L_{met}$ | 30 | nm |
| Lateral diffusion length, $L_{ld}$ | 17 – 45 | nm |
| Doping level of SOI layer, $N_A$ | $3\times10^{15}$ | $cm^{-3}$ |
| Gate SiO2 thickness, $t_{ox}$ | 2 | nm |
| Buried oxide layer thickness, $t_{box}$ | 100 | nm |
| SOI layer thickness, $t_{SOI}$ | 5 – 15 | nm |
| *EOT* of high-k gate insulator thickness | 2.0 | nm |
| Dielectric constant of high-*k* film, $\varepsilon_{high\text{-}k}$ | 3.9 – 50 | |

is $1.0\times10^{20}cm^{-3}$. For simplicity's sake we also assumed an $n^+$-poly-Si gate electrode with the doping of $1.0\times10^{20}cm^{-3}$. Since we must extract reliable characteristics of the USU SOI MOSFET from the simulations, we assumed device parameters of 90-nm technology node. Major device parameters are summarized in Table 1. The threshold voltage ($V_{th}$) is defined as the gate voltage ($V_g$) at which the drain current $I_d$ is equal to $(W/L_{met})\times10^{-7}$A. On-state drain current ($I_{on}$) was calculated at $V_g = V_{th} + 0.9$ V, with the drain voltage $V_d = 1.0$ V.

## 3. Results and Discussion

### 3.1 d. c. characteristics and switching performance: device *A*

First, we will discuss the characteristics of device *A*, as described in Fig. 1(a). In Fig. 3, threshold voltage ($V_{th}$) dependencies on underlap length ($L_{no}$) are shown for various $t_{SOI}$ values; it is assumed $L_{met} = 30$ nm. It is seen that the threshold voltage rises as the underlap length increases because the short-channel effect is suppressed. In addition, the incremental value of threshold voltage decreases as the underlap length increases. At $L_{no}= 20$ nm, a 5-nm-deviation of $L_{no}$ yields a threshold variation of at most 25 mV, even for $t_{SOI}= 15$ nm, where the short-channel effect is the most significant. The influence of local variation of the SOI layer

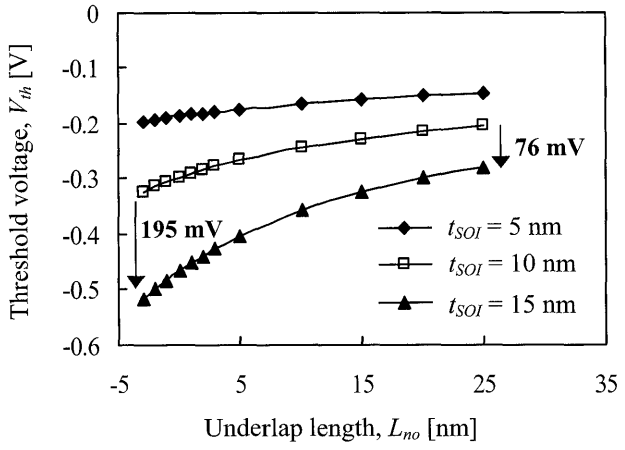


**Fig. 3** Threshold voltage dependence on underlap length ($L_{no}$).

thickness on the threshold voltage is shown by the two arrows: a thinner SOI layer results in a smaller variation of threshold voltage.

In the case of $L_{no}$ = -3 nm, the threshold voltage decreases by 195 mV as $t_{SOI}$ increases from 10 nm to 15 nm. In the case of $L_{no}$ = 25 nm, on the other hand, the decrease of threshold voltage is as small as 76 mV when $t_{SOI}$ increases from 10 nm to 15 nm. The impact of increase in $L_{no}$ results from the relaxation of lateral electric field along the underlap region[10]. This means that the increase in $L_{no}$ suppresses the threshold voltage variation. The underlap S/D structure is very useful for fabrication of short-channel devices. In fabrication of USU SOI MOSFET, the influence of doping fluctuation in underlap region should be examined. S.-I. Chang et al. investigated the sensitivity of the doping level on *GIDL* current[9]; their simulation results suggest that a 'worst-case-based' design is needed.

In Fig. 4, drive current ($I_{on}$) dependence of underlap length ($L_{no}$) is shown for various $t_{SOI}$ values; device A is assumed in simulations. For $t_{SOI}$ = 5 and 10 nm, the drive current decreases monotonously as $L_{no}$ increases. This is due to the increase in parasitic resistance of source and drain regions near the gate electrode edge, while the short-channel effects are well suppressed[11]. On the other hand, for $t_{SOI}$ = 15 nm, the drive current has a local peak as $L_{no}$ increases. When $L_{no}$ is still in a small value range, an increase in $L_{no}$ leads to the suppression of short-channel effects. However, when $L_{no}$ is in the large value range, the increase in $L_{no}$ leads to an increase of parasitic resistance of source and drain diffusions near the gate electrode edge. This suggests that the setting of the $t_{SOI}$ value directly impacts the maximization of drive current (i. e., minimization of intrinsic delay time[5]). In the present case, it is suggested that a better value of $t_{SOI}$ is between 10 and 15 nm. It is also worth mentioning that variation of the Ion value stemming from a local variation of $t_{SOI}$ value is minimal for $L_{no}$ = 3 nm.

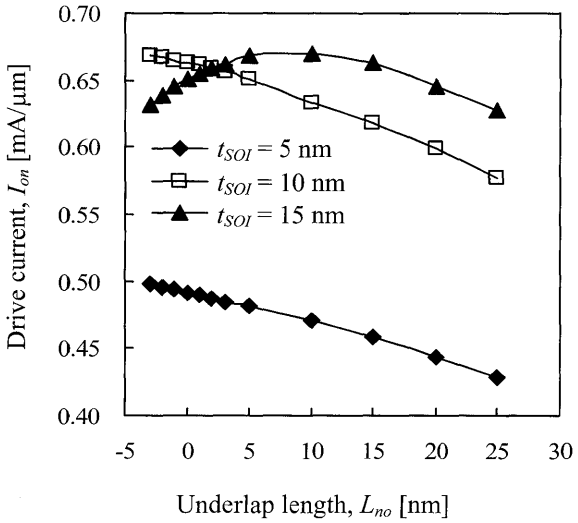


**Fig. 4** Drive current ($I_{on}$) dependence on underlap length ($L_{no}$).

### 3.2 RF analog characteristics: device *A*

In Fig. 5, cut-off frequency ($f_c$) and $g_m/g_d$ ratio dependencies on underlap length ($L_{no}$) are shown for various $t_{SOI}$ values. The $g_m/g_d$ ratio means the small-signal voltage gain ($A_V$) of device *A* - an intrinsic gain. If the cut-off frequency is extracted from the curve of $g_m/g_d$ ratio vs. frequency, as a frequency we get a 3-dB roll-off of the $g_m/g_d$ ratio. The $g_m/g_d$ ratio increases as $L_{no}$ increases, independently of $t_{SOI}$ values, which is primarily due to the reduction of $g_d$ as $L_{no}$ increases, because the increase in $L_{no}$ results in suppression of short-channel effects and an increase in parasitic resistance.

The cut-off frequency rises constantly as $L_{no}$ increases for $t_{SOI}$ = 5 nm. However, the cut-off frequency finds its maximum at around $L_{no}$ = 20 nm for $t_{SOI}$ = 15 nm. The mechanism is discussed below in detail. In order to analyze the analog behavior, in Fig. 6 the $g_m$ value and the effective gate capacitance ($C_{geff}$) are shown as a function of $L_{no}$. Fig. 6(a) shows the simulation result for $t_{SOI}$ = 5 nm and Fig. 6(b), for $t_{SOI}$= 15 nm. For $t_{SOI}$ = 5 nm, the recession rate of $C_{geff}$ is higher than that of $g_m$; the reduction of fringe capacitance ($C_{fringe}$) results in a rapid decrease in $C_{geff}$. Subsequently, the cut-off frequency rises constantly as $L_{no}$ increases. On the other hand, for $t_{SOI}$ = 15 nm, the recession rate of $g_m$ is higher than that of $C_{geff}$ for $L_{no}$ > 20 nm; the cut-off frequency curve shows a peak at around $L_{no}$ = 20 nm.

In simulations, the effective gate capacitance ($C_{geff}$) is primarily composed of the gate oxide capacitance ($S_g \times C_{ox}$), where $S_g$ is the gate electrode area covering the active region of the device, and the two fringe capacitances ($C_{fringe}$(source) + $C_{fringe}$(drain)). Briefly, we have $C_{geff}$ = $S_gC_{ox}$ + $C_{fringe}$(source) + $C_{fringe}$(drain). Since the doping level of the underlap region is very low, this underlap region is readily depleted by the built-in potential of junction. In addition, the underlap region of drain is considerably depleted by the effective gate-to-drain bias. As a

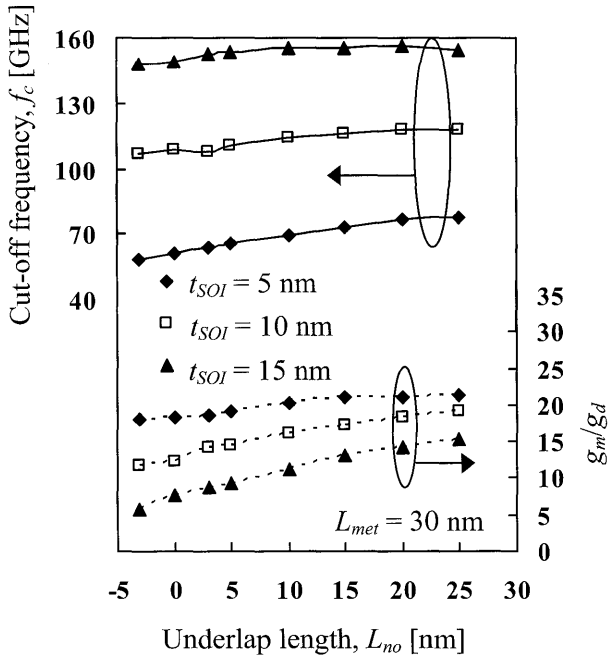


Fig. 5 Cut-off frequency ($f_c$) and gm/gd dependencies on underlap length ($L_{no}$).

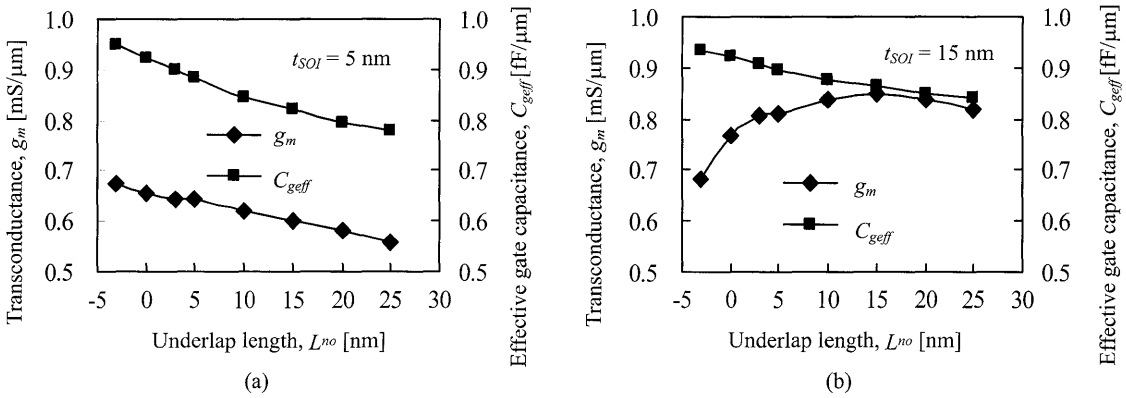


**Fig. 6** Transconductance ($g_m$) and effective gate capacitance ($C_{geff}$) dependencies on underlap length ($L_{no}$).
(a) $t_{SOI}$ = 5 nm (b) $t_{SOI}$ = 15 nm

result, $C_{fringe}$ is composed of gate-side-wall-insulator capacitance ($C_{swi}$), SOI layer capacitance ($\delta C_{SOI}$), and buried-oxide layer capacitance ($\delta C_{BOX}$). Briefly we have $C_{fringe} = \{1/C_{swi} + 1/\delta C_{SOI} + 1/\delta C_{BOX}\}^{-1}$. Since the dimensions of the device are quite small, the fringe capacitance greatly shares $C_{geff}$, as anticipated from the above description. A large $L_{no}$ lowers the doping level of the underlap region. So, $C_{geff}$ decreases rapidly as $L_{no}$ increases, although it seems to approaching specific minimal value.

### 3.3 Impact of high-*k* gate dielectric on performance of USU SOI MOSFET devices: devices *B* and *C*

In the following, three different devices *A*, *B* and C are examined in order to consider the influence of high-*k* gate dielectric on device characteristics. A band-to-band tunneling model [12, 13] is introduced in simulations. Fig. 7 shows the $I_d$-$V_g$ characteristics of USU SOI MOSFET for $L_{met}$ = 30 nm; $HfO_2$ film ($\varepsilon_{high\text{-}k}$ = 25[14]) is assumed as a high-*k* gate dielectric. The horizontal

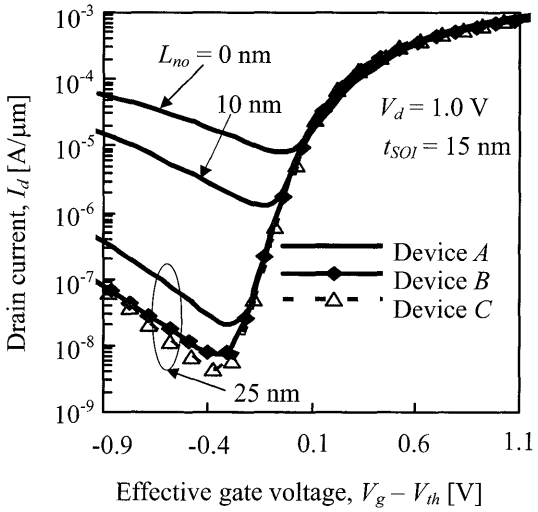


**Fig. 7** $I_d$-$V_g$ characteristics of USU SOI MOSFET for $L_{met}$ = 30 nm; devices B and C have a high-*k* gate dielectric with $\varepsilon_{high\text{-}k}$ = 25.

axis is given by $V_g$-$V_{th}$ for the sake of comparing the of gate-induced drain leakage (*GIDL*) current. When $L_{no}$ increases, or a high-*k* gate dielectric is introduced, *GIDL* current is reduced. In the former case, it seems that, as $L_{no}$ increases, the S/D − field relaxation and low-impurity-density region of the drain diffusion reduces the *GIDL* current[13]; and in the latter case, that reduction of the S/D fringe electric-field results in a low *GIDL* current. Therefore, use of a high-*k* gate dielectric can be seen to reduce *GIDL* current[9]. However, Fig. 8 shows that *GIDL* current reduces as the relative dielectric constant of high-*k* material ($\varepsilon_{high\text{-}k}$) increases, and that it increases again with the $\varepsilon_{high\text{-}k}$ value. This last behavior of the *GIDL* current looks strange because it can be anticipated that a high $\varepsilon_{high\text{-}k}$ value simply results in a significant short-channel effect[15]. In order to investigate the mechanism of the above behavior of the *GIDL* current, we evaluated the source-to-drain profile of the surface electric-field of the device with a high-*k* gate dielectric. Simulation results for device *B* are shown in Fig. 9 for $\varepsilon_{high\text{-}k}$ values of 3.9, 10, and 50, respectively. In the case of $\varepsilon_{high\text{-}k}$ = 50, we can see a very high electric field region far from the gate edge, and it is this region that causes a high *GIDL* current. Since the peak in the electric-field profile is located near the maximal-doping position of drain diffusion,

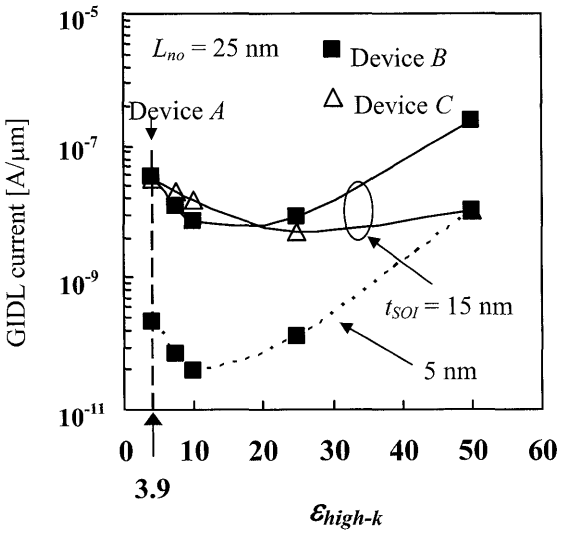


Fig. 8 Relationship between *GIDL* current and $\varepsilon_{high\text{-}k}$ at $V_g$-$V_{th}$ = -0.4 V and $V_d$ = 1.0 V. The solid line represents $t_{SOI}$ = 15 nm, and the dotted line, $t_{SOI}$ = 5 nm. The following device parameters are assumed: $L_{met}$ = 30 nm, $L_{no}$ = 25 nm, *EOT* = 2 nm, $t_{box}$ = 100 nm.

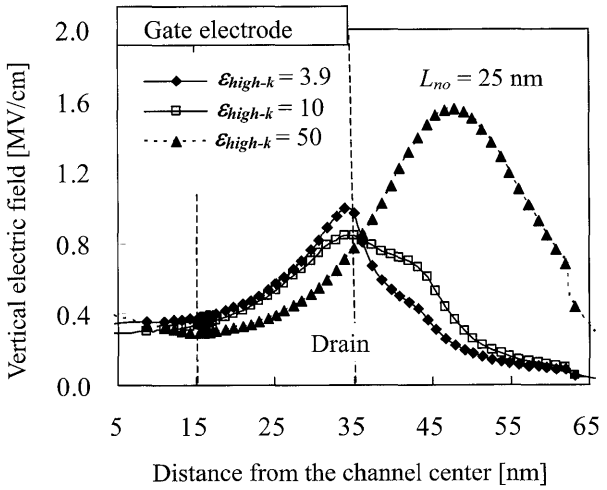


Fig. 9 Surface vertical electric-field profiles of USU SOI MOSFET (device B) for three-different $\varepsilon_{high\text{-}k}$ values at $V_g$ = $V_{th}$ -0.4 V and $V_d$ = 1.0 V. The following device parameters are assumed: $L_{met}$ = 30 nm, $L_{no}$ = 25 nm, *EOT* = 2 nm, $t_{box}$ = 100 nm, and $t_{SOI}$ = 15 nm.

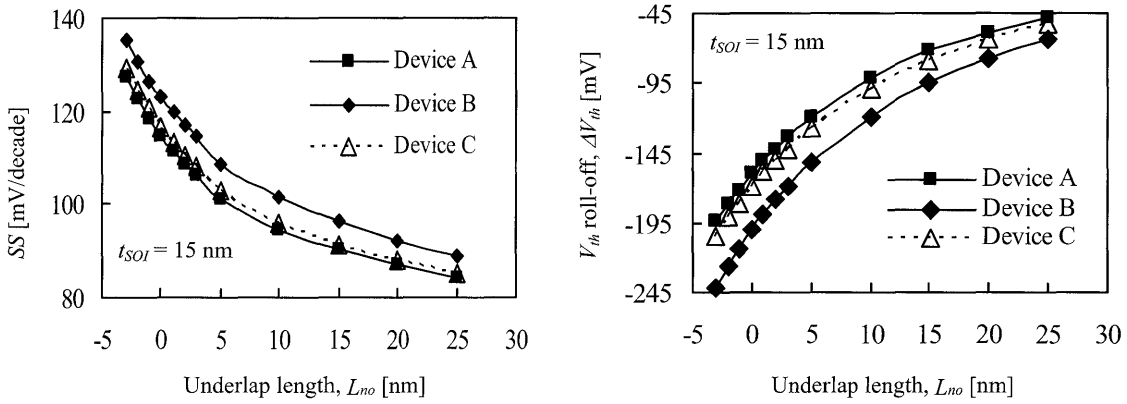


**Fig. 10** Impact of the value of $L_{no}$ on short-channel effects of devices with $\varepsilon_{high\text{-}k}$ = 25 at $V_d$ = 1.0 V.
(a) Subthreshold swing (SS) at $L_{met}$ = 30 nm.
(b) Threshold voltage roll-off ($\Delta V_{th}$). $\Delta V_{th} = V_{th}(L_{met}$ = 30nm) − $V_{th}$ ($L_{met}$ = 50nm).

we can conclude that the background physics of the high *GIDL* current is the same as the original one[12]. Thus, we must find the optimal $\varepsilon_{high\text{-}k}$ value, so as to reduce the *GIDL* current[16]. In this paper, it is seen that $HfO_2$ is a good candidate, and that a stacked-gate dielectric relaxes the short-channel effects.

The impact of $L_{no}$ on subthreshold swing (*SS*) and threshold voltage roll-off ($\Delta V_{th}$) is shown in Figs. 10(a) and 10(b), where it is assumed that $t_{SOI}$ = 15 nm, $L_{met}$ = 30 nm, and $\Delta V_{th} = V_{th}$ ($L_{met}$ =30 nm) − $V_{th}$($L_{met}$=50 nm). $HfO_2$ ($\varepsilon_{high\text{-}k}$ = 25) is assumed in Fig. 10. A high-*k* dielectric degrades *SS* and $\Delta V_{th}$. It is worth stating that the stacked gate dielectric (device *C*) effectively suppresses the undesired degradation of *SS* and $\Delta V_{th}$. Since the physical thickness of gate insulator of device *C* is thinner than that of device *B*, the fringe electric field of device *C* is higher than that of device *B* ; the stacked-gate insulator has successfully suppressed both *DIBL* and *BIIBL*[17].

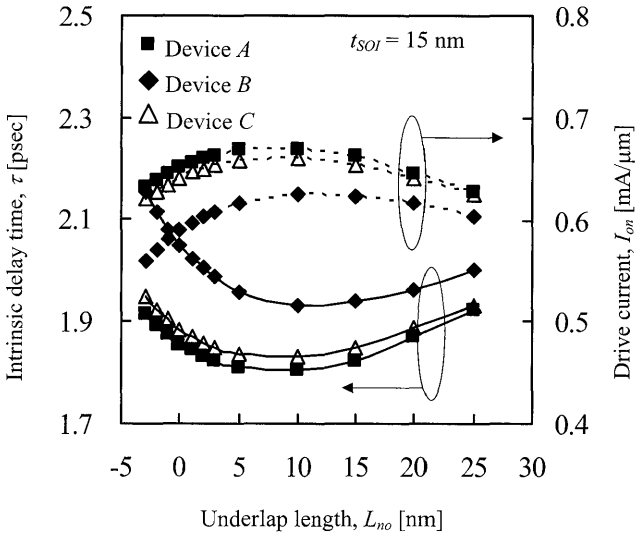


**Fig. 11** Behavior of $\tau$ ($=C_gV_{on}/I_{on}$) and $I_{on}$ shown as a function of $L_{no}$ for various device structures. It is assumed $L_{met}$ = 30 nm, $V_{on}$ = 1.0 V, and $\varepsilon_{high\text{-}k}$ = 25.

Fig. 11 shows dependencies of intrinsic delay time ( $\tau$ ) and $I_{on}$ on $L_{no}$, where $\tau = C_g V_{on}/I_{on}$, $C_g$ is the physical gate capacitance, and $V_{on}$ = 1.0 V. When $L_{no}$ increases, $I_{on}$ increases, because of the slight suppression in short-channel effects. After reaching a peak, it then decreases. Thereby, the intrinsic delay time ( $\tau$ ) shows a certain minimal value. So, we must carefully consider the introduction of high-$k$ gate dielectric as the intrinsic delay time ( $\tau$ ) increases due to short-channel effects. When we require high-speed devices with a low *GIDL* current, the stacked gate dielectric should be applied to the devices.

### 3.4 Impact of simulation model on simulation results

The simulation model often has a strong impact on simulation results, and, in the case of ultra-thin SOI MOSFET, the simulation results should be carefully considered[17]. We can anticipate that the influence of underlap region on device characteristics will be significant when quantum effects are incorporated in simulations, because quantum-mechanical surface depletion (surface 'dark space') enhances the resistance value of the underlap region. In order to estimate the impact of quantum effects, as mentioned above, we utilized a density-gradient model (DGM)[18] as well as a hydrodynamic transport model in our *DESSIS* simulations. Recently, the impact of quantum effect on FinFET with an underlap-gate structure has been discussed[7], where d. c. characteristics are primarily evaluated.

In Fig. 12, we show drive current ($I_{on}$) and effective gate capacitance ($C_{geff}$) as a function of underlap length ($L_{no}$); it is assumed $L_{met}$ = 30 nm, $t_{ox}$ = 2 nm, $t_{box}$ = 100 nm, and $t_{SOI}$ = 15 nm. It can be seen that the fundamental behavior of both $I_{on}$ and $C_{geff}$ are almost the same, regardless of the simulation model used, and that DGM reduces both $I_{on}$ and $C_{geff}$. Surface 'dark space' reduces the effective gate capacitance (~6 %) because $C_{geff}$ can be estimated by $\varepsilon_{ox}/\{t_{ox}+(\varepsilon_{ox}$

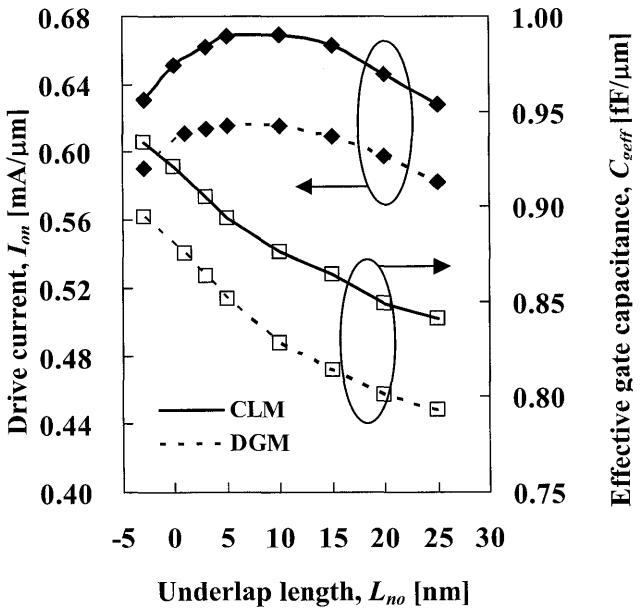


Fig. 12 Drive current ($I_{on}$) and effective gate capacitance ($C_{geff}$) as a function of underlap length ($L_{no}$). It is assumed $L_{met}$ = 30 nm, $t_{ox}$ = 2 nm, $t_{box}$ = 100 nm, and $t_{SOI}$ = 15 nm.

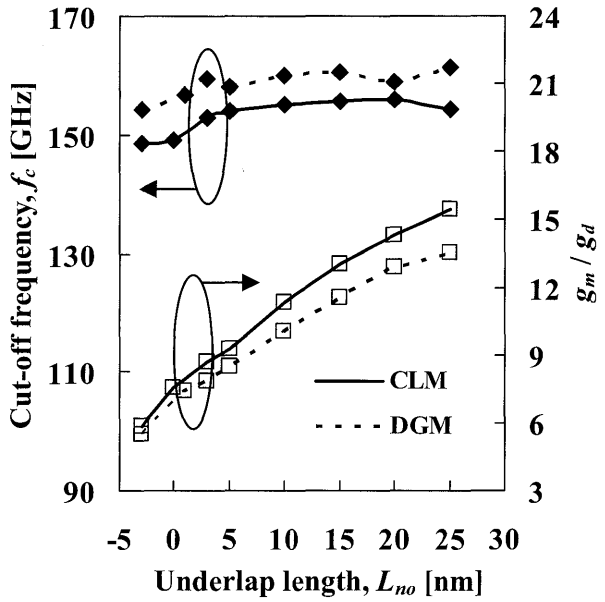


Fig. 13 Cut-off frequency ($f_c$) and intrinsic gain ($g_m/g_d$) as a function of underlap length ($L_{no}$). It is assumed $L_{met}$ = 30 nm, $t_{ox}$ = 2 nm, $t_{box}$ = 100 nm, and $t_{SOI}$ = 15 nm.

$/ \varepsilon_s) t_{inv}$}, where $t_{inv}$ is the inversion layer thickness and es is the silicon dielectric permittivity. So, we might conclude that the reduction of $C_{geff}$ due to DGM primarily results from the surface 'dark space.' Since the reduction rate of $I_{on}$ due to DGM (~8 %) is almost the same as that of $C_{geff}$, it can be concluded that the reduction of $I_{on}$ is primarily responsible for the reduction of $C_{geff}$. It is also thought that a surplus reduction of $I_{on}$ of about 2 % is responsible for the parasitic resistance of source and drain diffusions.

In Fig. 13, we show the cut-off frequency ($f_c$) and small-signal gain ($g_m/g_d$) as a function of underlap length ($L_{no}$) ; it is assumed that $L_{met}$ = 30 nm, $t_{ox}$ = 2 nm, $t_{box}$ = 100 nm, and $t_{SOI}$ = 15 nm. It can be seen that the fundamental behavior of $f_c$ and $g_m/g_d$ is almost identical, regardless of simulation model, and that DGM promotes an increase in $f_c$ and a slight decrease in small-signal gain ($g_m/g_d$). Since $C_{geff}$ is reduced, due to quantum effects, $f_c$ naturally rises. The influence of quantum effects on intrinsic gain ($g_m/g_d$) appears somewhat complicated, and further investigation is needed. In the present simulation results, the reduction rate of $g_m$ is shown to be slightly higher than that of gd. In other words, the impact of parasitic resistance on $g_m$ is stronger than that on $g_d$.

From the above simulation results, we can conclude that electrical characteristics are strongly influenced by DGM, but that fundamental behaviors of those characteristics are almost independent of the transport model. Much of the discussion described above will be useful in creating a design guideline for underlap gate SOI MOSFET.

## 4. Conclusion

This paper describes the performance prospect of underlapped single-gate ultra-thin (USU) SOI MOSFET with a low-$k$ or high-$k$ gate dielectric from the viewpoint of digital and analog applications. As already known, the impact of increase in underlap length on device

characteristics results from the relaxation of lateral electric-field along the underlap region. This means that the increase in underlap length suppresses the threshold voltage variation as well as suppressing short-channel effects, indicating that the underlap S/D structure will be very useful for the fabrication of short-channel devices. In addition, the thickness of the SOI layer directly impacts the maximization of drive current (i. e. minimization of intrinsic delay time). So, the SOI layer thickness and the underlap length must be carefully determined.

On the other hand, analog RF characteristics are also influenced in use of underlap region. Since the fringe capacitance is reduced in the introduction of underlap region, the effective gate capacitance is also reduced, while voltage gain of the device rises. Since the apparent rise in cut-off frequency stems from the reduction of voltage gain, the advancement of analog performance is inherently limited.

Use of a high-$k$ gate dielectric reduces the *GIDL* current, while the short-channel effects are degraded. In the case of a very high dielectric constant, however, a very high electric-field region appearing far from the gate edge becomes a new source of high *GIDL* current. So, optimization of the dielectric constant of the gate insulator is required.

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