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Performance Evaluation of Fully-Depleted SOI MOSFET-Based Diodes Applied to Schenkel Circuit for RF-ID Chips

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Abstract

The feasibility of using the SOI-MOSFET as a quasi-diode to replace the Schottky-barrier diode (SBD) in the Schenkel circuit is examined by experiments and simulations. Unlike the SBD, the reverse-biased current of the SOI-MOSFET-based quasi-diode is much lower than its forward-biased current (I_F). The driving current of the quasi-diode (I_F) is increased by the excellent subthreshold swing value (S) of the SOI MOSFET; the trade-off between boost-up efficiency(η) and I_F should be taken into account. An a. c. analysis indicates that the channel-doping level of the quasi-diode should be optimized to suppress the floating-body effect for RF applications.

1. Introduction

Since RF-ID chips have no internal power supply, they need a way of using the received signal as an energy source; a common approach is the Schenkel circuit[1, 2]. The basic Schenkel circuit is shown in Fig. 1. It usually consists of capacitors and p-n diodes. Modern RF applications such as RF-ID chips often use Schottky-barrier diode (SBD) in this circuit[2-4]. Unfortunately, the reverse-biased current (I_R) of an SBD is not significantly lower than the

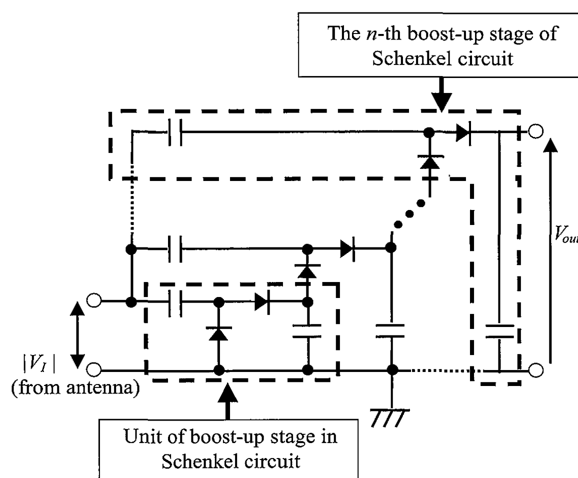

Fig. 1 Schematic of Schenkel circuit.

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forward-biased current (I_F), because the requirement for high drive currents results in a low barrier height. In addition, the a. c. signal voltage received is very small in RF-ID systems. Overall, Schenkel circuits that use SBD's fail to offer high efficiency.

In this paper, we discuss the use of the SOI-MOSFET-based quasi-diode (SOI-QD) to replace the SBD used in Schenkel circuits. We estimate experimentally the possible efficiency improvement with SOI-QD using various SOI MOSFET's, and a. c. analyses of SOI-QD to investigate operation stability in the RF band are conducted using a 2D device simulator (Synopsys *DESISS* [5]).

2. Remaining Issues with the Conventional Schenkel Circuit and an Advanced Proposal

At first, we used the circuit simulator PSPICE[6, 7] to examine the performance of a Schenkel circuit that used Schottky barrier diode (SBD), pn-junction diode (PND) or conventional bulk MOSFET-based quasi-diode (CB-QD). In the CB-QD variant, the gate terminal and the drain terminal are connected, and the source terminal and the substrate terminal are also connected. We assumed that the SBD and PND had a junction area of 46.1 μm^2, and that the gate width and gate length of the bulk MOSFET were 20.6 μm and 0.32 μm, respectively. All devices had identical active areas. For simplicity, the circuit simulations employed the empirical model (Level=3)[6]. To acquire realistic device performance from the PND and SBD variants, we introduced the minority carrier lifetime model shown in the Appendix.

Fig. 2 shows simulated rectifier characteristics of the various diodes in a low voltage range of input anode voltage (V_A). We can see that SBD has the largest driving current among the three diodes, as well as the highest reverse-biased current. Fig. 3 shows the performance of 5-stage Schenkel circuits that use the three different diodes for an input voltage V_A of 100 mV. It is shown that the conventional bulk-MOSFET-based quasi-diode successfully boosts the input signal from a very low level to an acceptable level, while SBD and pn-junction diode fail to do so. SBD failed to match this, despite its large driving current: since current SBD designs have a high I_R value, almost identical to I_F, in the low voltage range of 100 mV, the

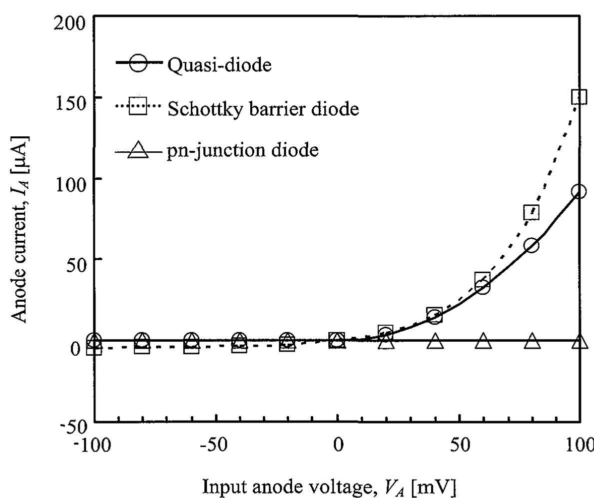

Fig. 2 Forward and reverse characteristics of various diodes (simulation results).

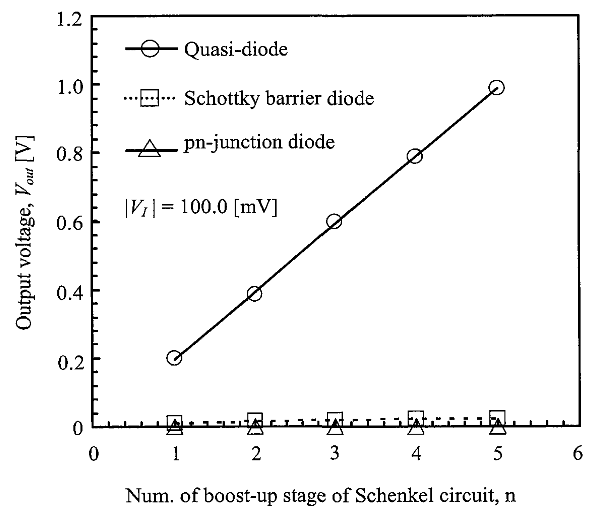

Fig. 3 Boost-up performance of Schenkel circuit with various diodes (simulation results).

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high leakage current (I_R) degrades the signal boost process. On the other hand, the I_F and I_R values of CB-QD are much smaller than those of SBD. However, CB-QD offers an acceptable level of boost. The main reason is that I_F of CB-QD is larger than its I_R, which means that the effective boost efficiency (η) of a Schenkel circuit should not be determined by the direct value of driving current, but by the ratio of I_F to I_R defined as

$$\eta = I_F/(I_F + |I_R|)\,. \quad (1)$$

Unfortunately, we cannot apply the above CB-QD to a practical Schenkel circuit as is, because it has a crucial drawback: a CB-QD made on an n-channel bulk MOSFET has a parasitic pn-diode between the drain and the substrate that can work when the drain is negatively biased. This effective reverse current I_R of CB-QD that passes through the parasitic pn diode degrades the η value.

Our solution is to base the quasi-diode on an SOI MOSFET instead of a bulk MOSFET to raise the η value. Fig. 4 shows the device structure assumed here and the terminal nodes of an SOI-MOSFET-based quasi-diode (SOI-QD). The n-channel fully-depleted (FD)-SOI MOSFET's used for evaluation of device performance had channel lengths, L, of 0.32 and 1.0 μm (see Table 1). Fig. 5 shows the I_D -V_G characteristics of the FD-SOI MOSFET's (L=0.32 and 1.0 μm) measured at V_D = 50 mV; the substrate bias was 0 V. The subthreshold swing (S) values of the two devices are quite different. It can be seen that, because of short channel effects, the S value is larger at L = 0.32 μm than at L = 1.0 μm.

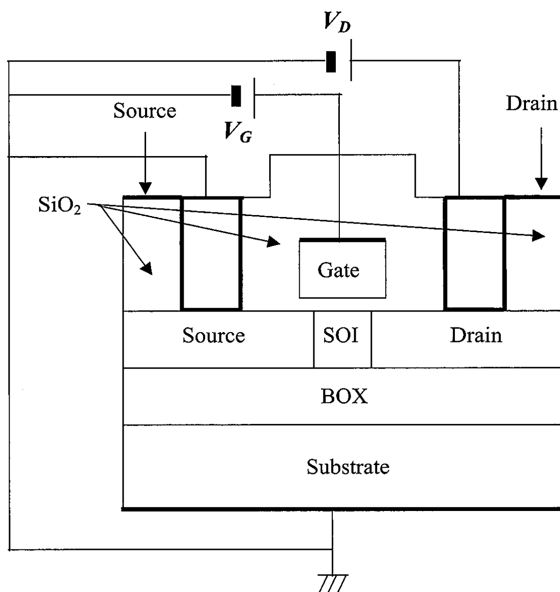

Fig. 4 SOI-MOSFET and terminal nodes for quasi-diode operation.

Since it is anticipated that the device characteristics are sensitive to substrate bias because of the thin buried oxide layer, we can produce SOI-QD's with various rectification characteristics by modifying the substrate bias (V_{BS}) applied to the FD-SOI MOSFET. It

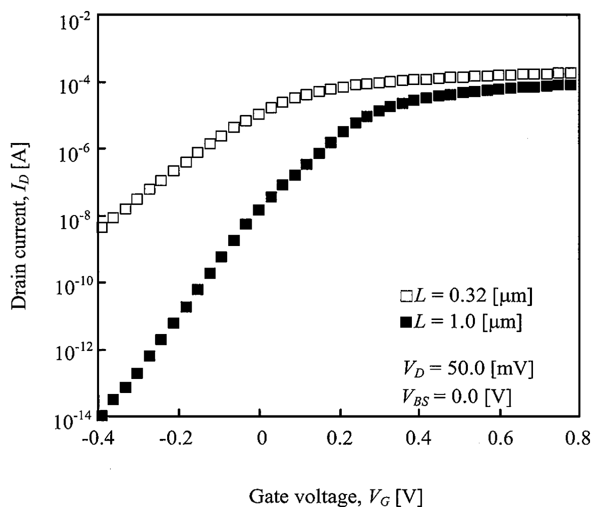

Fig. 5 I_D -V_G characteristics of fully-depleted SOI MOSFET (experimental results).

Table 1. Device parameters (experimental results).

L	0.32 (or 1.0) [μm]
W	20.6 [μm]
t_{SOI}	50.0 [nm]
t_{BOX}	80.0 [nm]
t_{OX}	7.0 [nm]
$N_{d,ch}$	3.0×10^{17} [cm^{-3}]

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should be noted that this technique modulates the threshold voltage of the FD-SOI MOSFET. We can vary the S value and the current level easily. As a result, the SOI-QD's rectification characteristics can be tuned to yield the best solution. In this paper, we apply a negative, zero or a positive V_{BS} value to the device; these conditions are labeled (i), (ii) or (iii), respectively (see Tables 2 and 3). It should be noted that the V_{BS} value at different L values is not identical when the threshold voltage (V_{TH}) is adjusted to be the same value. Fig. 6 shows the I_A-V_A characteristics of SOI-QD (i), (ii) and (iii).

Table 2. S values of SOI MOSFET near V_G= 0 V in various operation conditions.

<L = 0.32 [μm]>	S [mV/dec.]	<L = 1.0 [μm]>	S [mV/dec.]
V_{BS} = -3.0 [V]	211.5	V_{BS} = -0.25 [V]	169.0
V_{BS} = 0.0 [V]	142.3	V_{BS} = 0.0 [V]	71.8
V_{BS} = 3.0 [V]	132.1	V_{BS} = 1.5 [V]	71.5

Table 3. I_F, I_R, R_{ch}, and η values of SOI-QD in various operation conditions. Amplitude of input signal is 100 mV.

L = 0.32 [μm]	S	forward bias		reverse bias		η [%]
	[mV/dec.]	I_F [μA]	R_{ch} [kΩ]	I_R [μA]	R_{ch} [kΩ]	
V_{BS} = -3.0 [V]	211.5	90.0	1.1	-47.0	2.2	64.4
V_{BS} = 0.0 [V]	142.3	2.1	47.0	-0.89	110.0	70.7
V_{BS} = 3.0 [V]	132.1	1.2	81.0	-0.55	180.0	69.3
L =1.0 [μm]	S	forward bias		reverse bias		η [%]
	[mV/dec.]	I_F [μA]	R_{ch} [kΩ]	I_R [μA]	R_{ch} [MΩ]	
V_{BS} = -0.25 [V]	169.0	29.0	3.4	-11.0	0.0088	72.0
V_{BS} = 0.0 [V]	71.8	0.25	401.0	-0.016	6.2	94.0
V_{BS} = 1.5 [V]	71.5	0.0072	13900	-0.00026	3900	96.6

At first, we should consider the impact of L value, as shown in Fig. 6. In condition (i), the SOI-QD works near the threshold voltage (V_{TH}) because V_{BS} is positive. S is greater in condition (i) than in condition (ii), resulting in a smaller ratio of I_F/I_R and, thus, a smaller η value (see Tables 2 and 3, and Figs. 6(a) and 6(b)). In condition (i), however, since the channel resistance (R_{ch}) is reduced due to the lowering of the threshold voltage (V_{TH}), the driving current of the device increases. By contrast, in condition (iii), the device works in the subthreshold region because of the negative substrate bias (V_{BS}). The S value is smaller in condition (iii) than in condition (ii). The channel resistance (R_{ch}) in condition (iii) increases due to the raising of the threshold voltage (V_{TH}), resulting in a lower drive current, but identical ρ value to that seen in condition (ii) (see Fig. 6(c)).

Next, we will compare the performance of the two devices (L=1 and 0.32 μm) shown in Fig. 6. As mentioned above, the S value with L = 1.0 μm is smaller than that with L=0.32 μm. Accordingly, I_F/I_R is larger with L=1.0 μm than with L= 0.32 μm, and the η value when L= 1.0 μm is larger than that when L= 0.32 μm, as shown in Table 3. It should be noted that the difference in forward current level (I_F) at the same bias comes not only from the different W/L, but also the different S value. This means that we must take into consideration the trade-off

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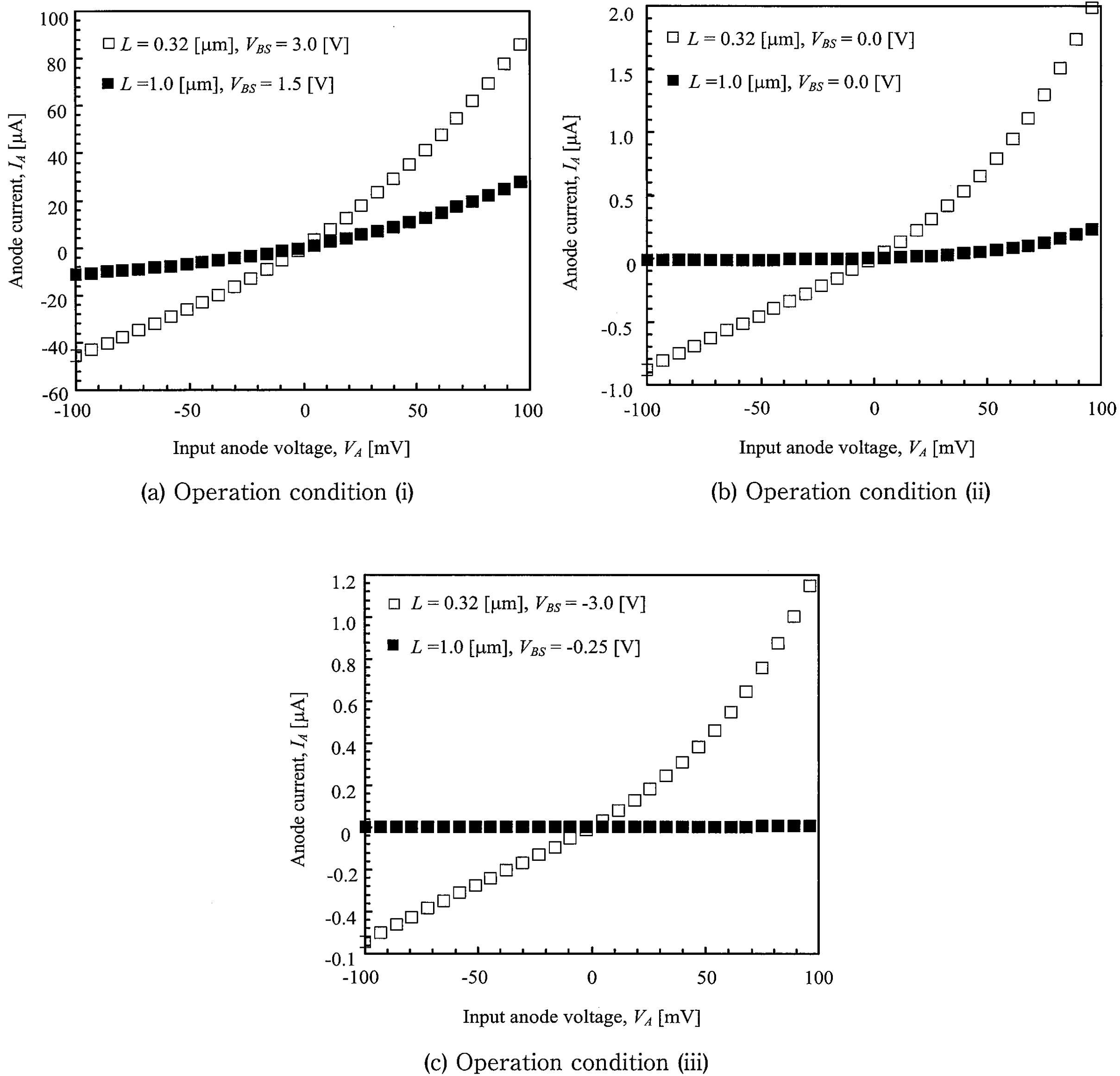

Fig. 6 I-V characteristics of SOI-QD (experimental results).

between η and I_F; that is, it is necessary to select the most suitable operation bias condition and to reduce the S value.

Finally, we shall briefly compare the performance of SBD, pn-diode and SOI-QD. Table 3 shows I_F, I_R and η of SOI-QD in various operation conditions when the input signal amplitude ($|V_A|$) is 100 mV. According to a recent report[3], when V_A = 100mV, the SBD has an I_F of about 1.0 nA and the pn-diode has an I_F of about 0.1 pA; this indicates that the SOI-QD has identical I_F to the other devices or has larger I_F in all conditions for the two L values examined. In addition, since the SOI-MOSFET has lower leakage current than the SBD and its subthreshold characteristic is excellent, a high boost efficiency can be expected when using the SOI-QD.

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3. Simulation-based Consideration of RF Performance of SOI-QD

In order to investigate the feasibility of using SOI-QD's in RF applications, we conducted extensive a. c. analyses using a 2D device simulator.

The assignment of terminal connections in simulations is shown in Fig. 4. The gate-to-source and gate-to-drain capacitances play important roles in the a. c. analyses because they yield both parasitic and fringing capacitances[8]. Since we must consider a realistic device structure in order to get reliable simulation results, we assumed an n-channel FD-SOI MOSFET with channel length L of 0.32 μm. Other device parameters W, t_{SOI}, t_{BOX} and t_{OX} are listed in Table 1. They are identical to those of the device used in the previous experiments, but the doping level of the SOI layer, $N_{d,ch}$, was changed from 6.0×10^{16}cm^{-3} to 3.0×10^{17}cm^{-3} in order to adjust the threshold voltage.

Fig. 7 shows simulated rectifier characteristics of the SOI-QD. Since the threshold voltage (V_{th}) rises sharply with the doping level of the SOI layer ($N_{d,ch}$), the forward-biased anode current (I_F) decreases greatly, and the reverse-biased anode current (I_R) also decreases. However, η increases on the basis of Eq. (1) because the reduction of I_R overwhelms that of I_F.

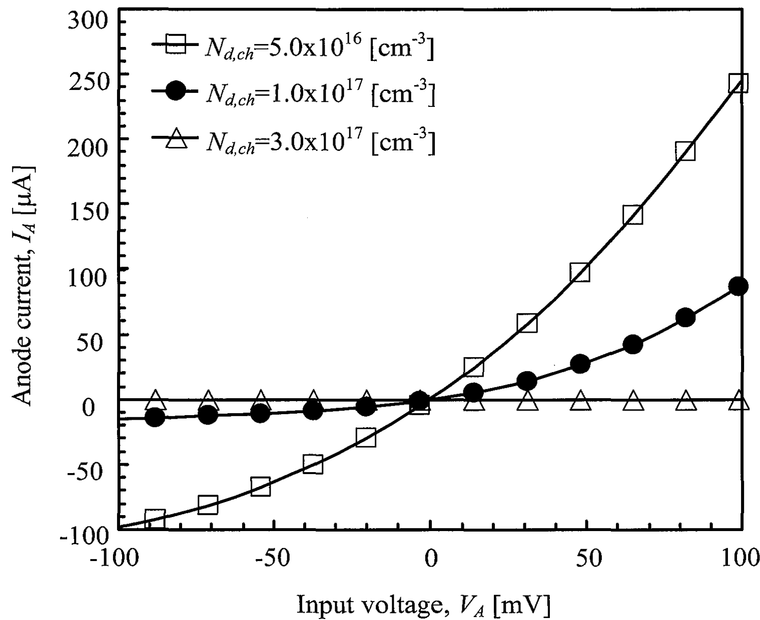

Fig. 7 Simulated I-V characteristics of quasi-diodes.

Fig. 8 shows the g_A-V_A curves for various $N_{d,ch}$ values; gA ($=dI_A/dV_A$) is the anode conductance. Fig. 8(a) is for $N_{d,ch}$=5×10^{16}cm^{-3}, Fig. 8(b) for $N_{d,ch}$= 1×10^{17}cm^{-3}, and Fig. 8(c) for $N_{d,ch}$= 3×10^{17}cm^{-3}. Frequency f was changed from 1 Hz to 10 GHz. In the case of $N_{d,ch}$= 5.0×10^{16}cm^{-3} (Fig. 8(a)), the g_A-V_A characteristic is not sensitive to frequency (1 Hz to 10 GHz). In the cases of $N_{d,ch}$= 1.0×10^{17}cm^{-3} (Fig. 8(b)) and 3.0×10^{17}cm^{-3} (Fig. 8(c)), the g_A-V_A characteristic is sensitive to frequency. In particular, when $N_{d,ch}$= 3.0×10^{17}cm^{-3}, the g_A-V_A characteristic reacts strongly to frequency.

Since the SOI layer is 50 nm thick, the fully-depleted condition is satisfied in two cases (Figs.

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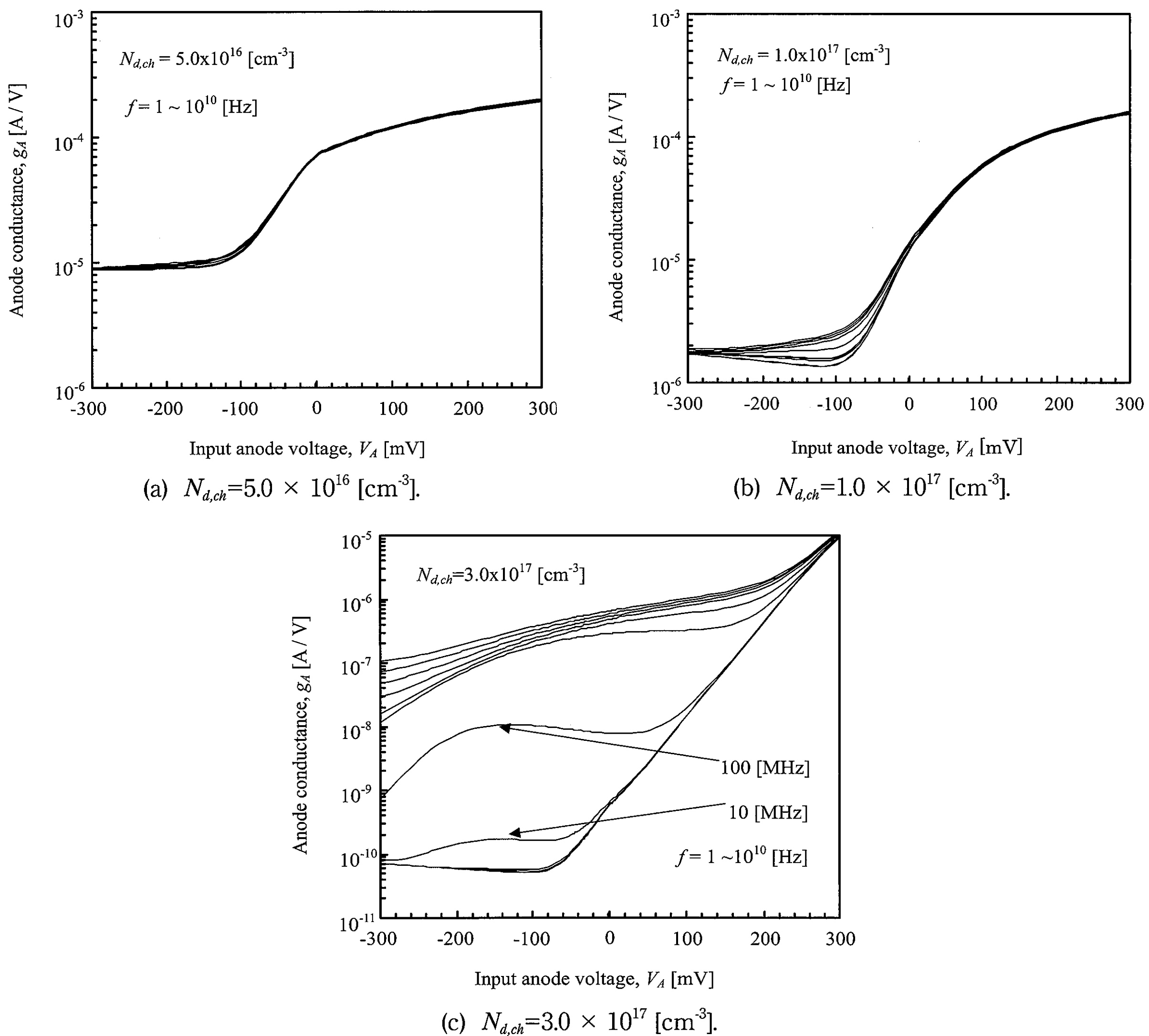
8(a) and 8(b)). Majority carriers (holes) are basically not responsible for device operation, and so parasitic bipolar action is not expected at the bias condition used ($|V_A| < 0.3$ V). Since the threshold voltage is very low (~0 V), electrons in the inversion layer rule device operation. In this case, the frequency dependence of the dielectric response of electrons ('majority carriers' near the surface) limits the g_A-V_A characteristic. The limit of the frequency response of electrons in Si is higher than 100 GHz[9], so the simulation results shown in Figs. 8(a) and 8(b) are acceptable. The smaller variation in g_A-V_A characteristics seen in Fig. 8(b) is related to the remaining hole density near the bottom of the SOI layer, which should be higher than that in Fig. 8(a).

We note that the fully-depleted condition is not satisfied in the case of $N_{d,ch} = 3.0\times10^{17}\text{cm}^{-3}$. That is, the majority carriers (holes), remaining near the SOI/buried oxide interface, play an important role in determining device operation - the typical floating body effect[10]. Since the g_A-V_A characteristics at frequencies above 10 MHz differ from those below 10 MHz (see Fig. 8(c)), the g_A-V_A characteristics at frequencies above 10 MHz are not normal. In the present



(a) $N_{d,ch}=5.0\times10^{16}$ [cm^{-3}].

(b) $N_{d,ch}=1.0\times10^{17}$ [cm^{-3}].

(c) $N_{d,ch}=3.0\times10^{17}$ [cm^{-3}].

Fig. 8 Simulated g_A - V_A characteristics.

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case, it is thought that the generation process of majority carriers (holes) will rule the dynamic operation of SOI-QD. Since the generation-recombination time constant is about 0.1 μsec in the present simulations, the hole generation process does not respond at frequencies above 10 MHz.

Fig. 9 shows the η-f characteristics of the SOI-QD from f = 1 Hz to 1 THz with the parameter of $N_{d,ch}$. However, the simulated value of η is not reliable for f > 100 GHz because physical models for devices are not proposed for such a high frequency; we simply focus on the behavior of η. In Fig. 9, we find that η values calculated by g_A in the low frequency region are almost identical to η values given experimentally for L= 1.0 μm. So this suggests that the g_A value can be directly applied to Eq. (1) in the RF region (see Table 3). In Fig. 9, we can see that the η value remains higher than 90 % independently of $N_{d,ch}$ up to 10 MHz. This is supported by the fact that the S value in the active range of I_A of SOI-QD is sufficiently small. However, when f is higher than 100 MHz, especially when $N_{d,ch}$=3.0×10^{17}cm^{-3}, η falls to 60 %. This is caused by the body-floating effect, as mentioned previously. On the other hand, at $N_{d,ch}$=5.0×10^{16}cm^{-3} and 1.0×10^{17}cm^{-3}, η remains high up to 10 GHz. As a result, SOI-QD's with $N_{d,ch}$=5.0×10^{16}cm^{-3} and 1.0×10^{17}cm^{-3} can be used in RF applications; when $N_{d,ch}$= 3.0×10^{17} cm^{-3}, the SOI-QD is no longer suitable because of the significant body floating effect.

In the above simulations, we assumed V_A=0.1 V, because we considered the case of short-distance communications. Since the above simulations show that the proposed SOI-QD produces almost identical performance at V_A < 0.1 V, we think that Schenkel circuits with SOI-QD's are also applicable to long-distance communications.

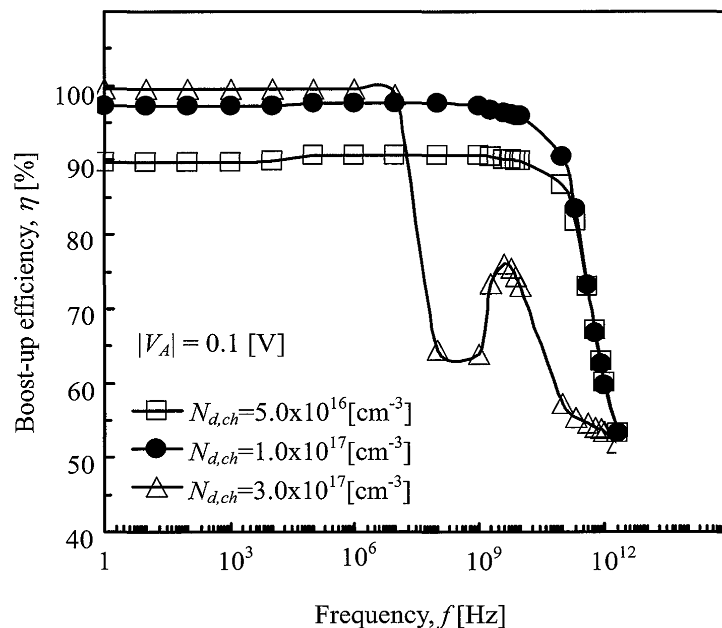

Fig. 9 η-f characteristics for various body doping levels.

4. Conclusion

The feasibility of replacing SBD's as quasi-diodes in the Schenkel circuit with SOI-MOSFET's was examined using experiments and simulations. The reverse-biased current (I_R) of the

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SOI-QD is much lower than its forward-biased current (I_F), and the driving current (I_F) is high because of the excellent S value provided by the SOI-MOSFET arrangement. The trade-off between boost efficiency (η)) and I_F should be taken into account. In addition, a. c. analyses using a 2D device simulator showed that the body doping concentration ($N_{d,ch}$) of the SOI layer should be optimized so as to maintain the fully-depleted condition for RF applications up to 100 GHz.

Acknowledgments

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Appendix:

Here we introduce a model for minority carrier lifetimes[5] used in *PSPICE* simulations to ensure consistency with *DESSIS* simulation results.

$$\tau = \tau_{max} + \frac{\tau_{max} - \tau_{min}}{1 + \left(N / N_{ref} \right)^{\gamma}}, \quad \text{(A1)}$$

where N is the doping density, N_{ref} is the doping parameter, γ is the fitting parameter, τ_{max} and τ_{min} are lifetime parameters. Parameter values used here are summarized in Table 4.

Table 4. Physical parameters in device simulations (*DESSIS*).

Parameters	Values
τ_{max}	1.0x10^{-5} sec for electrons
	3.0x10^{-5} sec for holes
τ_{min}	0.0 sec for electrons
	0.0 sec for holes
N_{ref}	1.0x10^{16}cm^{-3}
γ	1.0

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