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Impacts of Geometrical Aspect Ratio on Drivability and Short-Channel-Effects of Multi-Gate SOI MOSFET's

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Abstract

This paper proposes a design guideline for the aspect ratio ($R_{h/w}$) of the fin height (h) to fin width (w) of 3-D devices (FinFET like double-gate (DG) FET and triple-gate (TG)-FET) that is based on device simulations. Since any change in the aspect ratio yields the trade-off between drivability and short-channel effects, it is shown that optimization of the aspect ratio is essential in designing 3-D architectural devices. We found that the increase in w seems to bring a high drive current (I_{on}) and an enhancement of I_{on}, but that a large w is undesirable for shorter channel length (L) devices because the drain-induced barrier lowering (DIBL) effect is enhanced; TG-FET is superior to FinFET in terms of both drivability and short-channel effects. In addition, we found that the guideline of $w < L/3$ is essential for suppression of the short-channel effects of TG-FET's. We conclude, therefore, that a narrow, high fin is best for high performance TG-FET's that offer suppressed short-channel effects.

1. Introduction

As MOSFET's continue to be aggressively scaled in order to suppress short-channel effects (SCE's) and to advance device performance, the physical limit of conventional scaling is imminent[1]. In order to overcome this difficulty, the performance of 3-D devices has been investigated; for example, FinFET such as double-gate (DG) FET and triple-gate (TG) FET[2, 3] have been extensively studied, because it can be expected that mature devices will sufficiently suppress the SCE's and have high drivability[4]. However, such 3-D architectural devices cause new aspects or problems, such as the corner effect[5], and switching performance is sensitive to geometrical parameters[6]; driving current (I_{on}) and SCE's are also significantly influenced by geometrical parameters. Y. Liu et al. discussed the impact of the cross-section (aspect ratios ($R_{h/w}$) of the Si-fin height (h) to fin width (w)) of FinFET on SCE's[4]. J.-W. Yang and J. G. Fossum compared the performances of double-gate-like FinFET and TG-FET; they concluded that a double-gate-like FinFET is superior to TG-FET from the viewpoint of area penalty. They described a design guideline for double-gate like FinFET, but not for TG-FET[7]. However, taking into consideration various applications and the fabrication technology, it is not clear whether FinFET is actually superior to TG-FET, for FinFET has many disadvantages with regard to drivability and SCE's.

In this paper, we develop, with the aid of 3-D device simulations, a design guideline of

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FinFET and TG-FET; we examine SCE's and the enhancement of I_{on} of FinFET's and TG-FET's against the conventional DG-FET's over a wide range of aspect ratios ($R_{h/w}$ = h/w). Questions of engineering the aspect ratio and trade-off of drivability versus SCE suppression are also discussed.

2. Device Structures and Simulation Model

We applied Synopsis-*DESSIS* to 3-D device simulations[8]. Various device characteristics (drive current (I_{on}), subthreshold swing (*SS*), drain-induced barrier lowering (*DIBL*) and inversion carrier density (N_{tot})) were then evaluated as functions of $R_{h/w}$. The device structures assumed in these simulations are illustrated in Fig. 1, and device parameters are shown in Table I. Fig. 1(a) shows a bird's-eye-view of the devices; Figs. 1(b) and 1(c) show half cross-sectional views of the devices, FinFET and TG-FET, respectively. We simulated only one half of each device in order to reduce the simulation time. This is possible given the symmetry of the device structures. The top gate oxide thickness for FinFET and TG-FET are 40 nm and 2.0 nm, respectively. The gate length (L_g) is given by sum of channel length (L) and twice the 10-nm-long extension region. The silicon body is p-type. Source and drain contacts are put on to the top surface of the fin- i.e., the device has no contact with the side surfaces of the fin. In terms of fabrication concerns, this configuration gives the most realistic device structure[9]. The simulations assume a hydrodynamic transport model because of the very short channel. Since the mobility model significantly influences I-V characteristics, we chose the *Masetti*[10], *Lombardi*[11] and *Hydrodynamic Canali*[12] Models in our simulations[13]. However, the quantum-

Table 1. Device parameters assumed.

Parameters	Values [unit]
Channel length, L	20, 30, 100 [nm]
Top gate oxide thickness, t_{tox}	2, 40 [nm]
Side gate oxide thickness, t_{sox}	2 [nm]
Buried oxide thickness, t_{BOX}	100 [nm]
Si-fin width, w	5 - 40 [nm]
Si-fin height, h	5 - 40 [nm]
Si-fin doping conc., Na (p-type)	$1x10^{17}$ [cm^{-3}]
Source/drain doping conc., N_d (n-type)	$1x10^{20}$ [cm^{-3}]

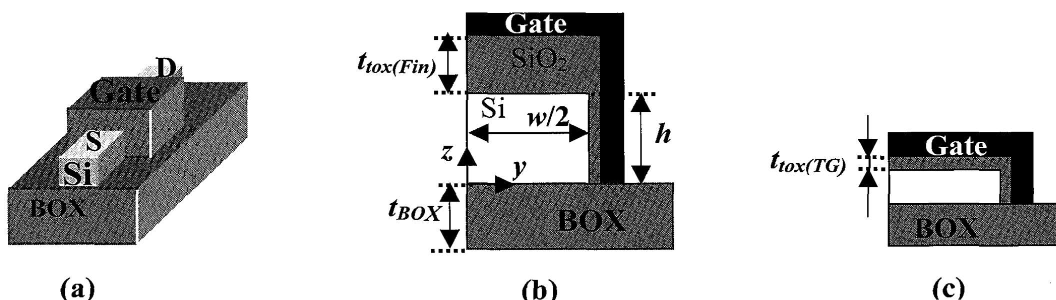


Fig. 1 Schematics of 3-D FET simulated.
(a) Bird's-eye-view of 3-D FET
(b) A half cross-sectional view of FinFET structure
(c) A half cross-sectional view of TG-FET structure

effect models are not included because the Si-fin is wider than 5 nm. Distinct quantum effects were ignored because they only slightly influence device characteristics[14].

3. Results and Discussions

3.1 Influence of aspect ratio ($R_{h/w}$) on short-channel effects

We must pay attention to the short-channel effects of FinFET and TG-FET because they have unusual 3-D structures[15]. Since drain-induced barrier lowering (*DIBL*) plays a significant role in short-channel devices[16], we examined the threshold voltage (V_{th}) from the viewpoint of the influence of drain potential, and the subthreshold swing (*SS*) in terms of geometrical factors.

At first, we will discuss the influences on V_{th} due to the drain potential. We extract a guideline that suppresses the short-channel effects of threshold voltage (V_{th}) from curves shown in Fig. 2. In Fig. 2, the $R_{h/w}$ dependence of *DIBL* (degradation of V_{th}) is shown for the case of fixed-*h* value or fixed-*w* value, where the *DIBL* is defined as $|\Delta V_{th}/\Delta V_d|$ $(=|V_{th\ (Vd=1.0\ [V])}-V_{th\ (Vd=0.1\ [V])}|/0.9)$[17]. It should be noted in the case of the fixed-*h* value that short-channel effects are significantly enhanced as *w* increases, while in the case of the fixed-*w* value, a wide variation of *h* yields little influence on the *DIBL* value. Generally speaking, a large *w* is undesirable in fin-type devices because the *DIBL* is enhanced[4]. FinFET shows a stronger *DIBL* effect than TG-FET, which indicates that, as expected, TG-FET is more suitable for suppressing the *DIBL*. This feature stems from the successful body potential control imposed by the top-gate-induced electric field in TG-FET. Therefore, we should employ TG-FET with a large $R_{h/w}$ value when we narrow the fin in order to suppress *DIBL* effects.

Next, we will discuss the influence of geometrical parameters on *SS*. In Fig. 3, $R_{h/w}$ dependence of ΔSS (degradation of *SS*) is shown in two different conditions, where ΔSS is defined as $SS_{(L=30\ nm)}-SS_{(L=100\ nm)}$ at V_d= 1 V. ΔSS is insensitive to $R_{h/w}$ for the fixed-*h* condition, while it rapidly falls as $R_{h/w}$ increases (or *w* is reduced). Accordingly, we can readily see that

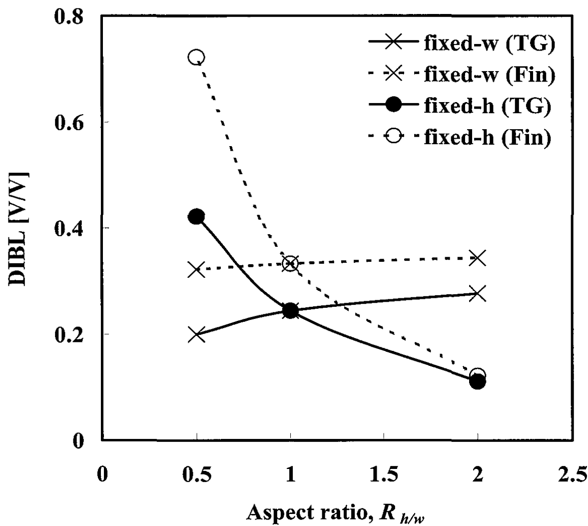


Fig. 2 Aspect ratio dependence of DIBL for 30-nm-channel device. DIBL is defined as $|\Delta V_{th}/\Delta V_d|$ $(=|V_{th}(V_d=1)-V_{th}(V_d=0.1)|/0.9)$.

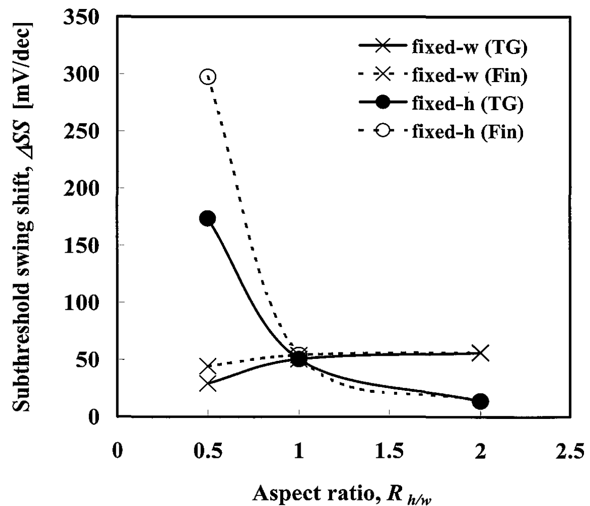


Fig. 3 Aspect ratio dependence of ΔSS at V_d = 1 [V] for 30-nm-channel device. ΔSS is defined as $SS(L=30\ [nm])-SS(L=100\ [nm])$.

the *DIBL* behavior is quite similar to ΔSS, as shown in Fig. 2; we can see that the fundamental mechanism is the same. By tuning $R_{h/w}$ for the fixed h value, we could realize a very small *DIBL* value of 0.1 V/V and a very small ΔSS value of 10 mV/dec.

In the present TG-FET or FinFET, $R_{h/w}$=2 is the best solution, as it satisfies the condition of $w<L/3$. T. Skotnicki et al. have already shown the guideline of $w<L/3$ for 2-D planar devices, but not for 3-D devices[1]. This confirms the value of this work. To examine the validity of this tentative guideline, we simulated I_{on} and SS for the fixed-w value of 10 nm as a function of $R_{h/w}$. Simulation results for 30-nm-channel devices are shown in Fig. 4. It is interesting to see that SS is smaller than 80 mV/dec, and that the large I_{on} and the small SS have a trade-off relation regardless of device structure. The present guideline of $w<L/3$ is very practical in terms of suppressing the standby power consumption. Tow further issues faced by the present guideline will be considered later.

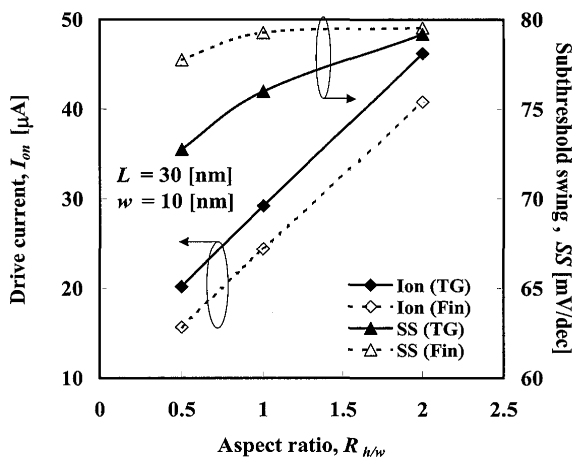


Fig. 4 Aspect ratio dependence of drive current and subthreshold swing of 30-nm-channel device with w of 10 nm at V_d = 1 [V]. Dashed line and solid line denote the simulation results for FinFET and TG-FET, respectively. Square symbols and triangular symbols denote I_{on} and SS, respectively.

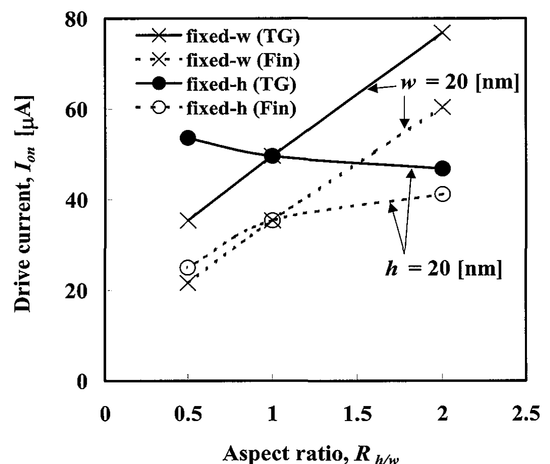


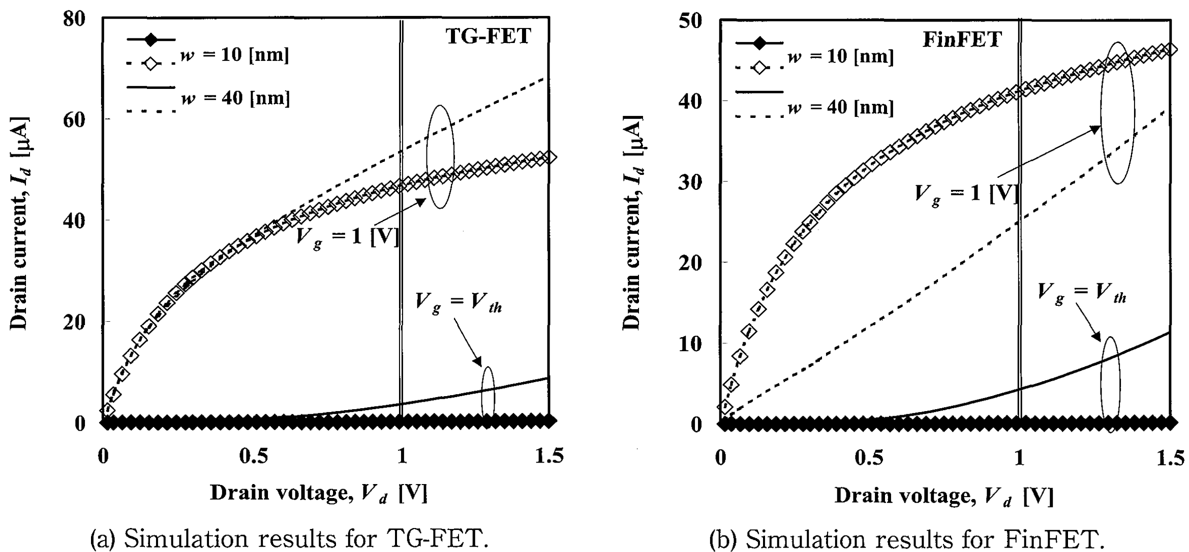
Fig. 5 Aspect ratio dependence of drive current at V_d = 1 [V] for 30-nm-channel device. Solid line and dashed line denote the results for TG-FET and FinFET, respectively. Cross symbols and circle symbols denote the results for the fixed-w of 20 nm and fixed-h of 20 nm, respectively.

3.2 Influence of aspect ratio ($R_{h/w}$) on drivability

Fig. 5 shows I_{on} dependence on aspect ratio ($R_{h/w}$) for 30-nm-channel FinFET and TG-FET. One group of curves is calculated for a fixed-h value of 20 nm and the other group for a fixed-w value of 20 nm, where the threshold voltage (V_{th}) is fixed at 0.25 V by changing the work function of the gate electrode. I_{on} is defined as the drain current (I_d) at V_g=V_d=1.0 [V]. In the case of a fixed-w value, I_{on} increases steadily as $R_{h/w}$ increases (h increases), regardless of device structure. This is because the increase in h (fin height) naturally yields an increase in channel width for both devices. However, we can see that the I_{on} of TG-FET is higher than that of FinFET, regardless of $R_{h/w}$. This means that the conductive channel below the top gate contributes to I_{on}. In contrast, I_{on} increases as $R_{h/w}$ falls (increase in w) in the case of a fixed-h value of 20 nm for TG-FET, while I_{on} decreases as $R_{h/w}$ falls (increase in w) in the case of a fixed-h value of 20 nm for FinFET. For TG-FET, the increase in I_{on} can be readily understood

because the conductive channel created below the top gate is widened as w increases. For FinFET, however, the decrease in I_{on} may stem from a lessening of the volume inversion effect [18].

We then considered whether this mechanism comes from the SCE's. Fig. 6 shows I_d-V_d characteristics for 30-nm-channel TG-FET (in Fig. 6(a)) and for 30-nm-channel FinFET (in Fig. 6(b)) for two different w values. It is assumed that h = 20 nm. The solid double line shows the condition of power supply voltage assumed here (V_d=1 [V]). In Fig. 6(a), we can see that I_d of the TG-FET with 40-nm w is larger than that of the TG-FET with 10-nm w, regardless of V_g condition. In addition, I_d of the 40-nm-w TG-EFT does not become saturated, while that of 10-nm-w TG-FET becomes saturated at V_g= 1 [V]. The former (the behavior of the 40-nm-w device) is due to the punch-through phenomenon (i. e., the fatal case of *DIBL*) as mentioned previously. An unusual drain current is established as V_d increases at the threshold condition in the 40-nm-w device. It is thought that the electrons near the fin bottom contribute to the present unusual Id behavior. For TG-FET, the increase in w suggests an increase in the effective channel width. In Fig. 6(b), on the other hand, I_d of 40-nm-w FinFET is smaller than that of 10-nm-w FinFET at V_g = 1 [V]. I_d of 40-nm-w device doesn't become saturated. At the threshold condition, I_d of 40-nm-w FinFET is much larger than that of 10-nm-w FinFET. These aspects of I_d behavior indicate that the controllability of the top gate is poor because of the thick gate oxide below the top gate electrode. Therefore, increasing the fin-width of short-channel FinFET's does not yield high drivability.



(a) Simulation results for TG-FET. (b) Simulation results for FinFET.

Fig. 6 I_d-V_d characteristics of 30-nm-channel TG-FET and 30-nm-channel FinFET for two different fin widths (w). The double solid line indicates V_d = 1.0 [V]. Diamond symbols denote simulation results for w = 10 nm, while symbol-less curves are for w = 40 nm. Solid lines and dashed lines denote I_d characteristics at V_g = V_{th} and V_g = 1 [V], respectively.

3.3 Advantages of TG-FET

In order to examine more carefully the advantages of TG-FET, we will consider the enhancement of I_{on} of TG-FET in relation to the planar double-gate (p-DG) SOI MOSFET for various $R_{h/w}$ values. The simulated enhancement rate of I_{on} is shown as a function of $R_{h/w}$ in Fig. 7 for the fixed-h value of 20 nm and the fixed-w value of 20 nm. The enhancement rate is defined by $(I_{on(TG)}$-$I_{on(p\text{-}DG)})/I_{on(p\text{-}DG)}$, where $I_{on(p\text{-}DG)}$ is extracted from 2-D simulations of the p-DG

SOI MOSFET. The enhancement rate increases as $R_{h/w}$ decreases, although for all $R_{h/w}$ values the enhancement rate is larger with fixed-*h* value than it is with fixed-*w* value. This behavior is attributed primarily to the short-channel effects, and secondarily to the contribution of effective top-gate width. The first mechanism is significant in the case of fixed-*h* value. The smaller the value of $R_{h/w}$, the more significant the influence of the short-channel effects becomes; namely, TG-FET with large *w* value suffers from the *DIBL* effect stemming from its 3-D geometry, as was previously discussed. The second mechanism dominates at a large $R_{h/w}$ for fixed-*h* value because the side-gate electrode can almost entirely control the body potential. In other words, the 3-D advantage of TG-FET that can utilize the increase in gate width is mostly lost.

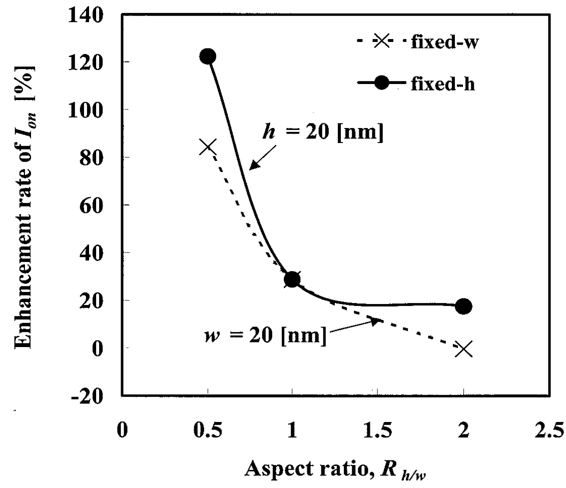


Fig. 7 Aspect ratio dependence of the enhancement rate of I_{on} of TG-FET compared to 2-D planar DG SOI MOSFET. It is assumed that the devices have 30-nm channels, and that I_{on} is calculated at $V_g = V_d = 1$ [V]. Dashed line and solid line denote the results for the fixed-*w* of 20 nm and the fixed-*h* of 20 nm, respectively.

As mentioned above, the enhancement rate for fixed-*h* is larger than that for fixed-*w*. Under the present condition of fixed-*w*, the *w* value does not satisfy the condition of $w<L/3$; the carrier density (N_{tot}) in the fin (not shown here) is lower than that in the present condition of fixed-*h* because of short channel effects, and the enhancement rate is smaller than is true for fixed-*h*. Thus, it can be concluded that, although a large enhancement in I_d cannot be expected, a narrow, high fin is best for realizing high performance TG-FET's because the short-channel effects are sufficiently suppressed,

3.4 Design guideline of 3-D FET's

The short-channel effect is still one of the more serious problems in short-channel 3-D FETs. $R_{h/w}$ should be large (i.e., *w* should be small) when the *h* value is fixed, so as to achieve the condition of $w<L/3$. It should be noted that the apparent enhancement of I_{on} (see Fig. 7) for $R_{h/w} < 1$ is primarily attributed to short-channel effects. The meaningful enhancement rate of I_{on} that we can expect in TG-FET is, at most, only 20 %. In addition, short-channel effects seem to be insensitive to $R_{h/w}$ (or *h* value) for fixed *w* (see Figs. 2 and 3). However, it should be noted that the condition of $w<L/3$ is not satisfied in the range of $R_{h/w}$ examined here. This means that when designing 30-nm-channel FinFETs or TG-FETs with suppressed short-

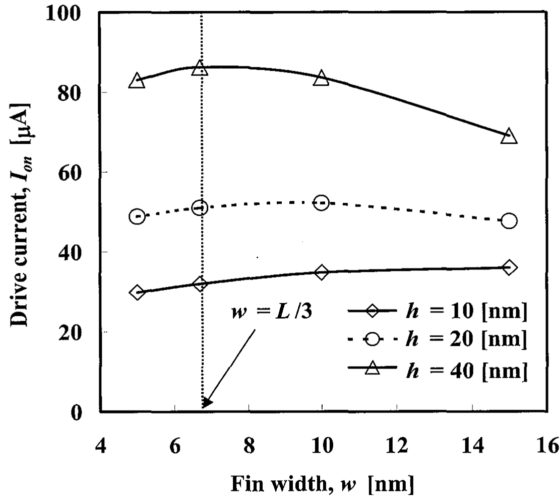


Fig. 8 Fin width dependence of drive current at V_g=V_d =1 [V] for 20-nm-channel TG-FET as a parameter of fin height. Open diamond, open circle and open triangle symbols are the results for h=10, 20, and 40 [nm], respectively. The dotted line indicates the condition of w= L/3.

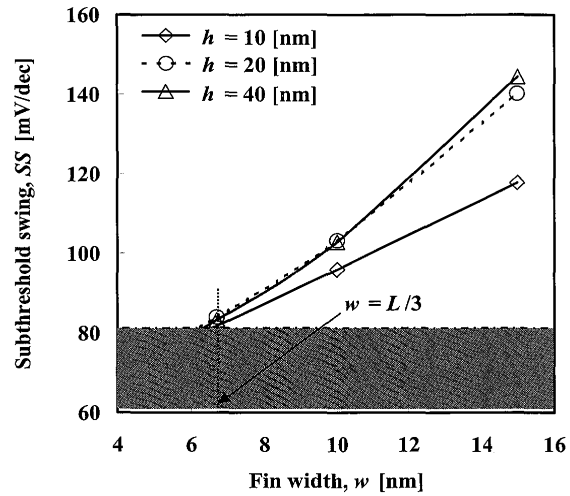


Fig. 9 Fin width dependence of subthreshold swing at V_d= 1 [V] for 20-nm-channel TG-FET as a parameter of fin height. Open square, open circle and open triangle symbols are the results for h = 10, 20, and 40 [nm], respectively. The dotted line indicates the condition of w = L/3. The shaded region satisfies the condition of SS < 80 mV/dec.

channel effects for a certain fixed-w value, we must reduce the fin width w down to 10 nm.

We also investigated the design feasibility of a 20-nm-channel TG-FET. Figs. 8 and 9 show fin width (w) dependence of I_{on} and SS of devices with a specific fin height h, respectively. The dashed line in both Figs. 8 and 9 indicates the condition of w = L/3. It is clearly seen from Fig. 8 that I_{on} rapidly increases as h increases, regardless of w. This can be understood as an increase in channel width, as was mentioned previously. However, we cannot expect a significant enhancement of I_{on} when w increases. In Fig. 9, the shaded region indicates that SS values are under 80mV/dec; in other words, the standby leakage current has been sufficiently suppressed. When w = L/3, SS of 20-nm-channel devices is about 80 mV/dec regardless of h. This means that the present guideline can also be applied in a similar manner to the design of sub-20-nm-channel devices. It is worthwhile to note that SS remains small regardless of h when w<L/3 is satisfied. Expected value of I_{on} should be determined by changing h.

4. Conclusion

In this paper, we studied, with the aid of 3-D device simulations, how the geometric configuration of the fin body influenced the drivability and short-channel effects of FigFET and TG-FET. We successfully extracted a key design guideline of 3-D FETs.

In order to realize 3-D FETs with high drivability, we must select TG-FET that has a large $R_{h/w}$ and a small w, because this combination nicely suppresses the short-channel effects. This primary guideline is correct provided the condition of w<L/3 is satisfied. When one needs a high I_{on} with sufficient suppression of SCE's, a high-fin device should be used, which ensures the proposed guideline is satisfied. In addition, it was demonstrated that the proposed

guideline is valid over a wide range of $R_{h/w}$.

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