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Design Of High Speed ALU Using Vedic Mathematics For Floating And Fixed Point Integers

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Abstract : **In this paper, we present a contrast and also study of numerous adders. Adder's circuit is important for making numerous electronic systems. The Intricacy in VLSI design boosts when the level of combination rises. In this paper, Adder is designed making use of a various method which is based upon MUX based adder; pass transistor, as well as reasoning 2-T logic. The efficiency of the system relies on the efficiency of interior components that are shown in the system. Here, the internal elements should be created in such manner in which, they must take in less power with minimal dead time. The recommended circuit is much better than the existing method concerning area and also hold-up. In several high-performance computing systems such as Digital Signal processors, FIR filters, Microprocessors, and also Microcontrollers, the Multipliers are the key parts where the adders are the standard foundation. The layout as well as the implementation of various 32-bit adders likes Ripple Carry Adder (RCA), Carry Increment adder (CINA) and Lug bypass adder (CBYA) for various full adder cells is done using the Verilog HDL. The outcomes are obtained by implementing Verilog code in Xilinx 14.5 ISE for the Spartan 3E household device with rate quality -5.**

Keywords: **RCA; Ripple Carry Adder; Carry Increment Adder (CINA); Fir Filter**;

1. INTRODUCTION

The needs of electronic devices are getting boosted day by day. Using portable digital gadgets has actually been increased gradually [1] the key demand of the mobile digital device is to lower the power intake and also location as well as to increase the speed of operations. VLSI is a procedure where billions of transistors are embedded onto a small chip. The need for the VLSI Designers is rather high for creating FPGA applications, System on CHIP and also ASIC. The Area along with minimum delay and power usages is one of the essential layout factors to consider for the IC designers in designing mobile digital gadgets and equipment circuits. The reliance of power intake is based on the variety of transistors utilized. The full adder [2] is just one of the fundamental foundations for many of the digital VLSI circuits. An adder is utilized to do addition of numbers. In many computers and also cpus, adders are made use of in Arithmetic as well as Reasoning Units (ALU). They are additionally utilized in various other parts of the cpu, where they are made use of to calculate address table indices, increment and also decrement drivers and comparable procedures. A full adder has three inputs and 2 results which are A, B, C, SUM and CARRY. Dynamic power dissipation contains about 90% of total power consumption it is due to changing task. Little bit switching LFSR reduces this switching activity by lowering number of transitions in between test variables hence bit swapping LFSR types reliable remedy for power intake in testing. Adders have really vital role in digital VLSI circuits. It is used to compute adders, table indices and also other applications. Efficiency of cpu and system, in VLSI can be enhanced by raising rate of adders and also multipliers that is to minimize hold-up.

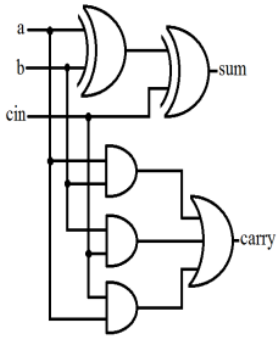

Fig.1.1. Conventional full adder cell[4] (FA).

2. PREVIOUS WORK:

The full adder adds binary numbers as well as accounts for worth's brought in as well as out. The full adders are normally an element and cascade of adders, which adds 8, 16, 32, etc. bit binary numbers. The XOR gate is the standard element of any type of building block of the full adder idea. The efficiency of a complete adder can be enhanced based on the performance of XOR entrance. The previous designs of XOR gateway were based upon 8 transistors or 6 transistors that are traditionally used in most of the styles. The main objective of minimizing the transistor matter is to decrease the size of XOR gateway so that the maximum variety of devices can be configured on a solitary silicon chip therefore minimizing the area as well as hold-up. In the conventional full adder, 2

XOR entrances are made use of whereas in the proposed technique; we have made use of 3 various logic designs which are MUX based full adder which uses only one XOR gateway, pass-transistor logic, as well as 2-T reasoning. Various treatments and also techniques are used to apply n-bit adders like Carry Save Adder, Carry Select Adder, Surge Carry Adder, Carry Look a Head Adder and so on,. All these techniques have their very own one-of-a-kind feature as a benefit. To design broadband adders CLA is utilized due to the fact that the next level bring is depends upon just primary inputs instead of the previous carry and main inputs. The adders plays a key role in ALU due to the fact that a lot of the math procedures performed by the adders. For faster math operations, quick adders called for. To make sure that CLAs are commonly made use of in ALU designs. Apart from the advantage of CLA, it has the drawback of circuit expenses. For every single following level of bring, variety of gates and also number of inputs per a gate also increased. Due to the constraints of number inputs per a gateway, the CLA is limited to 4-bit.

3. PROPOSED SYSTEM

By using carry look-ahead system, the breeding delay is minimized to four-gate degree irrespective of the variety of little bits in the adder. The VDHL equipment description language is made use of to give a gate degree design as well as simulation of each design. A number of differing setups of binary adders exist for inclusion right into ALU layout. VHDL is a general-purpose hardware description language, comparable syntax to the C programming language. VHDL permits different degrees of abstraction to be mixed in the very same version. So a hardware design can be specified interms of switches, entrances, RTL, or behavior code. Now a days most electronic design of cpus and relevant hardware system is created making use of a hardware summary language. Such a language offers 2 functions, first it provides on abstract description of the equipment to replicate as well as debug the layout. Second, with use logic synthesis and also hardware collection tools, this summary can be put together right into the hardware implementation. VHDL offers the principle of module. A module is the fundamental building block in VHDL. A component can be executed in regards to the preferred style formula without issue for the equipment application details. These components can be substituted instead of the 16-bit full adder components described previously without transforming any other element of the simulation. The simulation results will be unchanged.

In bring increment adder, various RCA blocks are used to compute the results. The very first RCA block is provided carry-in as input together with addends to get lug(c1) and amount. For the remainder RCA blocks, the carry-in is given as reasoning '0' to obtain momentary amount (sum1) and short-lived carry which are provided to increment circuit. Increment circuit contains half adders which add short-term sum and carries to obtain the actual amount (sum) and also bring (cy). The carry-out of increment circuit is obtained by carrying out OR operation in between lug (cy) as well as carry-out of the previous stage. As the carry-in for the RCA phases is reasoning '0' as well as therefore the bring breeding delay decreases. The design for the CINA 32bit is given in Fig.

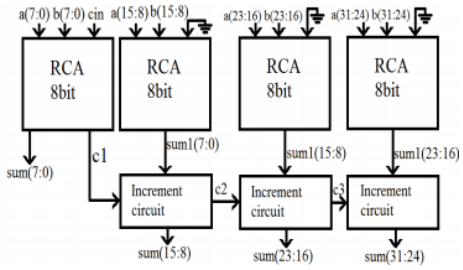

Fig.3.1. 32-bit carry increment adder.

The style objective is to reduce the number of entrances used; procedure speed is not of issue. The circuit is called for in several variations that take care of different information word dimensions, consisting of 4, 8 and 16. Think that we have common gate-level as well as 4-bit register-level elements readily available as foundation. The most affordable cost adders use ripple-carry propagation. 4 4-bit CLAs are interconnected as ripple adder type as shown in the fig. 8. Right here the lug is propagated to the next phase 4-bit CLA. The internal carry proliferation delay of 4-bit adder is lowered by utilizing the technique CLA. To ensure that the general speed of the 16-bit Adder is raised. Additionally the VHDL Primitive is developed by using quicker design elements. So that the sum hold-ups in addition to the bring delay is quite enhanced. For faster Complete Adders creates VHDL Primitive can be made use of to reduce design time and to attain the speed.

ALU was designed to perform the arithmetic and logical operations for the controller. Arithmetic operations performed are the 32-bit addition, subtraction, and multiplication. Logical operations performed are AND, OR, XOR, NAND, NOR, XNOR, NOT and Data Buffer. For designing the ALU, the authors had followed a flexible design that consists of smaller, but more manageable blocks, some of which can be re-used. Designing of half-adder, 2-bit multiplier, 4-bit Brent-Kung, 4-bit multiplier, 8-bit Brent-Kung adder, 8-bit multiplier, 8-bit full adder, 8-bit subtractor, 32-bit Brent-Kung adder, 32-bit multiplier, 32-bit full adder, 32-bit

subtractor, 32-bit arithmetic unit, logical unit and 32-bit ALU has been done.

4. SIMULATION RESULTS

The block diagram shown below fig 1.6 of our design consists Bit Swapping LFSR to generate 16 bit data using 2:1 multiplexer for the adder which is the Circuit Under Test (CUT). we can say that modified CSA with BEC and kogge stone adder instead of ripple carry adder, both along with Bit swapping LFSR as test pattern generator gives minimum delay. Table shows the maximum obtained path delay comparison of different adders. Fig represents simulation results out[0:7] , out[8:15] acts as two 8 bit addends and out as carry in.

ADDERS	DELAY	LUTs	IO Buffers
Ripple Carry Adder	7.670ns	29	10
Carry Select Adder(Full Adder)	8.478ns	30	10
Carry Select Adder(BEC and Kogge stone adder)	6.795ns	33	10

Fig.4.1. Maximum obtained path delay.

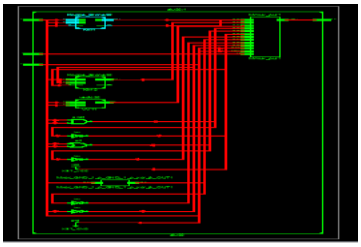

Fig.4.2. schematic output of alu.

Fig.4.3. ALU results.

DIVISION:

FLOATING point arithmetic (FPA) architectures underwent significant advancement by scientific research in the past several decades. FPA is a basic ingredient of a large set of scientific and engineering domain applications. To boost the application performances, the FPA architectures developed from scalar to vector architectures in various processing platforms. Arrays of single precision and double precision computing units are being used for floating point vector processing. The current research work is aimed towards the idea of unified vector-processing units.

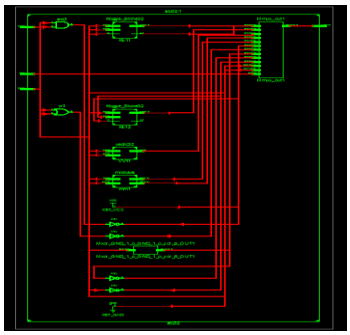

Fig.4.4. Vedic Wallace Divisor 32x32 Schematic Output.

Fig.4.5. Vedic Wallace Divisor 32x32 Simulation Result.

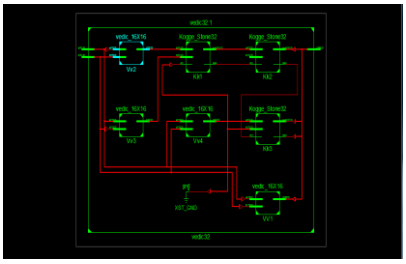

Fig.4.6. Vedic Wallace Multiplier 32x32 Schematic Output for multiplier

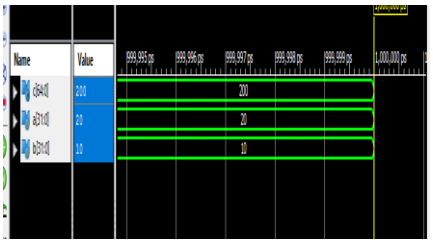

Fig.4.7. Vedic Wallace Multiplier 32x32 Simulation Result.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2445	303600	0%
Number of fully used LUT-FF pairs	0	2445	0%
Number of bonded IOBs	133	700	19%

Fig.4.8. Design summary.

CONCLUSION

It is evident that the LUTs are less for RCA. The LUTs increased by 38% and 59% for CINA and

CBYA respectively. The slices (area) are increased by 37% and 54% for CINA and CBYA respectively when compared with the RCA. The more the fan-out the more the load driving capacity. The fan-out is increased by 23% and 46% for CINA and CBYA respectively when compared with the RCA. However, CBYA with FA1 has 36% less delay than the RCA with FA and hence provides the least delay. It is also evident that the delay produced by opting to modified full adder 2 results in decrease of the delay for RCA, CINA and CBYA. Hence for implementation of RCA, CINA and CBYA, the use of modified full adder as basic cell will improve the performance in terms of the delay provided. Further, this work can be extended in designing and comparing for different sized adders like 64-bit, 128 bit. The work can also be extended in designing and comparing other 32-bit adders like carry save adder and carry skip adder.

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