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Design Of High Performance Comparator Using Mixed Logic Line Decorder

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Abstract: **This paper presents a combined reasoning layout method for line decoders, by combining pass transistor double worth logic, transmission gateway logic and also fixed complementary metal-oxide semiconductor. Two brand-new geographies are presented for the 2-4 decoders, a 14-transistor geography aiming on reducing transistor matter and also power dissipation and also a 15-transistor topology aiming above power-delay efficiency. In each instance both normal as well as inverting decoders are applied, yielding a total amount of four brand-new designs. Moreover, by utilizing mixed-logic 2-4 decoders integrated with basic CMOS blog post decoder, designed 4 new 4-16 decoders. All proposed decoders have full-swinging capability and also reduced transistor matter compared to their traditional CMOS equivalents. Finally, a variety of comparative EZ wave simulations at the 130nm (PYXIS GDK) shows that the recommended circuits provide a substantial improvement in power and delay, exceeding CMOS in almost all situations.**

Keywords: **2-4 Decoders; 4-16 Decoders; CMOS; Mixed Logic Circuits;**

1. INTRODUCTION

Address decoder is essential elements in all SRAM memory block which react to very high frequency. Accessibility time and power usage of memories is greatly figured out by decoder layout. Style of an arbitrary accessibility memory (RAM) is normally divided into two parts, the decoder, which is the wiring from the address input to the word line, and the sense as well as column circuits, which includes the bit line to the data input/output circuits. Because of huge amount of storage cells in memories it can be discovered different remedies of address decoder layouts leading to power intake decrease as well as efficiency improvement. Usually different kinds of pre charging vibrant decoders are made use of. Design of vibrant decoder is complicated as well as having even more likelihood of incorrect sensing. Standard fixed decoder gives extra exact outcome however it is having extra variety of transistors with huge hold-up. Some options use hierarchical decoders with pre decoding and also executed binary tree decoder constructed by De-multiplexers. Decoders plays a crucial role in memory applications so we introduce high-speed a mixed-logic layout technique for line decoders. Address decoder using NAND-NOR alternating phases with pre decoder and also reproduction inverter chain circuit is suggested and also compared to conventional and also global block design, utilizing 130nm CMOS modern technology. Postpone and power dissipation is decreased in proposed layout over existed layout. Just recently reported reasoning design contrasts based upon full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power reliable than corresponding CMOS. Broadband multiplier is executed with the help of Corresponding Pass transistor Reasoning (CPL) is a household of CMOS layout. Same CPL strategy is made use of to apply Math as well as Logic Device [ALU] in for raising the design rate. Transmission button theory is presented which is used for CMOS electronic circuit design. Facility reasoning gate is carried out in based upon pass transistor twin voltage reasoning for reduced power applications. Paper defines concerning create a Karnaugh map based method that can be made use of to efficiently manufacture pass transistor logic circuits, which have balanced lots on true and complementary input signals. The approach is related to the generation of fundamental two-input as well as three-input logic gateways in CPL, DPL as well as DVL. The approach is basic and can be extended to synthesize any type of pass-transistor network. Over papers describes different methods to execute reasoning designs which offers better because terms of location, hold-up as well as power intake.

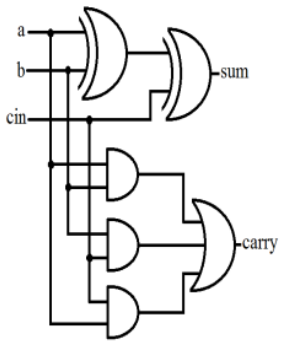

Fig.1.1. Conventional full adder cell[4] (FA).

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2. PREVIOUS WORK:

The regularly producing variety of transistors made up on a chip as well as the growing transistors trading rate in late years has allowed uncommon execution change in COMPUTER frameworks by a number of solicitations of nefariousness. Grievously, such stunning execution enhancements have actually been joined by a growth in power and insistence dispersal of the frameworks. Higher power and insistence scrambling in top quality systems need all the more expensive squeezing and cooling advancements, boost cost as well as decomposes structure steady top quality. Power dispersal is depicted as the rate of imperativeness handed down from resource to structure/device. Power minimization is among the standard stress and anxieties in today VLSI design procedures in viewpoint of the necessary reasons. One is the lengthy battery working life important of versatile and helpful gizmos and second is a straight result of extending variety of transistors on only chip prompts higher power spreading as well as it can provoke unflinching quality as well as IC product packaging problems. The reduced power needs of existing digital systems have tried the sensible research study in the direction of the assessment of mechanical, building and also circuital plans that enable a decreasing of the essentialness scattered by a digital circuit. Among the major vehicle drivers of insistence dispersing in CMOS circuits is a direct result of the charging and also releasing of the center factor capacitances of the circuits, present both as a pile and a bloodsucker. Such little the total power scattered by a circuit is called dynamic power. To minimize the vibrant power, an optional approach to manage the common systems of vigor usage decrease, called adiabatic trading has actually been suggested in the current years. In such method, the course towards charging as well as discharging the center factor capacitances is handed down in such a way so little step of imperativeness is misused as well as a healing of the essentialness established away on the capacitors is specialist.

3. PROPOSED SYSTEM

In digital systems, discrete quantities of informationare represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined here are n-to-m line decoders, which generate the m = 2n minterms of n input variables.

2–4 Line Decoders

A 2–4 line decoder generates the 4 minterms D0−3 of 2 input variables A and B. Its logic operation is summarized in Table I. Depending on the input combination; one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2–4 decoder generates the complementary minterms I0−3, thus the selected output is set to 0 and the rest are set to 1. In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gates, whereas an inverting decoder requires 2 inverters and 4 NAND gates, both yielding 20 transistors.

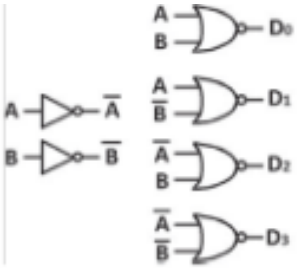

Fig.3.1. 2–4 line decoders implemented with CMOS logic.

4–16 Line Decoder

With 2–4 Predecoders A 4–16 line decoder generates the 16 minterms D0−15 of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minterms I0−15. Such circuits can be implemented using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2n predecoded lines that serve as inputs to the final stage decoder. Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates, and an inverting one can be implemented with 2 2–4 decoders and 16 2- input NAND gates. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

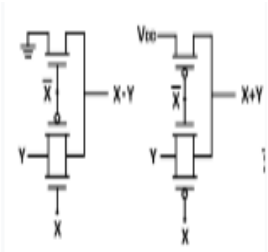

Fig.3.2 CMOS logic.

4. SIMULATION RESULTS

Proposed system of the project is done using 32 nm technology. CMOS Logic used in the project for 32 nm technology provides the layout design for a particular circuit which shows the area and the power required to design a circuit. In the extension

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of the project 18nm technology is used. Change in the nanometer technology gives the power difference. With the decrease in the nanometer technology in the extension particular area and power required for the 2-4 4-16 decoder will be reduced. The extension process is exactly similar to the proposed one but when nanometer technology is changed in the software, VDD and Vbias changes which lets the output to give high performance than the proposed system.

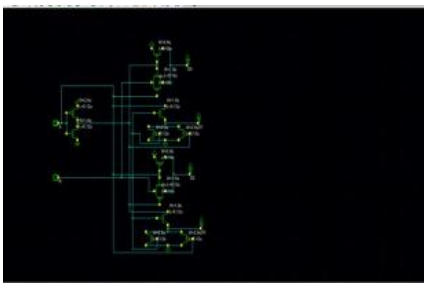

Fig.4.1. Simulation module.

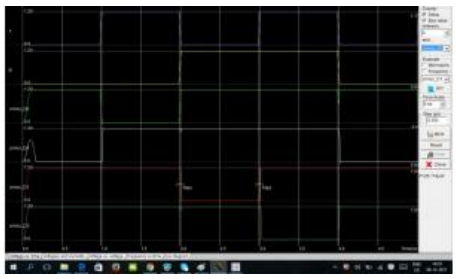

Fig.4.2. schematic design, layout design and waveforms of 2-4 inverting low power decoder.

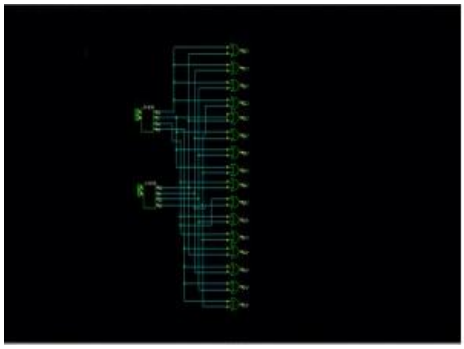

Fig.4.3. Simulation model 2.

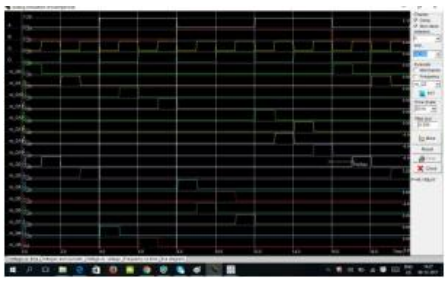

Fig.4.4. schematic design, layout design and waveforms of 4-16 high performance decoder

5. CONCLUSION

The proposed method we have use mixed logic to design line decoders so that we achieve less delay, and also reduced number of gates. So that the area for the design will be reduced and also power consumption is less. It is possible that if the power is reduced then the temperature will also get reduced. Thus we propose the above design for area efficient and low power consumption for decoders.

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