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Probability-Driven Multi-Bit Flip-Flop Integration With Clock Gating

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Abstract: **Data-driven clock gated (DDCG) and multi bit flip-flops (MBFFs) are two low-power design techniques that are usually treated separately. Combining these techniques into a single grouping algorithm and design flow enables further power savings. We study MBFF multiplicity and its synergy with FF data-to-clock toggling probabilities. A probabilistic model is implemented to maximize the expected energy savings by grouping FFs in increasing order of their data-to-clock toggling probabilities. We present a front-end design flow, guided by physical layout considerations for a 65-nm 32-bit MIPS and a 28-nm industrial network processor. It is shown to achieve the power savings of 23% and 17%, respectively, compared with designs with ordinary FFs. About half of the savings was due to integrating the DDCG into the MBFFs. The proposed architecture of this paper analysis the logic size, area and power consumption using Tanner tool.**

Key words: **MBFF, DDCG, FFS, MIPS, Industrial Network Processor, Data To Clocking Toggling.**

I. INTRODUCTION

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of mixes and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree. Clock gating logic can be added into a design in a variety of ways: 1. Coded into the RTL code as enable conditions that can be automatically translated into clock gating logic by synthesis tools (fine grain clock gating). 2. Inserted into the design manually by the RTL designers (typically as module level clock gating) by instantiating library specific ICG (Integrated Clock Gating) cells to gate the clocks of specific modules or registers. 3. Semi-automatically inserted into the RTL by automated clock gating tools. These tools either insert ICG cells into the RTL, or add enable conditions into the RTL code. These typically also offer sequential clock gating optimizations.

II. LITERATURE SURVEY

Clock power is the major contributor to dynamic power for modern integrated circuit design. A conventional single-bit flip-flop cell uses an inverter chain with high drive strength to drive the clock signal. Clustering several such cells and forming a multibit flip-flop can share the drive strength, dynamic power, and area of the inverter chain, and can even save the clock network power and facilitate the skew control. Hence, in this paper, we focus on post placement multibit flip-flop clustering to gain these benefits. Utilizing the properties of Manhattan distance and coordinate transformation, we model the problem instance by two interval graphs and use a pair of linear-sized sequences as our representation. Digital System Clocking is assuming ever greater importance as clock speeds increase, doubling every three years. This the first book to focus entirely on clocked storage elements, "Flip-Flops" or Latches"—provides an in-depth introduction to the subject for both professional computer design engineers and graduate-level computer engineering students. In Digital System Clocking: High-Performance and Low-Power Aspects, you will find information on. Our method simultaneously performs (1) activityaware register clustering that reduces clock tree power not only by clumping registers into a smaller area, but pulling the registers with similar activity pattern close to shut off more time for the resultant sub trees; (2) timing and activity based net weighting that reduce net switching power by assigning a combination of activity and timing weights to the nets with higher switching rates or more critical timing; (3) gate control logic optimization that still set the gate enable signal high if a register is active

III. EXISTING SYSTEM

The data of digital systems are usually stored in flip-flops (FFs),each of which has its own internal clock driver. In an attempt to reduce the clock power, several FFs can be grouped into a module called a multi bit FF (MBFF) that houses the clock drivers of all the underlying FFs. We denote the grouping of kFFs into an MBFF by a k-MBFF. Kapoor et al. reported a 15% reduction of the total dynamic power in a 90-nm processor design. Electronic design automation tools, such as Cadence Liberate, support MBFF characterization. The benefits of MBFFs do not come for free. By sharing common drivers, the clock slew rate is degraded, thus causing a larger short-circuit current and a longer clock-to-Q propagation delay tp CQ.

To remedy this, the MBFF internal drivers can be strengthened at the cost of some extra power. It is therefore recommended to apply the MBFF at the RTL design level to avoid the timing closure hurdles caused by the introduction of the MBFF at the backend design stage. Due to the fact that the average data-to-clock toggling ratio of FFsis very small, which usually ranges from 0.01 to 0.1, the clock power savings always outweigh the short-circuit power penalty of the data toggling. An MBFF grouping should be driven by logical, structural, and FF activity considerations. While FFs grouping at the layout level have been studied thoroughly, the front-end implications of MBFF group size and how it affects clock gating (CG) has attracted little attention. This brief responds to two questions. The first is what the optimal bit multiplicity k of data-driven clock-gated (DDCG) MBFFs should be. The second is how to maximize the power savings based on data-to-clock toggling ratio (also termed activity and data toggling probability).

IV. PROPOSED SYSTEM

Clearly, the best grouping of FFs that minimizes the energy consumption can be achieved for FFs whose toggling is highly correlated. Using toggling correlations for MBFF grouping has the drawback of requiring early knowledge of the value change dump vectors of a typical workload. Such data may not exist in the early design stage. More commonly available information is the average toggling bulk probability of each FF in the design, which can be estimated from earlier designs or the functional knowledge of modules. FFs' toggling probabilities are usually different from each other. An important question is therefore how they affect their grouping. We show below that data-to-clock toggling probabilities matter and should be considered for energy minimization.

In the following paragraphs, we combine the activity p and the MBFF multiplicity k in a design flow aimed at minimizing the expected wasted energy. Fig. illustrates that the power savings of the 2-MBFF, 4-MBFF, and 8-MBFF, respectively, are used. Knowing the activity p of an FF, the decision as to which MBFF size kit best fits follows the interim lines, lines (d). To obtain the per-bit power consumption, lines (d) in Fig, representing an MBFF realistic operation, were divided by their respective multiplicity. The result is shown in Fig. Figure Power consumption ofk1-bit FFs compared to k-MBFF: 2-MBFF (a), 4-MBFF (b) and 8-MBFF (c). Line (a) is the power consumed byk1-bit FFs driven independently of each other. Line (b) is the ideal case of simultaneous (identical) toggling. Line (c) is the worst case of exclusive (disjoint) toggling. Line (d) is an example of realistic toggling. To maximize the power savings, Fig. 3 divides the range of FF activity into regions. The black line follows the power consumed by a 1-bit UN gated FF. The triangular areas bounded by the black line and each of the green, blue, and red per-bit lines show the amount of power savings per activity obtained by grouping an FF in the2-MBFF, 4-MBFF, and 8-MBFF, respectively. It shows that for a very low activity, it pays to group FFs into an 8-MBFF. As activity increases, there will be some point where the 4-MBFF over takes and pays off more than the 8-MBFF. At some higher activity, the2-MBFF overtakes and pays off more than the 4-MBFF, up to an activity where the power savings stops. The remaining FFs can be grouped into UN gated MBFFs, simply to reduce the number of internal.

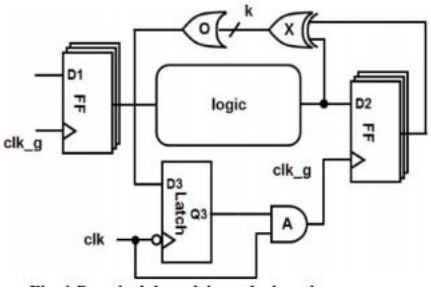

Fig.4.1. Practical data-driven clock gating.

V. RESULTS

Estimating the FFs toggling probabilities involves running an extensive test bench representing typical operation modes of the system to determine the size k of a gated FF group by solving (1). 2) Running the placement tool in hand to get preliminary preferred locations of FFs in the layout. 3) Employing a FFs grouping tool to implement the model and algorithms presented in Sections III and IV, using the toggling correlation data obtained in Step 1 and FF locations' data obtained in Step 2. The outcome of this step is k-size FF sets (with manual overrides if required), where the FFs in each set will be jointly clocked by

a common gater. Introducing the data-driven clock gating logic into the hardware description (we use Verilog HDL). This is done automatically by a software tool, adding appropriate Verilog code to implement the logic described in Fig. The FFs are connected according to the grouping obtained in Step 3. A delicate practical question is whether to introduce the gating logic into RTL or gate-level description. This depends on design methodology in use and its discussion is beyond the scope of this paper. We have introduced the gating logic into the RTL description.

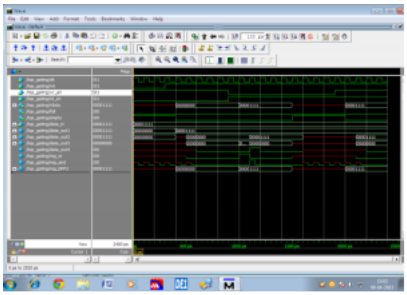

Fig. 5.1 Output Waveform of Clock Gated Synchronous FIFO

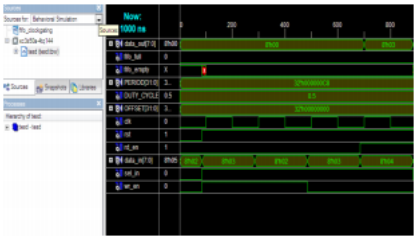

Fig.5.2. Output Wave form of Synchronous FIFO Using Multibit Flipflop with Data Driven Clock Gating.

VI. CONCLUSION

Clock gating is used in fifo to reduce the power consumption. For further power saving data driven clock gating and multibit flip-flops are used in sequential circuits. Common clock gating is used for power saving. But clock gating still leaves larger amount of redundant clock pulses. Multibit flip-flop is also used to reduce power consumption. Using of Multibit Flip-Flop method is to eliminate the total inverter number by sharing the inverters in the flipflops. Combination of Multibit Flip-Flop with Data driven clock gating will increase the further power saving. Xilinx software tool is used for implementing this proposed system. The combination of data-driven gating with MBFF in an attempt to yield further power savings.

VII. REFERENCES

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