Recognition And Abolition Of Error Byusing Approximate Adder

MALE KONDAL GOUD
M. Tech student, Dept of ECE, Nishitha College of Engineering & Technology, Hyderabad, TS, India.

J SHIVA SHANKAR
Assistant Professor, Dept of ECE, Nishitha College of Engineering & Technology, Hyderabad, TS, India.

Abstract: **Approximate computing is emerging as a new paradigm to improve digital circuit performance by relaxing the requirement of performing exact calculations. Approximate adders rely on the idea that for uniformly distributed inputs, long carry-propagation chains are rarely activated. Unfortunately, however, the above assumption on input signal statistics is not always verified; in this paper we focus on the case when the inputs have a Gaussian distribution. We show that for Gaussian inputs the error probability of previously proposed approximate adders approaches 25% for low sigma values, which is much larger than the uniform case. On the basis of this analysis, we propose an approximate adder with a correction circuit that drastically reduces the error rate for Gaussian distributed operands. In order to investigate the performance of our approach in a real application, simulated results for a simple audio processing system are reported. Implementation results in 65nm technology are also presented.**

Keywords: **Multiplexer, ACA, Error Correction, Adder, Distribution, Accuracy, Efficiency.**

I. INTRODUCTION

Many applications from domains such as machine learning, image and video processing can tolerate errors in their arithmetic operations without affecting the end user experience. This feature can be used to design arithmetic circuits which are faster, consume less power and area, while making a trade-off with the accuracy of the output. The focus of the current paper is on approximate adder circuits which have been studied earlier in various works. These designs do not allow for configuring the accuracy of a circuit dynamically during the runtime. Dynamic reconfiguration has many applications such as when a mobile phone is low on battery we can switch to a very low power mode by sacrificing accuracy. Another example is that in a complex signal processing circuit, different component arithmetic circuits can be configured to different accuracy levels based on their impact on the final output of the DSP block. Many applications from domains such as machine learning, image and video processing can tolerate errors in their arithmetic operations without affecting the end user experience. This feature can be used to design arithmetic circuits which are faster, consume less power and area, while making a trade-off with the accuracy of the output. The focus of the current paper is on approximate adder circuits which have been studied earlier in various works. The main problem associated with ACA/GeAr adders is that most of the correction stages have to be enabled to make enhancement in the more significant bits of the result. This makes them perform poorer than accurate adders like CLA even in a pipelined implementation. The other adder, GDA, suffers from two drawbacks. First, it has no error detection and correction mechanism, and second, GDA in its scope, cannot be pipelined, which results in greater delays to get results of higher accuracy. The goal of correction part is to make the inaccurate result closer to the accurate one after each stage of correction. Correcting the least-significant sub-adders first is not good because this makes a little difference in the accuracy of the output as it is still far away from the accurate result.

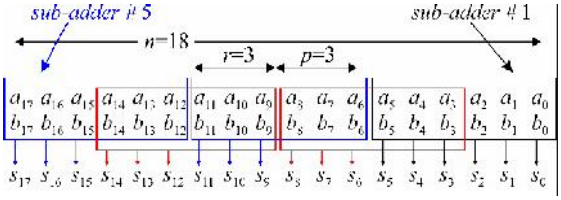

Fig.1.1. SCL function diagram.

II. RELATED STUDY

In order to improve the error rate for Gaussian distributed operands, we propose a simple heuristic approximate adder with output correction circuit. From previous section, we know that an error occurs whenever A and B have opposite signs, A+B>0 (while the speculative adder fails giving a negative sum) and both |A| and |B| are sufficiently small (so that the sum A+B is also small). In the architecture of Fig. 5, the first condition is checked by computing the xor between the MSBs of the two operands; the second condition occurs when the speculative adder output is negative and hence is signalled by the MSB of the last sub-adder. In order to check the third condition, we perform the nor between the L MSBs of the first sub-adder: this signal will be high whenever the sum output is positive and is smaller that 2(r+p−L). When the three conditions are verified, the output is assumed to be the positive value produced by the first sub-adder: the signal E1 in Fig. 5 is low and all the outputs from the second through the last subadder

are driven to zero. Similarly, we check the L MSBs of the second sub-adder: if they are all zero (and the other two above mentioned conditions are verified) the signal E2 in Fig. 5 is low and all the outputs from the third through the last subadder are driven to zero. Proposed an accuracy configurable adder circuit called Gracefully-degrading adder (GDA) which allows for reconfigurable sub-adder widths and carry chain considerations during runtime. It uses carry prediction units which can be both approximate and correct. It has no error detection unit. The correction techniques employed in above adders require more power and clock cycles to arrive at results with significant accuracy, which makes them perform poorer than correct adders when high accuracy is needed.

III. AN OVERVIEW OF PROPOSED SYSTEM

Accuracy in amplitude or Ac $_{camp}$ is defined as Ro/Rc * 100, where Ro is the obtained result and Rc is the correct result. We can say error amplitude Er $_{ramp}$ = 100 – Ac $_{camp}$. Figure 4a shows a error histogram of results obtained after stage1 correction by the two techniques. Each point E on the x-axis represents that the output error magnitude is in range E-1 to E%, (E-1 exclusive), and the y-axis shows the number of errors. For example, the bar plotted on x=2, gives the number of errors with magnitude 1 to 2% and so on. As can be seen clearly from the graph, for Ac $_{curus}$, most of the errors have magnitude of 0 to 1%, and there are fewer errors with higher magnitude, as compared to the conventional technique, where most errors lie in higher magnitude side. This demonstrates the efficiency of Ac$_{curus}$. In the figure, the red bars are overlapped over the blue ones for facilitating clarity in graph. Similarly, figure 4b shows the results after stage2 of correction. Here, for Accrues, almost all of the results lie in 0 to 1%, while very little improvement is seen for conventional technique.

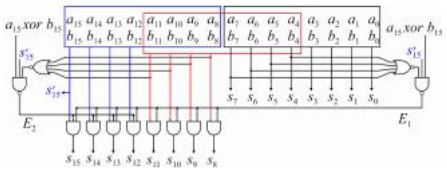

Fig.3.1. Proposed system.

The main problem associated with ACA/GeAr adders is that most of the correction stages have to be enabled to make enhancement in the more significant bits of the result. This makes them perform poorer than accurate adders like CLA even in a pipelined implementation. The other adder, GDA, suffers from two drawbacks. First, it has no error detection and correction mechanism, and second, GDA in its scope, cannot be pipelined, which results in greater delays to get results of higher accuracy.

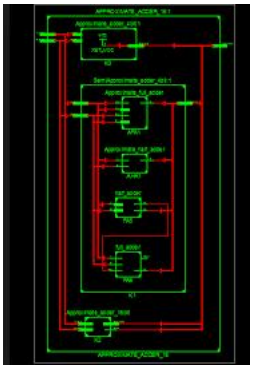

Fig.3.2. Design model.

IV. CONCLUSION

In this paper, we proposed a new approach for designing accuracy configurable adder circuits. The main idea is that by performing arithmetic from MSB first to LSB, we get very good estimates of the result within the initial stages of the computational pipeline. The idea although simple yields substantial benefits over the existing approaches. We believe this technique can be extended to other arithmetic operations such as multiplications.

V. REFERENCES

[1] V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, “Impact: Imprecise adders for low-power approximate computing,” in Low Power Electronics and Design (ISLPED) 2011 International Symposium on, Aug 2011, pp. 409–414.

[2] S.-L. Lu, “Speeding up processing with approximation circuits,” Computer, vol. 37, no. 3, pp. 67–73, Mar 2004.

[3] N. Zhu, W. L. Goh, and K. S. Yeo, “An enhanced low-power highspeed adder for error-tolerant application,” in Integrated Circuits, ISIC ’09. Proceedings of the 2009 12th International Symposium on, Dec 2009, pp. 69–72.

[4] N. Zhu, W. L. Goh, W. Zhang, K. S. Yeo, and Z. H. Kong, “Design of low-power high-speed truncation-error-tolerant adder and its application in digital signal processing,” Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 18, no. 8, pp. 1225–1229, Aug 2010.

[5] P. Kulkarni, P. Gupta, and M. Ercegovac, “Trading accuracy for power with an under designed multiplier architecture,” in VLSI Design (VLSI Design), 2011 24th

International Conference on, Jan 2011, pp. 346–351.

[6] A. B. Kahng and S. Kang, "Accuracy-configurable adder for approximate arithmetic designs," in Proceedings of the 49th Annual Design Automation Conference, ser. DAC '12. New York, NY, USA: ACM, 2012, pp. 820–825.

[7] M. Shafique, W. Ahmad, R. Hafiz, and J. Henkel, "A low latency generic accuracy configurable adder," in Proceedings of the 52Nd Annual Design Automation Conference, ser. DAC '15. New York, NY, USA: ACM, 2015, pp. 86:1–86:6.

[8] A. Verma, P. Brisk, and P. Ienne, "Variable latency speculative addition: A new paradigm for arithmetic circuit design," in Design, Automation and Test in Europe, 2008. DATE '08, March 2008, pp. 1250–1255.

