B Raju* et al.
(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH
Volume No.6, Issue No.6, October - November 2018, 8897-8898

Design And Accomplishment Of Sleep Convention Logic With High Accuracy

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Abstract: **Sigma-Delta (∑-Δ) analog to digital converters are well known for its use in high accuracy wireless communication applications. It is alternative for low power, high resolution (greater than 12 bits) converters, which can be ultimately integrated on digital signal Processor ICs. In this work Over Sampling concept is used to address the problem of power dissipation and noise in ADCs. In this paper a Second order Sigma-Delta Modulator is implemented using CMOS 0.13µm technology using a ï1.2 V power supply. This brief presents a second-order incremental delta–sigma analog-to-digital converter (ADC) for CMOS image sensors (CISs). The ADC that employs a cascade of integrators with a feed forward architecture uses only one operational transconductance amplifier (OTA) by sharing the OTA between the first and second stages of the modulator. Further power and area savings are achieved by using a self-biasing amplifier and the proposed level-shifting technology, which allows active signal summation at the quantize input node without using an additional OTA.**

Keywords: **ADC, CIS, OTA, CMOS, Sigma-Delta, Integrators, 12 Bits, Modulator, Self Biasing Amplifier.**

I. INTRODUCTION

Advances in the integrated circuit (IC) technology have paved way for more compact and efficient implementation of digital logic on silicon. This indeed moved many types of signal processing to the digital domain. One of the major applications of this phenomenon is in data converters i.e., Analog-to-Digital converter (ADC) and Digital-to-Analog converter (DAC). Among the various Analog-to-Digital data, converters usually successive approximation or dual slope ADCs are used when high resolution is desired. But to achieve higher accuracy, trimming is required. The main constraint using these architectures is the design of high precision sample and hold circuits. The over sampling converters use digital signal processing techniques in place of complex and precise analog components, which, gives scope to achieve much higher resolution than the Nyquist rate converters. Sigma Delta ADC, a type of oversampling ADC is highly tolerant to analog circuit imperfections, thus making it a good choice to realize embedded ADC interfaces in modern systems-on-chip (SoCs). The sigma-delta ADC works on the principle of sigma-delta modulation. The sigma-delta (ΣΔ) modulation is a method for encoding high-resolution signals into lower resolution signals using pulse-density modulation. It falls under the category of oversampling ADC's as it samples the input signal at a rate much higher than the Nyquist rate. A sigma-delta ADC comprises of an analog block of modulator and a digital block of decimator.

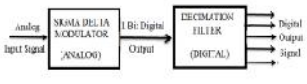

Fig.1.1. Functional diagram.

II. RELATED STUDY

The decimator which is a crucial part of a sigma-delta ADC converts this one bit stream from modulator to an N bit stream according to resolution of ADC. This relaxes the requirement for high precision analog circuits required for the modulator stage and also increases the final output resolution of the ADC. There have been a number of approaches to realize low power Delta Sigma modulators. In this paper, some low power optimization methods have been adopted in the design at both system and circuit level. A CIFB topology is used to design the system which ensures stable operation and low power consumption. A single-bit comparator and an advanced SC integrator topology based on Transmission Gates, which achieve high SNR is chosen. The CIFF architecture without an input feed forward path has been chosen in this brief for two reasons. First, the pixel output behaves similarly to a dc signal; thus, the first integrator has a negligible output swing, even without the direct input signal feed forward path. Second, the proposed level-shifting technique, which will be explained shortly, allows active signal summation without increasing power consumption or hardware complexity.

III. AN OVERVIEW OF PROPOSED SYSTEM

Previously mentioned issues can be relaxed by using a self biasing scheme. As shown in Fig, the amplifier has two inverters connected in parallel whose current is regulated by an upper PMOS (MP) transistor and a lower NMOS (MN) transistor through negative feedback. While one inverter (INV2) amplifies an input signal, the other inverter

(INV1) establishes the amplifier's bias condition. In this brief, as in Fig, two switches, which are driven by two-phase non overlapping clocks, are added to allow the inverters to exchange roles. While INV1 works as an amplifier for the first integrator, INV2 sets the bias current (Φ2). In the next phase (Φ1), INV2 integrates the charge from the first integrator and INV1 sets the bias current. A schematic of the modulator. The upper and lower sides of the circuit are the first and second integrators of the modulator, respectively. Notice that sharing an amplifier between adjacent stages often degrades the linearity of the ADC due to the residual charge stored on the input parasitic of the amplifier. However, this brief does not suffer from the effect of residual charge. When INV1 is used to set the bias current, its input is shorted to a common-mode voltage for input sampling. This resets INV1 and removes the residual charge on its input parasitic.

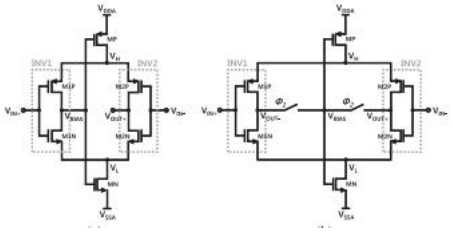

Fig.3.1. Amplifier circuit.

The amplifier noise, particularly the 1/f noise of the input transistors, should be carefully considered to improve the ADC's noise performance beyond 12 bits or higher. Chopping or an auto zeroing technique can be employed to minimize the noise. In addition, compared with conventional inverters, the thermal noise generated from the additional transistors (MN and MP) needs to be suppressed in order not to limit the noise performance.

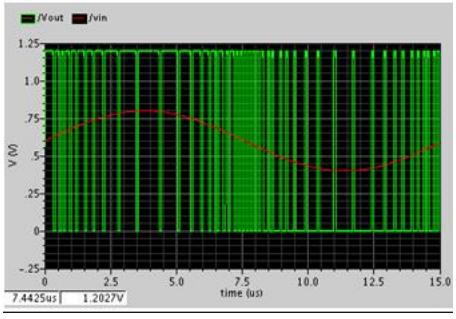

Fig.3.2. Output waveforms.

IV. CONCLUSION

A low-power, small-size 10-bit incremental ΔΣ ADC for CISs has been proposed and fabricated in the 0.18-µm CIS technology. The ADC saves power and die area by sharing a self-biasing amplifier and by using the proposed level-shifting technique to perform signal summation. The ADC occupies a die area of 0.002 mm2 and dissipates 29.5 µW from a 1.8- V supply. Operating at 20 MS/s, the measured SNDRs with 156.25- and 78.125-kHz signal bandwidths are 57.7 and 62.3 dB, respectively, for an 11.3-kHz input signal. The measured DNL and INL are less than +0.22/−0.2 and +0.71/−0.89 LSB, respectively.

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