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Design Of Power Droop Reduction During Scan-Based Logic BIST

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Abstract: **A new low power test pattern generator which can effectively reduce the average power consumption during test application is developed. The new test pattern generator reduces the weighted switching activity (WSA) of the circuit under test (CUT) by suppressing transitions at some primary inputs which make many transitions. Moreover, the new test pattern generator does not lose fault coverage. Experimental results on the ISCAS benchmark circuits show that average power reduction can be achieved up to 33.8% while achieving high fault coverage.**

I. INTRODUCTION

The principle testing areas in VLSI are execution, fetched, testing, region, dependability and power. The interest for versatile processing gadgets and correspondences framework are expanding quickly. These applications require low power dispersal for VLSI circuits. The power scattering amid test mode is 200% more than in typical mode [1]. Subsequently it is critical viewpoint to streamline control amid testing. Power enhancement is one of the fundamental difficulties. There are various factors that affect the cost of chip like packaging, application, testing etc.

In VLSI, as indicated by thumb lead 5000 of the aggregate incorporated circuits cost is because of testing. Amid Testing two key challengers are:

- Cost of testing that can't be scaled.
- Engineering exertion for creating test vectors increments as multifaceted nature of circuit increments.

In light of 1997 SIA information, the upper bend demonstrates the creation cost of transistor and lower bend demonstrates the testing expense of transistor. Figure 1 demonstrates that the creation cost diminishes throughout the decades as indicated by Moore's law yet the testing cost as constant.[2]

There are main two sources of power dissipation in digital circuits; these are static and dynamic power dissipation. Static power dissipation is mainly due to leakage current and its contribution to total power dissipation is very small. Dynamic power dissipation is due to switching i.e. the power consumed due to short circuit current flow and charging of load capacitance is given equation.

$$P=0.5V_{dd}2E\ (sw)\ CL.Fclk$$

Where Vdd is supply voltage, E(sw) is the normal number of yield changes per 1/fclk, fclk is the clock recurrence and CL is the physical capacitance at the yield of the entryway. Dynamic power scattering added to add up to control dissemination. From the above condition the dynamic power relies upon three parameters: Supply voltage, Clock recurrence, exchanging movement. To decrease the dynamic power dispersal by utilizing initial two parameter just to the detriment of circuit execution. However, control lessening utilizing the exchanging movement doesn't corrupt the execution of the circuit.

- Power dispersal amid the testing is one of most critical Based on 1997 SIA information, the upper bend demonstrates the issue [12]. There are a few explanations behind this power expanded in test mode.
- To test vast circuit, circuits are parceled to the test time however this parallel testing result in inordinate vitality and power dispersal.
- Due to the nonappearance of at-speed outfit openness, delay is exhibited in the circuit in the midst of testing. This reason control scattering.In the progressive useful information vectors connected to a given circuit in ordinary mode have huge relationship, while the relationship between's back to back test examples can be low This can cause huge exchanging action in the circuit amid test than that amid its typical task. Power scattering in CMOS circuits is propositional to exchanging action. This inordinate exchanging action, amid test might be in charge of cost and unwavering quality execution check self-sufficiency and Technology related issues.

II. EXISTING METHOD

2.1The low power TPG

The thought behind the utilization of such a low power TPG is to lessen the quantity of advances on essential contributions at each clock cycle of the test session, subsequently diminishing the general exchanging movement produced in the CUT. Give us a chance to consider a CUT with n essential sources of info. A n-arrange crude polynomial LFSR with a clock CLK would be utilized as a part of a regular pseudo-irregular BIST conspire. Here,

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we utilize an altered LFSR made out of n D-type flip-lemon and two tickers CLW2 and CLW2", and developed as portrayed in Figure 2 (n=6 in the case of Figure 2). As one can watch, this altered LFSR is really a blend of two d2-arrange crude polynomial LFSRs, every one of them being driven by a solitary clock CLW2 or CLW2". The D cells having a place with the principal LFSR (alluded to as LFSR-1 in the spin-off) are interleaved with the cells of the second LFSR (alluded to as LFSR-2 in the spin-off).

The accompanying equipment design age approaches have been utilized [1].

1. ROM.- One technique is to store a decent test-design set (from an ATPG program) in a ROM on the chip.

2. LFSR.- Another technique is to utilize a direct criticism move enroll (LFSR) to produce pseudo-arbitrary tests.

3. Parallel Counters-. A parallel counter can create a whole test succession, however this can utilize especially test time if the quantity of sources of info is expansive.

4. Altered Counters. Adjusted counters have likewise been fruitful as test-design generators, however they additionally go for long test arrangements.

5. LFSR and ROM. For essential test mode, the best methodologies is to utilize a LFSR to produce test-designs with an ATPG program. These extra test-examples can either be put away in a ROM on the chip for a second test, they can be connected in a sweep fasten keeping in mind the end goal to rationale the adhered blame scope to 100%.

6. Cell Automaton. In this approach, each example generator cell has a rationale doors, a flip-slump to associations just to neighboring entryways. The cell is react to create the cell machine.

2.2 Existing BIST TPG Structure

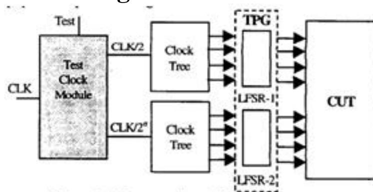

Fig 1: The complete BET TPG structure

The total BIST TPG structure proposed in this paper is delineated in Figure 3. This structure is first made out of a test clock module which gives test clock signals CLW2 and CLW2O from the ace check CLK utilized as a part of the typical mode. The flag "Test" permits to change from the test mode (=O) to the typical mode. As two diverse clock speeds are required for the TPG, two check trees are utilized as a part of our proposed BIST plot as opposed to a solitary one. These clock trees are precisely composed to effectively adjust the clock signals encouraging each piece of the altered LFSR. At long last, the TPG is associated with the CUT. Contributions of the CUT to be associated with the interleaved LFSR have been chosen by following the request of the contributions to the netlist.

III. PROPOSED METHODOLOGY

The proposed Architecture of linear feedback shift register is implemented by Modified LFSR module.

3.1 Modified LFSR module

In BIST, the linear feedback shift register (LFSR) is widely used to generate test patterns due to its low area overhead. However, if a conventional LFSR is used as a test pattern generator, power consumption dissipated in the CUT can be significantly higher since the probability of generating logic value 1 or 0 at each LFSR stage is 0.5. To reduce power consumption during test, the probability should be modified. If the probability is modified, switching activities at inputs of CUT will be reduced. However, suppressing activities of every input results in a loss of fault coverage. For the maintenance of the fault coverage, all inputs should not be suppressed but some inputs selected by the adequate criterion should be suppressed. We propose the criterion selecting some inputs.

Depending on the circuit structure, the transitions at some nodes are higher than those at other nodes during BIST. The nodes of which transitions contribute to the total WSA more than others are defined as ‘heavy nodes’. If the excessive transitions of heavy nodes are reduced, the average power proportional to the total WSA of the CUT will be reduced effectively. Moreover, the fault coverage will not be affected. To reduce the transitions of heavy nodes, ‘heavy inputs’ are defined as primary inputs which can make transitions at heavy nodes. If the transitions at heavy inputs are reduced, the transitions at heavy nodes are also reduced. To suppress heavy inputs, outputs of AND/OR gate trees are applied to the inputs. To develop this idea, heavy nodes and heavy inputs of the circuit under test should be selected by the adequate criterion. the random patterns generated by the conventional LFSR are applied to the CUT first and the WSA value for each node is computed. Then the WSA values for all nodes are sorted from the maximum to the minimum. After sorting, the high ranked nodes are regarded as heavy nodes. For each heavy node in the CUT, heavy inputs which can affect the heavy nodes are selected using the Select_heavy_Inputs() algorithm. When backtraces are performed, the proper logic values 1 or 0 for each heavy input are determined to suppress transitions at heavy nodes.

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To increase fault coverage, deterministic patterns are generated by ATPG (Automatic Test Pattern Generation). These patterns can detect random-pattern-resistant faults which are undetected by most of randomly generated test patterns, hence high fault coverage and reduced test time can be expected if the patterns are applied to the CUT. The probability of applying logic value 1 to each heavy input is calculated to increase the sampling probabilities of deterministic test patterns. According to the heavy input probability set, the number of gates for each heavy input is determined. If the probability is about 0.25, just one AND gate is used, and if the probability is about 0.125, cascade of two AND gates is used. When the probability is about 0.75 or 0.875, one OR gate or cascade of two OR gates is used, respectively.

Figure 2 shows the Modified LFSR module. The proposed LFSR is composed of a primitive polynomial LFSR and an AND/OR gate tree.

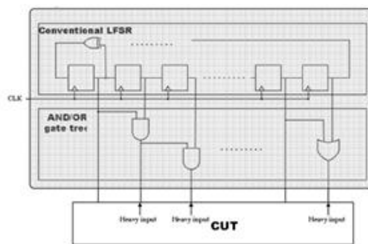

Figure2. Modified LFSR module

3.2 PROPOSED ARCHITECTURE

BIST is basically same as off-line testing using ATE where the test pattern generator and the test response analyzer are on-chip circuitry (instead of equipments). As equipments are replaced by circuitry, so it is obvious that compressed implementations of test pattern generator and response analyzer are to be designed [11]. The basic architecture of BIST is shown in Figure 3 Hardware Test Pattern Generator: This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs (of the CUT).

As the test pattern generator is a circuit (not equipment) its area is limited. So storing and then generating test patterns obtained by ATPG [1-3] algorithms on the CUT using the hardware test pattern generator is not feasible. In other words, the test pattern generator cannot be a memory where all test patters obtained by running ATPG algorithms (or random pattern generation algorithms) on the CUT are stored and applied during execution of the BIST [2]. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns.

The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2n, if there are n flip-flops in the register) as possible. Input Multiplexer: This multiplexer is to allow normal inputs to the circuit when it is operational and test inputs from the pattern generator when BIST is executed. The control input of the multiplexer is fed by a central test controller. Output response compactor: Output response compacter performs lossy compression of the outputs of the CUT (here we have used Half adder to test). As in the case of off-line testing, in BIST the output of the CUT is to be compared with the expected response (called golden signature). If CUT output does not match the expected response, fault is detected. Similar to the situation for test pattern generator, expected output responses cannot be stored explicitly in a memory and compared with the responses of the CUT.

Read Only Memory (ROM): Stores golden signature that needs to be compared with the compacted CUT response.

Comparator: Hardware to compare compacted CUT response and golden signature (from ROM).

Test Controller: Circuit to control the BIST. Whenever an IC is powered up (signal start BIST is made active) the test controller starts the BIST procedure. Once the test is over, the status line is made high if fault is found. Following that, the controller connects normal inputs to the CUT via the multiplexer, thus making it ready for operation. Among the modules discussed above, the most important one is hardware test pattern generator (LFSR).The other ones are standard digital blocks. In the next two sections we will discuss this blocks in details.

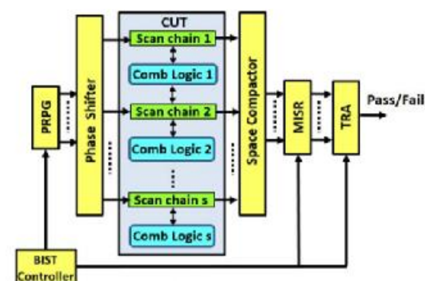

Figure 3: BIST Architecture

We consider the customary output based LBIST (ConvLBIST) design appeared in Fig. 1 [8], [10]–[12], [14]. The state flip-flops (FFs) of the CUT are filter FFs, masterminded into many output chains (s examine chains in Fig. 1). The pseudorandom design generator is executed by a LFSR [10], [12], [14]. The PS, which diminishes the connection among the test vectors connected to contiguous sweep chains [10], is made out of a XOR arrange

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extending the quantity of yields of the LFSR to coordinate the quantity of output chains s [10].

The Space Compactor compacts the yields of the s check chains to coordinate the quantity of contributions of the Multiple-Input Signature Register (MISR). The MISR, the test reaction analyzer, and the BIST Controller are the same as in combinational output based LBIST [8], [12]. Concerning the sweep FFs, our approach requires that, amid move stages, they keep up the last test vector connected to the CUT at their yields. This is ensured by the sweep FF in [24], which is as often as possible utilized in microchips [24], and considered here as a noteworthy illustration.

With a particular true objective to decide a numerical delineation of our proposed course of action, we make the going with streamlining assumptions for Conv-LBIST.

1) All output chains have a similar number of sweep FFs.

2) The greatest AF between two after test vectors T m I and T m i+1 is the same for all output chains (m = 1 ...s). Be that as it may, by rationale level recreations performed by the Synopsys Design Compiler instrument, we have confirmed that our approach can accomplish the same AF decrease additionally if such disentangling speculations are not fulfilled.

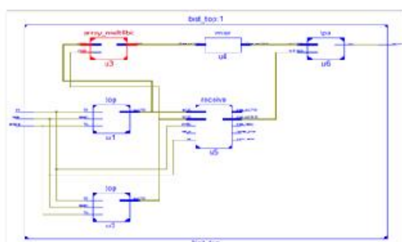
IV. EXPERIMENTAL RESULTS

4.1 simulation waveforms

4.2 design summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	83	5888	1%
Number of Slice Flip Flops	16	11776	0%
Number of 4 input LUTs	146	11776	1%
Number of bonded IOBs	4	372	1%
Number of MULT 18X18SIOs	1	20	5%
Number of GCLKs	1	24	4%

4.3 RTL SCHEMATIC



4.4 timing report

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KORCY:CI->O     2  0.844  0.527  u3/Madd_old_p_8_addsub0000_xor
LUT4:I1->O      1  0.643  0.000  u3/Madd_old_p_10_addsub0000_lut
MUXCY:S->O      1  0.632  0.000  u3/Madd_old_p_10_addsub0000_cy
XORCY:CI->O     2  0.844  0.527  u3/Madd_old_p_10_addsub0000_xo
LUT3:I1->O      1  0.643  0.000  u3/Madd_old_p_12_addsub0000_lut
MUXCY:S->O      1  0.632  0.000  u3/Madd_old_p_12_addsub0000_cy
XORCY:CI->O     2  0.844  0.527  u3/Madd_old_p_12_addsub0000_xo
LUT4:I1->O      1  0.648  0.000  u3/Madd_old_p_14_addsub0000_lut
MUXCY:S->O      1  0.632  0.000  u3/Madd_old_p_14_addsub0000_cy
XORCY:CI->O     3  0.844  0.611  u3/Madd_old_p_14_addsub0000_xo
LUT4:I1->O      1  0.643  0.000  u3/Madd_p_addsub0000_lut<11> (
MUXCY:S->O      1  0.632  0.000  u3/Madd_p_addsub0000_cy<11> (u
XORCY:CI->O     2  0.844  0.527  u3/Madd_p_addsub0000_xor<12> (
LUT4:I1->O      1  0.643  0.000  u3/p<12>12 (u3/p<12>11)
MUXF5:I0->O     1  0.276  0.563  u3/p<12>1_f5 (product_out<12>)
LUT4:I0->O      1  0.648  0.000  u6/Mcompar_out_cmp_eq0000_lut<
MUXCY:S->O      1  0.632  0.000  u6/Mcompar_out_cmp_eq0000_cy<
MUXCY:CI->O     1  0.269  0.420  u6/Mcompar_out_cmp_eq0000_cy<7
OBUF:I->O          4.520         bist_out_OBUF (bist_out)
----------------------------------------
Total              29.822ns (23.060ns logic, 6.762ns route)
                            (77.3% logic, 22.7% route)
```

V. CONCLUSION

All in all, a new low power test design generator, which can diminish exchanging action amid test application, is proposed. Utilizing AND/OR doors tree, the proposed test design generator brings down changes at substantial contributions of which advances will cause numerous advances at inside hubs, in this manner normal power is diminished. In addition high blame scope can be accomplished since AND/OR door tree increment the testing likelihood of the examples that can identify irregular safe issues. The exploratory outcomes on ISCAS benchmark circuits demonstrate that power diminishment of up to 33.8% and high blame scope can be accomplished.

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