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Low Power Consumed Multiplier Design by ANT Architecture with Fixed Width Replica Redundancy Block

SHAIK.NASEERAHMED
Pursuing M.Tech (VLSI&ESD) from SKR College of Engineering & Technology, Manubolu, SPSR Nellore.AP.

V.NANUKU NAIK
M. Tech, Assistant Professor in Deportment of ECE, SKR College of Engineering & Technology, Manubolu, SPSR Nellore.AP.

Abstract: **In this paper, we propose a dependable low-control multiplier configuration by receiving algorithmic commotion tolerant (ANT) engineering with the settled width multiplier to assemble the lessened accuracy copy excess square (RPR). The proposed ANT engineering can take care of the demand of high accuracy, low power utilization, and zone proficiency. We plan the settled width RPR with mistake remuneration circuit by means of examining of likelihood and insights. Utilizing the halfway item terms of information remedy vector and minor info redress vector to bring down the truncation blunders, the equipment unpredictability of mistake pay circuit can be improved. In a 12 × 12 bit ANT multiplier, circuit zone in our settled width RPR can be brought down by 44.55% and control utilization in our ANT configuration can be spared by 23% as contrasted and the condition of-workmanship ANT outline.**

Keywords: Algorithmic Commotion Tolerant (ANT); Settled Width Multiplier; Lessened Exactness Imitation (RPR); Voltage Overscaling (VOS);

1. INTRODUCION

THE RAPID development of versatile and remote figuring frameworks as of late drives the requirement for ultralow control frameworks. To bring down the power dispersal, supply voltage scaling is generally utilized as a viable low-control method since the power utilization in CMOS circuits is corresponding to the square of supply voltage [1]. Be that as it may, in profound submicrometer process innovations, commotion obstruction issues have raised trouble to plan the solid and productive microelectronicssystems; subsequently, the outline strategies to upgrade clamor resistance have been broadly created [2]–[12].

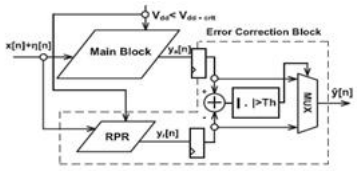

Fig. 1. ANT architecture [2].

A forceful low-control strategy, alluded to as voltage overscaling (VOS), was proposed in [4] to bring down supply voltage past basic supply voltage without relinquishing the throughput. Notwithstanding, VOS prompts serious debasement in motion to-clamor proportion (SNR). A novel algorithmic commotion tolerant (ANT) strategy [2] consolidated VOS primary square with lessened exactness reproduction (RPR), which battles delicate blunders adequately while accomplishing critical vitality sparing. Some ANT distortion outlines are introduced in [5]– [9] and the ANT plan idea is additionally stretched out to framework level in [10]. Be that as it may, the RPR outlines in the ANT plans of [5]– [7] are planned in an altered way, which are not effortlessly embraced and rehashed. The RPR plans in the ANT outlines of [8] and [9] can work in a quick way, yet their equipment many-sided quality is excessively unpredictable. Therefore, the RPR plan in the ANT outline of [2] is as yet the most well known plan in view of its straightforwardness. In any case, embracing with RPR in [2] should even now pay additional zone overhead and power utilization. In this paper, we additionally proposed a simple way utilizing the settled width RPR to supplant the full-width RPR obstruct in [2]. Utilizing the settled width RPR, the calculation blunder can be revised with bring down power utilization and lower region overhead. We take utilization of likelihood, measurements, and halfway item weight examination to locate the estimated remuneration vector for a more exact RPR outline. All together not to expand the basic way delay, we limit the pay circuit in RPR must not be situated in the basic way. Subsequently, we can understand the ANT plan with littler circuit region, bring down power utilization, and lower basic supply voltage.

2. ANT ARCHITECTURE DESIGNS

The ANT technique [2] includes both main digital signal processor (MDSP) and error correction (EC) block, as shown in Fig. 1. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay T_{cp} of the system becomes greater than the sampling period T_{samp}, the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique [2], a replica of the MDSP but with

reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output *ya*[*n*]; however, RPR output *yr* [*n*] is still correct since the critical path delay of the replica is smaller than T_{samp} [4]. Therefore, *yr* [*n*] is applied to detect errors in the MDSP output *ya*[*n*]. Error detection is accomplished by comparing the difference |*ya*[*n*] − *yr* [*n*]| against a threshold *Th*. Once the difference between *ya*[*n*] and *yr* [*n*] is larger than *Th*, the output ˆ*y*[*n*] is *yr* [*n*] instead of *ya*[*n*]. As a result, ˆ*y*[*n*] can be expressed as

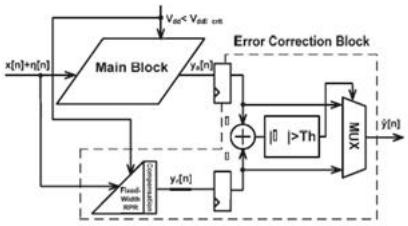

Fig. 2. Proposed ANT architecture with fixed-width RPR.

$$\hat{y}[n] = \begin{cases} y_a[n], & \text{if } |y_a[n] - y_r[n]| \le Th \\ y_r[n], & \text{if } |y_a[n] - y_r[n]| > Th. \end{cases} \quad (1)$$

Th is determined by

$$Th = \max_{\forall \text{input}} |y_o[n] - y_r[n]| \quad (2)$$

where *yo*[*n*] is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation [2].

3. PROPOSED ANT MULTIPLIER DESIGN USING FIXED-WIDTH RPR

In this paper, we additionally proposed the settled width RPR to supplant the full-width RPR hinder in the ANT plan [2], as appeared in Fig. 2, which can not just give higher calculation accuracy, bring down power utilization, and lower zone overhead in RPR, yet in addition perform with higher SNR, more zone productive, bring down working supply voltage, and lower control utilization in understanding the ANT design. We show our settled width RPR-based ANT plan in an ANT multiplier.

The settled width plans are normally connected in DSP applications to keep away from limitless development of bit width. Cutting off n-bit minimum critical piece (LSB) yield is a famous answer for develop a settled width DSP with n-bit information and n-bit yield. The equipment multifaceted nature and power utilization of a settled width DSP is typically about portion of the full-length one. In any case, truncation of LSB part brings about adjusting mistake, which should be remunerated decisively. Numerous writings [13]–[22] have been introduced to decrease the truncation blunder with steady revision esteem [13]– [15] or with variable remedy esteem [16]–[22]. The circuit unpredictability to remunerate with steady amended esteem can be less difficult than that of variable adjustment esteem; nonetheless, the variable revision approaches are typically more exact.

In [16]– [22], their remuneration technique is to repay the truncation blunder between the full-length multiplier and the settled width multiplier. Be that as it may, in the settled width RPR of an ANT multiplier, the remuneration blunder we have to amend is the general truncation mistake of MDSP square. Not at all like [16]– [22], our remuneration strategy is to repay the truncation blunder between the full-length MDSP multiplier and the settled width RPR multiplier. In these days, there are many settled width multiplier outlines connected to the full-width multipliers. Nonetheless, there is still no settled width RPR configuration connected to the ANT multiplier plans.

To accomplish more exact blunder pay, we repay the truncation mistake with variable remedy esteem. We build the blunder remuneration circuit for the most part utilizing the fractional item terms with the biggest weight at all huge fragment. The mistake remuneration calculation makes utilization of likelihood, insights, and direct relapse investigation to locate the inexact pay esteem [16]. To spare equipment multifaceted nature, the remuneration vector in the fractional item terms with the biggest weight at all critical section is straightforwardly infuse into the settled width RPR, which does not require additional pay rationale entryways [17]. To additionally bring down the pay blunder, we likewise consider the effect of truncated items with the second most noteworthy bits on the mistake compensation.We propose a mistake remuneration circuit utilizing a basic minor information redress vector to pay the mistake remained. All together not to expand the basic way delay, we find the remuneration circuit in the noncritical way of the settled width RPR. As contrasted and the full-width RPR outline in [15], the proposed settled width RPR multiplier performs with higher SNR as well as with bring down hardware zone and lower control utilization.

A. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP and maintain the SNR of whole system while lowering supply voltage. In the case of using fixed-width RPR to realize ANT architecture, we not only lower circuit area and power consumption, but also accelerate the computation speed as compared with the conventional full-length RPR. However, we need to compensate

huge truncation error due to cutting off many hardware elements in the LSB part of MDSP.

In the MDSP of n-bit ANT Baugh–Wooley array multiplier, its two unsigned n-bit inputs of X and Y can be expressed as

$$X = \sum_{i=0}^{n-1} x_i \cdot 2^i, \qquad Y = \sum_{j=0}^{n-1} y_j \cdot 2^j. \tag{3}$$

The multiplication result *P* is the summation of partial products

of *xi y j* , which is expressed as

$$P = \sum_{k=0}^{2n-1} p_k \cdot 2^k = \sum_{j=0}^{n-1}\sum_{i=0}^{n-1} x_i y_j \cdot 2^{i+j}. \tag{4}$$

The (*n*/2)-bit unsigned full-width Baugh–Wooley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(*β*)], minor ICV [MICV(*α*)], and LSP, as shown in Fig. 3. In the fixedwidth RPR, only MSP part is kept and the other parts are removed. Therefore, the other three parts of ICV(*β*), MICV(*α*), and LSP are called as truncated part. The truncated

ICV(*β*) and MICV(*α*) are the most important parts because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm.

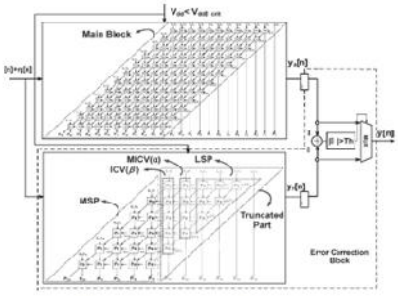

Fig. 3. 12 × 12 bit ANT multiplier is implemented with the six-bit fixed-width replica redundancy block.

To evaluate the accuracy of a fixed-width RPR, we can exploit the difference between the (*n*/2)-bit fixed-width RPR output and the 2*n*-bit full-length MDSP output, which is expressed as

$$\varepsilon = P - P_t \tag{5}$$

where *P* is the output of the complete multiplier in MDSP and *Pt* is the output of the fixed-width multiplier in RPR. *Pt* can be expressed as

$$\begin{aligned} P_t &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i \\ &\quad + f\left(x_{n-1}y_{\frac{n}{2}}, x_{n-2}y_{\frac{n}{2}+1}, x_{n-3}y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}}y_{\frac{n}{2}+2}\right) \\ &\quad + f\left(x_{n-2}y_{\frac{n}{2}}, x_{n-3}y_{\frac{n}{2}+1}, x_{n-4}y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}}y_{n-2}\right) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i + f\,(\mathrm{ICV}) + f\,(\mathrm{MICV}) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i + f\,(\mathrm{EC}) \end{aligned} \tag{6}$$

where *f (*EC*)* is the error compensation function, *f (*ICV*)* is the error compensation function contributed by the input correction vector ICV(*β*), and *f (*MICV*)* is the error compensation function contributed by minor input correction vector MICV(*α*). The source of errors generated in the fixed-width RPR is dominated by the bit products of ICV since they have the largest weight. In [8], it is reported that a low-cost EC circuit can be designed easily if a simple relationship between *f (*EC*)*

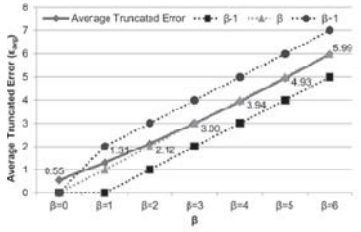

Fig. 4. Statistical curves of average truncation error in the LSP block and the curves of compensation function with $\beta - 1$, β, and $\beta + 1$ in the 12-bit fixed-width RPR-based ANT multiplier.

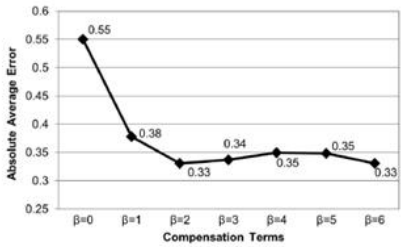

Fig. 5. Analysis of absolute average compensation error under various *β* values in the 12-bit fixed-width RPR-based ANT multiplier.

and *β* is found. It is noted that *β* is the summation of all partial products of ICV. By statistically analyzing the truncated difference between MDSP and fixed-width RPR with uniform input distribution, we can find the relationship between *f (*EC*)* and *β*. As shown in Fig. 4, the statistical results show that the average truncation error in the fixed-width RPR multiplier is approximately distributed between *β* and *β*+1. More precisely, as *β* = 0, the average truncation error is close to *β* + 1. As *β* > 0, the average truncation error is very close to *β*. If we can select *β* as the compensation vector, the compensation vector can directly inject into the fixed-width RPR as compensation, which does not need extra compensation logic gates [17].

We go further to analyze the compensation precision by selecting β as the compensation vector. We can find that the absolute average error in $\beta = 0$ is much larger than that in other β cases, as shown in Fig. 5. Moreover, the absolute average error in $\beta = 0$ is larger than $0.5*2(3n/2)$, while the absolute average error in other β situations is smaller than $0.5*2(3n/2)$. Therefore, we can apply multiple input error compensation vectors to further enhance the error compensation precision. For the$\beta > 0$ case, we can still select β as the compensation vector. For the $\beta = 0$ case, we select $\beta + 1$ combining with MICV as the compensation vector.

Before directly injecting the compensation vector β into the fixed-width RPR, we go further to double check the weight for the partial product terms in ICV with the same partial product summation value β but with different locations. As shown in Table I, the average error value for each ICV vector with the same partial product term summation value is nearly the same even their partial product term's location is different. That is to say that no matter ICV = (1,0,0,0,0,0), ICV = (0,1,0,0,0,0), ICV = (0, 0, 1, 0, 0, 0), ICV = (0, 0, 0, 1, 0, 0), ICV = (0, 0, 0, 0, 1, 0), or ICV = (0, 0, 0, 0, 0, 1), their weight in each partial product term for truncation error compensation is nearly the same. Therefore, we apply the same weight of unity to each input correction vector element. This conclusion is beneficial for us to inject the compensation vector β into the fixed-width RPR directly. In this way, no extra compensation logic gates are needed for this part compensation and only wire connections are needed.

TABLE I
RELATION BETWEEN THE PARTIAL PRODUCT TERM'S LOCATION IN ICV AND THE STATISTICAL COMPENSATION ERROR E_{AVG}

Row	*ICV*	ε_{avg}	*F(ICV)*
1	(1,0,0,0,0,0)	1.328	1
2	(0,1,0,0,0,0)	1.303	1
3	(0,0,1,0,0,0)	1.293	1
4	(0,0,0,1,0,0)	1.293	1
5	(0,0,0,0,1,0)	1.303	1
6	(0,0,0,0,0,1)	1.328	1

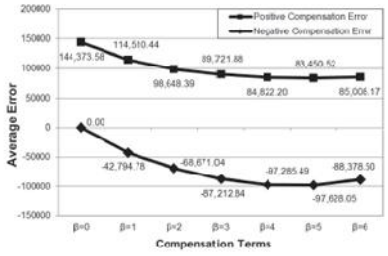

Fig. 6. Analysis of average positive and negative compensation error under various β values in the 12-bit fixed-width RPR-based ANT multiplier.

For the $\beta = 0$ case, we go further to analyze the error profile in the ICV and MICV. In ICV, we can find that all the truncation errors are positive when $\beta = 0$, as shown in Fig. 6.

It implies us that if we adopt the multiple compensation vectors for the average compensation error terms are larger than $0.5*2(3n/2)$, we can lower the compensation error effectively and no additional compensation error will be generated. The multiple compensation vectors are constructed by ICV(β) combined with MICV(α). The weight of MICV(α) is only half of ICV(β). The summation of all partial products of MICV(α), which is denoted as βl , have four possible values of 0, 1, 2, and 3 as n = 12 and β = 0. In Fig. 7, the statistical results show that the average truncation error contributed by the MICV in the case of β = 0 is approximately proportional to α. Moreover, the absolute average truncation error in the situation of α = 0 is smaller than 0.5*2(3n/2), while the absolute average truncation error in the situation of βl > 0 is larger than 0.5*2(3n/2). For the case of the absolute average truncation error is smaller than 0.5*2(3n/2), βl = 0, selecting β as the compensation vector is suitable. However, for the case of the absolute average truncation error is larger than 0.5*2(3n/2), selecting β as the compensation vector is not suitable since insufficient error compensation will occur. Therefore, we adopt ICV together with MICV to amend this insufficient error compensation case when β = 0 and βl > 0 as well. If β = 0 is contributed by βl > 0, we will inject one more carry-in compensated vector in the weight of 2(3n/2). In this way, we can remove the cases of |ε| > 0.5*2(3n/2) effectively.

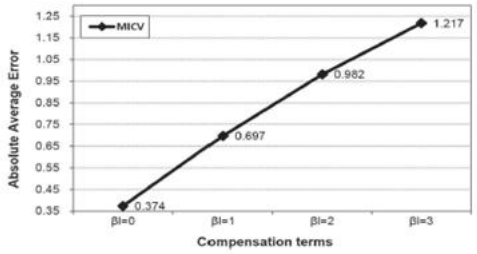

Fig. 7. Analysis of absolute average compensation error under various β_l values while $\beta = 0$ in the 12-bit fixed-width RPR-based ANT multiplier.

Finally, the proposed error compensation algorithm is expressed as (7), as shown at the bottom of the page.

As shown in Fig. 8, we can demonstrate that the compensation error is effectively lowered by adopting ICV together with MICV while comparing with the case of fixed-width RPR only applying the compensation vector of β and with the case of full-width RPR.

$$f(\mathrm{ICV}) = \begin{cases} 0, & \text{if } \beta_l = 0 \\ \beta, & \text{if } \beta_l = 1, \text{ or } \beta_l = 2 \ \& \ (\mathrm{up} - \mathrm{MICV} \neq 0 \ \& \ \mathrm{down} - \mathrm{MICV} \neq 0) \\ \beta - 1, & \text{if } \beta_l = 2 \ \& \ (\mathrm{up} - \mathrm{MICV} = 0 \text{ or } \mathrm{down} - \mathrm{MICV} = 0), \ \beta_l = 3, \\ & \text{or } \beta_l = 4 \ \& \ (\mathrm{up} - \mathrm{MICV} \neq 0 \ \& \ \mathrm{down} - \mathrm{MICV} \neq 0) \\ \beta - 2, & \text{if } \beta l = 4 \ \& \ (\mathrm{up} - \mathrm{MICV} = 0 \ \text{ or } \ \mathrm{down} - \mathrm{MICV} = 0) \end{cases} \quad (7)$$

B. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

To realize the fixed-width RPR, we construct one directly injecting ICV(β) to basically meet the statistic distribution and one minor compensation vector MICV(α) to amend the insufficient error compensation cases.

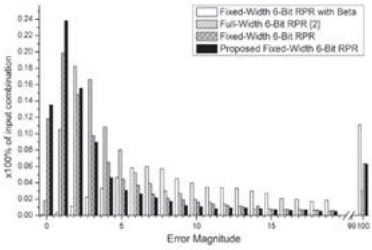

Fig. 8. Comparison of absolute error between the proposed design, the fixed-width RPR with compensation vector β only, and the full-width RPR in the 12-bit fixed-width RPR-based ANT multiplier.

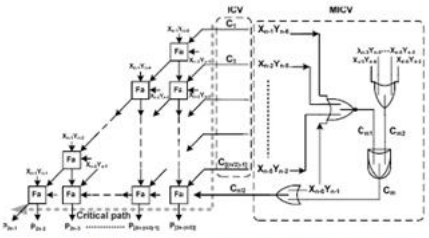

Fig. 9. Proposed high-accuracy fixed-width RPR multiplier with compensation constructed by the multiple truncation EC vectors combined ICV together with MICV.

The compensation vector ICV(β) is realized by directly injecting the partial terms of Xn−1Yn/2, Xn−2Y(n/2)+1, Xn−3Y(n/2)+2, . . . , X(n/2)+2Yn−2. These directly injecting compensation terms are labeled asC1,C2,C3, . . . ,C(n/2)−1 in Fig. 9. The other compensation vector used to mend the insufficient error compensation case is constructed by one conditional controlled OR gate. One input of OR gate is injected by X(n/2)Yn−1, which is designed to realize the function of compensation vector β. The other input is conditional controlled by the judgment formula used to judge whether β = 0 and βl _= 0 as well. As shown in Fig. 8, the term Cm1 is used to judge whether β = 0 or not. The judgment function is realized by one NOR gate, while its inputs are Xn−1Yn/2, Xn−2Y(n/2)+1, Xn−3Y(n/2)+2, . . . , X(n/2)+2Yn−2.

The term Cm2 is used to judge whether βl _= 0. The judgment function is realized by one OR gate, while its inputs are Xn−2Yn/2, Xn−3Y(n/2)+1, Xn−4Y(n/2)+2, . . . , X(n/2)+1Yn−2. If both of these two judgments are true, a compensation term Cm is generated via a two-input AND gate. Then, Cm is injected together with X(n/2)Yn−1 into a two-input OR gate to correct the insufficient error compensation. Accordingly, in the case of β = 0 and βl _= 0 as well, one additional carry-in signal C(n/2) is injected into the compensation vector to modify the compensation value as β + 1 instead of β. Moreover, the carry-in signal C(n/2) is injected in the bottom of error compensation vector, which is the farthest location away from the critical path. Therefore, not only the error compensation precision in the fixed-width RPR can be enhanced, the computation delay will also not be postponed. Since the critical supply voltage is dominated by the critical delay time of the RPR circuit, preserving the critical path of RPR not be postponed is very important. Finally, the proposed high-precision fixed-width RPR multiplier circuit is shown in Fig. 9. In our presented fixed-width RPR design, the adder cells can be saved by half as compared with the conventional full-width RPR. Moreover, the proposed high-precision fixed-width RPR design can even provide higher precision as compared with the full-width RPR design.

4. PERFORMANCE COMPARISONS

To evaluate and compare the performance of the proposed fixed-width RPR based ANT design and the previous fullwidth RPR-based ANT design, we implemented these two ANT designs in a 12-bit by 12-bit multiplier. The main performance indexes are the precision of RPR blocks, the silicon area of RPR blocks, the critical computation delay of RPR blocks, the error probability of RPR blocks under VOS, and the lowest reliable operating supply voltage under VOS. Through quantitative analysis of experimental data, we can demonstrate that our proposed design can more effectively restrain the soft noise interference resulting from postponed computation delay under VOS when the circuit operates with a very low-voltage supply. Moreover, hardware overhead and power consumption can also be lowered in the proposed fixed-width RPR-based ANT design. Finally, we implemented our proposed 12-bit by 12-bit fixed-width RPR- based ANT multiplier design in TSMC 90-nm CMOS process technology.

First, we compare the proposed fixed-width multiplier with other literature designs [2], [17], respectively. All performance comparisons are evaluated under 12-bit ANT-based multiplier designs. To evaluate the truncation error compensation performance, we define the index of absolute mean error (εavg), mean-square error (εms), maximum truncation error (εmax), and variance of error (εv), respectively. The comparison basis is the fixed-width RPR without any compensation vector and the definition of various error evaluation indexes are expressed as

$$\varepsilon_{\text{avg},\%} = \frac{\varepsilon_{\text{avg}}}{\varepsilon_{\text{avg (Truncated)}}} \times 100\% \quad (8)$$

$$\varepsilon_{\text{ms},\%} = \frac{\varepsilon_{\text{ms}}}{\varepsilon_{\text{ms(Truncated)}}} \times 100\% \quad (9)$$

$$\varepsilon_{\text{max},\%} = \frac{\varepsilon_{\text{max}}}{\varepsilon_{\text{max(Truncated)}}} \times 100\% \quad (10)$$

$$\varepsilon_{v,\%} = \frac{\varepsilon_{v}}{\varepsilon_{v\text{(Truncated)}}} \times 100\%. \quad (11)$$

The smaller value of εavg, εms, εmax, and εv represents the more accurate EC performance. The precision analysis results of various fixed-width RPR multipliers or full-width RPR multiplier are shown in Table II. The fixed-width RPR multipliers are the six-bit multipliers while their LSPs are truncated and various error compensation vectors are applied. The full-width RPR multiplier is the six-bit by six-bit multiplier. As shown in Table II, the fixed-width RPR designs usually perform with higher truncation errors than that of the full-width RPR design because more computation cells are truncated. However, with appreciate error compensation vector or multiple truncation error compensation vectors, the fixed-width RPR designs still have the chance to perform with lower truncation errors. As shown in Table II, the absolute mean error, the mean square error, the maximum error, and the variance of error in our proposed fixed-width RPR multiplier can be lowered to 21.39%, 5.57%, 9.18%, and 9.00%, respectively, in the 12-bit by 12-bit ANT multiplier design. All these truncation error evaluation indexes are the lowest ones as compared with the state-art-designs of [2] and [17] because multiple truncation EC vectors combined ICV together with MICV are applied to lower the truncation errors based on probability and statistics analysis.

TABLE II
COMPARISONS OF THE ABSOLUTE MEAN ERROR, THE MEAN-SQUARE ERROR, AND THE VARIANCE OF ERROR UNDER VARIOUS RPR-BASED 12-BIT ANT MULTIPLIER DESIGNS

Various RPR Designs in ANT Multiplier	$\varepsilon_{avg,\%}$	$\varepsilon_{ms,\%}$	$\varepsilon_{max,\%}$	$\varepsilon_{v,\%}$
MSP	100%	100%	100%	100%
Fixed-Width RPR with β [17]	22.71%	6.25%	10.08%	9.89%
Full-Width RPR [2]	28.03%	8.45%	12.69%	10.43%
Proposed Fixed-Width RPR	21.39%	5.57%	9.18%	9.00%

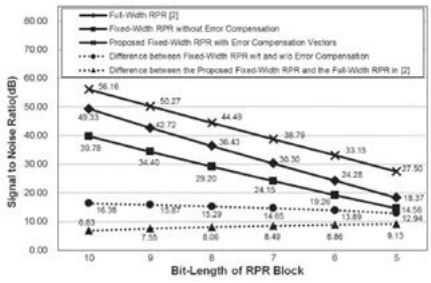

Fig. 10. Comparisons of the output signal SNR for various RPR designs with different truncated bits.

To confirm the consistency of the compensation accuracy, we compare the output signal quality in terms of SNR for various RPR designs with different truncated bits, which is shown in Fig. 10. In the 12-bit ANT multiplier, the truncated RPRs are analyzed from word length of five to ten bits. As shown in Fig. 10, the output SNR of our proposed six-bit fixedwidth RPR-based ANT multiplier design can be maintained

to 33.15 dB. As compared with the directly truncated six-bit fixed-width RPR, the signal quality can be improved with 13.89-dB enhancement. At the same time, the SNR in the full-width RPR-based ANT design is 24.28 dB. With various truncation bits, the output SNR differences between our proposed fixed-width RPR-based ANT multiplier design and the conventional full-width RPR-based ANT design are ranged from 6.83 to 9.13 dB. The analysis results show that the output signal quality of the conventional full-width RPR-based ANT design is influenced by the truncation error. However, the output SNR of the our proposed fixed-width RPR-based ANT design can still be maintained high and is not severely influenced by the truncation error because a precise error compensation vector is applied.

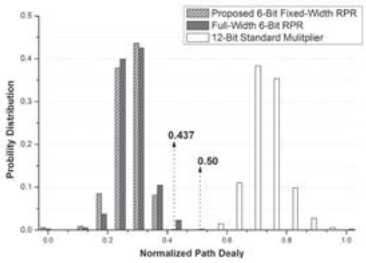

Fig. 11. Comparisons of delay profiles for the six-bit fixed-width RPR, the six-bit full-width RPR, and the 12-bit full-length multiplier.

To lowering supply voltage beyond critical supply voltage without sacrificing the throughput and without leading to severe SNR degradation, the critical computation delay in the RPR block must be as fast as possible. The shorter computation delay in RPR can bring the benefits of lower overscaling supply voltage adopted. The comparison of delay profiles under various 10 000 input random patterns for the presented six-bit fixed-width RPR design, the previous six-bit full-width RPR design, and the standard 12-bit fulllength multiplier are shown in Fig. 11. Because the computation word length in the RPR block is less than that in the main block computation unit, the critical computation delay and the average computation delay in the RPR block can all be shorter. In the presented fixed-width RPR design, the critical computation delay and the average computation delay can be further shortened since the fanout and wires loading of adder cells are lowered to be close to half. As shown in Fig. 11, the critical computation delay in the proposed RPR block can be shortened by 56.3% as compared with

the main computation block. As compared with the previous full-width RPR, the critical computation delay in our proposed RPR block can also be shortened by 12.6%.

To determine the optimized bit-length of fixed-RPR, comparisons of the Kvos and RPR area with different bit length of RPR block are shown in Fig. 12. Our goal is to select the bit length of fixed-RPR, which can achieve the lowest Kvos. The smaller RPR can perform with higher speed, lower power consumption, and lower area. However, RPR with lower bit length would also lead to SNR degradation. Therefore, a tradeoff between hardware area and RPR bit length is needed. In this paper, the optimized bit length of fixed-RPR is selected as six based on the lowest Kvos analysis results shown in Fig. 12.

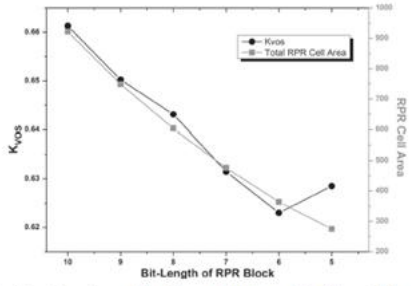

Fig. 12. Comparisons of the Kvos and RPR area with different bit length of RPR block.

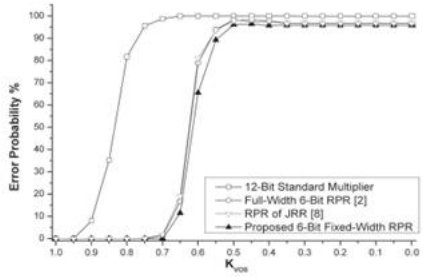

Fig. 13. Comparisons of the error probability of various RPR blocks under different VOS scale.

To evaluate the signal quality performance of various designs under VOS, we compare the error robability of various RPR blocks under VOS by injecting 10 000 input random patterns as test bench. Here, we follow the definition of the VOS factor, Kvos, defined in [2]–[10] to identify the level of the supply voltage can be reliably lowered. The Kvos is ranged from one to zero. The lower Kvos means the lower supply voltage is adopted and lower power is consumed. The error probability of zero represents all the input patterns can be computed reliably and correctly under VOS, while the increase of error probability represents that there are some computation errors occurring in the computation unit. As shown in Fig. 13, the error probability in the standard 12-bit full-length multiplier increases sharply as Kvos goes below 0.9. Our proposed fixed-width RPR design and the fullwidth RPR design can more effectively restrain the soft noise interference resulting from postponed computation delay under VOS. The sharply increase of error probability in both the six-bit full-length RPR multiplier and the six-bit fixed-length RPR multiplier can be suspended until Kvos goes below 0.65.

To further identify the lowest achievable reliable Kvos, we compare the output SNR of various RPR designs under different Kvos. The desirable SNR is expected to be higher than 25 dB. As shown in Fig. 14, the output SNR in the standard multiplier is lower than 25 dB while the Kvos is scaled below 0.851. The conventional full-width RPR can maintain the output SNR is higher than 25 dB until the Kvos is scaled below 0.658. The breakdown point of Kvos in our proposed fixed-width RPR design is further lower than that of the conventional full-width design since the presented RPR design can compute more precisely. As a result, the reliably Kvos can be scaled to 0.623 while the output SNR of our presented fixed-width RPR can still be maintained to be higher than 25 dB. In the latest literature joint residue number system RPR (JRR)-based ANT design [8] with moduli set (127, 128, 129, 257), the reliably Kvos can be further lowered to 0.551 while the multiplier output SNR can still be maintained to be higher than 25 dB. It is mainly because that the JRR design can operate in higher speed in the main multiplier block

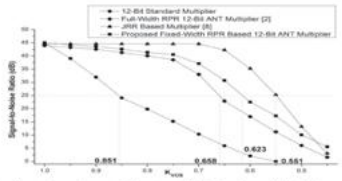

Fig. 14. Comparisons of the output SNR of various RPR designs under different Kvos.

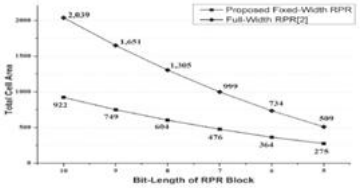

Fig. 15. Comparisons of the total logic synthesis cell area of various RPR designs with different bit length.

The RPR area is another key factor that will affect the power saving. Hence, we compare the circuitry area occupied by the fixed-width RPR multiplier and the full-width RPR multiplier. The truncated RPRs are analyzed from word length of five to ten bits using Synopsys design complier CAD tool. The total synthesized logic cell silicon area for various RPR designs is plotted in Fig. 15. As illustration, the silicon area in the proposed design can be averagely saved by 45.51% as compared with various word length full-width RPR multiplier designs. Under the case of six-bit fixed-width RPR multiplier design, the chip area occupied by total logic cells can be saved by 44.55% as compared with the six-bit full-width RPR design.

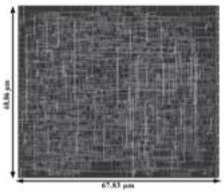

Fig. 16. Chip layout of the proposed 12-bit fixed-width RPR-based ANT multiplier design.

TABLE III
PERFORMANCE SPECIFICATION SUMMARY OF THE PROPOSED 12-BIT FIXED-WIDTH RPR-BASED ANT MULTIPLIER DESIGN

Design Name	Fixed-Width RPR Based ANT Multiplier
Word Length (n)	12 bits
Product Word Length (n)	24 bits
Transistor/Gate Count	1372
Power Supply	1 V
Power Dissipation	0.393 mW (@0.6V)
Chip Size	4616.5 μm^2
Process Technology	TSMC 90nm CMOS
Max Frequency	200MHz

Finally, we implement the proposed 12-bit fixed-width RPR-based ANT multiplier in TSMC 90-nm process, as shown in Fig. 16. The silicon chip area of proposed ANT multiplier circuit is 4616.5 μm2. With lower achievable reliable supply voltage and lower silicon area in the presented RPR block, the power consumption in the proposed 12-bit fixed-width RPR-based ANT multiplier design can be saved by 47.3% as compared with the full-width RPR-based ANT design. The chip specification is summarized in Table III.

In Fig. 17, we evaluate the power saving performance under various ANT designs. In Fig. 17(a), we compare the power consumption of various multiplier designs under different Kvos. Under lower Kvos, the power consumption can be lowered. However, the hardware complexity increase in the ANT-based design would lead to power consumption increase. In the standard multiplier, its Kvos can only be lowered to 0.851 and its power consumption is 752 μW under such Kvos. In the proposed ANT design, the RPR design is simpler and with lower truncation compensation error. Therefore, the Kvos can be lowered to 0.623 and the power consumption can be lowered to 393 μW with 52.3% power saving. At the same time, the Kvos in the full-width RPR-based ANT design [2] can be lowered to 0.658 and its power consumption can be lowered to 435 μW. As for the JRR design, its Kvos can be lowered to 0.551. However, it needs four parallel multipliers in the RNS computing system, which occupies larger circuitry area. Therefore, the lowest power in the JRR design can only be lowered to 468 μW. The area overhead of our proposed 12-bit fixed-width RPR-based ANT multiplier design is 12.4% as compared with 12-bit standard multiplier, and the power overhead is 4.7% in normal voltage supply. However, the power consumption of proposed multiplier design can be saved by 52.3% as compared with standard multiplier under VOS operation.

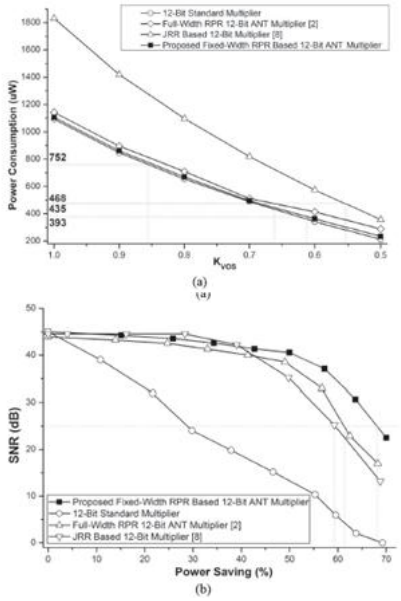

Fig. 17. Power-saving comparisons under various design environments. (a) Comparisons of the power consumption of various multiplier designs under different Kvos. (b) Comparisons of the SNR under different power saving percentage.

In Fig. 17(b), we further compare the output signal SNR under different power-saving environments. In the JRR design [8], its Kvos can be lowered to 0.551 and its lowest power saving can achieve 59% as compared with the standard multiplier with normal supply voltage. In the proposed fixedwidth RPR-based ANT design, the critical path is lowered with higher compensation precision and lower hardware area. Therefore, the lowest power saving in the proposed design can achieve 68%, while the full-width RPR-based ANT design can achieve 62%. The desirable SNR here is expected to be 25 dB. For the case the system requirement in signal quality is higher than 25 dB, the merits in these designs can still be maintained.

To further consider the temperature and process variation, performance comparisons of the output SNR under variou s process corners with different Kvos are shown in Fig. 18. As illustration, we perform the postlayout simulation under typical–typical corner with 25 °C, fast–fast corner with 0 °C, and slow–slow corner with 100 °C. Under these three design corners, the Kvos in the proposed ANT design are 0.623, 0.582, and 0.683, respectively. The low-voltage low-power merit in the presented ANT design can still be preserved under process deviation and high-temperature environments.

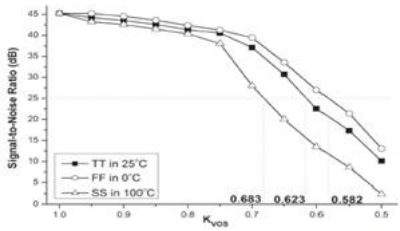

Fig. 18. Comparisons of the output SNR of various process corners under different Kvos.

5. CONCLUSION

In this paper, a low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. The proposed 12-bit ANT multiplier circuit is implemented in TSMC 90-nm process and its silicon area is 4616.5 μm2. Under 0.6 V supply voltage and 200-MHz operating frequency, the power consumption is 0.393 mW. In the presented 12-bit by 12-bit ANT multiplier, the circuitry area in our fixed-width RPR can be saved by 45%, the lowest reliable operating supply voltage in our ANT design can be lowered to 0.623 *V*DD, and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

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AUTHOR's PROFILE

Shaik.Naseerahmed, Pursuing M.Tech (VLSI&ESD) from SKR College of Engineering & Technology, Manubolu, SPSR Nellore.AP.

V.Nanuku Naik, M.tech, Assistant Professor in Deportment of ECE, SKR College of Engineering & Technology, Manubolu, SPSR Nellore.AP.

