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Reversible FIR Filter Designing For Speech Singal Processing

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Abstract: **In this paper, a proficient engineering of FIR channel structure is exhibited. For accomplishing low power, reversible logicmode of task is actualized in the plan. Territory overhead isthe tradeoff in the proposed outline. From the amalgamation results,the proposed low power FIR channel engineering offers 18.1 % of intensity sparing when contrasted with the traditional plan. The territory overhead is 2.6% for the proposed engineering.**

1. INTRODUCTION

Advanced Signal Processing is utilized as a part of extensive variety of uses, for example, radio, TV, video and so forth. Its primary fundamental instrument Finite Impulse Response (FIR) advanced channels. The separating requires number juggling activities. The viper and multiplier module expend much circuit territory and power. The unpredictability of the channel is basically a direct result of the augmentation activity in FIR channel. For low power configuration input bit width of the module is very critical.

The adders, Wallace, dadda multipliers are connected for channels to dispose of intensity utilization because of undesirable information changes [1]. In [2] they introduced a multipliers strategy, in light of include and move technique and regular sub articulation end for low territory, low power and fast usage of FIR channels. Limited drive reaction channels are broadly utilized as a part of different DSP applications.

The general FIR channel can be communicated as the accompanying condition:

$$y(n) = \sum_{k=0}^{N-1} C_k x(n-k) \qquad (1)$$

Where N speaks to the length of the FIR channel, the kth coefficient and x(n-k) is the information at time moment n-k.

where M is the tap number of the FIR channel, ck are the channel coefficients, and x(n-k) is the information signals. The above conditions can likewise communicated in Z area as

$$Y(z) = x(z)\, H(z) \qquad (2)$$

Where H(z) is the exchange capacity of FIR channel in Z area and is given by

$$H(z) = \sum_{k=0}^{L-1} h(k) z^{-1} \qquad (3)$$

A FIR channel of request N is described by N+1 coefficients and when all is said in done, require N+1 multipliers and N two-input adders [7]. Structures in which the multiplier coefficients are definitely the coefficients of the exchange work are called coordinate shape structures

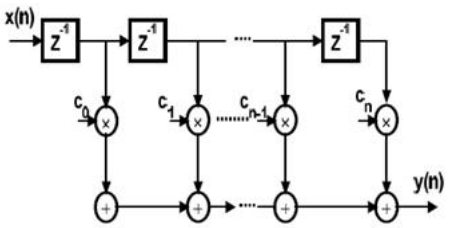


Figure.1 Direct form FIR Filter structure

In advanced flag handling, math tasks like multipliers and adders assume a noteworthy part. Multiplier possesses a bigger region in the FIR Filter. The basic multipliers utilized will be Wallace, dadda multipliers. The adders utilized for examination are Ripple Carry Adder, Carry lookahead snake, Carry spare viper and Carry select viper. Every one of the blends of the snake and multipliers are utilized as a part of the plan. Among all the blend the FIR Filter with Carry lookahead viper and Wallace multiplier gives better outcome when contrasted with alternate mixes. The association of the paper is as per the following: area II demonstrates the customary FIR channel configuration, Section III portrays the proposed low power reversible rationale based plan of FIR channel, Results and talk are exhibited in Section IV lastly conclusion is displayed in Section V

2. CONVENTIONAL FIR FILTER DESIGN

FIR filter consists of multipliers, delay element and adders. The various multipliers and adders are described as follows:

A Multipliers:

Multiplication involves 2 basic operations: the generation of the partial product and their accumulation. Therefore, there are two possible ways to speed up the multiplication thereby reducing the complexity, and as a result reduces the time needed to accumulate the partial products . Both solutions can be applied simultaneously.

Both the multipliers consist of three stages. In the first stage the partial product matrix is formed. The second stage the obtained partial product matrix is reduced to a height of two. In the third stage the two rows are combined by carry propagating adder structure. Both Wallace and Dadda multipliers are used for reducing the partial products. The partial product are reduced as soon as possible in Wallace multiplier. Dadda multiplier performs the minimum reduction necessary at each level to perform the reduction in the same number of levels as Wallace multiplier. Both the multipliers exhibit similar delay because same number of pseudo adder levels are used to perform the partial product reduction. Wallace multiplier uses smaller carry propagating adder, while Dadda multiplier uses larger carry propagating adder. Dadda's multiplier is the fast multiplier.

Wallace and Dadda multipliers are unsigned multipliers while Baugh Wooley multiplier is a signed multiplier. Baugh and Wooley [3] have presented the modifications required to use the signed operands with column compression multipliers.

A 1Wallace Multiplier:

In Wallace tree multiplication, for 4bit multiplicand and multiplier there will be 16 partial products. The partial products are formed by using AND gates. A parallel (n,m) counter is a circuit which has n inputs and produces m outputs. A full adder is an implementation of a (3,2) counter which takes 3 inputs and produces 2 outputs. Similarly a half adder is an implementation of a (2,2) counter which takes 2 inputs and produces 2 outputs. Totally 3 stages of partial product reduction for 4 bit multiplication. If there are p rows of partial products, rows are grouped and the remaining p mod 3 rows are passed to the next stage. These rows are summed using full adders [(3,2) counters] if there are 3 partial products in 1 column and using half adders[(2,2) counter] if there are 2 partial products in 1 column. The resulting sum and carry of the full adder and half adder are passed on to the next stage. Finally in the last stage Full adders are used to obtain the product.

The height of the matrix in the jth reduction stage, is given by the following recursive equations [4]

$$w_0 = N \quad (4)$$

$$w_{j+1} = 2.\left\lfloor \frac{w_j}{3} \right\rfloor + w_j \bmod 3 \quad (5)$$

The principle of Wallace tree multiplication can be extended to longer wordlengths. Four reduction stages are required with matrix heights of 6, 4, 3 and 2.

A 2Dadda Multiplier:

Dadda multipliers are derived from parallel multipliers presented by Wallace in [5]. In the first stage of the dada multiplier, partial products are formed by using N2 AND gates. In the second stage, the partial product matrix is reduced to a height of two. Dadda multipliers use a minimal number of (3,2) and (2,2) counters at each level during the compression to achieve the reduction. The reduction procedure for Dadda compression trees is given by the following recursive algorithm [6].

1. Let $d_1 = 2$ and $d_{j+1} = \lfloor 1.5 . d_j \rfloor$. D_j

Is the height of the matrix for the jth stage. Repeat until the largest jth stage is reached in which the original N height matrix contains at least one column which has more than partial products.

2. In the jth stage from the end, place (3,2) and (2,2) counters as required to achieve a reduced matrix. Only columns with more than partial products or which will have more than partial products as they receive carries less significant (3,2) and (2,2) counters are reduced.

3. Let j = j-1 and repeat step 2 until a matrix with a height of two is generated. This occurs when j= 1.

The 8 x 8 Dadda multiplier requires four reduction levels with matrix heights of 6,4,3 and 2. 64 AND gates, 35 (3,2) counters, 7 (2,2) counters and 14 bit Carry propagate adder are required to form 16-bit product.

B Adders:

B 1 Ripple Carry Adder (RCA) The basic unit of ripple carry adder is full adder. It can be constructed by connecting full adders in cascaded, with the carry out of the previous 1-bit full adder is given as carry-in to the next 1-bit full adder in the chain. In this cascaded structure, carry out propagates or ripples through the circuit. Ripple carry adder occupies smaller area on the chip and offers high performance to random input data. The delay of the ripple carry adder depends on the length of the propagation path. Due to this reason, RCA is not suitable for circuits with non-random input operands. In the ripple carry adder, the output is known only after the carry of the previous stage is produced. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage which is worst case addition. As the result, the final sum and carry bits will be valid after a considerable delay.

The delay associated with RCA is given as:

tRCA = ntFA (6)

where n is the number of 1-bit FAs connected in RCA and tFA is the delay associated with 1-bit full

adder circuit. This critical delay increases linearly with number of bits (n)[8].

B.2 Carry Look-Ahead Adder (CLA)

The major problem associated with ripple carry adder is its delay which increases with number of bits or depends upon the propagation path from least significant bit to most significant bit. In ripple carry, it is required that carry should be passed through all lower bits to compute the sum for higher bits. Therefore, for fast applications, a better design is required which can be achieved by carry look-ahead adder (CLA). CLA solves the problem of delay in RCA by calculating the carry signal in advance based on the input signal. Therefore, CLA provides lower delay than RCA at the price of more complex hardware and large area on the chip. Generate and propagate logic is used in the CLA. The main advantage of CLA is that carry delay and sum delay are independent of the number of bits one need to add. The disadvantage of the carry look-ahead adder is that the carry logic becomes complicated for more than 4-bits[8].

B.3 Carry Select Adder (CSL)

In a ripple carry adder, every full adder cell has to wait for the carry in signal before generating carry out, which is time consuming. One way to get rid of this problem is to assumeboth possible values of the Cin, i.e., Cin = 0 and Cin = 1. After that, it is required to evaluate the result for both possibilities in advance. After knowing the correct value of Cin, the correct result will be chosen with the help of 2:1 MUX. This idea is implemented in the design of carry select adder. Therefore, carry select adder computes two results in parallel. Each result is computed for two different values of carry in. The carry select adder is simple and fast. Addition of two n-bit (a,b) numbers is performed by breaking the input into two blocks. For each carry save block, sum and carry values are propagated for both carry-in =0 and carry-in = 1. The actual carry-out value is then fed into a multiplexer that picks the correct sum and carry-out for the next block. When the two phases of carry-in are equal, the total gate delay is minimal[8].

B.4 Carry Save Adder (CSA)

In carry save adder, carries are saved as partial carries rather than propagated. These partial carries are added to the next operand during the next addition. One can accelerate each addition by postponing the carry propagation. The carry save addition), followed by a carry propagate (carry propagate) addition. A carry save adder sums up a partial sum and partial carry from the previous stage as well as operand and produces a new partial sum and partial carry.

3. PROPOSED LOW POWER REVERSIBLE LOGIC BASED

DESIGN OF FIR FILTER

The proposed method of low power FIR filter design consists of multipliers, delay elements and adders, realized using reversible logic gates. Reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is a one-toone correspondence between the vector inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us uniquely recover the inputs from outputs. The following are the important design constraints for reversible logic circuits: Reversible logic circuits should have minimum quantum cost. Reversible logic gates do not allow fanouts. The design can be optimized so as to produce minimum number of garbage outputs. The reversible logic circuits must use minimum number of constant inputs. The reversible logic circuits must use a minimum logic depth or gate levels[8].

A REVERSIBLE GATES:

a. FREDKIN GATE:

Fredkin gate is a conservative gate (Figure.2). Hamming weight of the input vector is same as the hamming weight of the output vector. It has 3 gate inputs and 3 gate outputs(3*3). It has a quantum cost* five. Fredkin gate is used as delay element in the filter design.

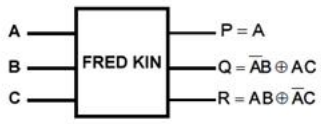


Figure.2 Fredkin gate

***Quantum Cost** (**QC**) of any reversible circuit is the total number of 2x2 quantum primitives which are used to form equivalent quantum circuit

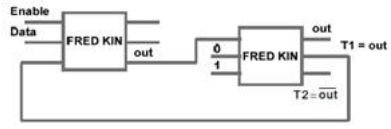


Figure. 3 Fredkin gate used as Dlatch

b. PERES GATE:

Peres gate has 3 gate inputs and outputs in case of half adder (Figure.4), Peres gate has 4 inputs and 4 outputs (4*4) in full adder realization (Figure.5). Its quantum cost is five.

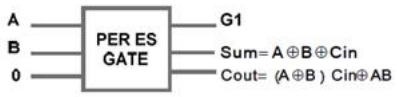


Figure.4 Peres gate as half adder

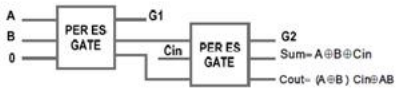
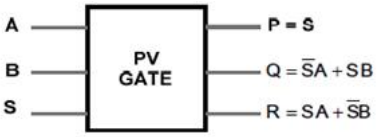


Figure.5 Peres gate as full adder

c.PV GATE:

PV gate has 3 gate inputs and outputs (3*3) (Figure.6).



S acts as select line , Q and R are the outputs

Figure. 6 PV gate as mux

d.TOFFOLI GATE:

Toffoli gate has 3 gate inputs and outputs and it is replaced in the position of AND and XOR gates.

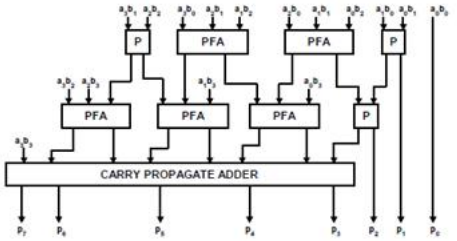
Figure. 7 Toffoli gate as AND and XOR gates

B Reversible Multipliers:

The Conventional Wallace tree and dadda multipliers are realized using reversible logic.

B.1 Reversible Wallace multiplier

For 4 bit multiplication totally there are 3 stages of partial product reduction. If there are p rows of partial products, rows are grouped and the remaining p mod 3 rows are passed to the next stage. These rows are summedusing fulladders [(3,2) counters] if there are 3 partial productsin 1 column and using half adders[(2,2) counter] if there are 2 partial products in 1 column. The resulting sum and carry of the full adder and half adder are passed on to the next stage. Finally in the last stage Full adders are used to obtain the product.The full adder block is replaced by the Peres full adder. Similarly, half adder block is replaced by Peres half adder block.Figure.8 shows the 4x4 reversible Wallace multiplier.

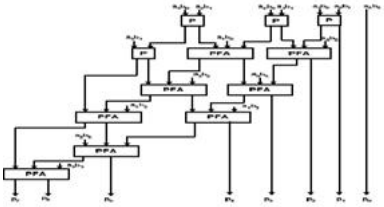


P – Peres reversible gate as half adder, PFA – Peres reversible gate as full adder

Figure.8 Reversible Wallace multiplier

B.2 Reversible Dadda multiplier:

In the Dadda multiplication,[Figure.9] the first stage consists of N2 AND gates, forming the partial products. The successive reduction levels involves the Peresfull adder and Peres half adder blocks leading to the resultant product.



P – Peres reversible gate as half adder, PFA – Peres reversible gate as full adder

Figure.9 Reversible Dadda multiplier

C Reversible Adder:

Among the adders discussed in the conventional design, Carry lookahead adder realization in reversible logic gives better result when compared to the Ripple carry adder, Carry select adder and Carry save adder. In the adder blocks, the full adder is replaced by Peres gate. In CLA, the generate and propagate block is replaced by the Peres gate and Toffoli reversible gates, since addition and multiplication operation are present in the corresponding reversible gates. The Figure.10 shows the generate propagate logic (GPL) realization in Carry look ahead adder.

The inputs to the GPL are a, b and c and the outputs are p,q,c1

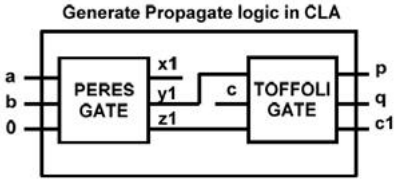


Figure.10 Generate propagate logic in CLA

4. RESULTS AND DISCUSSION

The proposed design is verilog coded and synthesized in SOC encounter using CMOS 180 nm library for different filter orders. Following are the specifications on the FIR filters implemented.

• Input sequence and coefficients are 8-bit data.

• Input sequence are the speech sequences are taken from ITU-T Test Signals for Telecommunication Systems, which includes Artificial voices, real speech and other artificial voices.

• The filter structure follows equiripple characteristics.The average of the filter coefficients of 8 tap filter is taken as the input threshold xth i.e., 2-7.

In the following discussions, as a metric of power savings, the power consumption ratio in case of leakage power, dynamic power and total power are P_{rl}, P_{rd}, P_{rt} respectively, which means the ratio of the proposed reversible filter power consumption to the conventional direct form f_i .

Following are the analysis and results of FIR filter realization with Wallace multiplier and different adders namely CLA, CSL and CSA both in normal form (Conventional method) and using proposed reversible logicdesign.

TABLE I. COMPARISON OF LEAKAGE POWER(LP) IN MILLI WATTS FOR SPEECH SIGNAL CASE

8-tap FIR filter with Wallace multiplier and various adders			
Filter structure	Conventional design LP(mw)	Proposed reversible design LP (mw)	Power saving ratio(1-P_{rl})%
Wallace + CSA	0.002189	0.001993	8.9%
Wallace + CSL	0.002564	0.002167	15.4%
Wallace + CLA	0.003190	0.002621	17.8%
8-tap FIR filter with Dadda multiplier and various adders			
Filter structure	Conventional design LP(mw)	Proposed reversible design LP (mw)	Power saving ratio(1-P_{rl})%
Dadda + CSA	0.002609	0.002539	2.6%
Dadda + CSL	0.003014	0.002705	10.25%
Dadda + CLA	0.003564	0.003108	12.7%

The Table I shows the Leakage power in milli watts for various filter designs. From the table it is inferred that the proposed reversible filter consumes less power and the power saving ratio is high for Wallace design.

$$(1 - p_{r_l})\ \% = \left(1 - \frac{proposed\ design\ power}{conventional\ design\ power}\right)\%$$

TABLE II. COMPARISON OF DYNAMIC POWER (DP) IN MILLI WATTS FOR SPEECH SIGNAL CASE

8-tap FIR filter with Wallace multiplier and various adders			
Filter structure	Conventional design DP(mw)	Proposed reversible design DP (mw)	Power saving ratio(1-P_{rd})%
Wallace + CSA	3.999099	3.361873	15.9%
Wallace + CSL	4.552737	3.802179	16.4%
Wallace+ CLA	6.66818	5.461040	18.1%
8-tap FIR filter with Dadda multiplier and various adders			
Filter structure	Conventional design DP(mw)	Proposed reversible design DP (mw)	Power saving ratio(1-P_{rd})%
Dadda + CSA	6.164732	5.449934	11.6%
Dadda + CSL	6.856818	5.961732	12.9%
Dadda + CLA	8.052809	6.987122	13.2%

The Table II shows the Dynamic power in milli watts for various filter designs. From the table it is inferred that the proposed reversible filter consumes less power and the power saving ratio is high for Wallace design.

$$(1 - p_{r_d})\ \% = \left(1 - \frac{proposed\ design\ power}{conventional\ design\ power}\right)\%$$

The total power saving for Wallace and Dadda multipliers based FIR filter is calculated from leakage and dynamic power. The summation of LP and DP in milli watts gives the total power.

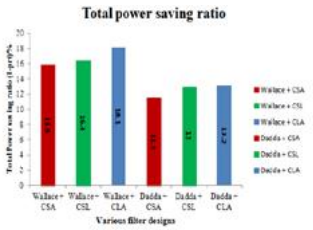


Figure.11 Comparison of Total power saving ratio

From the Figure.11 it is inferred that the power saving ratio is high for the filter designed using proposed reversible Wallace multiplier and Carry lookahead adder.The power saving ratio is about 18.1% for 8 tap FIR filter realized in direct form.

TABLE III. COMPARISON OF AREA IN mm^2 FOR SPEECH SIGNAL CASE

8-tap FIR filter with Wallace multiplier and various adders		
Filter structure	Conventional design	Proposed reversible design
Wallace + CSA	0.02762	0.02852
Wallace + CSL	0.02955	0.03006
Wallace + CLA	0.02625	0.02694
8-tap FIR filter with Dadda multiplier and various adders		
Filter structure	Conventional design	Proposed reversible design
Dadda + CSA	0.02315	0.02952
Dadda + CSL	0.03155	0.03262
Dadda + CLA	0.02739	0.03530

The above table shows the area comparison for various filter designs. Area overhead is introduced by the proposed design and it is about 2.6%increase in area for proposed Wallace multiplier with carry look ahead adder.

5. CONCLUSION

In this paper, low power reversible FIR filter architecture is proposed. In the proposed method the input data samples and filter coefficients are given as input to the multipliers and adders designed using reversible logic gates. The proposed scheme is compared with the FIR filter realized using normal multipliers and adders and the simulation results, shows that the proposed FIR filter designed using reversible Wallace multiplier and carrylookahead adder gives power saving ratio of about 18.1% with small area overhead of 2.6%. The technique can be used in phonetic signal

processing system. The proposed work can be extended to adaptive filter.

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