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Reduced Number of Switches for Seven Level Inverter

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Abstract— **Multilevel inverters hold attractive features, which make them to be utilized in wide range of applications. But with increase in number of output levels, the number of semiconductor switches in the respective configurations increase which may lead to vast size and hikes the installation cost of the inverter. Here the project presents effective configurations for seven level inverter. A configuration is built with single DC voltage source with a series of capacitors, diodes, seven active switches including a H-bridge for generation of seven level output. Other configurations are built with three dc voltagge sources, six active switches and four dc voltage sourc es, five active switches. Multi carrier based Pulse Widt h Modulation technique is used for the switching of gate trigger circuitry. Computer aided simulation is done to validate the considered approach using MATLAB/SIM ULINK. The performance quality in terms of Total Harm onic Distortion of the considered multilevel inverter structures are compared with each other to obtain the effective topology for seven level output.**

Index Terms— **Inverters; multilevel sy stems; phase disposition (PD); pulse width modulation (PWM); total harmonic distortion (THD)**

I. INTRODUCTION

Power electronics means the effective combination of three areas namely power, control and electronics. This means that any load can be made to perform better by controlling the power with electronic devices. As a result of rapid changes in the type of loads, the load requirements have been changing drastically in an emphatic way.

In order to make up to the load requirements there should be a conditioner or modulator present in between the system to condition the input so that it can be utilized by the load effectively. These type of power conditioners are essential and important in the present booming period of electronics . Before power electronic devices, there used to exist similar devices like vacuum tubes, mercury-arc rectifiers etc. to convert alternate to direct or direct to alternating current but those are uncontrolled in nature. But the power electronic devices made it possible to make available the wide control and conversion of alternate to direct and direct to alternate conversion possible under controllable situations.

Power electronics has set a new tendency in the grounds of power conversion and its control. So, power electronics can be easily interpreted as t he merger of power and electronics. Power includes generation, transmission and utilization of energy at high performance and the electronics is the one that concerns about data and signals of low power level.

Principles of both power and electronics are included in the power electronics, which is use d in power levels that are much larger than signal level. In other means electronic devices rated at power level rather than signal level can be easily said as the power electronics

Jin-Sung Choi, and Feel-soonKang, have recommended a new topology o f multilevel inverter as a fundamental block [1]. The proposed topology is generalized using series connection of the fundamental blocks. A great perfection in voltage levels number with minimum switching devices has been obtained. Multilevel inverter has superior features over conventional and recent new topologies in terms o f the required power semiconductor switches, isolate d dc supplies, number of output voltage level, driver num ber, total power losses and cost. Because of substantial increase in voltage levels with less semiconductor switches this topology can be a good candidate for converters used in power applications especially in high voltage applications.

Gnana Prakash M, et al have proposed a six switch topology and explained that multilevel inverter has a number of advantages [2]. It ha s drawbacks in the higher levels because of using more number of semiconductor switches which leads to vast size and price of the inverter is very high. So in order to overcome this problem multilevel inverter is considered with reduced number of switches. The proposed method is well suited for a high power application and it built with three Dc sources and six Switches. Multi carrier PWM technique is used for sine wave generation.

S. Umashankar, et al have recommended a simplified five-level inverter with reduced component count comprising of floating input DC sources connected in opposite polarities through power switches [3]. The structure requires lesser active switches as compared with conventional cascaded H-bridge topology with much reduced switching losses. For symmetric DC source configuration, it is established that the switches with higher voltage stresses can be operated at lower switching frequency as compared with

switching frequency of switches with lower voltage stress.

M. F. Kangarlu and E. Babaei, proposed a sub-multilevel inverter and then a cascaded sub-multilevel inverter as a generalized multilevel inverter in both symmetric and asymmetric conditions [4]. The number of the dc voltage sources in each sub-multilevel inverter is equal but their values are different from one sub-multilevel inverter to another. Therefore, the proposed multilevel inverter can be categorized in asymmetric group. The optimal structures for the proposed multilevel inverter were obtained considering several factors such as the number of switching devices, number of dc voltage sources, number of output voltage levels, standing voltage on the switches and etc.

The project throws light on a way to generate seven level output by using different topologies and using different number of switches namely five switches, six switches and seven switches. The pulse width modulation technique used here is carrier based one where one reference wave and multiple carrier waves are used to produce gating signals. Depending on placement of carrier waves one over the other these are classified as in phase, opposite phase and alternate opposite phase disposition.

In the carrier based PWM technique a reference wave generally a sinusoidal wave is compared with the carrier waves generally the triangular wave to generate the gating signals to the switches placed in the circuit.

In the Seven switch configuration sinusoidal reference wave is used and three triangular carrier waves by using logic gates these pulse waveforms are converter to gating signals to the seven switches present in the circuit. In the Six switch configuration also sinusoidal reference wave is used and six triangular carrier waves. Here six carrier waves because here bipolar PWM technique is used. By comparing these six carrier waves with the reference sinusoidal wave six pulses are obtained. These six pulses are directly applied to the six switches placed in the circuit which triggers the power electronic devices placed in the circuit. In the Five switch configuration also sinusoidal reference wave is used along with five triangular carrier waves. By comparing these five carrier waves with reference wave we obtain five pulses which are fed to the five switches present in the circuit. So in all these three topologies the common thing is the reference wave and the carrier wave. The Seven level output distortion levels depend on the modulation index of the circuit. Modulation index depends on the amplitude of reference wave and the carrier wave. So by varying the amplitudes of the reference and carrier waves modulation index is set and Fast Fourier Transform (FFT) analysis is done to know the Total Harmonic Distortion (THD). THD should be minimum for better performance.By varying the Modulation index values from 0.8 to 1.0 the THD values are to be noted so that the best configuration can be sorted out at a particular modulation index which can be used to get the best performance in terms of harmonic distortion.

II. SEVEN LEVEL TOPOLOGY

Six Switch Design:

The number of Power electronic switches and the number of dc sources for the projected architecture is defined by: P= (2*X– 5), Where P= number of stages and

X= no. of switches and P = (2*Y + 1) Where, Y=no. of dc voltage sources.

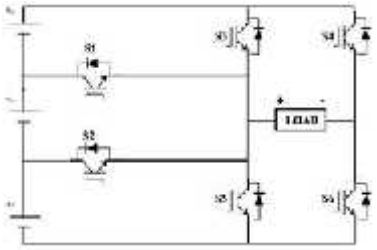

Fig: 2.10. Illustration of Six device architecture

Switching Scheme

In these extensions the switching schem e used is the Phase Disposition Pulse Width modulation (PDPWM). It uses both reference wave and carrier wave. Generally in phase disposition scheme for an N-level inve rter we have to use (N-1) carrier waves. So for the seven leve l inverter used here we have to use (7-1) i.e., six carrier wav es.

III. SIMULATION DESIGN AND RESULTS

Simulation model and results of Six switch structure:

Below figure illustrates the SIMULATION model of the considered configuration to be simulated to obtain the multilevel output at the load terminals. The Simulation model consists of the Power electronic switches, here MOSFETs are used for construction of this. These switches are triggered at different time periods based on the reference and the carrier waves. The reference wave is compared against the carrier waves. The reference wave considered can be a sinusoidal wave, a trapezoidal wave or a stepped wav e. Here in this sinusoidal reference wave is considered.

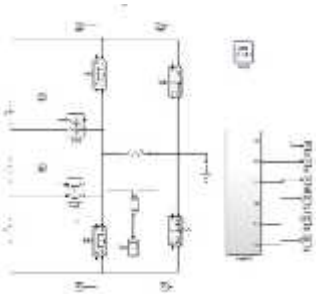

Fig: 3.1. Illustration of Simulation model with six switches.

Switching logic design

The sub-system used here gene rates the switching signals taking the reference signal and the carrier signal as the input and generating the gating signals to the switches present in the circuit.The technique used here is a Phase Disposition (PD) or In Phase Disposition (IPD).The output is shown at the resistance terminals which is a seven level output which contains harmonics and is near to sinusoidal wave.

Seven Level inverter with Modulation Index 1.0

Modulation index is calculated with the formula below because here the carrier waves used are six in number.

Ma = Am/ 6Ac

The FFT analysis shows the Total Harmonic

Distortion (THD) level of the output obtained at the load terminals. As the modulation reaches to unity the THD level decreases, which makes the load to perf orm better.

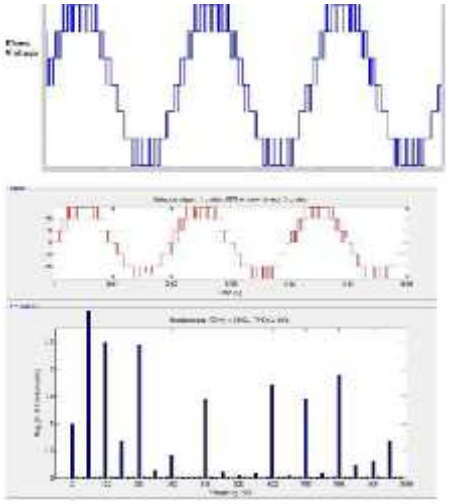

Fig: 3.2. Phase voltage and its FFT analysis with M.I.1.0

For a Seven level Multi Level Inverter:

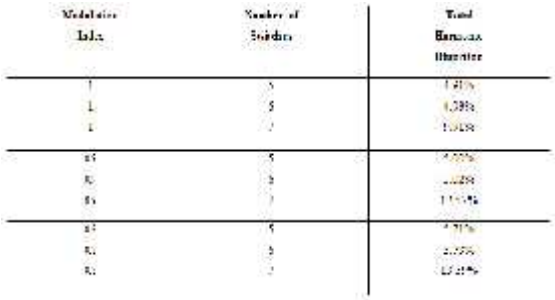

Table: 3.1 Assessment of THD for MLIs with different MI's

From above table it can be inferred that low Total Harmonic Distortion among a bove all combinations is ultimately the five switch topology of all three M.I's considered here.

IV. CONCLUSION

Each MLI has its own mixture of advantages and disadvantages and for any one particular application, one topology will be more appropriate than the others. Carrier based modulation technique is easy and efficient. The carrier based technique is used i n this thesis for generation of switching signals.

The aim of this project is to reduce the number of switches for better performance. The seven level converter with different number of switch es namely five switch, six switch and seven switch are executed. These seven level inverters are built in MATLAB /SIMULINK environment. By comparing all the THD valu es the Five Switch Seven level inverter gives the lowest T HD of 4.71% compared to Switch 4.73% and Seven Switch 9.91% at Unity Page Modulation Index.

Modulation Index	Number of Switches	Total Harmonic Distortion
1	5	4.91%
1	6	4.93%
1	7	9.91%
0.9	5	5.00%
0.9	6	5.02%
0.9	7	12.57%
0.8	5	5.71%
0.8	6	5.73%
0.8	7	13.59%

So, at Modulation Index unity five switch inverter gives 5% low THD than Seven Switch. At Modulation Index 0.9 also Five switch inverter gives 7.57% less THD than the Seven switch configuration and at Modulation Index 0.8 also Five Switch inverter gives 7.88% less THD than the Seven switch configuration. Here the PWM technique used is the In-Phase Disposition (IPD) technique for paralleling sine wave and the carrier waves. So, lastly five Switch Seven level inverter configuration is better than the six and seven switch topologies when THD is taken as comparative parameter.

V. REFERENCES

[1] Jin-Sung Choi, and Feel-soonKang, "7-Level PWMInverterEmployingSeries-Connected Capacitors Paralleled to a Single DC Voltage Source," IEEE Transactions on Industrial Electronics, 2014.

[2] Gnana Prakash M, Balamurugan M, Umashankar S, "A New Multilevel Inverter with Reduced Number of Switches," International Journal of Power Electronics and Drive System (IJPEDS), Vol. 5, No. 1, July 2014, pp. 63~70, 2014.

[3] S. Umashankar, T. S. Sreedevi, V. G. Nithya, and D. Vijayakumar,**"**A New 7-Level Symmetric Multilevel Inverter with Minimum Number of Switches,"Hindawi Publishing Corporation, ISRN lectronics2013.

[4] M. F. Kangarlu and E. Babaei, "A Generalized Cascaded Multilevel Inverter Using Series Connection of Sub multilevel Inverters," IEEE Trans. Power Electronics. vol. 28, no. 2, pp. 625-636, 2013.

[5] Mokhberdoran and A. Ajami, "Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology," IEEE Trans. Power Electron., vol. 29, no. 12, pp. 6712-6724, 2014.

[6] S. Gautam and R. Gupta, "Switching Frequency Derivation for the Cascaded Multilevel Inverter Operating in Current Control Mode Using Multiband Hysteresis Modulation," IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1480-1489, 2014.

[7] Jing Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," IEEE Trans. Power Electron., vol. 21, no. 1, pp. 140-147, 2006.

[8] Ajami, M. R. J. Oskuee, A. Mokhberdoran, and A. Van den Bossche, "Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches," IET Power Electron. vol. 7, no. 2, pp. 459-466, 2014.

[9] Kai-Ming Tsang and Wai-Lok Chan, "Single DC source three-phase multilevel inverter using reduced number of switches," IET Power Electron. vol. 7, no. 4, pp. 775-783, 2014.

