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VLSI Based Robust Router Architecture

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Abstract: **The focus of this Paper is the actual implementation of Network Router and verifies the functionality of the Five port router using the latest verification methodologies and Hardware Verification Languages. In the proposed design the FSM is designed with reduced number of states. Due to reduction of states the amount of time to produce the response became less obviously the frequency is improved. At the same time the memory required to design of this Router chip is also reduced. In the existed design number of LUTS are 724. In the existed design the total memory usage is 297148 kilobytes and the maximum frequency is 76.374MHz, whereas in the proposed design the number of LUTS are 240.In the proposed design, the total memory usage is 249164 kilobytes and the maximum frequency is 81.162MHz.**

Keywords-**Network-On-Chip; Simulation Router; FIFO; FSM; Register Blocks**

I. INTRODUCTION

A router is a device that forwards data packets between computer networks. This creates an overlay internetwork, as a router is connected to two or more data lines from different networks. When a data packet comes in one of the lines, the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table or routing policy, it directs the packet to the next network on its journey. Routers perform the "traffic directing" functions on the Internet. A data packet is typically forwarded from one router to another through the networks that constitute the internetwork until it reaches its destination node.

The most familiar type of routers are home and small office routers that simply pass data, such as web pages, email and videos between the home computers and the Internet. An example of a router would be the owner's cable or DSL router, which connects to the Internet through an ISP [1]. More sophisticated routers, such as enterprise routers, connect large business or ISP networks up to the powerful core routers that forward data at high speed along the optical fiber lines of the Internet backbone. Though routers are typically dedicated hardware devices, use of software-based routers has grown increasingly common.

In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing). In this scenario, the computer that is connected to the Internet is acting as the router for the second computer to obtain its Internet connection. Going a step up from ICS, we have a category of hardware routers that are used to perform the same basic task as ICS, albeit with more features and functions.The routers allows to share one Internet connection computers. These are called broadband or Internet connection sharing routers, these routers allow you to share one Internet connection computers.

Routing is the process of choosing best paths in a network. In the past, the term routing was also used to mean forwarding network traffic among various networks. However, this latter function is much better described as simply forwarding. Routing is performed for many kinds of networks, including the telephone network (circuit switching), electronic data networks (such as the Internet), and transportation networks.

This article is concerned primarily with routing in electronic data networks using packet switching technology. In packet switching networks, routing directs packet forwarding (the transit of logically addressed network packets from their source toward their ultimate destination) through intermediate nodes. Intermediate nodes are typically network hardware devices such as routers, bridges, gateways, firewalls, or switches. In many instances, an ISP will allow you to use a router and connect multiple computers to a single Internet connection and pay a nominal fee for each additional computer sharing the connection. This is when home users will want to look at smaller routers, often called broadband routers that enable two or more computers to share an Internet connection. Within a business or organization, This may need to connect multiple computers to the Internet, but also want to connect multiple private networks not all routers are created equal since their job will differ slightly from network to network. General-purpose computers can also forward packets and perform routing, though they are not specialized hardware and may suffer from limited performance.

The routing process usually directs forwarding on the basis of routing tables which maintain a record of the routes to various network destinations. Thus, constructing routing tables, which are held in the

router's memory, is very important for efficient routing. Most routing algorithms use only one network path at a time. Multipath routing techniques enable the use of multiple alternative paths. In case of overlapping or equal routes, the following elements are considered in order to decide which routes get installed into the routing table (sorted by priority).

When multiple routers are used in interconnected networks, the routers exchange information about destination addresses, using a dynamic routing protocol which is mainly used in Telecom sector. Each router builds up a table listing the preferred routes between any two systems on the interconnected networks.

A router has interfaces for different physical types of network connections, (such as copper cables, fiber optic, or wireless transmission). It also contains firmware for different networking protocol standards. Each network interface uses this specializedcomputer software to enable data packets to be forwarded from one protocol transmission system to another.

Routers may also be used to connect two or more logical groups of computer devices known as subnets, each with a different sub-network address. Verilog is used as Hardware Description Language (HDL). Modelsim and Xilinx ISE [5] is used as Electronics Design Automation (EDA) tool for simulation.

II. ROUTER DESIGN PRINCIPLES

Specified the compact contest limit and the short implementation window, the design adopted a set of design principles to spend the on hand time as proficiently as possible. This document provides specifications for the Router is a packet base protocol. Router drives the incoming packet which comes from the enter port to output ports based on the address contained in the packet.

The router is a "Network Router" has a one input port from which the packet enters. It has three amount produced ports where the packet is driven out. Packet contains 2 parts. They are data and address sequence. Packet width is 8 bits and the length of the packet can be between 1 byte to 63 bytes. Packet header contains three fields DA and length. Goal address (DA) of the packet is of 8 bits. The switch drives the packet to internal ports based on this destination address of the packets.

The router chains five similar connections at the same time as shown in Figure 1. It uses store and forward type of flow control in count to FSM Controller deterministic steering which improves the act of router. The router is an "association Router" has a one input port from which the packet enters. It has five ports where the packet is motivated out. The Carton contains 2 parts, they are data and address sequence. Packet width is 8 bit and the length of the device can be sandwiched between 1 byte to 63 bytes. Packet header contains five fields DA and length. Goal address (DA) of the envelope is of 8 bits.

The switch drives the packet to respective ports based on this destination tackle of the packets. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 62.

The register has a positive edge clock, an active high clock enable and an active high asynchronous reset [1]. The output of the register is the input of the de-mux. The data input to the register is transferred to the output port at the positive edge of the clock if and only if the enable is 1 and the reset is 0. If the reset is 1, then the output port of the register is set to zero's. If the enable is 0, then the output port keeps its current value. Since ROUTER is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocols do not use a clock pulse, but the data should be timed very accurately. Since ROUTER has a clock signal, the clock can vary without disrupting the data.

The data rate will simply change along with the changes in the clock rate. The five Router Design is done by using of five blocks.The blocks are 8-Bit Register, Router controller and output block [4]. The router controller is design by using FSM design, and the output block consists of five ways to transmit the payload. These functions are discussed clearly. The design follows Full duplex synchronous serial data with variable length of transfer word up to 64 bytes.

The Receiver (Rx) and Transmitter (Tx) on both rising or falling edge of serial clock independently 5 receivers select lines with Fully static synchronous design with one clock domain

III. OPERATION

The Router can operate with a single master device and with one or more slave devices.

If a single slave device is used, the RE pin may be fixed to logic low if the slave permits it. Some slaves require the falling edge (high-low transition) of the slave select to initiate an action such as the mobile operators, which starts conversion on said transition. With multiple slave devices, an independent RE signal is required from the master for each slave device.

IV. RESULTS

In this section, the Simulation Waveforms for 1X5 Router is shown in Figure 2.

Waveforms

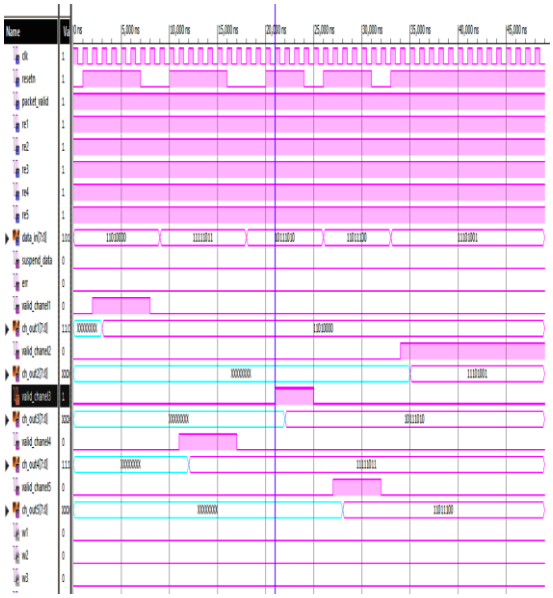

Figure 2- Simulation of 1X5 Router

The RTL Schematic [2] and Top- Level view is shown in Figure 3 and Figure 4

RTL Schematic

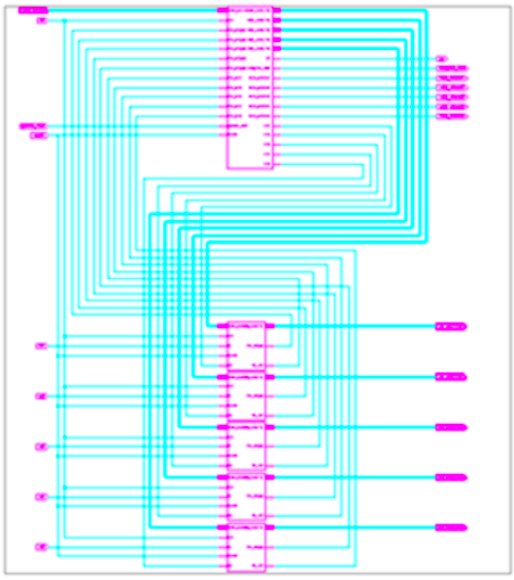

Figure 3- RTL Schematic of Five Port Router

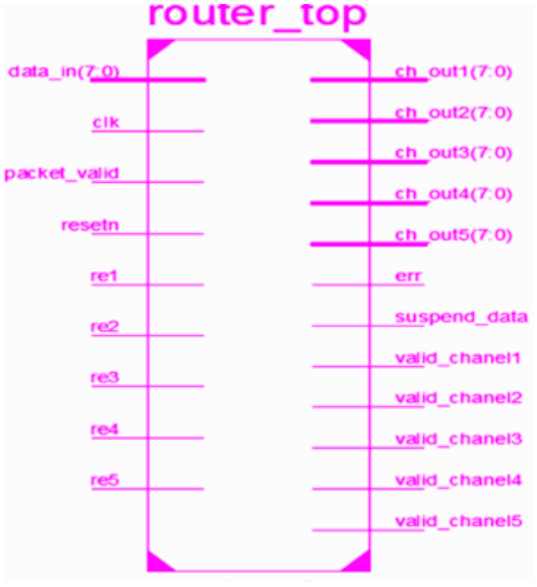

Figure 4- Top-Level Schematic view of Five Port Router

In this section the Logic Utilization available and used in the design is

Table 1-Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number ofSlices	162	4656	3%
Number of Slice Flip Flops	141	9312	1%
Number of 4 input LUTs	315	9312	3%
Number of bonded IOBs	63	232	27%
Number of GCLKs	2	24	8%

Total memory usage is 249164 kilobytes

Maximum Frequency: 81.612 MHz

V. CONCLUSION

In this paper, a reduced area (NUMBER OF LUT'S)of a five port router is presented. The proposed router structure functionality is implemented in Verilog HDL and proven that this architecture consumes less resources in terms of no of LUT'S, slices and number of IO Buffers. In this paper the Xilinx ISE EDA Tool is used for synthesis and for simulation.

The data which can be send through the router is reached the destination with 9.375ns latency which is better than the 1x3 router Architecture. In future there is a chance to estimate the power consumption also.

VI. REFERENCES

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