Low-Power Selective Pattern Compression Techniques In Digital VLSI Circuits

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Abstract: **In this paper, we discuss a productive test-autonomous pressure method for concurrent decrease of test data volume and test power for sweep based test applications. The pre-created test sets acquired from ATPG device are separated into two gatherings in view of the quantity of unspecified bits in every test set. Test pressure system is connected just to the gathering of test sets which contain more unspecified bits and the power decrease strategy is connected to the rest of the test sets. In the proposed approach, the unspecified bits in the pre-produced test sets are specifically mapped with 0s or 1s in view of their viability in diminishing the test data volume and power consumptions. We additionally display a basic decoder design for on-chip decompression. Exploratory results on ISCAS'89 benchmark circuits show the viability of the proposed procedure contrasted and other test-free pressure systems.**

Keywords: **ATPG; LP-SPC; SoC;**

I. INTRODUCTION

In test-free pressure strategies, test pressure technique is connected to the pre-created test sets. A run of the mill programmed test design era (ATPG) apparatus is utilized to create test sets for the given blame records. In these methodologies, unspecified bits (additionally called as couldn't care less bits or X-bits) in the test sets are loaded with rationale values and encoded with appropriate coding hypothesis. The power dissemination of the digital ICs amid test mode is higher when contrasted with its typical mode of operation. This powerful scattering amid test mode influences the circuit unwavering quality because of hoisted normal power amid stacking and emptying of the test boosts and its reaction.. We introduce a low-power particular example pressure (LP-SPC) strategy to diminish the test data volume and test power consumption at the same time in full-check consecutive circuits. Test pressure methodology is connected just to the gathering of test sets which contain more unspecified bits and the power diminishment strategy is connected to the rest of the test sets. One specific example pressure conspire is considered as a base plan for our pressure procedure. Our pressure method concentrates on decrease of both normal and pinnacle power and the test data pressure. In the proposed approach, we have mapped the unspecified bits to either 0 or 1 to acquire the greatest pressure keeping up the pinnacle power under safe cutoff.

II. TEST POWER REDUCTION

A commonplace circuit in an industry contains 95% to 98% of X-bits in the test sets produced by ATPG. We have adaptability to fill these X-bits with rationale 0 or 1 to get completely determined test sets without influencing the circuit's blame scope. In customary ATPG, these X-bits are arbitrarily filled to get completely determined test set. The filling of X-bits in the test set with appropriate rationale esteem is the way to decrease move power, catch power what's more, test data volume. Shockingly, it is unrealistic to utilize a similar X-bit for the lessening of catch power, move power and test data volume at the same time. One normal practice to minimize the power scattering amid sweep based testing is to decrease the quantity of output cell's flag moves. These can be ordered into three classes:

The aggregate power consumption in sweep based testing is not just in light of the quantity of moves in test set additionally on relative position of where the move happens. One regular metric used to assess the test power is the weighted moves metric (WTM). The WTM is firmly connected to the exchanging action in the inner hubs of CUT amid output move operation. sweep vectors with higher WTM disperse more power in CUT.

The WTM for the scan-in test stimuli t_j can be determined by

$$WTM_j = \sum_{i=1}^{l-1}(l-i)\left(t_j i \oplus t_j i + 1\right) i$$

where l is the scan-chain length and $t_j = t_{j;1}; t_{j;2}; t_{j;3} ::: t_{j;l}$ is the scan vector with $t_{j;1}$ scanned in before $t_{j;2}$ and so on. The average power (P_{avg}) and the peak-power (P_{peak}) in scan-in mode for a test set $T_D = \{t_1, t_2, t_3 ....t_n\}$ can be estimated as

$$P_{avg} = \frac{\sum_{j=1}^{n}\sum_{i=1}^{l-1}(l-i)(t_j\,i^{\oplus}\,t_j\,i+1)}{n}\quad \textbf{ii}$$

$$P_{peak=}\ \max_{j\varepsilon(1,2,n)}\sum_{i=1}^{l-1}(l-i)\big(t_j\,i^{\oplus}\,t_j\,i+1\big)\quad \textbf{iii}$$

Equations (i). And (ii) show that, reducing the test vector's transition and the weight $(l-i)$ are the key factors for reducing the average and peak-power. The same equations can be used to estimate also the average and peak-powers in scan-out mode. We consider the number of transitions in scan cells for each scan-chain to compute the capture-power. This is because of the linear relationship exists between capture transitions on the scan-chain and peak-power of the circuit. So, it is attempted to minimize the Hamming distance between test stimuli and its response on each scan cell. This will reduce the peak-power of the circuit in test mode. Filling the entire or larger number of unspecified bits in the test set to reduce the peak-power may affect the compression efficiency and may increase the total power, i.e. scan-in and scan-out transitions. It is required to maintain the capture-power within the circuit's peak-power limit for proper operation. Filling one unspecified bit in the test stimuli may affect many unspecified bits in the test response which may cause capture-power violations. So, it is necessary to estimate the impact of filling of each unspecified bit in the test set. The logic values are assigned to the unspecified bit(s) based on its impact on capture-power. The impact of filling of one unspecified bit with the logic value v (i.e. 0 or 1) for the nth scan cell of mth test vector can be computed as

$$C_{impact}(m,n,v)\quad \sum_{for\ all\ n}R_{m,n}\oplus S_{m,n}\ -\ \sum_{for\ all\ n}R_{m,n}\odot S_{m,n}\ \textbf{iv}$$

Where $S_{m,n}$ and $R_{m,n}$ are logic values of the test stimulus and response of same scan cells respectively. The two terms of the right side of Equation (iv) represent the number of inconsistent furthermore, reliable piece combines separately. It can be noticed that, both $R_{m,n}\oplus S_{m,n}$ and $R_{m,n}\odot S_{m,n}$ terms will be 0, if both of its esteem is unspecified. That is, X $\oplus$ 1,

$$X\bigoplus 0\ ,X\bigoplus 0\ X\bigoplus 0\ ,X\bigoplus 0\ ,X\bigoplus 0\ ,X\bigoplus 0\ ,X\bigoplus 0\ ,$$

$$X\bigoplus 0\ ,X\bigoplus 0\ X\bigoplus 0\ ,X\bigoplus 0\ ,X\bigoplus 0\ ,X\bigoplus 0\ ,X\bigoplus 0\ ,$$

$X\oplus 0\ ,X\oplus 0\ X\oplus 0, X\oplus 0\ X\oplus 0\ ,X\oplus 0\ ,X\oplus 0\ X\oplus 0\ ,X\oplus 0$ and X $\odot$ X are evaluated as 0. Therefore, the unspecified bit with smaller value of C_{impact} (*m; n; v*) is to be filled first in order to minimize the capture transitions effectively. In the proposed power reduction technique, first the unspecified bits are filled based on minimum-transition filling (MT-filling) to minimize the shift-power, and the number of capture transitions are computed. If the capture transition of the given test set is within the threshold limit, then corresponding test set need not be considered for capture-power reduction. The

threshold limit is decided based on switching activities of the CUT. If the capture transitions exceed the threshold, then one unspecified bit with smallest

C_{impact} (m ,*n, v*) (Computed using Equation iv) is filled into the logic value *v* and the remaining unspecified bits are filled to minimize the WTM. If capture-power violation still exists, then unspecified bit with next smallest C_{impact} (*m; n; v*) is to be filled. The process is iterated till the capture-power becomes lesser than the threshold limit .The process of reducing capture and shift-powers are illustrated as follows. Figure I shows the test stimuli and its response as 1XX100X0 and X0X11X10 respectively. The threshold for capture transition is assumed as 3 in this case, i.e, maximum 3 scan cells are allowed to switch in capture mode. If we conduct MT-filling on the test set, Then stimuli and its response becomes 11110000 and 10001010 . The capture transition is computed as 5 which violates the threshold limit. So, it is necessary to compute *Cimpact* for unspecified bits. For example, filling the S2 bit into 0 results in two inconsistent and three consistent bit-pairs, so the *Cimpact*(*m;S2;*0) becomes -1 as shown in Figure ii. The *Cimpact* for S2=1, S3=0 are 0 and -2 respectively as shown in Figure 3.1(c) and (d). Similarly the *Cimpact* for S3=1, S7=0 and S7=1 are computed as 1, 2 and -1 respectively. Since the *Cimpac t(m;S3;*0 (*m; S3;* 0) has the smallest value, the scan cell S3 is filled with logic 0 and other unspecified bits in thetest sets are filled to minimize WTM. Presently, the catch move is 3 and WTM for sweep in and examine out modes are processed as 8 and 13 individually.
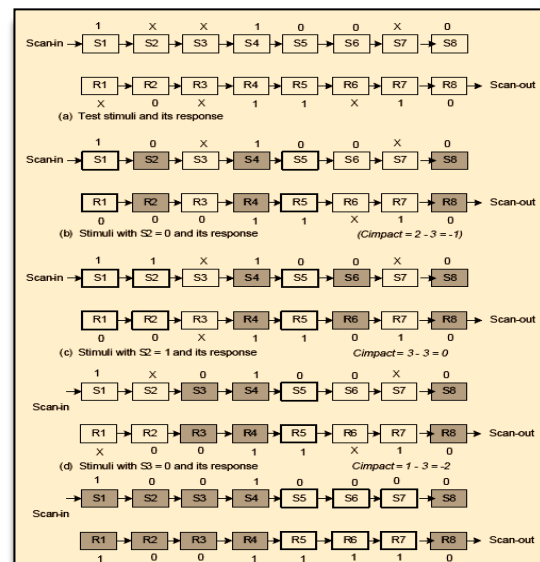

Figure I : Example for filling X-bits to reduce the test power

III.   LOW-POWER SELECTIVE PATTERN COMPRESSION

The test set with more unspecified bits can

accomplish higher pressure proportion. In this way, the proposed LP-SPC procedure considers the test sets which contain more unspecified bits for test data pressure, and the rest of the test sets normal power lessening. That is, the whole test sets are partitioned into two gatherings in view of the measure of unspecified bits in every test set.

The test sets which contain lesser unspecified bits than the limit esteem are indicated as normal power decrease (APR) assemble. The unspecified bits in the APR gathering are filled according to the methodology depicted in the last area to decrease the power. The rest of the test sets are indicated as test data pressure (TDC) aggregate and unspecified bits in this gathering are filled to accomplish high test data pressure. The test sets in TDC gathering are packed according to the following technique. In TDC aggregate, every test set is separated into number of portions with equivalent.
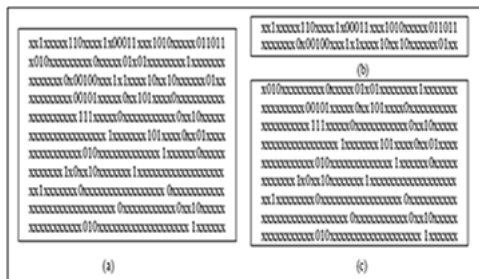

Figure II : Procedure for grouping patterns. (a) Original test sets (b) APR group (c) TDC group

Seg 1		Seg 2	
Pattern	code	Pattern	code
00000000	0	00000000	0
00100001	1	00100001	1
Seg 3		Seg 4	
00000000	00	00000000	00
10001101	11	10001101	11

Table 3.1: Pattern encoding procedure with encoder size *m*=3

data in every fragment are combined and modified in a manner that the resultant examples shrivel into least conceivable examples. The most extreme conceivable examples in every portion are constrained to 2m or less, where m is the span of the encoder. The proposed LP-SPC method can be shown as follows. Figure II (a) contains eleven test sets, each with 40-bits wide. These test sets can be partitioned into two gatherings in light of the measure of unspecified bits in every test set. Give us a chance to consider the limit to isolate the test set to order the gathering as 30% for this situation. That is, the test set which contains 30% or less unspecified bits are considered into APR amasses and the rest are considered for TDC aggregate. Accordingly, the

APR and TDC bunches contain 2 and 9 test sets as appeared in Figures II (b) and II (c) separately. The unspecified bits in APR gathering are dispatched so as to diminish the power as depicted in segment 2. The unspecified bits in the TDC gathering are filled as follows. Let the encoder size is m=3. Every test set can parcel into 5 fragments with size of 8-bits each. The example encoding methodology for TDC gathering is appeared in Table 3.1. The principal portion contains the following nine examples: x010xxxx, xxxxxxxx, xxxxxxxx, xxxxxxxx, xxxxxxxx, xxxxxxx1, xx1xxxxx, xxxxxxxx and xxxxxxxx. Table 3.1 demonstrates the resultant code words for examples in every section. The aggregate number of consolidated examples (Tp) in every portion chooses the code word measure, e.g. Tp=2 for the primary section. In this way, we can encode designs in the primary portion with 1-bit code words. On the off chance that the Tp esteem is in the middle of 2 and 4, then codeword size will be 2-bits as in section 2. On the off chance that Tp> 8, then the codeword measure should be expanded to 4 etc. At long last, the nine test sets in TDC gathering are encoded with 8-bit code words as 10001001, 00110000, 01000001, 00001110, 01100100, 11101000, 10000000, 00000001 and 01100001. The pressure proportion can be ascertained as

$$\text{Comp. ratio } \% = \frac{T_D - (T_E - T_P)}{T_D} \times 100 \qquad \textbf{3.3.1}$$

Where, T_D and T_E are the size of uncompressed test set and encoded test set respectively,

And , TP is the span of test sets in the APR assembles. For this situation, the pressure proportion is registered as,

$$\left\{ \frac{440 - (72 + 80)}{440} \times 100 \right\} = 65.45\% \qquad \textbf{3.3.2}$$

The pattern transformation can be done to get the original test data by using proper remapping hardware logic in decoder.

IV. CONCLUSION

A few productive low-power test data pressure strategies are proposed for concurrent lessening of test data volume and test power in output based test applications. The proposed low-power specific example pressure (LP-SPC) strategy depends on the way that the test set with more unspecified bits can accomplish higher pressure proportion. The power lessening method depends on cautious mapping of the unspecified bits in pre-registered test sets to 0 and 1. We have appeared through investigation and analyses that the LP-SPC procedure can lesser the test application time.

V. FUTURE WORKS

We can broaden these systems for multi-check based implanted center to upgrade both test data pressure

and the test application time. The high rate of X-bit gives a chance to discover filter chain sharing from various centers, so that the relating test sets can be blended and afterward communicated to different chains in parallel testing. By sharing output chain contributions among a few centers it is conceivable to decrease test data volume and abbreviate test application time fundamentally, since centers that share chains are tested simultaneously.

VI. REFERENCES

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