High-Speed Multioutput CLA-Adders Using 8-Bit MCC Adder In Domino Logic

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Abstract: **Adders are the critical parts of processor circuits. The performance of processors increases by improving the performance and functionality of adders. Carry look-ahead (CLA) adder's principle remains dominant in High-speed adder architectures, so the carry delay can be improved by calculating each stage in parallel. In this project by using an 8-bit Manchester carry chain (MCC) adder block in multi output domino CMOS logic. The even and odd carries of this adder are computed in parallel by two independent 4-bit carry chains. Implementation of wider adders based on the use of 8-bit adder module improves the operating speed compared to adders based on the standard 4-bit MCC adder module. Proposed design technique can be used for the implementation of 8, 16, 32 and 64 bit adders in multi output domino logic by using mentor graphics.**

Keywords: **Carry Look Ahead; Manchester Carry Chain Adder; CMOS; VLSI;**

I. INTRODUCTION

ADDITION is the most commonly used arithmetic operation and also the speed-limiting element to make faster VLSI processors. With the rapid growth of the portable electronics market in the last few years, the emphasis in VLSI design is shifting from high speed to low power. Portable applications like wireless communication and imaging systems (digital diaries, smart cards) demand high-speed computations, complex functionalities, and often real-time processing capabilities along with low power consumption. Traditional approaches to minimizing the power consumption of static complementary metal-oxide semiconductor (CMOS) logic networks have advocated straightforward reduction in the supply voltage. Since the dynamic power is proportional to the square of the supply voltage, this is the most effective technique for power reduction. The resulting increase in delay can be effectively compensated through increased data-path parallelism in special-purpose signal-processing applications and by careful transistor sizing [1], [2]. In some situations it has been recommended that the threshold voltage of the transistors be reduced to improve the circuit performance [3], [4]. However, the static power component of the power dissipation has an inverse exponential dependency on the threshold voltage. This implies that reducing the threshold voltage could cause a significant increase in the static power component. Methodologies for minimizing the sum total of static and dynamic energy consumption in general-purpose CMOS circuits have been proposed in [5- 7]. Total power is minimized through careful selection of supply and threshold voltage values and device sizes such that the leakage and switching components of the dissipation are equal. The use of dual-threshold voltages for power reduction has been examined in [8] and [9]. In both the methods, all the transistors in the circuit are initially set to have a low threshold voltage. Subsequently, using the algorithms developed, the threshold voltage of some of the gates that do not lie on critical paths is increased. The leakage power can be reduced by up to 50% without affecting the performance of the circuit. In this paper we explore a mixed-swing topology wherein multiple supply voltages are used in a dual-rail domino logic gate that offers simultaneous power and delay reductions. Dynamic logic gates and circuits have been excellent choice in the design of high-performance modules such as multiple bit adders, subtractors, multipliers, comparators, multiplexers, registers, etc in modern VLSI microprocessors [1]. The advancement in fabrication technology along with the shrinking device size has allowed for placement of nearly two billion transistors on Intel's latest processor [2]. The digital logic gates and circuits designed using dynamic domino technique is considerably faster than the logic gates and circuits designed with standard static logic style. The aggressive technology scaling to improve the performance as well as the integration level makes the noise play a major role in design parameters like area, power and speed [3]. Therefore the digital integrated circuit noise has become one of the most important issues in the design of deep submicron VLSI chips [4] - [9]. The performance of the dynamic circuits can be significantly improved by precise design and properly sizing the transistors. Usually in all the digital circuits the transistor gate length remains uniform. So the size of the transistor in digital circuits depends on the width of the transistor. In this paper the multiple bit domino adders are implemented with L=0.016nm technology along with a supply voltage of 0.7V. The modern technologies move towards smaller, faster, and

cheaper computing systems. This has been facilitated by exponential increase in device density and operating frequency through VLSI technology scaling. We require improved digital logic technique and style which is at the same time energy efficient, fast and noise robust. CMOS technology is the dominant logic style in today's IC design because of its high speed, low power and high packaging density. High-speed adders based on the CLA principle remain dominant, since the carry delay can be improved by calculating each stage in parallel. The Manchester carry chain (MCC) is the most common dynamic (domino) CLA adder architecture with a regular, fast, and simple structure adequate for implementation in VLSI. The recursive properties of the carries in MCC have enabled the development of multi-output domino gates, which have shown area–speed improvements with respect to single-output gates. a new 8-bit carry chain adder block in multi-output domino CMOS logic is proposed. The even and odd carries of this adder are computed in parallel by two independent 4-bitcarry chains. We propose the design of an 8-bit adder module which is composed of two independent carry chains. These chains have the same length (measured as the maximum number of series-connected transistors) as the 4-bit MCC adders. According to our simulation results, the use of the proposed 8-bit adder as the basic block, instead of the 4-bitMCC adder, can lead to high-speed adder implementations. To evaluate the speed performance of the proposed (PROP) design over the conventional (CONV) one, 8, 16, 32 and64-bit adders have been designed according to the carry chain principle and simulate using mentor graphics in a standard 130-nm CMOS technology. The PROP design provides a performance improvement than the CONV design for the 8-bitadder. The MCC is an efficient and widely accepted design approach to construct CLA adders. In this brief, we have present new Manchester design style that is based on two independent carry chains. Each chain computes, in parallel with the other, half of the carries. In this way, the speed performance is significantly improved with respect to that of the standard MCC topology.

II. 8-BIT MCC CIRCUIT OF EXISTED SYSTEM

It can be implemented as parallel combination of two 4bit MCC's these are shown in below figures as

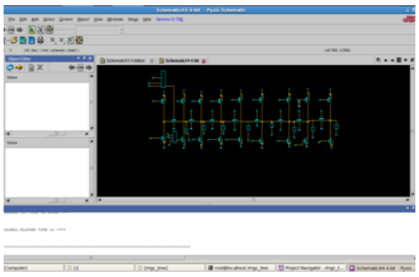

Fig (i): conventional 8-bit MCC carry chain implemented in domino CMOS logic

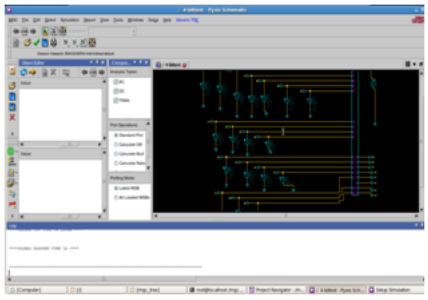

Fig (ii). 8-bit MCC symbol circuit:

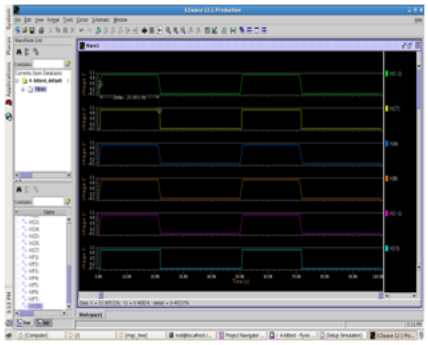

Fig (iii) conventional 8 bit MCC output wave forms

III. PRACTICAL RESULTS

Power consumption of 8-bit MCC in conventional: 23.645 uw

Delay of 8-bit MCC in conventional: 20.401 ns

IV. CONCLUSION

A high speed and an efficient 8 bit Manchester Carry Chain implemented in domino CMOS logic is suitable for Carry Look-Ahead Adders in processor applications is discussed in this project. This circuit is designed and simulated using MENTOR- GRAPHICS software. This design realizes better improvement in reducing the delay by introducing parallelism concept in carry chains. As a result, the 2 separate carry chains namely odd carry chain and even carry chain work in parallel thus increases speed of operation by reducing the delay considerably compared with 4 bit MCC. Hence this 8 bit carry chain is more efficient and can operate at low supply voltages with high speed, thus making this carry chain suitable for most of the high speed processor applications. This high speed Manchester Carry Cain is found to have a delay less than compared to conventional 4 bit MCC delay . Even though the delay of 8 bit MCC gets reduced, number of transistors gets increased in the high speed 8 bit Manchester Carry Chain. As a further work reducing the area of this chain and further reducing the delay by analyzing this design in submicron technology and implementing it in a variable bits like 16 bit, 32 bit Manchester Carry Chain in multi output domino CMOS logic can be considered.

V. FUTURE SCOPE

We design our logic circuit by using transmission gate logic will minimize number of transistors, Minimize all

internal capacitances, by minimizing the active area of the transistors, and thus minimizing power

VI. REFERENCES

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