



Design of Low Power and High Speed Carry Select Adder Using Brent Kung Adder

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Abstract- In this paper, Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. In this paper, structures of 16-Bit Regular Linear Brent Kung CSA, Modified Linear BK CSA, Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA are designed. Power and delay of all these adder architectures are calculated at different input voltages. The results depict that Modified SQRT BK CSA is better than all the other adder architectures in terms of power but with small speed penalty. The designs have been synthesized at 45nm technology using Tanner EDA tool.

Keywords- Brent Kung (BK) Adder; Ripple Carry Adder (RCA); Regular Linear Brent Kung Carry Select Adder; Modified Linear BK Carry Select Adder; Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA;

I. INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. Adders are used in multipliers, in DSP to execute various algorithms like FFT, FIR and IIR. Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important constraint. Design of low power, high speed data path logic systems are one of the most essential areas of research in VLSI. In CSA, all possible values of the input carry i.e. 0 and 1 are defined and the result is evaluated in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. Conventional Carry Select Adder [1] is designed using dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA ($C_{in}=1$) is replaced by Brent Kung adder. As, RCA (for $C_{in}=0$) and Brent Kung adder (for $C_{in}=1$) consume more chip area, so an odd-one scheme i.e., Binary to Excess-1 converter is introduced. Also the square root adder architectures of CSA [2] are designed using Brent Kung adder in order to reduce the power and delay of adder.

In this paper, Modified Square Root Carry select

Adder using Brent Kung adder is proposed using single BK and BEC instead of dual RCAs in order to reduce the power consumption with small penalty in speed.

This paper is organized as follows: In section 2, parallel prefix adders are illustrated. Section 3 explains Regular Linear BK CSA and section 4 give details of Modified Linear BK CSA. In section 5, Regular Square Root BK CSA is elucidated. The structure of Modified Square Root BK Carry Select Adder is enlightened in Section 6. Simulation Results and comparison are evaluated in section 7 and section 8 concludes.

II. PARALLEL PREFIX ADDERS

Parallel prefix adders [3] are used to speed up the binary additions as they are very flexible. The structure of Carry Look Ahead Adder (CLA) is used to obtain parallel prefix adders [4]. Tree structures are used to increase the speed [5] of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation. The construction of parallel prefix adder [6] involves three stages:

1. Pre-processing stage
2. Carry generation network
3. Post processing stage

Pre-processing stage

Generate and propagate signals to each pair of inputs A and B are computed in this stage. These

signals are given by the following equations:

$$P_i = A_i \text{ xor } B_i \quad (1)$$

$$G_i = A_i \text{ and } B_i \quad (2)$$

Carry generation network

In this stage, we compute carries equivalent to each bit. Implementation of these operations is carried out in parallel. After the computation of carries in parallel they are segmented into smaller pieces. Carry propagate and generate are used as intermediate signals which are given by the logic equations 3&4:

$$C_{P_i:j} = P_i:k+1 \text{ and } P_k:j \quad (3)$$

$$C_{G_i:j} = G_i:k+1 \text{ or } (P_i:k+1 \text{ and } G_k:j) \quad (4)$$

The operations involved in fig.1 are given as:

$$C_{P0} = P_i \text{ and } P_j \quad (3(i))$$

$$C_{G0} = (P_i \text{ and } G_j) \text{ or } G_i \quad (3(ii))$$

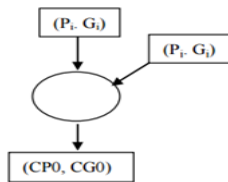


Fig. 1 Carry Network

Post processing Stage

This is the concluding step to compute the summation of input bits. It is common for all the adders and the sum bits are computed by logic equation 5 & 6:

$$C_{i-1} = (P_i \text{ and } C_{in}) \text{ or } G_i \quad (5)$$

$$S_i = P_i \text{ xor } C_{i-1} \quad (6)$$

Brent-Kung Adder

Brent-Kung adder [7] is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in Brent Kung adders. But the gate level depth of Brent-Kung adders [8] is $O(\log^2(n))$, so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Fig.2.

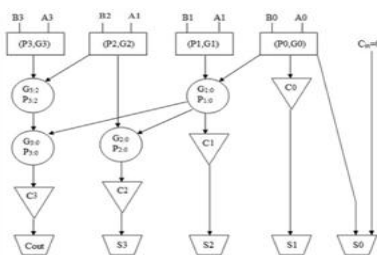


Fig. 2 Block Diagram of 4-Bit Brent Kung Adder

III. REGULAR LINEAR BRENT KUNG CARRY SELECT ADDER

Conventional Carry Select Adder consists of dual Ripple Carry Adders and a multiplexer. Brent Kung Adder [9] has reduced delay as compared to Ripple Carry Adder. So, Regular Linear BK CSA is designed using Brent Kung Adder. Regular Linear KS CSA consists of a single Brent Kung adder for $C_{in}=0$ and a Ripple Carry Adder for $C_{in}=1$. It has four groups of same size. Each group consists of single Brent Kung adder, single RCA and multiplexer. We use tree structure form in Brent Kung adder to increase the speed of arithmetic operation. The block diagram of Regular Linear BK CSA is shown in Fig.3.

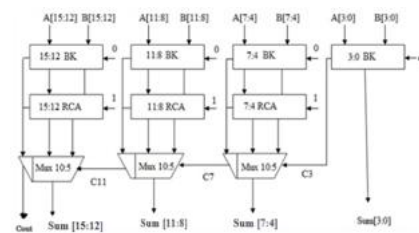


Fig. 3 Block Diagram of 16-bit Regular Linear BK Carry Select Adder

In group 2 of Regular Linear CSA, there are single BK for $C_{in}=0$ and single RCA for $C_{in}=1$. Now, the C_3 tells whether the input carry is 0 or 1 and depending on its value the output of particular block is selected. If $C_3=0$ then the output of BK with $C_{in}=0$ is selected using 10:5 multiplexer and if $C_3=1$ then output of RCA with $C_{in}=1$ is selected using the MUX. A 4-bit Sum [7:4] and an output carry, C_7 is obtained at the output of group 2. The schematic of 16-Bit Regular linear BK CSA is shown in Fig. 4. Now, power and delay of this circuit is calculated.

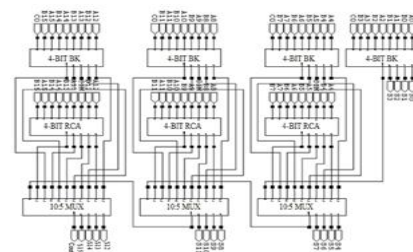


Fig. 4 Schematic of 16-Bit Regular Linear BK CSA

IV. MODIFIED LINEAR BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for $C_{in}=0$ and Brent Kung adder for $C_{in}=1$ and is therefore area-consuming. So, different add-one schemes like Binary to Excess-1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified in order to obtain a reduced area

and power consumption. Binary to Excess-1 converter is used to add 1 to the input numbers. So, here Brent Kung adder with $C_{in}=1$ will be replaced by BEC because it requires less number of logic gates for its implementation so the area of circuit is less. A circuit of 4-bit BEC and truth table is shown in Fig. 5 and Table I respectively.

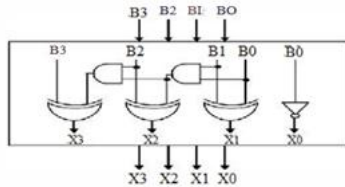


Fig. 5: 4-bit Binary to Excess-1 code Converter

The Boolean expressions of 4-bit BEC are listed below, (Note: functional symbols, - NOT, & AND, ^XOR).

$$X0 = \neg B0$$

$$X1 = B0 \oplus B1$$

$$X2 = B2 \oplus (B0 \& B1)$$

$$X3 = B3 \oplus (B0 \& B1 \& B2)$$

TABLE I. TRUTH TABLE OF 4-BIT BINARY TO EXCESS-1 CONVERTER

Binary Logic Bo B1B2B3	Excess-1 Logic XOXIX,X.
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Linear Modified BK CSA is designed using Brent Kung adder for $C_{in}=0$ and Binary to Excess-1 Converter for $C_{in}=1$ in order to reduce the area and power consumption with small speed penalty. Linear Modified BK CSA consists of 4 groups.

Each group consists of single BK adder, BEC and multiplexer. The block diagram of Linear Modified BK CSA is shown in Fig.6.

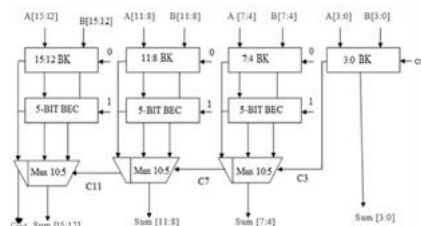


Fig.6 Block Diagram of 16-bit Linear Modified BK Carry Select Adder

To replace the N-bit Brent Kung adder, an N+1 bit BEC is required. The importance of BEC logic comes from the large silicon area reduction when designing Linear Modified BK CSA for large number of bits. The schematic of Linear Modified BK CSA is shown in Fig. 7.

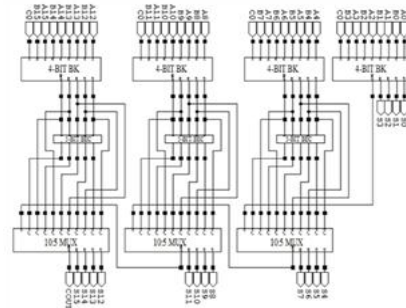


Fig.7 Schematic of 16-bit Linear Modified BK CSA

V. REGULAR SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung CSA consumes large area and to reduce its area a new design of adder is used called Regular Square Root Brent Kung Carry Select Adder.

Regular Square Root BK CSA has 5 groups of different size Brent Kung adder. Each group contains single BK for $C_{in}=0$, RCA for $C_{in}=1$ and MUX. The block diagram of the 16-bit regular SQRT BK CSA is shown in Fig. 8. High area usage and high time delay are the two main disadvantages of Linear Carry Select Adder. These disadvantages of linear carry select adder can be rectified by SQRT CSA [10]. It is an improved version of linear CSA. The time delay of the linear adder can decrease, by having one more input into each set of adders than in the previous set. This is called a Square Root Carry Select Adder.

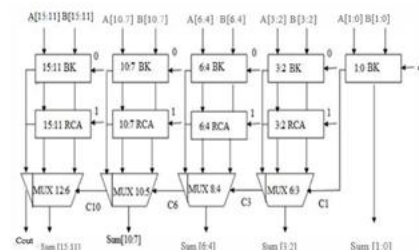


Fig. 8 Block Diagram of 16-bit Regular Square Root BK Carry Select Adder

The schematic of 16-bit Regular Square Root BK Carry Select Adder is shown in Fig. 9. There are 5 groups in Regular Square Root BK Carry Select Adder [11]. Here single Brent Kung adder is used for $C_{in}=0$ and ripple carry adder is used for $C_{in}=1$ and then there is a multiplexer stage. Due to the presence of RCA and BK, this circuit consumes large area.

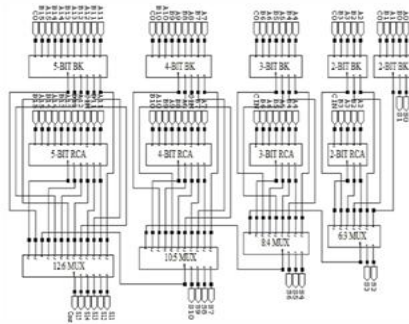


Fig. 9 Schematic of 16-Bit Regular SQRT BK CSA

VI. MODIFIED SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Modified Square Root Brent Kung Carry Select Adder has been designed using Brent kung adder for $C_{in}=0$ and BEC for $C_{in}=1$ and then there is a multiplexer stage. It has 5 groups of different size Brent Kung adder and Binary to Excess-1 Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA therefore it consumes less area. The block diagram of the 16-bit modified Square Root BK Carry Select Adder is shown in Fig. 10.

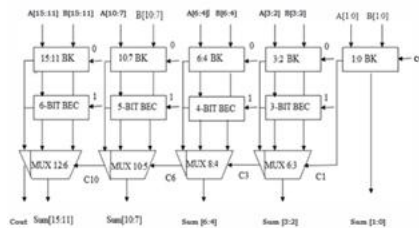


Fig. 10 Block Diagram of 16-bit Modified SQRT BK CSA

Each group contains one BK, one BEC and MUX. For N- Bit Brent Kung adder, N+1 Bit BEC is used. Fig.11 shows the schematic of 16-Bit Modified SQRT CSA. Power consumption and delay of this adder is calculated for 16-Bit word size.

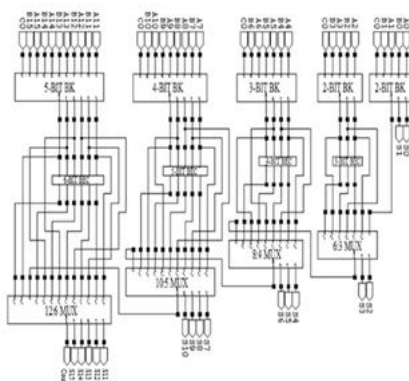


Fig. 11 Schematic of 16-Bit Modified SQRT BK CSA

VII. SIMULATION RESULTS AND COMPARISON

Various adders were designed in Tanner EDA version 13.0 tool using Predictive Model Beta Version 45nm CMOS technology. Power consumption delay of various adders like Regular Linear BK CSA, Regular SQRT BK CSA, Modified Linear BK CSA and Modified SQRT BK CSA has been calculated for 16-Bit word size. The comparison of various adders for different parameters like delay and power consumption is shown in Table II. The result analysis shows that Modified Square Root Brent Kung Carry Select Adder shows better results than all the other adder architectures in terms of power consumption at different input voltages but with a small speed penalty. The graphical representation of comparison of Regular Linear BK CSA and Modified Linear BK CSA for different input voltages for power consumption is shown in fig. 12. Results show that modified linear BK CSA shows better results than Regular Linear BK CSA.

TABLE II. COMPARISON OF DIFFERENT ADDERS FOR POWER CONSUMPTION AND DELAY AT VARIOUS INPUT VOLTAGES

Adder	Supply Voltage									
	Power(W)					Delay (s)				
	0.6V	0.8V	1.0V	1.2V	1.4V	0.6V	0.8V	1.0V	1.2V	1.4V
Regular Linear BK CSA	1.78E-08	3.47E-08	5.37E-08	1.78E-07	1.02E-06	1.13E-10	6.44E-11	4.63E-11	2.47E-11	8.78E-12
Linear Modified BK CSA	1.24E-08	2.16E-08	4.13E-08	1.12E-07	7.43E-07	1.21E-10	1.04E-10	1.02E-10	6.27E-11	6.41E-11
Regular Square Root BK CSA	1.23E-08	3.48E-08	7.42E-08	1.74E-07	1.03E-06	8.08E-11	6.34E-11	4.11E-11	3.64E-11	3.03E-11
Modified Square Root BK CSA	1.29E-08	2.84E-08	4.12E-08	1.00E-07	8.9E-07	1.24E-10	9.16E-11	9.10E-11	8.03E-11	6.22E-11

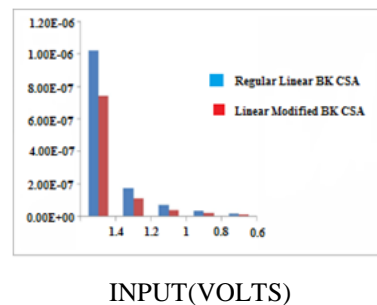


Fig. 12 Comparison of Regular Linear BK CSA and Modified Linear BK CSA for power comparison at different input voltages

The graphical representation of comparison of Regular SQRT BK CSA and Modified SQRT BK CSA at different input voltages for power consumption is shown in fig. 13.

Results show that modified SQRT BK CSA shows better results than Regular SQRT BK CSA. The graphical representation of comparison of Regular linear BK CSA and Modified SQRT BK CSA for power consumption at different input voltages is shown in Fig. 14. The graphical representation of comparison of different adders for delay at different input voltages is shown in Fig. 15.

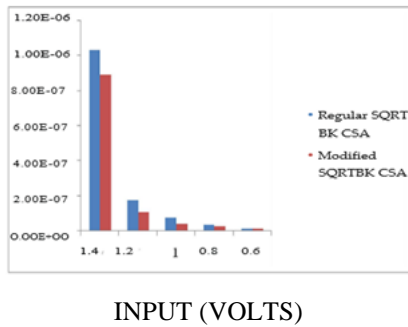


Fig. 13 Comparison of Regular Sqrt BK CSA and Modified Sqrt BK CSA for power comparison at different input voltages

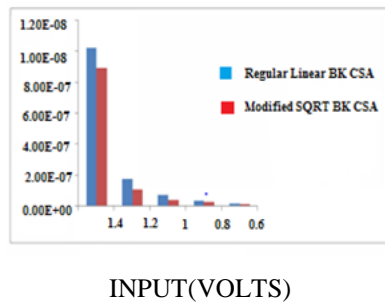


Fig. 14 Comparison of Regular Linear BK CSA and Modified Sqrt BK CSA for power comparison at different input voltages

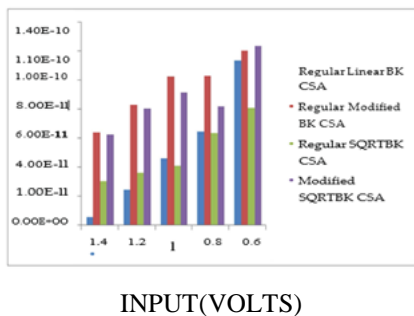


Fig. 15 Comparison of different adders for delay at different input voltages

Fig. 16, Fig. 17 and Fig. 18 shows the power Vs Temperature graphs for Regular linear BK CSA and modified linear BK CSA, regular Sqrt BK CSA and modified Sqrt BK CSA, regular linear BK CSA and modified Sqrt BK CSA respectively. From the graphical representation it is clear that Modified Linear and Square Root BK CSA have reduced power consumption but they have increased delay in comparison to Regular Linear and Square Root BK CSA.

Modified Sqrt Brent Kung carry select adder consumes less power than all the other adder architectures at different input voltages and as the input voltage is reduced, the power consumption also reduces.

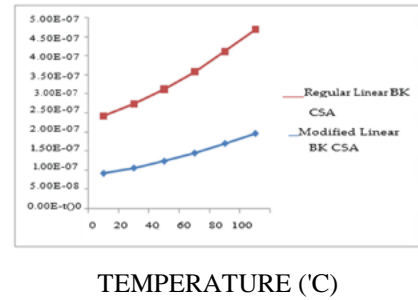


Fig. 16 Power Vs Temperature for Regular Linear BK CSA and Modified Linear BK CSA

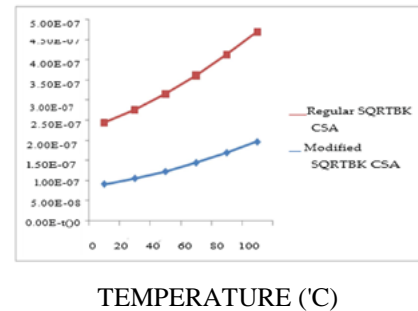


Fig. 17 Power Vs Temperature for Regular Sqrt BK CSA and Modified Sqrt BK CSA

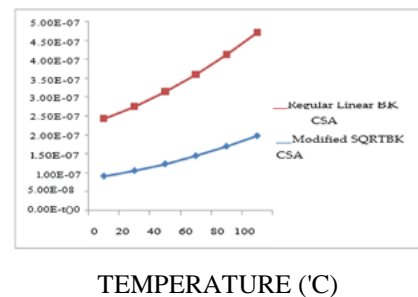


Fig. 18 Power Vs Temperature for Regular Linear BK CSA and Modified Sqrt BK CSA

VIII. CONCLUSION

In this work, a Modified Square Root BK Carry Select Adder is proposed which is designed using single Brent kung adder and Binary to Excess-1 Converter instead of using single Brent kung adder for $C_{in}=0$ and Ripple Carry Adder for $C_{in}=1$ in order to reduce the delay and power consumption of the circuit. Here, the adder architectures like Regular Linear BK CSA, Modified Linear BK CSA, Regular Sqrt BK CSA and Modified Sqrt BK CSA are designed for 16-Bit word size only

This work can be extended for higher number of bits also. By using parallel prefix adder, delay and power consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore BrentKungadder is used. The synthesized results show that powerconsumption of Modified Sqrt BK CSA is reduced in comparison to Regular Linear CSA but with small speedpenalty. The calculated results conclude that

Modified Square Root BK Carry Select Adder is better in terms of power consumption when compared with other adder architectures and can be used in different applications of adders like in multipliers, to execute different algorithms of Digital Signal Processing like Finite Impulse Response, Infinite Impulse response etc.,.

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