

A Chandrika Rani et al. (IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH Volume No.4, Issue No.6, October – November 2016, 5169-5178.*

Compensation Of Voltage Sags With Transformer Less Active Voltage Quality Regulator Using Fuzzy Controller

A.CHANDRIKA RANI PG Scholor, Dept of EEE (EPE) SKD, Gooty, Andhrapradesh, India.

N.NARASIMHULU Associate Professor & HOD, Dept of EEE SKD, Gooty, Andhrapradesh, India

Dr. R.RAMACHANDRA

Principal

SKD, Gooty, Andhrapradesh, India

Abstract:- **Change from the rated level in the voltage causes the severe damage to the industries and sensitive loads. If deviation from the rated value is much more, it may be dangerous to the domestic loads also. To avoid this problem so many compensating devices are there in existence. In order to compensate voltage sags in a better way a series connected shunt structured transformer less circuit is designed known as Active Voltage Quality Regulator with Parasitic Boost Circuit (PB-AVQR) where this may handle deep sags which are up to 50% of the rated values in voltage levels. This design may also help in compensation of deep voltage sags. High operating efficiency is obtained due to application of the DC link voltage adaptive control method. Here in this design the storage devices inductors and capacitors plays an important role in supplying the missing voltage which is necessary to the load stations, when the sag occurs in the system. For achieving the exact compensation of sags the duty ratio of the power electronic devices used in the model is maintained perfect with the use of the FUZZY controller. By using the Fuzzy controller instead of the PI controller in the control circuit fastness of the compensation is much improved and also the efficiency is increased, The THD of the output voltage waveform is much reduced which is more desirable. Simulations using MATLAB/SIMULINK are carried out to verify the performance of the proposed circuit.**

*Key words:-***Dynamic Voltage Restorer (DVR); Dynamic Sag Correction; Long Duration Deep Sag; Parasitic Boost Circuit; Series Connect Compensator; Fuzzy Controller;**

I. INTRODUCTION

Power quality is the main important issue for a utility supplying electrical power to the consumer. Power quality is nothing but voltage, frequency, current and some other electrical parameters should be under the rated values. Even a small distraction in power quality may lead to heavy losses for commercial and industrial consumers. There are so many problems related to this power quality issue such as the Transients, harmonics, Voltage variations, faults, Sag and Swells. The term power quality is rather general concept. Broadly, it may be defined as provision of voltages and system design so that user of electric power can utilize electric energy from the distribution system successfully, without interference on interruption. Power quality is defined in the IEEE 100 Authoritative Dictionary of IEEE Standard Terms as the concept of powering and grounding electronic equipment in a manner that is suitable to the operation of that equipment and compatible with the premise wiring system and other connected equipment Utilities may want to define power quality as reliability. From the Power Quality market or industry perspective, it is any product or service that is supplied to users or utilities to measure, treat, remedy, educate

engineers or prevent Power Quality issues, problems and related items.

Sags and Their Causes: A short duration voltage variation is often referred as sagging. When there is a decrease between 0.1 to 0.9pu in rms voltage, sagging takes place as shown in figure1.1.

Fig.1.1: Voltage waveform affected by sag

Voltage sags/swells caused by unsymmetrical line to line, single line-to-ground (SLG), double line-toground and symmetrical three phase faults effects on sensitive loads. Voltage sags can occur at any instant of time, with amplitudes ranging from 10- 90% and a duration lasting for half a cycle to one minute. Voltage swell, on the other hand is defined as an increase in rms voltage or current at the power frequency for durations from 0.5 cycles to 1 minute. In simple words swell can be defined as sudden rise of the voltage from its rated value. Due to the fact that voltage swells are less common in

distribution systems, they are not as important as voltage sags. Voltage sag and swell can cause sensitive equipment (such as found in semiconductor or chemical plants) to fail, or shutdown, as well as create a large current unbalance that could blow fuses or trip breakers. These effects can be very expensive for customers ranging from minor quality variations to produce downtime and equipment damage. The causes of voltage sags on a transmission level system are similar to those on a distribution system. They include the weather (especially lightning), construction accidents, transportation accidents (helicopter or light planes are common culprits), animals or a fault on another part of the system causing "sympathetic" sags. There have been recorded instances of the nesting habits of large birds in the towers resulting in phase-to-ground faults when the insulators were "shorted out" by bird droppings that were made into a conductive path during rain storms. Lightning is often attributed with being the most common cause of faults on overhead transmission and distribution lines. The fault can occur by lightning directly striking a phase conductor, or by striking a grounded object, such as shield wire or tower, which is called a backflash.A flashover develops from the voltage path across the phase conductors to ground or to another other phase, resulting in flow of fault current. Transmission related voltage sags are normally shorter in duration than distribution voltage sags. Similar to the transmission system causes, weather (lightning, wind, ice), animal contact, contamination of insulators, construction accidents, motor vehicle accidents, falling or contact with tree limbs can result in voltage sags. In various studies, 50% or more of the recorded low/high RMS events were caused by load equipment in the same building. Sudden increases in the current requirement can have the same effect within a facility's wiring as on a utility distribution system. Voltage sags can be caused by fault conditions within the building, or the startup of large inductive loads, such as motors, that create a temporary in rush current condition. The starting of large horsepower motors that would draw adequate current are typically longer in duration than 30 cycles, and the associated voltage magnitudes are not as low as with a utility fault. The voltage sag condition lasts until the large current demand decreases, or the fault is cleared by a protective device. In the plant, this will typically be a fuse or a plant feeder breaker.

Transients: When you flip the switch, it takes a brief moment for the inductors and capacitors to get charged to where they react steadily with the alternating current. In some situations these transients are also called as the surges. There are two types of transients they are the Oscillatory transients and Impulsive transients. Various

reasons like faults in the power system, failures in the equipment, etc. may create the interruptions in the network, which may lead to the change in the voltage/current.

Harmonics: Harmonics cause distortion in current and voltage waveforms which results in the deterioration of the power system. Non-linear loads are the main reason for the cause of harmonics, even linear loads also cause harmonics but not much severe.

Faults: There are different types of faults occurring in the power system which may affect the power quality. They are like Line to Ground (LG) fault, Double Line to Ground (LLG), Triple Line (LLL) faults etc**.** These may create damage to the end user also both in the economical and technical point of view which may damage the equipment using in the load side.

METHODS OF COMPENSATION: Mainly the decrease of voltage levels even for the small instant of time may create large financial problems, if the sag exists for the more time not only economically it leads to technical problems also. So deep sags for the larger interval of time cannot be ignored which are more intolerable than the shallow sags.So there are many devices in existence for the compensation of these sags, mostly used devices are series connected in the line where their duty is to inject the missing voltage into the line. If the fault existing in the power system for less interval of time the switch gear which is used in power system will manage to extinct the fault within a less span of time. Actually these compensating devices are divided into two groups, they are the inverter-based regulator and direct ac-ac converters. The series connected devices mostly comes under the category of the voltage sourced inverter based structures. Under these series connected devices Dynamic Voltage Regulator (DVR) is the one, which is widely used. Not only DVR some circuits which are designed without transformer can also be used for the compensation of voltage sags, they are like Dynamic Sag Corrector (DySC) and so many improvised circuits of DySC.

Dynamic Voltage Regulator: Among the power quality problems (sags, swells, harmonics…) voltage sags are probably the most severe disturbances. In order to overcome these problems the concept of custom power device has become introduced recently. One of those devices is the Dynamic Voltage Restorer (DVR), which is one of the most efficient and modern custom power device used in power distribution networks. A DVR is a series-connected solid-state device that injects voltage into the system in order to regulate the load side voltage. It is normally installed in a distribution system between the supply and a critical load feeder at the so-called point of

common coupling (PCC).Its primary function is to rapidly boost up the load-side voltage in the event of a voltage sag in order to avoid any power disruption to that load. There are various circuit topologies and control schemes that can be used to implement a DVR. Together with voltage sags and swells compensation, DVR can also have other features like: line voltage harmonics compensation, reduction of transients in voltage and fault current limitations. Mainly the structure of the compensating circuit is changed where some devices are eliminated and some are added in order to reduce the power quality problems. The general configuration of the DVR as shown in figure 1.2 consists of:

- An Injection/ Booster transformer
- A Harmonic filter
- Storage Devices
- A Voltage Source Converter (VSC)
- DC charging circuit
- A Control and Protection system

Fig.1.2: Basic structure of DVR

Here in the DVR circuit as both voltage source converter (VSC) and injection transformer are used the cost incurring on DVR will increase much. As injection of voltage during the sag is done by transformer, some extra switchgear must be used in order to protect the transformer from the various faults. This switchgear will again lead to increase in cost and maintenance. So in order to reduce the cost, and for compensating the deep sags a new topology is introduced. DySC is one of such circuit which will help in compensation of sags, by using this DySC circuit even the maintenance is also reduced.

Dynamic Sag Corrector:

Fig.1.3: Single-phase DySC configuration

In this structure Dynamic Sag Corrector (DySC) as in figure 1.3 there is no series transformer. Instead of series transformer elements like inductors and capacitors will help in injecting the missing voltage into the line. There are so many types of sag correcting structures. The circuit working is based on the DC link voltage which is taken from the capacitors in the circuit. As there is no series transformer the cost of these circuits is much less than the DVR.When the line voltage differs from the rated value, the missing one will be injected by DySC through its half-bridge series converter (V1, V2) and output filter (*Lf , Cf*) to maintain the load voltage at its rated value. During this period of time, the energy needed for the compensation is provided by the residual supply via passive shunt converter (D1, D2, *L*1) and stored in the dc-link capacitors (*C*1*, C*2).As the DC link voltage cannot charge more than the rated peak value, so this structure of DySC cannot compensate the sags deeper than 50%. The ride-through time of the DySC in deeper voltage sags is limited by the dclink energy storage, and it is inadequate to provide reliable protection for sensitive loads. As in the basic circuit, the sags deeper than the 50% of voltage cannot be compensated which exists for more time interval. So even the basic structure of Sag corrector circuit is not good enough in compensation, sometimes backup grid is needed to compensate the higher voltage sags.So some changes have been done in these structures in order to make it capable of compensating the deep sags which are occurring for more interval of time. The position of shunt converter and series converter are changed in such a way that DC link voltage can be charged more than the peak value, so that structure can compensate the sags which are very deep and exist for more time. The changed structure of DySC will form the boosting circuit. So resulting circuit can be named as transformerless active voltage quality regulator with the parasitic boost circuit (PB-AVQR). The DC link adaptive control method is adapted in this circuit, so the high efficiency is obtained even for the low cost and less complex circuit.

II. WORKING PRINCIPLE AND TOPOLOGY OF PB-AVQR

Mainly PB-AVQR structure consists of five important parts namely bypass switch, filter circuit, half bridge inverter, shunt converter and storage module. Under the normal operating conditions bypass switch will be in ON state, whenever voltage levels varies from the actual value switch will goes into the OFF position and the compensating circuit will comes into the picture. The inverter will be controlled in such a way that it makes the compensating circuit to deliver the missing voltage into the line.

Analysis of Circuit: Here for the analysis of circuit we have to take each and every aspect into consideration, like triggering angles of thyristors which will make the analysis tedious. So for the simplified analysis Diodes are placed in the circuit instead of thyristors. The analysis will be same and circuit can be called as SPB-AVQR as in figure 2.4.

Fig.2.4: SPB-AVQR Topology

The control strategy which we are using is sinusoidal pulse width modulation or PI controller can be used for the sake of triggering the power electronic devices. As IGBT1 (V1) and IGBT2 (V2) are also creating parallel circuit, their switching sequence will show much effect on the DC link voltage. Indirectly this will show effect on the output voltage.

Mode 1 of operation:

Fig.2.5: Operating condition during V2 ON condition

Fig.2.6: Operating condition during V2 OFF condition

The figures 2.5 & 2.6 give us operation of the circuit in the positive half cycle.

During the positive half cycle as shown in figure 2.5 ,when IGBT2 (V2) is switched on ,inductor L1 will be charged through diode D2 from the grid, in the mean time capacitor C2 will discharge the energy which will compensate the reduced voltage at the load side.When IGBT (V2) is switched off, as shown in figure 2.6, the energy stored in the inductor during previous period is released to dclink capacitors *C*1 and *C*2 through anti parallel diode of IGBT1 (VD1). So the reduced voltage from the supply voltage will be compensated with the help of energy supplied from inductor.So here in this process of charging and compensation there is no need of extra source in order to compensate. Energy needed is taken from the source itself where the circuit will charge itself from source.

Mode 2 of operation:

Fig.2.7: Operating condition during V1 ON condition

Fig.2.8: Operating condition during V1 OFF condition

During the negative half cycle when IGBT1 (V_1) is switched on as shown in the figure 2.7 that is in the negative half cycle inductor L_1 is charged via diode D_1 through IGBT1 (V₁) and compensation of load is done by C_1 . When this IGBT1 (V₁) is switched off as shown in figure 2.8 inductor L_1 will releases energy to capacitors C_1 and C_2 through the anti parallel diode of IGBT2 (V_2) . So in each half cycle one capacitor will discharges the required energy which is actually obtained from the supply source via charging.Here actually the compensation is mainly depends on the duty ratio given to the circuit. The duty ratio of all the devices will depends on the controller used.Switching on and off that is triggering and extinction depends on controller where it decides as per the load requirement and maintain the load voltage always a constant value. So theoretically compensation ability of the circuit is unlimited as long as supply is capable of supplying the power. But boost circuit is parasitic in nature on the series inverter and the two switches are controlled according to the missing voltage, so there exists some restrictions.

III. THEORETICAL ANALYSIS

DC link voltage is the key parameter which will decide the maximum injected voltage for the compensation. The relation between the DC link voltage and other system parameters and feasibility in mitigating deep sags will obtained based on circuit model.

As working principles of both positive and negative half cycles of the circuit are same we can analyze any of the cycles and implement the same to other.

Fig.3.1: Waveforms of supply voltage, load voltage, and UaN. When V2 On/Off.

Fig.3.2: Waveforms of supply voltage, load voltage, and UaN. When V1 On/Off.

 U_{aN} is actually switching pulse voltage which is mainly depends on the supply voltage and load voltage required, where some extra DC-link voltage is added or subtracted in order to get the desired switching pulses from the controller as shown in figures 3.1 and 3.2 both in positive and negative half cycles respectively.

As we are using in-phase compensation the energy needed to maintain load voltage is given by

$$
E_0 = (T_0 \Delta V / 2V_{ref})P_0 \tag{3.1}
$$

Where T_0 is the grid voltage period time, V_{ref} is the rated rms value of the load voltage, P_0 is the rated load power, and ΔV is the rms value of the missing voltage.During steady state compensation the energy needed should be supplied from the supply itself. The simplified circuit model of circuit is illustrated in figure 3.3 & 3.4, where compensation loop including the filter and the load is ignored and only the charging circuit is considered.

Fig.3.3: Simplified model when V2 turned on

Fig.3.4: Simplified model when V2 turned off

 V_s is the supply rms voltage. The state equations are given by

$$
L_1 \frac{dI_{on}}{dt} = \sqrt{2}V_s \sin(\omega t)
$$
 (3.2)

$$
L_1 \frac{dI_{off}}{dt} = \sqrt{2}V_s \sin(\omega t) - V_{dc1} - V_{dc2}
$$
 (3.3)

The above equations can be discretized as

$$
L_1 \Delta I_{onn} = \sqrt{2} V_s \sin(\omega n T_s) t_{onn} (3.4)
$$

$$
L_1 \Delta I_{offn} = [\sqrt{2} V_s \sin(\omega n T_s) - 2 V_{dc}] t_{offn} \qquad (3.5)
$$

where t_{on} and t_{off} are, respectively, the turn-on and turn-off time of V2 in the n_{th} switching cycle, Ts is the switching period, V_{dc} is the steady-state dc-link voltage, and ΔI_{onn} or ΔI_{offn} represents the variation amount in charging current during *ton* or *t*offn. As the analysis is within the positive half-cycle of the grid, there exists a constraint $n \leq T_0 / 2Ts$, apparently, t_{on} and t_{offn} here are actually the inverter's duty cycle.

$$
t_{onn} = \frac{r_s}{2} \left[1 + \frac{\sqrt{2\Delta V} \sin(\omega n T_s)}{V_{dc}} \right] (3.6)
$$

$$
t_{offn} = \frac{r_s}{2} \left[1 - \frac{\sqrt{2\Delta V} \sin(\omega n T_s)}{2} \right] (3.7)
$$

The charging energy provided by the grid in nth switching cycle via boost circuit can be expressed as

$$
E_{in\,n} = \frac{1}{2} L_1 \Delta l_{on\,n}^2 + L_1 I_{off(n-1)} \Delta l_{on\,n} \tag{3.8}
$$

The energy provided in the nth switching cycle can be written as follows

$$
E_{inn} = \frac{T_s^2 V_s^2 A^2}{4L_1} \left(1 + \sqrt{2}BA\right)^2 + \frac{\sqrt{2}T_s^2 V_s A}{2L_1 V_{dc}} \times
$$

$$
\left(V_{dc} + \sqrt{2}\Delta V A\right) \sum_{k=n_0}^{n-1} (\sqrt{2}V_{ref}C - V_{dc})
$$
 (3.9)

Where

 $A=sin\omega nT_s$

$$
B = \frac{\Delta V}{V_{dc}}
$$

C = sin($\omega K T_s$)

As we obtain E_1 , added with n ranging from 1 to $T_0/2T_s$. The overall energy balance equation is given as

$$
E_1 = T_s^2 V_s^2 \left(\sum_{n=1}^{\frac{T_0}{2T_s}} A^2 + 2\sqrt{2} B \sum_{n=1}^{\frac{T_0}{2T_s}} A^3 + 2B^2 \sum_{n=1}^{\frac{T_0}{2T_s}} A^4 \right) + T_s^2 \sqrt{2} V_s^2
$$

$$
\frac{T_s^2 \sqrt{2} V_s}{2L_1} \sum_{n=n_0}^{n_e} \left[\left(A + \sqrt{2} B A^2 \right) \sum_{k=n_0}^{n-1} \left(\sqrt{2 V_{ref} C} - V_{dc} \right) \right]
$$

(3.10)

I_{max} is expressed as

$$
I_{max} = \frac{\sqrt{2}T_sV_s\sin(\omega n_{max}T_s)}{2L_1} \left[+\sqrt{2}B\sin\omega n_{max}T_s \right] +
$$

$$
\sum_{n=n_0}^{n_{max}} \frac{T_s}{L_1} (\sqrt{2}V_{ref}C - V_{dc})
$$
 (3.11)

Where n_{max} is the switching cycle when I_{offn} reaches its maximum value and n_{max} can be written as follows

$$
n_{max} = ceil\left[\frac{r_{0}(\pi - \arcsin\frac{V_{dc}}{V_{ref}})}{2\pi T_{s}}\right]
$$
(3.12)

As we cannot obtain the DC link voltage directly an iterative algorithm is given where T_s , V_s , T_o , V_{ref} , L_1 , and P_0 are all treated as constants.

But this theoretical analysis of SPB-AVQR may differ from PB-AVQR with small differences due to consideration of α for VT3 and VT4 in main circuit.

The charging process begins after the VT3 or VT4 is triggered, so the initial superposition instant n_0 is now determined by α denoted by n_1 and the energy balance equation is written as follows

 $T_{\rm c}$ $\frac{T_0 \Delta V}{2V_{ref}} P_0 = \frac{T_s^2 V_s^2}{4L_1}$ $\frac{\int_{S}^{2} V_{S}^{2}}{4L_{1}} \left(\sum_{n=n_{1}}^{n_{e}} A^{2} + 2\sqrt{2} B \sum_{n=n_{1}}^{n_{e}} A^{3} \right)$ 2B2n=n1neA4+Ts22Vs12L1n=n1neA+2BA2k=n1n *−*12*VrefC–Vdc* (3.13)

$$
n_1 = ceil(\frac{\alpha T_0}{2\pi T_s})\tag{3.14}
$$

Furthermore, the thyristors are triggered only once in each half-cycle and the current through them should be higher than the holding current to maintain the triggered state. So, α is required to meet the constraint expressed as follows

$$
\sqrt{2} V_{\text{ref}} \sin \alpha > V_{\text{dc}} \tag{3.15}
$$

This theoretical analysis is done based on the SPB-AVQR circuit which can also be implemented for PB-AVQR circuit.

IV. SIMULATION MODELS AND RESULTS

SYSTEM PARAMETERS: The four main parameters which we have to design for the best operation of the proposed circuit are C_1 , C_2 , L_f $\&$ C_f , charging inductor L_1 . Here nominal voltage is nothing but the required output load voltage. The switching frequency of the power electronic devices will decide the duty ratio of total circuit.

The filter capacitor and inductor will be designed in such a way that it will be suitable to circuit in order to eliminate the harmonics in the output voltage. So in order to design the circuit for the desired operation certain ratings of devices and different parameters should be taken into the consideration. Some of the system parameters are given in table 5.1.

Description	Parameters	Real Value
Nominal voltage	V_{ref}	220V
Line frequency	F_0	50Hz
Switching frequency	F_s	$15K$ hz
DC-link capacitor	C_1/C_2	4700µF
Filter inductor	L_f	1.5mH
Filter Capacitor	C_f	$20 \mu F$
Charging inductor	L_1	2mh

Table 5.1: System Parameters

DYSC CIRCUIT'S SIMULATION:

Fig.5.1: Simulation diagram of DySC

In the figure 5.1 there are three voltage sources connected in which only one source will be in action at any instant. In this circuit we create artificial sag by applying the voltage source which is less than the rated value of voltage.At the instant of 0.1sec by switching on the 180v source sag is created, by applying 100v at 0.4sec. a deep sag can be created which exists from 0.4s to 1.0s. The bypass switch in the circuit will identify the decrease of the voltage level and the switch will comes into off condition then DySC circuit will comes into picture. The controller used in the circuit will decide the switching frequency of the circuit. Here in this circuit operation when voltage decreases from the rated value the energy stored in inductors and capacitors will supply the missing voltage, these storage modules will charge from the source itself according to the duty ratio.In the figure 5.2 input voltage and output voltage of the figure 5.1 are given to the scope in order to verify the waveforms of the respective ones.

Fig.5.2: Measurement block

The results which are obtained from the scope are as shown in the figure 5.3, here it is clearly known that at the instants of 0.4 and 0.1sec artificially sags are created. For the interval of 0 to 0.1 sec voltage source 220V will be in the ON condition, but during the interval 0.1 to 0.4 sec 220V source will turn OFF and 180V source will comes into the ON condition. As same as in second interval during 0.4 to 0.7 sec 100V source will take action and remaining two sources will remain in the OFF condition. These artificial sags are compensated by the DySC circuit which is known by seeing the output voltage waveform.

Fig.5.3: Voltage obtained after compensation by DySC

When the voltage drops to 180v at 0.1 sec, DySC circuit can compensate the sag and maintains the output voltage at the rated value that is 220V. But when voltage drops less than 100v at 0.4sec DySC cannot compensate perfectly to the required load voltage which means that load voltage is slightly less than the rated value.

PB-AVQR CIRCUIT'S SIMULATION: In the proposed circuit when the voltage drops to 180v at 0.1 sec, circuit can compensate the sag upto the rated value. Even when voltage drops less than 100v at 0.4sec this PB-AVQR circuit can compensate the deep sags, where as DySC cannot compensate less than 100v sag. The transient response can be improved by increasing the set value for DC link voltage. Even DySC compensates the deep sags but obtained voltage is not upto the rated value and the THD is also very high.Where as in PB-AVQR the deep sags can also be compensated to rated level of the load voltage. The controller used in the circuit will plays important role in compensation of deep sags.

Fig.5.4: PB-AVQR circuit simulation model

From the figure 5.4 it is evident that, creation of voltage sag in the PB-AVQR's simulation circuit is as same as the DySC circuit which is given in figure 5.1.It is clear that there are some structural changes are being made in the circuit of PB-AVQR which will increase the compensation ability of the circuit. The power electronic devices thyristors and IGBTs are used where as in DySC diodes are used. When the normal rated value of the voltage is applied to the circuit the bypass switches will be in on state and PB-AVQR circuit will not comes into the picture. When the voltage level decreases from the nominal value bypass switch will goes into off condition and the PB-AVQR circuit will take its action. The control circuit which is used in the circuit will decide the switching frequency.After the simulation of the circuit the results will be seen in the measurements block.

Fig.5.5: Voltage obtained after compensation by PB-AVQR

In the above figure 5.5 we can easily observe that when voltage sag occurred after 0.1sec as 180v the resulting load voltage is 220v and when sag is upto 100v at 0.4 sec also the PB-AVQR circuit compensates it to rated level even it is existing for the more time. This makes us to come to conclusion that PBAVQR circuit may handle the deep sags even for long duration of time.

PB-AVQR circuit's control circuits:The various types of controllers which we can use for the controlling purpose of the switching pulses of the power electronic devices which have to work according the required voltage for the storage devices when the fault occurs are PI and Fuzzy, even we can use the advanced controllers which are based on the new technologies.The THD value is

much decreased after using fuzzy controller when compared to usage of other controllers like PI.

PI Controller Circuit:

Fig.5.6: PI controller circuit

The PI controller as shown in the figure 5.6 can be used as the controlling circuit of the PB-AVQR circuit where we will give the rms value of load voltage to it through gain and integrator. Thus obtained voltage waveform is compared with the required voltage value. Switching pulses will be genetated where it will decide the duty ratio of the each power electronic device, which will decide the storing energy value into the storage devices.

Fig.5.7: THD obtained by PI controller

Total Harmonic Distortion of the output load voltage waveform is given in figure 5.7 which is obtained by using the PI controller. The THD value thus obtained by using the PI controller is 3.67% which is obtained by simulation of the circuit. But it vary to small extent in the real time.

Fuzzy Controller:

Fig.5.8: FUZZY controller used in PB-AVQR control circuit

Here in the Fuzzy controller all the working and operation is as same as in the PI controller but in

fuzzy controller certain rules are described and it is undergone some training process which will make the decision taken by it as precise one and the controller operation is very fast compared to PI controller. The simulation diagram of the Fuzzy controller is as shown the figure 5.8.As in the figure 5.9 the load voltage obtained by the PB-AVQR circuit after using fuzzy controller is smooth and the THD value is much decreased where the value varies from 1.8 to 1.9. And also by using this controller speed of response is increased and efficiency is also increased, along with these benefits reliability is also improved.It is evident from the figure 5.10 for the fundamental frequency 50 Hz for each cycle of load voltage THD value obtained is 1.88% which is very much desired. This value can be further reduced by using advanced controllers.

Fig.5.9: Output Voltage with reduced THD

Fig.5.10: THD obtained by Fuzzy controller

By comparing the results of the both the controllers that is PI and Fuzzy we can observe that THD values obtained from Fuzzy is less than the PI .They have obtained as 3.73% for PI and 1.88% THD for fuzzy controller.

COMPARISION: In the table 2 the comparison of DySC, PB-AVQR and Fuzzified PB-AVQR in various aspects like output voltage value, speed of response, Reliability, THD, type of controller used in respective circuits is given. Again the proposed circuit is compared with those former circuits. From all these comparisons it came to be found that Fuzzified PB-AVQR circuit ranks better than other two circuits especially in maintaining less THD and improving power quality.

Table 5.2: Comparison of DySC, PB-AVQR and Fuzzified PB-AVQR

	DySC	PB-AVQR	Fuzzified PB-AVQR (Proposed work)
Output voltage value	Slightly less than value	Same as required output value	Same as required output value
Speed of response	Slow	Fast	Very fast
Reliability	Good	Good	Very good
$THD(\%)$	More than 5	3.73	1.88
Controller used	РI controller v	PI Controller CONCI HEION	Fuzzy controller

V. CONCLUSION

The proposed circuit Fuzzified transformer less boost circuit is a better solution for long duration deep voltage sags which can be compensated in very less interval of time with more efficiency and reliability. This circuit is cost effective and also having less weight as we didn't use any transformer. The circuit equations and working principle are given in theoretical analysis. Simulation results are presented in order to check the feasibility of the circuit for deep voltage sags. As DC link voltage adaptive method is used for fuzzified PB-AVQR circuit, the efficiency is also relatively high compared to other controller used circuits. The THD value of the output voltage is much reduced with the usage of FUZZY controller when compared to PI controller. From this comparison it is evident that fuzzified PB-AVQR is far most better than the PB-AVQR circuit using the PI controller.In future in order to increase the speed of operation and to increase the efficiency instead of Fuzzy controller PSO and still new technologies can be used.

VI. REFERENCES

- [1] A Transformerless Active Voltage Quality Regulator With the Parasitic Boost CircuitYong Lu, Student Member, IEEE, Guochun Xiao, Member, IEEE, Bo Lei, Student Member, IEEE,Xuanlv Wu, Student Member, IEEE, and Sihan Zhu
- [2] A. E. Aroudi, M. Orabi, L. Mart´ınez-Salamero, and T. Ninomiya, "Investigating stability and bifurcatios of a boost PFC circuit under peak current control," in Proc. IEEE Int. Symp. Circuits Syst., 2005, vol. 3,pp. 2835–2838
- [3] W. Zhang, G. Feng, Y.F.Liu, and W. Bin, "DSP implementation of predictivecontrol

strategy for power factor correction (PFC)", in Proc. 19thAnnu. IEEE Appl. Power Electron. Conf., 2004, vol. 1, pp. 67–73.

- [4] G. F. Teng, G. C. Xiao, Z. Zeng, Z. H. Ye, F. Zhuo, and Z. A. Wang, "Adigital control strategy based on repetitive and multi-loop control for anactive voltage quality regulator," in Proc. Int. Power Electron. Conf., 2010,pp. 2656–2662.
- [5] G.C. Xiao, Z.L. Hu,L. Zhang, and Z.A. Wang, "Variable Dc-bus control strategy for an active voltage quality regulator", in Proc. 24th Annu. IEEEAppl. Power Electron. Conf., 2009, pp. 1558–1563.
- [6] M. F. McGranaghan, D. R. Mueller, and M. J. Samotyj, "Voltage sags inindustrial systems", IEEE Trans. Ind. Appl., vol. 29, no. 2, pp. 397–403,Mar./Apr. 1993.
- [7] Z. Fedyczak, R. Strzelecki, and G. Benysek, "Single-phase PWM AC/ACsemiconductor transformer topologies and applications," in Proc. 33rdAnnu. IEEE Power Electron. Spec. Conf., Jun. 2002, pp. 1048–1053.
- [8] A. Bendre, D. Divan, W. Kranz, and W. Brumsickle, "Equipment failures caused by power quality disturbances," inProc. IEEE IAS Conf. Record,2004, pp. 482–489.
- [9] T. Jimichi, H. Fujita, and H. Akagi, "Design and experimentation of adynamic voltage restorer capable of significantly reducing an energy storage element", IEEE Trans. Ind. Appl., vol. 44, no. 3, pp. 817–825,May/Jun. 2008.
- [10] A. K. Sadigh, E. Babaei, S. H. Hosseini, and M. Farasat, "Dynamic voltage restorer based on stacked multicell converter," in Proc. IEEE Symp. Ind. Electron. Appl., 2009, pp. 419–424.
- [11] D. Divan, A. Bendre, W. Kranz, and R. Schneider, "Dual source dynamic sag correctors-a cost effective topology for enhancing the reliability of dual source systems," inProc. 38th IAS Annu. Meet., 2003, vol. 2, pp. 940–947.
- [12] J. Hoyo, H. Calleja, and J. Arau, "Three-Phase PWM AC/AC cuk converter for voltage sag compensation," inProc. 37th IEEE Power Electron. Spec.Conf., 2006, pp. $1 - 5$.
- [13] A. Sannino, M. G. Miller, and M. H. J. Bollen, "Overview of voltage sagmitigation," inProc. IEEE Power Eng. Soc. Winter Meet., 2000, vol. 4,pp. 2872– 2878.
- [14] W. E. Brumsickle, R. S. Schneider, G. A. Luckjiff, D. M. Divan, andM. F.

McGranaghan, "Dynamic sag correctors: Cost-effective industrial power line conditioning,"IEEE Trans. Ind. Appl., vol. 37, no. 1, pp. 212–217, Jan./Feb. 2001

- [15] D. M. Vilathgamuwa and H. M. Wijekoon, "Control and analysis of a new dynamic voltage restorer circuit topology for mitigating long duration voltage sags," inProc. 37th IAS Annu. Meet. Ind. Appl. Conf., 2002, vol. 2, pp. 1105–1112
- [16] M. H.Bollen, Understanding Power Quality Problems, Voltage Sags and Interruptions. Piscataway, NJ, USA: IEEE Press, 2002.
- [17] M. F. Alves and T. N. Ribeiro, "Voltage sag: an overview of IEC and IEEE standards and application criteria", in Proc. IEEE Transmiss. Distrib. Conf., 1999, vol. 2, pp. 585–589.
- [18] S. Subramanian and M. K.Mishra, "Interphase AC–AC topology for voltage sag supporter," IEEE Trans. Power Electron., vol. 25, no. 2, pp. 514–518, Feb. 2010.
- [19] Y. H. Chen, C. Y. Lin, J. M. Chen, and P. T. Cheng, "An inrush mitigation technique of load transformers for the series voltage sag compensator", IEEE Trans. Power Electron., vol. 25, no. 8, pp. 2211–2221, Aug. 2010.

AUTHOR's PROFILE

A.Chandrika rani was born in 1992. She completed her professional career of education in B.Tech (EEE) at kvsrcew Institute of technology in the year of 2013 and pursuing M.Tech

from Sri Krishnadevaraya engineering college, Gooty, Anantapur(AP). She is interested in Electrical Power Engineering.

Mr. N. Narasimhulu has completed his professional career of education in B.Tech (EEE) from JNTU Hyderabad. He obtained M.Tech

degree from JNTU, HYDERABAD.Now he is pursuing Ph.d from JNTU ANANTAPUR. At present working as an Associate Professor and Head of the EEE Department in Srikrishna Devaraya Engineering College, Gooty of Anantapuramu district (AP).

Dr. R.RAMACHANDRA has completed his professional career of education in B.Tech (MECHANICAL) from JNTU Hyderabad. He obtained M.Tech

degree from JNTU, Hyderabad. He obtained Phd degree from JNTU, Hyderabad At present working as Principal in Srikrishna Devaraya Engineering College, Gooty of Anantapuramu district (AP)