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Design and Implementation of Low Power Truncated Multiplier by Adopting Ant Architecture Using Fixed-Width RPR Block

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Abstract: **The suggested ANT architecture can satisfy the need for high precision, low power consumption, and area efficiency. To reduce the ability dissipation, supply current scaling is broadly used as a good low-power technique because the power consumption in CMOS circuits is proportional towards the square of supply current. While using partial product relation to input correction vector and minor input correction vector to reduce the truncation errors, the hardware complexity of error compensation circuit could be simplified. We design the fixed-width RPR with error compensation circuit via analyzing of probability and statistics. Within this paper, we advise a dependable low-power multiplier design by adopting algorithmic noise tolerant (ANT) architecture using the fixed-width multiplier to construct the lower precision replica redundancy block (RPR). Inside a 12 × 12 bit ANT multiplier, circuit area within our fixed-width RPR could be decreased and power consumption within our ANT design could be saved, in contrast to the condition-of-art ANT design.**

Keywords: **Algorithmic Noise Tolerant (ANT); Fixed-Width Multiplier; Reduced-Precision Replica (RPR); Voltage Over Scaling (VOS);**

I. INTRODUCTION

A singular algorithmic noise tolerant (ANT) technique combined VOS primary block with reduced-precision replica (RPR), which combats soft errors effectively while achieving significant economical. To reduce the ability dissipation, supply current scaling is broadly used as a good low-power technique because the power consumption in CMOS circuits is proportional towards the square of supply current. However, the RPR designs within the ANT designs are made inside a customized manner, which aren't easily adopted and repeated. The RPR designs within the ANT designs can operate in an exceedingly fast manner, however their hardware complexity is simply too complex. While using fixed-width RPR, the computation error could be remedied with lower power consumption minimizing area overhead [1]. We take utilization of probability, statistics, and partial product weight analysis to obtain the approximate compensation vector for any more precise RPR design. So as not to improve the critical path delay, we restrict the compensation circuit in RPR should not be found in the critical path. Consequently, we are able to realize the ANT design with smaller sized circuit area, lower power consumption, minimizing critical supply current.

II. METHODOLOGY

To satisfy ultralow power demand, VOS can be used in MDSP. However, underneath the VOS, when the critical path delay Tcp from the system becomes more than the sampling period Tsamp, the soft errors will occur. It results in severe degradation in signal precision. Within the ANT technique, a duplicate from the MDSP however with reduced precision operands and shorter computation delay can be used as EC block. Under VOS, there are a variety of input-dependent. The fixed-width designs are often used in DSP applications to prevent infinite development of bit width. Reducing n-bit least significant bit (LSB) output is a well-liked means to fix create a fixed-width DSP with n-bit input and n-bit output. The hardware complexity and power use of a set-width DSP is generally about 50 % from the full-length one [2]. However, truncation of LSB part leads to rounding error, which must be compensated precisely. Many literatures happen to be given to lessen the truncation error with constant correction value or with variable correction value. The circuit complexity to pay with constant remedied value could be simpler compared to variable correction value however, the variable correction approaches are often more precise. Within this paper, we further suggested the fixed-width RPR to exchange the entire-width RPR block within the ANT design, which could not just provide greater computation precision, lower power consumption, minimizing area overhead in RPR, but additionally perform with greater SNR, more area efficient, lower operating supply current, minimizing power consumption in realizing the ANT architecture. We demonstrate our fixed-width RPR-based ANT design within an ANT multiplier. Compared to the entire-width RPR design, the suggested fixed-width RPR multiplier not just performs with greater SNR but additionally with lower circuitry area minimizing power consumption. Within the ANT design, the part of RPR would be to correct the errors occurring within the creation of MDSP and

keep the SNR of whole system while lowering supply current. Within the situation of utilizing fixed-width RPR to understand ANT architecture, we not just lower circuit area and power consumption, but additionally accelerate the computation speed compared to the traditional full-length RPR. However, we have to compensate huge truncation error because of reducing many hardware elements within the LSB a part of MDSP. To judge the precision of the fixed-width RPR, we are able to exploit the main difference between your (n/2)-bit fixed-width RPR output and also the 2n-bit full-length MDSP output. The origin of errors generated within the fixed-width RPR is covered with the part products of ICV given that they possess the largest weight. By statistically analyzing the truncated distinction between MDSP and glued-width RPR with uniform input distribution, we are able to discover the relationship between f (EC) and ß. Therefore, we are able to apply multiple input error compensation vectors to help boost the error compensation precision. Before directly injecting the compensation vector ß in to the fixed-width RPR, we go further to make sure the load for that partial product terms in ICV with similar partial product summation value ß however with different locations. We are able to lower the compensation error effectively with no additional compensation error is going to be generated. To understand the fixed-width RPR, we construct one directly injecting ICV (ß) to essentially satisfy the statistic distribution and something minor compensation vector MICV (a) to amend the inadequate error compensation cases [3]. Therefore, not just the mistake compensation precision within the fixed-width RPR could be enhanced; the computation delay won't also be postponed. Because the critical supply current is covered with the critical delay duration of the RPR circuit, preserving the critical road to RPR't be postponed is essential. The primary performance indexes would be the precision of RPR blocks, the plastic section of RPR blocks, the critical computation delay of RPR blocks, the mistake possibility of RPR blocks under VOS, and also the cheapest reliable operating supply current under VOS. Through quantitative analysis of experimental data, we are able to show our suggested design can better restrain the soft noise interference caused by postponed computation delay under VOS once the circuit operates having a really low-current supply. First, we compare the suggested fixed-width multiplier along with other literature designs, correspondingly. All performance comparisons are evaluated under 12-bit ANT-based multiplier designs. The truth analysis outcomes of various fixed-width RPR multipliers or full-width RPR multiplier are proven. The fixed-width RPR designs usually perform with greater truncation errors compared to the entire-width RPR design because more computation cells are truncated [4]. However, with appreciate error compensation vector or multiple truncation error compensation vectors, the fixed-width RPR designs have the opportunity to perform with lower truncation errors. To verify the consistency from the compensation precision, we compare the output signal quality when it comes to SNR for a number of RPR designs with various truncated bits. To lowering supply current beyond critical supply current without having to sacrifice the throughput and without resulting in severe SNR degradation, the critical computation delay within the RPR block should be as quickly as possible. Therefore, a tradeoff between hardware area and RPR bit length is required. Within this paper, the enhanced bit period of fixed-RPR is chosen as six in line with the cheapest Kvos analysis results. The RPR area is yet another main factor which will modify the power saving. Hence, we compare the circuitry area occupied through the fixed-width RPR multiplier and also the full-width RPR multiplier [5].

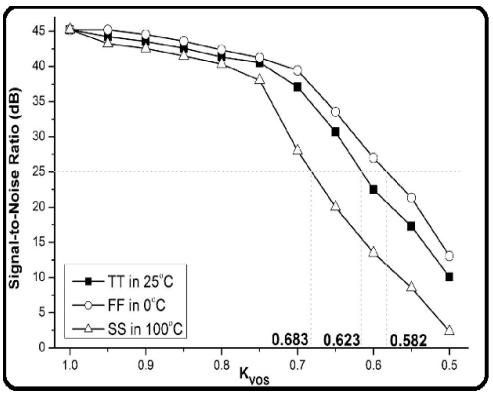

Fig.Proposed model comparisons

III. CONCLUSION

The suggested 12-bit ANT multiplier circuit is implemented in TSMC 90-nm process and it is plastic area is 4616.5 µm2. Under .6 V supply current and 200-MHz operating frequency, the ability consumption is .393 mW. Within this paper, a minimal-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. Within the presented 12-bit by 12-bit ANT multiplier, the circuitry area within our fixed-width RPR could be saved, the cheapest reliable operating supply current within our ANT design could be decreased to .623 VDD, and power consumption within our ANT design could be saved compared to the condition-of-art ANT design. The truncated RPRs are examined from word period of 5 to 10 bits using Synopsys design compiler CAD tool. Finally, we implement the suggested 12-bit fixed-width RPR-based ANT multiplier in TSMC 90-nm process.

IV. REFERENCES

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