K. Mounika* et al.
(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH
Volume No.4, Issue No.6, October – November 2016, 4472-4475.

Self Referenced Edge Detection for CMOS PWM Transceiver

K.MOUNIKA
M.Tech Student
Dept. of Electronics and Communication Engineering,
Kakatiya Institute of Technology and Science,
Warangal, Telangana, India, 506015.

P.CHIRANJEEVI
Assistant Proffesor
Dept. of Electronics and Communication Engineering
Kakatiya Institute of Technology and Science,
Warangal, Telangana, India, 506015.

***Abstract*— A Self Referenced Edge Detection technique is used to implement the CMOS PWM Transceiver circuit is presented. In this paper, A Self Referenced Edge Detection technique is implemented to analyze a CMOS PWM Transceiver circuit, by comparing the rising edge that is self-delayed by about 0.5 T and the modulated falling edge in one carrier clock cycle. An Area-efficient and high robustness (against timing fluctuations) edge detection enabling PWM communication is achieved without requiring elaborate phase-locked loops. Self-referenced edge detection circuit has the capability of timing error measurement while changing the length of self delay element, adaptive data-rate optimization and delay-line calibration are realized. The measured results with a 65-nm CMOS prototype demonstrate a 2-bit PWM communication, high data rate (4Gbps), small peak to peak jitter(4.8ns), and high reliability (BER > 10−12) with small area occupation (540 μm2) and with high RMS (1.3). For reliability improvement, error check and correction associated with intercycle edge detection is introduced and its effectiveness is verified by 2-bit PWM measurement.**

Index Terms— pulse width modulation (PWM); self-referenced; transceiver; CMOS; jitter; RMS.

I. INTRODUCTION

The development of CMOS devices are motivated for the requirement of decreased power supply voltage and to develop time-domain circuits, the pulse width modulation (PWM) scheme is a promising approach which is used in many applications like voltage regulators, Frequency converters, the PC speakers, wireline transceivers, CMOS imagers [4], Modern semiconductor switches(MOSFETS). However, conventional PWM transceiver design [1]–[3] requires large-area and power-hungry phase-locked loops (PLLs) for multiphase sampling clock generation.

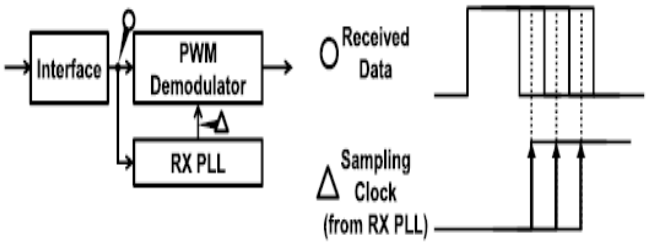

Fig. 1: Conceptual diagram of the conventional PWM receiver in 2-bit PWM.

This describes the impact of newly proposed Self-referenced Edge Detection technique on the design of an area-efficient and highly robust PWM transceiver. This technique introduces a timing comparison between the rising edge that is self-delayed by about 0.5T and the data-modulated falling edge in one carrier clock cycle in proposed PWM transceiver and also analyzing techniques of proposed PWM transceiver like Adaptive data-rate optimization and error check and correction (ECC) technique are introduced.

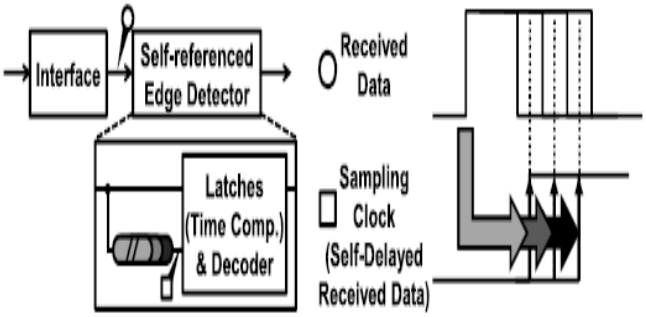

Fig. 2: Conceptual diagram of the proposed PWM receiver in 2-bit PWM.

This description introduced as follows. The proposed PWM transceiver is introduced in Section II. Section III introduces adaptive data-rate optimization. Section IV presents ECC and the measurement results

are summarized in Sections V. Discussion is described in Section VI. Section VII concludes this brief.

II. SELF REFERENCED EDGE DETECTION FOR PWM TRANSCEIVER

Figs. 1 and 2 show a conceptual diagram of the conventional and proposed receiver design for a 2-bit PWM. A conventional PWM receiver exploits a PLL for generating time-shifted sampling clocks. Our newly proposed PWM receiver using a self-referenced edge detector employs latches as timing comparators and a thermometer-binary decoder (Unary coding). The proposed self-referenced edge detection utilizes the self-delayed by 0.5 rising edge instead of the PLLs sampling clock. By comparing this self-delayed rising edge and the data-modulated falling edge in one carrier clock cycle, edge detection can be realized. The proposed structure removes the elaborate PLL; hence, high area efficiency is obtained.

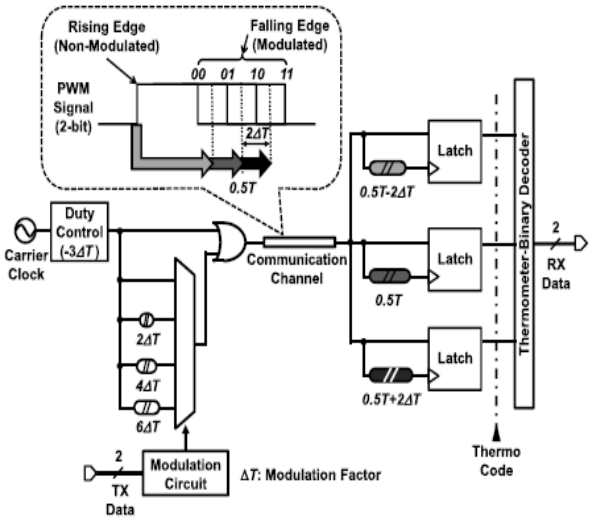

Fig. 3: Circuit implementation of the proposed PWM transceiver architecture in 2-bit PWM.

Fig. 3.3 shows the schematic diagram of the proposed transceiver architecture. The transmitter section consists of a duty controller, four delay elements with length of multiples of modulation factor T (nT), selector controlled by the PWM modulator, and OR logic. The receiver consists of three delay elements with various lengths about a half of the clock period 0.5T, three latches, and a thermometer-binary decoder. The outputs of the three latches are thermometer codes that are obtained by using the thermometer-binary decoder which converts thermometer codes to binary code.

III. ADAPTIVE DATA-RATE OPTIMIZATION

Fig. 4 shows a conceptual diagram of the adaptive data-rate optimization and delay-line calibration. The receiver has the same configuration as the reference-clock-free timing jitter measurement circuit using self-referenced clock with nT delay [6]. In [6], nT –delay clocks generates two uncorrelated edges. By comparing these two uncorrelated edges, √2-times timing jitter can be obtained.

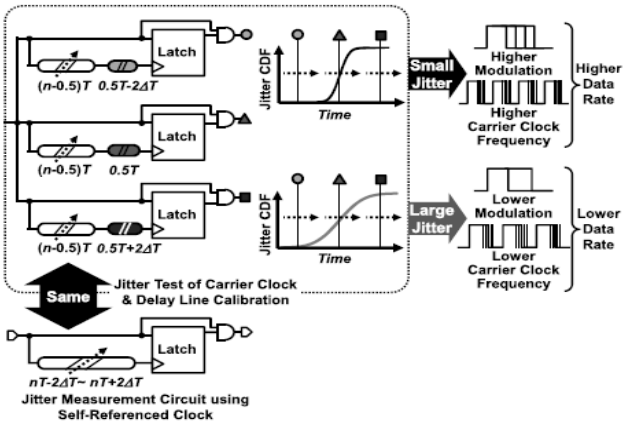

Fig.4: Conceptual diagram of the adaptive data-rate optimization and delay-line calibration associated with timing jitter measurement using self-referenced edge detection.

Thus, the timing error measurement is realized by only changing the length of the delay. By using the obtained timing error information of the carrier clock, the modulation factor T, and the carrier clock frequency can be optimized. Since the timing error of the carrier clock primarily determines the bit error rate, smaller jitter. This smaller jitter obtained by taking cumulative distribution function of jitter with respect to clock time which enables both higher modulation and a higher carrier clock frequency, which results in a higher data rate. Moreover, the delay lines for communication can be calibrated while processing the timing error measurement.

IV. ERROR CHECK AND CORRECTION

This section introduces the ECC circuit for improving the performance of the proposed PWM transceiver using self-referenced edge detection.

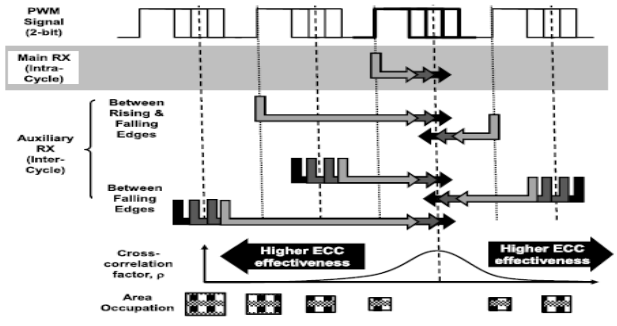

Fig. 5: Conceptual image of the proposed ECC circuit.

Fig. 5 shows the conceptual diagram of the proposed ECC technique. The time difference of the adjacent falling edges is detect by using inter cycle detection which gives auxiliary receiver, as shown in Fig. 5. Delay length design of the auxiliary receiver can be determined by the autocorrelation function of the jitter of the carrier clock [7], [8]. In typical situation, correlation decreases as the number of cycles between the preceding and succeeding edges increases.

Thus, a larger number of inter reference cycles are expected to be effective for error detection. However, to be large number of inter reference cycles causes area penalty. Therefore, we have to consider the trade-off between ECC effectiveness and area overhead in designing the ECC circuits. Fig. 6 shows the conceptual image of the ECC function in 1-bit PWM that is enabled by comparing the received data from the main receiver and that from the auxiliary receiver.

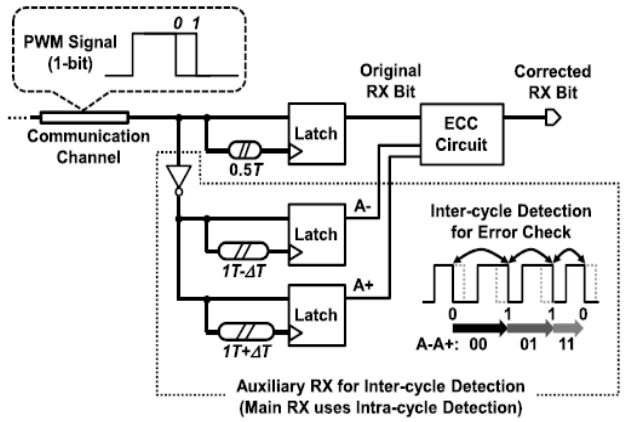

Fig. 6: Schematic diagram of the proposed receiver with ECC capability for 1-bit PWM.

Since the implemented ECC uses only 1T -delayed edges for error correction, successive errors cannot be recovered. As stated above, instead of using 1T -delay as in Fig. 6, 0.5T -delay (comparing with the latter rising edges instead of the earlier rising edges) or a longer delay is possible. Thus, the proposed technique is flexible and can be optimized under the characteristic of timing error.

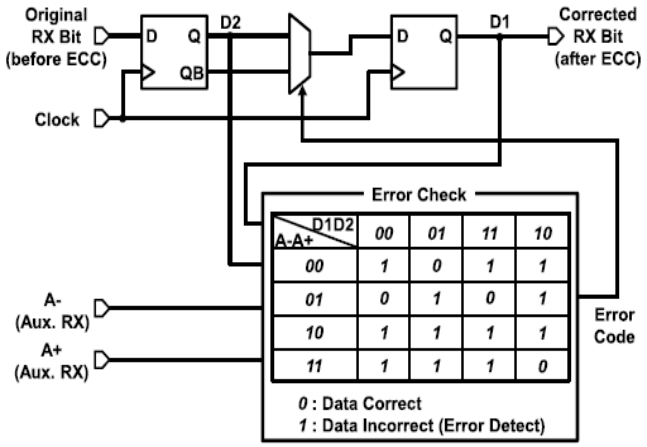

Fig. 7: Schematic diagram of the proposed ECC circuit containing latches and error detecting logic for 1-bit PWM.

Fig. 7 shows the schematic diagram of the ECC circuit for 1-bit PWM. The ECC circuit consists of D-latches and an error detector. ECC utilizes the successive received data from the main receivers, D1 and D2, and data from the auxiliary receivers, A+ and A−. An error code is generated when a discrepancy between the received data from the main and auxiliary receiver occurs, and the original RX bit is inverted and then gives corrected receiver data.

V. MEASUREMENT RESULT

Fig. 8 shows the measured waveform of the input and output signal. A carrier clock and shifted 2-bit pseudorandom bit sequence (PRBS) were applied to a CMOS PWM Transceiver with self referenced edge detection.

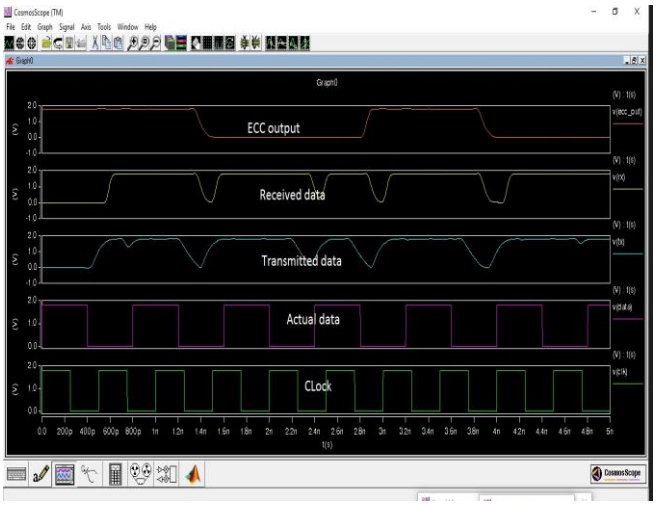

Fig. 8: The measured waveform of the input and output signal.

Table1: Measurements and Results

	This work	*Conv.(1) JSSC2001*	*Conv.(2) JSSC2007*	*Conv.() JSSC2008*
Area(μ)	*540*	*354,44*	*14,359*	*4,103,532*
Technology (CMOS-nm)	*65nm CMOS*	*0.25 μm CMOS*	*0.18 μm CMOS*	*0.18 μm CMOS*
Power Supply	*1.2 V*	*2.5V*	*1.2V*	*1.8V*
Data Rate	*4Gbps (2-bit) 2.003Gbps(1-bit)*	*400Mbps*	*270Mbps*	*1Gbps*
BER	<	*N/A*	<	<
Channel	*3.2 μ m on-chip*	*30cm IEEE1394a*	*N/A*	*30cm PCB trace*
Jitter of Clock	*0*	*13.9ps*	*26.6ps*	*5.9ps*
Feature	*Without PLL/DLL*	*With PLL*	*With DLL*	*With PLL*
RMS	*1.3*	*N/A*	*N/A*	*N/A*

Data communication was successfully verified with data rate of 4Gbps (=2 Gbps/bit × 2 bit) and also the data rate of 2Gbps (=2Gbps × 1 bit). The maximum data rate is 4 Gbps. And also the measurement result for clock jitter is zero with RMS of 1.3. High reliability with a BER < 10−12 was also verified.

VI. DISCUSSION

A. Another Topology of the Proposed CMOS PWM Transceiver Using Self-Referenced Edge Detection: This section introduces another topology of the proposed

CMOS PWM transceiver using self-reference edge detection. Instead of using both rising and falling edges, another topology utilizes only rising or falling edges. Since this topology can remove the limitation of implementation, it expands the application of the proposed technique.

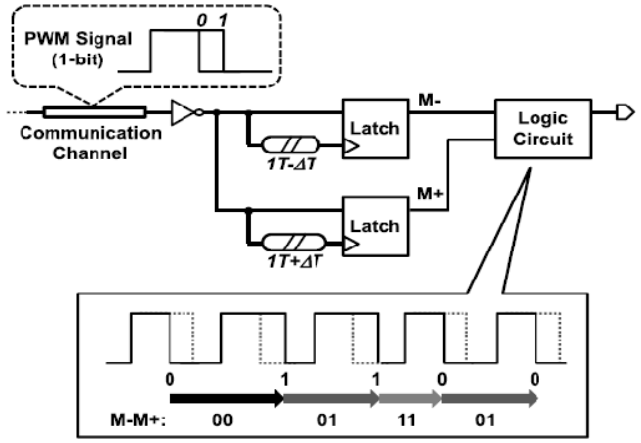

Fig9: Conceptual image of another topology of the proposed CMOS PWM transceiver using self-referenced edge detection.

Fig.9 shows the conceptual image of another topology of the proposed CMOS PWM transceiver using self-referenced edge detection. It is well known that the timing jitter can be expressed as the accumulation of the period jitter [11]. By applying this characteristic to the PWM, PWM edges can be expressed by the accumulation of the period. For instance, when the previous bit is 0 and the period, M−M+, is 00, the current data become 1, as shown in the bottom part of Fig. 8.

VII. CONCLUSION

A Self Referenced Edge Detection technique is implemented on the CMOS PWM Transceiver circuit and also analyzed by comparing the self-delayed rising edge and modulated falling edge. This edge detection enables area-efficient and high-robustness for PWM communication without exploiting PLLs. The data-rate optimization and ECC with inter stage edge detection was introduced. The results are verified in a different technique such as the measured results have demonstrated 2-bit PWM communication, high data rate (4 Gbps), zero jitter, less RMS (1.3), and high reliability (BER <) with small area occupation (540 µm2).

REFERENCES

[1] W.-H. Chen, G.-K. Dehang, J.-W. Chen, and S.-I. Liu, "A CMOS 400-Mb/s serial link for AS-memory systems using a PWM scheme," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1498–1505, Oct. 2001.

[2] W.J. Choe, B.-J. Lee, J. Kim, D.-K. Jeong, and G. Kim, "A single pair serial link for mobile displays with clock edge modulation scheme," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 2012–2020, Sep. 2007.

[3] C.-Y. Yang and Y. Lee, "A PWM and PAM signaling hybrid technology for serial-link transceivers," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 5, pp. 1058–1070, May 2008.

[4] M. Takihi, K. Niitsu, and K. Nakazato, "Charge-conserved
analog-to-time converter for a large-scale CMOS biosensor array," in *Proc. IEEE Int. Symp. Circuits and Syst.*, Jun. 2014.

[5] M.-T. Chung and C.-C. Hsieh, "A 0.5 V 4.95 μW 11.8 fps PWM CMOS imager with 82 dB dynamic range and 0.055 % fixed-pattern noise," in *Proc. IEEE ISSCC*, Feb. 2012, pp. 114–116.

[6] K. Niitsu, M. Sakurai, N. Harigai, T. J. Yamaguchi, and H. Kobayashi, "CMOS circuits to measure timing jitter using a self-referenced clock and a cascaded time difference amplifier with duty-cycle compensation," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2701–2710, Nov. 2012.

[7] J. A. McNeill, "Jitter in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 870–879, Jun. 1997.

[8] K. Niitsu *et al.*, "A clock jitter reduction circuit using gated phase blending between self-delayed clock edges," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 142–143.

[9] A. Sai, Y. Kobayashi, S. Saigusa, O. Watanabe, and T. Itakura, "A digitally stabilized type-III PLL using ring VCO with 1.01 psrms integrated jitter in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 98–100.

[10] B. Shen, G. Unruh, M. Lugthart, C.-H. Lee, M. Chambers, and C. Parrella, "An 8.5 mW, 0.07 mm2 ADPLL in 28 nm CMOS with sub-ps resolution TDC and < 230 fs RMS jitter," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2013, pp. 192–193.

[11] M. Ishida *et al.*, "A programmable on-chip pico second
jitter-measurement circuit without a reference-clock input," in *Proc. IEEE ISSCC*, Feb. 2005, pp. 512–513.

[12] D. De Caro, C. A. Romani, N. Petra, A. G. M. Strollo, and C. Parrella, "A 1.27 GHz, all-digital spread spectrum clock generator/synthesizer in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1048–1060, May 2010.

[13] K.-J. Sham, M. R. Ahmadi, S. B. G. Talbot, and R. Harjani, "FEXT crosstalk cancellation for high-speed serial link design," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2006, pp. 405–408.

