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COMPARISON OF DIFFERENT DEVICE CONCEPTS TO INCREASE THE OPERATING VOLTAGE OF A TRENCH ISOLATED SOI TECHNOLOGY TO ABOVE 900V

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Abstract. *For gate driver ICs in three phase power applications level shifters with more than 900V operating voltage are required. The extension of the voltage rating of an existing trench isolated SOI process was done with different device concepts: Serial stacking of lower voltage devices was evaluated as an alternative approach to conventional quasi-vertical and charge compensated lateral devices which need layout and material modifications. Based on sufficient 900V trench isolation the different device concepts were tested with diodes and transistors. For the usage as level shifters the focus was to achieve the required breakdown voltages with minimum area.*

Key words: *Trench isolated SOI, integrated high voltage devices, high voltage device concepts*

1. Introduction and Motivation

A large part of globally generated electricity is used for mechanical drive applications. The increasing demand for energy savings pushed also by legislative requirements [1] leads to rising usage of inverters in many applications. In contrast to single phase 230V applications, where intelligent motor drivers are available which allow an adjustment of rotational speed and power demand; this is seldom the case for three phase applications due to cost and size restrictions. For compact three phase drive applications like industrial fans and pumps not only IGBTs and diodes but also high side capable gate driver ICs with appropriate operating voltages are required. The three phase approach however offers space reduction of the inverter due to the smaller DC-link and lower system currents compared to a single phase input. Also new topologies and control algorithms

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focus on the integration of the inverter into the motor, which was already presented in automotive applications [2], [3], [4], [5].

Special needs have to be fulfilled by the ASIC-technology for usage in an inverter application. First of all the level shifter must be capable of handling voltages of up to 750V. For a stable design there should be some safety margin for transients. This leads to a maximum application voltage of about 900V. These voltages also apply for the insulation of the floating high-side circuit. There are two different types of level shifters commonly used. The transistor based shifter [6] mostly used at lower DC-link voltages has some advantages over inductive approaches because of its lower sensitivity to spurious magnetic emissions commonly found in power electronic systems. The area required for high voltage integrated devices is huge because of the isolation requirements and the peak power requirements in the moment of signal transmission and transients. The inductive shifter [7] overcomes the problems of transients and can be used for higher DC-Link voltages, but the area required for the integrated air coils is even higher than the area of integrated high voltage devices. Therefore some manufacturers stack the transformer on top of the driver or receiver die.

Another approach is a capacitive shifter utilizing two integrated capacitors in a differential manner. These capacitors are much smaller than high voltage transistors and can be fabricated in the metal interconnect system of high voltage CMOS technologies with appropriate thickness of Inter Metal Dielectrics, IMD. The capacitance needed for proper operation of the shifter is much smaller than the capacitance needed in a discrete realization which is also more critical in proper isolation, lifetime, driving power and chip area. One major issue of this shifting approach is the susceptibility to voltage transients between the high side and low side circuits i.e. induced through shifting of the active or passive power switches of the connected half bridge. During the occurrence of such transients no information can be transferred across the capacitors and the high side circuit has to ignore such transient signals to prevent false switching of the high side power switch. As the impact of such transients is increased with higher rise and fall times of the power switches this approach is especially suitable for small power or high integration applications where a low EMI signature is more preferred than very high efficiencies which is achieved with slower switching power devices.

For proper driving of the power devices there is a need for MOS transistors with voltage capabilities of 20V to 30V. Another need is the interface to logic circuits. So the ASIC needs CMOS devices with an operating voltage in the range of 3V to 5.5V for maximum compatibility with common microcontrollers and Digital Signal Processors. Furthermore for close integration of power devices, driver and control electronics the ASIC must have an upper operating temperature of about 150°C.

All the low voltage devices described above to build an integrated level shifting device are available in the XDH10 technology of X-FAB in conjunction with high voltage capable trench isolation [8]. This isolation allows the integration of high side and low side circuits for one half bridge on a single die which reduces risks of isolation failures in the complete drive system and also reduces the complete systems size.

The bi-directionality together with the small temperature coefficient of the isolation leakage current makes trench isolated Silicon On Insulator, SOI, processes a good choice to manufacture such gate driver ICs [9], [10]. In this paper we present results to extend an existing 625V (operating conditions) trench isolated SOI process to operating voltages above 900V. This operating voltage requirement is necessary for the isolation between

high side and ground logic as well as for the level shifters used for the communication between both.

Trench isolated SOI allows the serial stacking of devices. Switched emitter BJT/MOSFET cascodes with a supply for the upper BJT element and a separate drive for the lower MOSFET [11] are known as well as cascodes consisting of an upper GaN HV HEMT in series with a lower n-channel low voltage MOSFET with the HEMT gate tied to ground [12]. A two chip 1200V half bridge gate driver with cascaded 600V devices is proposed in [13]. Based on a working isolation scheme stacked medium voltage diodes and transistors were investigated and compared with conventional quasi-vertical and charge compensated lateral high voltage devices. For area efficient level shifting functionality we investigated a single chip transistor cascode concept with a common gate connection.

2. The Base Process

A trench isolated Bipolar-CMOS-DMOS, BCD, process on 55 µm thick SOI wafers containing 5, 7 and 20V logic CMOS transistors, medium and high voltage n-channel DMOS and PMOS transistors as well as bipolar and other analogue devices like resistors and capacitors [8] was the base for the 900V extension. Isolation, SOI thickness as well as doping concentrations are sufficient to achieve typical breakdown voltages above 700V.

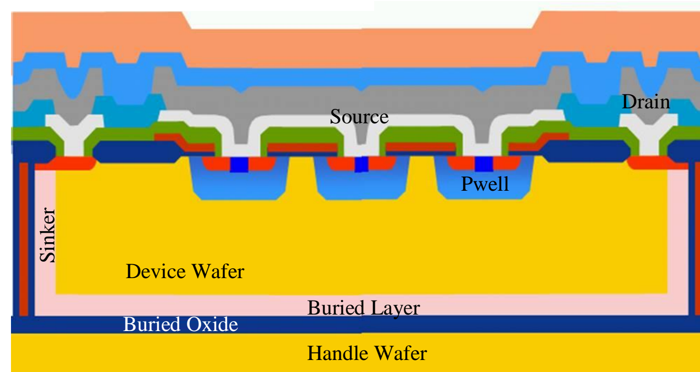

Fig. 1 Quasi vertical n-channel enhancement DMOS isolated with trench and buried oxide

Fig. **1** schematically shows the dielectric isolation topology, consisting of the vertical isolating trench, the trench adjacent doping layer (sinker), the Buried OXide, BOX, isolating the device wafer from the handle wafer and the highly doped buried layer above the BOX. Inside the isolation tub the standard high voltage device, a 750V n-channel quasi-vertical DMOS transistor is shown.

3. Experiments and Results

3.1. Isolation

A prerequisite for a 900V gate driver process and the characterization of its high voltage devices is a working isolation with sufficient overhead. Trenches, buried oxide, Inter Metal Dielectrics (IMD) as well as the surface topology need to withstand at least 1000V. The isolation capability was measured with current voltage characteristics between room temperature and 175°C. **Fig. 2** shows the investigated different trench tub layouts: single trench tubs with corner angles of 90°, single trench tubs with corner angles of 135° and double trench tubs with corner angles of 135°. The "high" potential was either applied to a pad inside the isolated tub or to the surrounding tub. Any early parasitic breakdown mechanism must be avoided, either in vertical direction from metal to metal layer - or from metal to silicon respectively - as well as in lateral direction by sufficient metal, pad and probe spacings and appropriate pad topologies.

As a criterion for isolation "breakdown" a leakage current of 0.1nA was used. Results of these measurements are shown in **Table 1**. More details of these measurements and test structures can be found in [14]. For 90° corners 600V and 800V were measured while for 135° corners 600V and 1020V were measured. For double trenches the measured voltages were above 1300V, above the maximum measurement range.

Fig. 2 Used trench tub layout geometries in top down view: 90° trench corner angle (left), 135° trench corner angle (center) and 135° double trench corner angle (right)

Table 1 Measured breakdown voltages of trench isolation test structures

Trench structure	Trench corner	Tub voltage	Breakdown voltage
single	90°	Gnd	600V
single	90°	+	800V
single	135°	Gnd	600V
single	135°	+	1020V
double	135°	Gnd	>1300V
double	135°	+	>1300V

3.2. 900V vertical diodes

The breakdown voltage of the quasi-vertical high voltage devices, as shown in Fig. **1**, is mainly defined by the SOI material which acts as drift region. Extending the operating voltage of such devices requires a modification of the thickness and doping of the SOI device wafer as well as a re-design of the field plate based edge termination region. Simple circular diodes were used for the first layout and SOI material related evaluation.

With an internal pad to contact the central electrode ("Source" in Fig. **1**, would be the anode of a similar diode) blocking voltages of about 1150V were measured, Fig 3. But for integrated high voltage devices it would be very convenient to contact the inner electrode by a metal wiring instead of a pad-bond wire connection. This requires a

crossing of the inner electrode metal wiring over the outer electrodes. Fig 3 also shows the blocking behavior of such a diode. The same diode layout but with a crossing wiring only has 750V breakdown voltage.

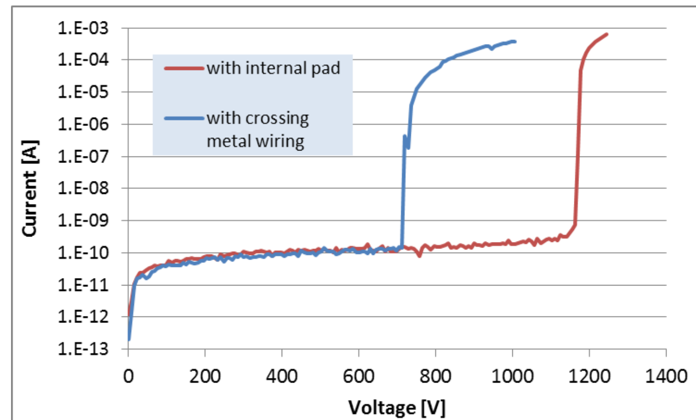

Fig 3 Breakdown voltage of quasi-vertical diodes with internal pad and with crossing metal wiring connection to the inner electrode 900V lateral diodes

3.3. 900V lateral diodes

For lateral diodes using a charge compensation mechanism different layouts were designed using an additional deep pwell region and an additional shallow ndrift doping. The circular designs were based on 2D simulation by using either the anode or the cathode region as a symmetry axis, **Fig. 4**, to create a 3D circular device. With the anode in the center breakdown voltages of 1000…1100V were measured while diodes with a similar cross-section but with the cathode in the center only reached about 100V, see **Fig. 5**.

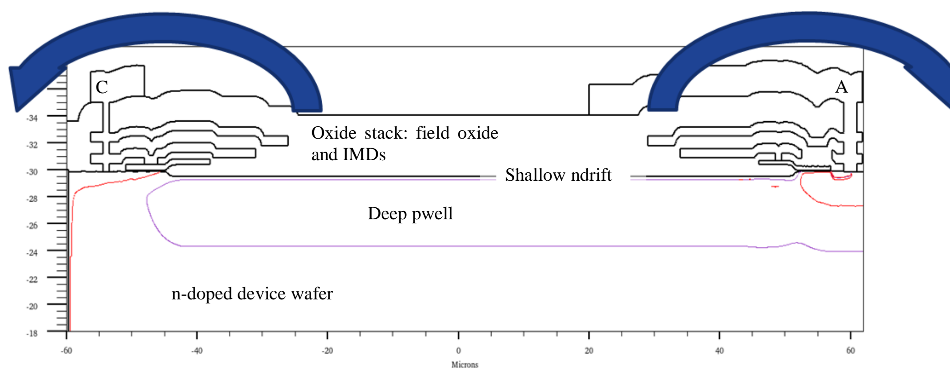

Fig. 4 Simulated 2D lateral diode structure, “A”: anode field plate metal stack, “C”: cathode field plate metal stack, for 3D layout a rotation either around the anode (right side) or the cathode region (left side) was done

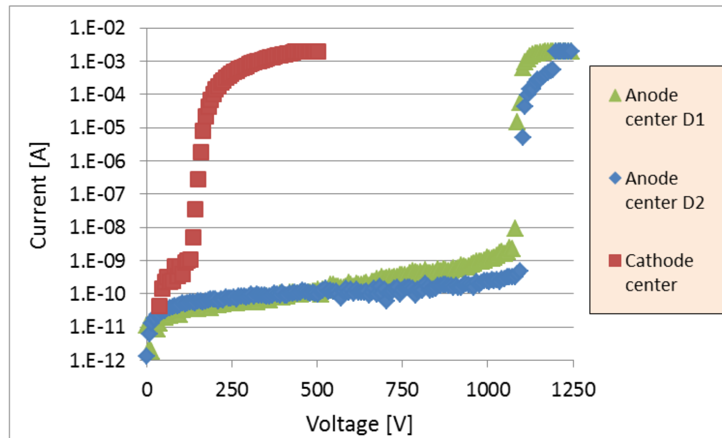

Fig. 5 Measured blocking characteristics of lateral diodes, “anode center” i.e. rotation around anode, “cathode center” i.e. rotation around cathode

For these diodes the deep pwell doping as well as the ndrift region (purple region in Fig. **4** and area above respectively) was varied by different implantation doses in the wafer process. Fig. **6** shows the achieved breakdown voltages versus the two doping concentrations for two different layouts. The simulated implantation results were used as 100% starting values. Maximum breakdown voltages above 1000V were measured at simulated deep pwell doping but at lower ndrift doping. Depending on layout, the breakdown voltages were lowered to 311V and 620V respectively with the used implantation dose variants.

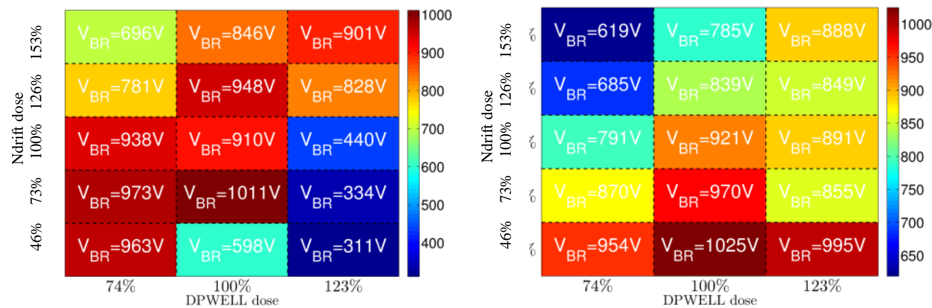

Fig. 6 Measured blocking voltage maps for different ndrift and deep pwell doping conditions, layout “A” left, layout “B” right, 6 sites per wafer measured

3.4 Stacked diodes

With a working dielectric isolation the SOI material allows an alternative approach: the serial stacking of isolated medium voltage diodes. As shown in the inset of Fig. **7** several isolated diodes in series were tested. Either two identical 600V diodes or up to four identical 300V diodes in series were stacked. Also variants were tested with and without the center of the serial diode stack being connected to the Handle Wafer, HW, of the SOI substrate by a Handle Wafer CoNTact, HWCNT.

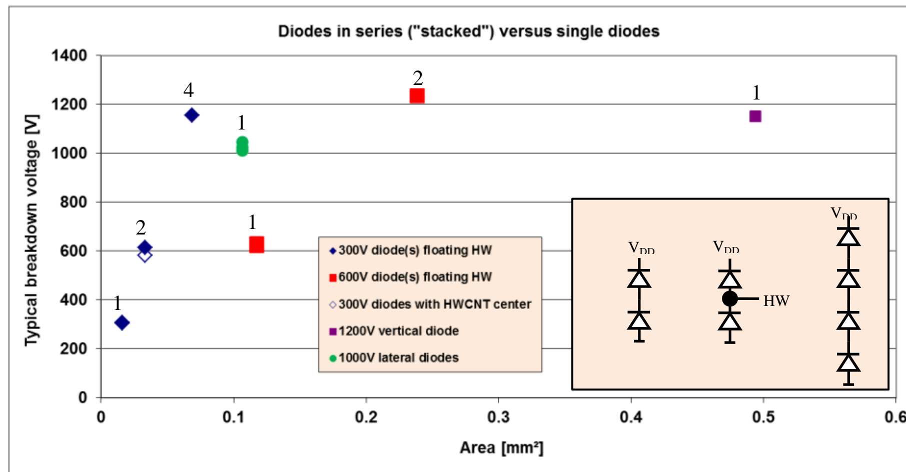

Fig. 7 Breakdown voltages versus device area for different diode stacks compared to conventional vertical and lateral diodes, numbers above symbols indicate numbers of stacked diodes

The measured breakdown voltages of these diode stacks as well as the best conventional vertical and lateral diodes versus required device layout area are shown in Fig. **7**. Totally isolated diode stacks i.e. with floating inner nodes between the stacked diodes were measured with breakdown voltages of about 1200V either with 4 individual 300V diodes in series but also the stacking of two 600V diodes leads to an overall breakdown of 1200V. Connecting the handle wafer "HW" electrically to a central potential also gives 600V for two stacked 300V diodes. Forward voltages were measured with 0.76V, 1.52V and 3.05V for the single diode, the 2 diode and 4 diode stacks respectively.

3.5. Stacked transistors

A similar stacking approach was evaluated with two transistors in series, a bottom transistor T1 with its Source connected to ground and a top transistor T2 connected with its Drain to Vdd, see **Fig. 8**. Main problem of this transistor stacking is the high Gate to Source voltage of the top transistor T2 during reverse blocking state which is equal to the negative Drain to Source voltage of T1. Therefore the total breakdown voltage target was set to >1000V and T1 should only have a medium breakdown voltage.

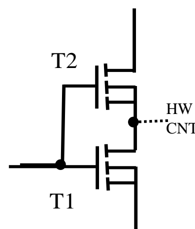

Fig. 8 Transistor stacking scheme

For the medium voltage bottom transistor T1 of the stack a 400V, 0.013mm² DMOS was available, but for the top transistor T2 it was necessary to develop a new device for 400V Gate voltage. The polysilicon gate electrodes of 0.2mm² large DMOS transistors were modified by changing from a “normal” <100nm gate oxide to a much thicker gate oxide of > 600nm with metal 1 or even about 1000nm gate oxide for a metal 2 gate electrode. These metal gate DMOS transistors, as well as the related transistor stacks, have threshold voltages of about 2.5 V for Metal 1 gates and about 12V for metal 2 gate transistors, see transfer characteristics in **Fig. 9**.

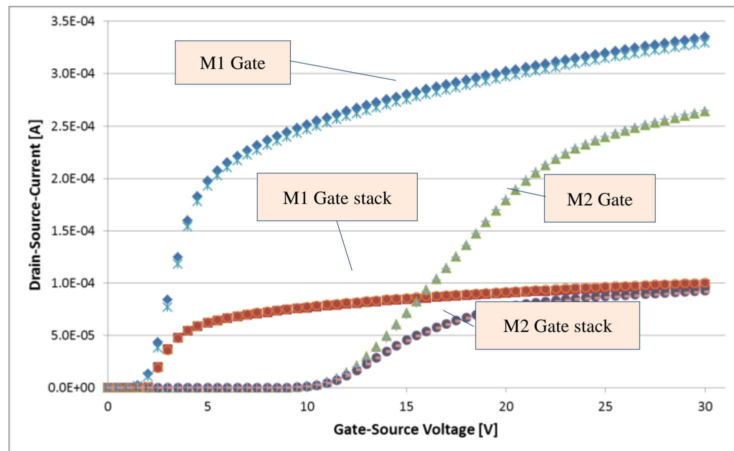

Fig. 9 Transfer characteristics of single metal gate transistors and transistor stacks

Fig. **10** shows the blocking behavior of the metal gate transistors with leakage currents below 100pA for both transistor types and breakdown voltages of 770V for the metal 1 gate devices but only about 720V and a round breakdown curve for the metal 2 gate device.

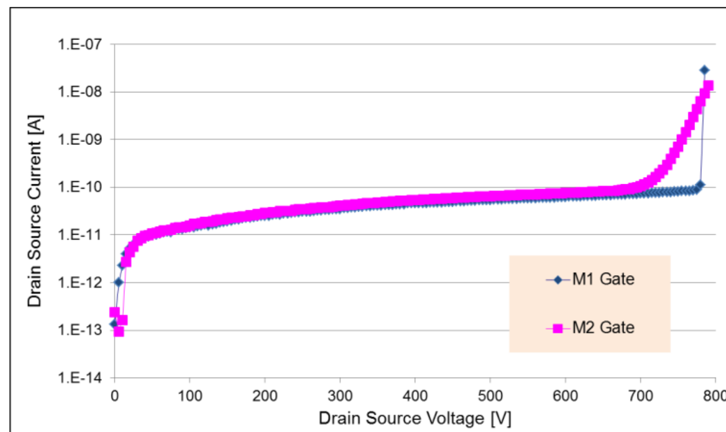

Fig. 10 Blocking characteristics of 700V metal gate transistors

Measurements have shown working transistor stacks with leakage currents of about 100pA and breakdown voltages of 1050V for the stacks using the metal 2 top transistor and 1100V for the metal 1 gate top transistors, see

Fig. **11**. The total area of the stacked DMOS transistors (T1+T2) is 0.215mm². It can also be observed in

Fig. **11** that both types of transistor stacks do not show an influence of the usage of a handle wafer contact i.e. no effect of an approximately 400V handle wafer potential could be seen. Also all stacks show a sharp breakdown behavior.

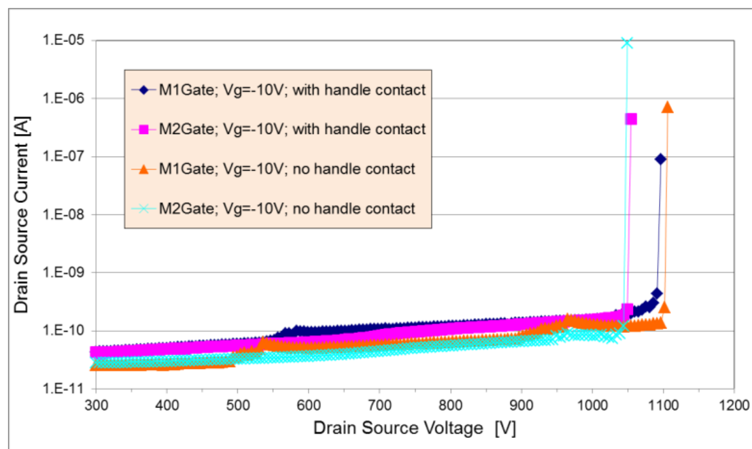

Fig. 11 Blocking characteristics of stacked transistors, inset with stacking scheme

Output characteristics of the transistor stacks are shown in Fig. **12**. Normal output behavior up to Drain voltages of 200V was measured with Gate voltages ranging from -10V up to +15V.

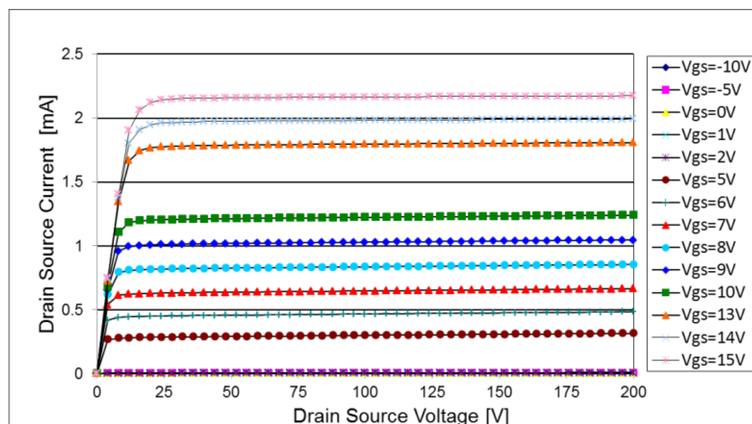

Fig. 12 Output characteristics of stacked transistors (M1-gate, no handle wafer contact)

4. DISCUSSION

The observed difference of the trench isolation capability with regards to voltage polarity and corner geometry has been observed already for lower voltages [15], [16]. For 900V applications single trench isolation might be sufficient with 135° corner angles and correct polarity. Double trench isolation structures give enough margins to measure (and operate) above 1000V. The double trench isolation capability of up to 1300V is the basic requirement for further device related high voltage measurements without any parasitic isolation failures.

With the working isolation conventional quasi-vertical diodes can be designed using adequate material parameters and layouts. But increasing the SOI thickness means to increase also the trench depth i.e. longer etch times and higher trench aspect ratios are necessary with linked technological problems. Furthermore also the transistor layout, especially the edge termination region which lowers the curvature of the electric field lines of the blocking pn-junction between anode and cathode close to the surface region, needs to be re-designed. The measured breakdown voltages of vertical diodes up to 1200V clearly show the functionality of the modified SOI wafer material and the edge termination design. These breakdown voltages have been measured with an internal pad to the anode center of the circular diode. Connecting the anode in the center of the diode by a Metal 3 wire means that this wire has to cross over the circular cathode region at the diode edge. A certain part of the Metal 3 cathode field plate (on cathode potential) has to be removed in the layout and an anode wiring in Metal 3 (on anode potential) crossing the cathode region has to be inserted instead of it. This layout modification leads to a disturbance of the electrical field distribution under the edge termination field plates and results in a reduction of breakdown voltage by 400V.

As a second type of devices lateral diodes with breakdown voltages above 1000V were simulated, designed, processed and measured. With a correct rotational axis the 2D simulation can be transferred into 3D diode structures. Since we were not able to perform 3D simulations on these large geometries we can only assume on the reason for the drastic breakdown voltage reduction when rotating around the cathode region. In that case the electric field in the drift region below the cathode is bended in a convex shape and therefore a large field crowding occurs. Much larger radii would be necessary to compensate this effect and to avoid the early breakdown.

Highest breakdown voltages have been measured at the simulated deep pwell and close to the simulated ndrift doping conditions. Compared to the vertical 1200V vertical diodes the 1000V lateral diodes have a much smaller area requirement. But this area improvement has to be paid by two additional process layers for the deep pwell and ndrift regions and, even more critical, the doping sensitivity of the breakdown voltage. Up to 15V per one percent ndrift doping change and up to 30V per one percent deep pwell doping variation was observed. Especially the shallow ndrift doping is expected to be very sensitive to e.g. variation of implant oxide thickness etc. Either a very robust and stable wafer processing or larger safety margin in the breakdown voltage specification would be necessary for the lateral approach.

As a third approach serial stacked diodes have been evaluated. With this stacking approach also diode breakdown voltages of about 1200V can be achieved, e.g. by stacking two 600V diodes or by stacking four 300V diodes in series. A mathematically correct addition of breakdown voltages was achieved. One big advantage of stacked medium voltage diodes is the reduced area consumption: Only 50% of the area of a single 1200V vertical diode is necessary for a diode stack with two 600V diodes and only less than 20% for a stack with four 300V diodes. Compared to 1000V lateral diodes the stacked

diode approach is still significantly smaller. Another advantage of the stacking approach is the reduced effect of crossing wires. While for "real" 1200V devices a severe 400V reduction due to this crossing was observed this effect is much smaller for lower breakdown devices used in the stacking approach. But the diode stacking also has a drawback: not only the breakdown voltages add up, also the forward voltages do add up in a mathematically correct manner. For diodes operating in forward mode this might be an issue.

While the diode stacks consist of similar diodes (similar in terms of layout and electrical parameters) per stack the transistor stacks used unsymmetrical devices: To reduce the gate voltage requirements of the top transistors a small sized, medium voltage bottom transistor was combined with a larger high voltage top transistor. In blocking mode also an almost mathematical correct addition of the breakdown voltages of the two transistors was observed. The necessary area of 0.215mm² for the stack is less than half of the expected 0.5mm² a single vertical DMOS with a similar breakdown voltage would require.

The differences of the metal gate transistors in breakdown voltage are repeated in the stack: 1100V breakdown was only achieved with a Metal 1 Gate transistor as top T2 whereas the Metal 2 Gate stacks only achieved 1050V. With the change from a polysilicon Gate electrode to a Metal 1 and Metal 2 Gate electrode respectively the polysilicon layout elements in the DMOS design - especially the gate and source field plates - were replaced by design elements in Metal 1 and Metal 2 respectively. With this change in the design the oxide thickness between these field plates and the silicon is getting thicker. This change in the field plate design leads to a change of the electric field distribution. The rounded breakdown characteristic of Metal 2 Gate transistors is also indicating a sort of reach through and not a pure Avalanche breakdown mechanism for the Metal 2 Gate device. This would explain the lowered breakdown voltage of Metal 2 Gate transistors. In the Metal 2 Gate transistor stacks this pre-breakdown leakage current is suppressed by the bottom transistor in series still operating in blocking mode and thus limiting the current flow. Only when both transistors are in breakdown mode the current can raise and an Avalanche like current increase can be observed in the characteristics.

Under forward conditions of course the on-resistances of the two transistors in series also add up. Increasing the transistor areas would decrease the total on-resistance at the costs of area saving of the stacking approach. For driver applications this trade-off might be an issue but for level shifting devices the on-resistance is only of minor importance.

5. Summary and Outlook

Different high voltage device concepts - quasi-vertical, lateral charge compensated and serial stacking - have been evaluated and compared. With all three device topologies the required parameters for three phase gate driver ICs transistor based level shifters were achieved. The advantages of the quasi-vertical approach are the higher robustness against process tolerances and a lower mask count while the lateral device concept requires smaller area consumption.

The basic functionality of diode and transistor cascode approaches (stacking of existing high voltage devices) to achieve breakdown voltages far above those of the single devices was proven. Compared to 900V single devices the cascode approach combines several advantages: highest area efficiency, smallest development effort, low mask count and a high robustness against process tolerances. The addition of diode forward voltage and transistor on-resistance are likely critical for driver applications or diode forwards

operation. But for the required level shifting functionality the isolation and transistor breakdown voltages as well as transistor dc characteristics are very interesting.

Switching characteristics and reliability investigations are items of further work. Especially unsymmetrical switching i.e. one transistor already slightly "on" while the second one still in off-state, is a concern. A locally reduced breakdown voltage e.g. below the crossing wires, will lead to a locally concentrated avalanche mechanism. Therefore further edge termination layout improvement to avoid the breakdown voltage reduction due to crossing wires is topic of further work.

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