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CONSIDERATION OF CONDUCTION MECHANISMS IN HIGH-K DIELECTRIC STACKS AS A TOOL TO STUDY ELECTRICALLY ACTIVE DEFECTS

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Abstract. *In this paper conduction mechanisms which could govern the electron transport through high-k dielectrics are summarized. The influence of various factors – the type of high-k dielectric and its thickness; the doping with a certain element; the type of metal electrode as well as the measurement conditions (bias, polarity and temperature), on the leakage currents and dominant conduction mechanisms have been considered. Practical hints how to consider different conduction mechanisms and to differentiate between them are given. The paper presents an approach to assess important trap parameters from investigation of dominant conduction mechanisms.*

Key words: *high-k dielectrics; conduction mechanisms; electrically active defects*

1. INTRODUCTION

Since the invention of metal oxide semiconductor field effect transistor (MOSFET) transistor in 1947 at Bell Laboratories and the first integrated circuit (IC) built independently at Texas Instruments 11 years later astonishing progress has been made in Si technology, achieved through continual scaling of semiconductor devices. The phenomenal scaling trends are popularly known as Moore's law which predicts that the number of components per chip increases exponentially, doubling over 2-3 year period. The key factor enabling the unprecedented scaling trends was the material properties (and the resultant electrical properties) of SiO_2 and its interface with Si. For quite a long time the main electronic device - MOS transistor consisted of Si substrate, SiO_2 as gate dielectric and poly-Si gate electrode. SiO_2 formed the perfect gate dielectric material successfully scaling from thickness of about 100 nm 40 years ago to a mere 1.2 nm at 90 nm node. This represents a layer only four atoms thick. Therefore, the ultimate scaling of device dimensions has pushed the thickness of SiO_2 to its physical limits where unacceptably high direct tunneling currents were flowing

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through devices. This resulted in increased power dissipation, accelerated oxide degradation and inferior reliability. Indeed, the leakage current flowing through the transistors, arising from the direct tunnelling of charge carriers could exceed 100 A/cm^2, which lies well above the specifications given by the International Technology Roadmap for Semiconductors (ITRS), especially for low operating power and low standby power technologies (Fig. 1). In fact, in this thickness range the SiO_2 is not an insulator any more. The only feasible solution of this problem was the replacement of SiO_2 with alternative dielectrics that have higher permittivity (high-*k* dielectrics) so that the required capacitance can be obtained with physically thicker layers. The integration of high-k dielectric into Si nano-technology posed a lot of serious problems such as: dielectric and interface charges, reduced channel mobility, charge trapping and degradation of parameters over operating time of the device. All these issues are defined by the electronic structure and bonding in high-k dielectrics which are distinctly different from those of SiO_2. SiO_2 has polar covalent bonds with a low coordination. Unlike SiO_2, high-k oxides have higher atomic coordination numbers and greater ionic nature in their bonding due to large difference in electronegativity of the metal and O atoms. As a result, high-k dielectrics have much larger density of electrically active defects compared to silicon dioxide. Electrically active defects are defined as atomic configurations which give rise to electronic states in the oxide band gap which can trap carriers. These defects influence very strongly the trapping behavior as well as the transport mechanisms, hence the leakage currents flowing through them. However, one of the key requirements for MOS

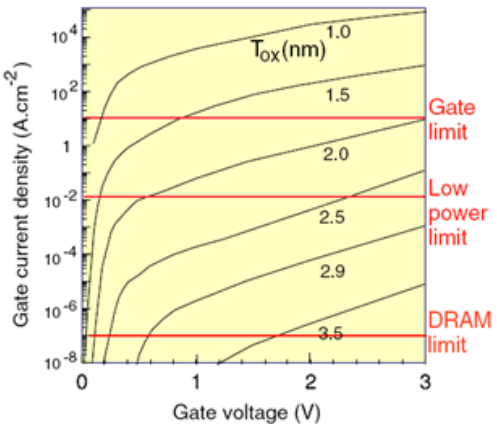

Fig. 1 Leakage current vs. voltage for various SiO_2 thicknesses [1].

devices, especially DRAM capacitor (and any kind of memory device which relies on charge storage) is to maintain low leakage current density of the dielectric. High leakage will cause the capacitor to lose its charge representing the stored binary information before the refreshing pulse. It is well known that also the performance of MOSFETs strongly depends on the breakdown properties and the current transport behavior of the gate dielectric film. Low leakage current is a stringent requirement to provide low standby-power consumption for several types of devices (so-called low power applications (e.g. mobile phones, cameras, etc.)) (Fig. 1). For high performance applications (e.g. CPUs)

high current density can be acceptable (see gate limit in Fig. 1) but current flow through the dielectric causes increased power dissipation and heating, which on its turn limits the reliability of devices. Therefore, investigation of leakage currents and conduction mechanisms of high-k dielectric films have attracted a lot of attention and a huge research effort has been dedicated to address this issue for all kinds of micro- and nano-electronic devices. Next, various conduction mechanisms in dielectric layers are presented shortly and after that their operation in different dielectric stacks is demonstrated. Some practical hints how to consider different conduction mechanisms and to differentiate between them are also given. Useful information on the trap parameters as well as structural alterations in the layers obtained by these considerations is also presented.

2. CONDUCTION MECHANISMS IN DIELECTRICS

The perfect insulator is free of traps with a negligible free carrier concentration in thermal equilibrium. Therefore, the ideal MOS structure is an insulating device where no dc current is flowing. In practice, this is not true, especially for thin dielectric layers and high electric fields, which is the case in up-to-date MOS devices. The macroscopic leakage current behaviour in MOS (MIM) capacitor structure is governed most strongly by the properties of metal/dielectric contact and the defect status of the dielectric film, hence two kinds of conduction mechanisms are considered: electrode-limited and bulk-limited conduction mechanisms. The electrode-limited mechanisms depend strongly on electrode material and metal/dielectric barrier height. They include injection of the carrier over the Schottky barrier at the metal/dielectric interface by thermionic emission (Schottky emission) and tunnelling through the thin barrier (direct and Fowler-Nordheim (FN) tunneling). The bulk-limited mechanisms are governed by the material properties of dielectric and especially the existence of traps and ionized centers in the bandgap of dielectric. Generally speaking, the bulk-limited conduction mechanisms are trap-assisted mechanisms, among which the most commonly considered are: Poole-Frenkel (PF) mechanism, trap-assisted tunnelling and space-charge limited current.

2.1. Electrode-limited conduction mechanisms

Schottky emission

The Schottky effect is a thermionic emission of electrons over the potential barrier ϕ_b at the metal-insulator interface which is enhanced in the presence of electric field. The current density governed by Schottky emission is given by Richardson-Dushman equation.

$$J = C_{RD} T^2 \exp\left(-\frac{\phi_b - \sqrt{q^3 E / 4\pi\varepsilon_0 k_r}}{kT}\right) \tag{1}$$

Here, J is the current density, T is the temperature, E is the electric field, ϕ_b is the Schottky barrier height, k_r is the dynamic dielectric constant and constants ε_0, q, k, h and C_{RD} are the permittivity of the free space, electron charge, Boltzmann constant, Planck constant and Richardson-Dushman constant (C_{RD} =120 $Acm^{-2}K^{-2}$ for the free electron approximation), respectively. The factor $\sqrt{q^3 E / 4\pi\varepsilon_0 k_r}$ represents the reduction of the

surface barrier ϕ_b by the electric field. If Schottky emission is the dominating mechanism, the plot of $ln(J/T^2)$ vs. $E^{1/2}$, called Schottky plot, should give a straight line. From y-intercept the barrier height ϕ_b could be extracted. There is a requirement for ε_r, extracted from the slope of the Schottky plot, to be self-consistent. This means that ε_r value is between optical (high frequency) and static dielectric constant (measured from capacitance methods) for an examined dielectric. Usually the ε_r value is very close to the optical dielectric constant, which is equal to the square of the refractive index n ($k_r = n^2$). Schottky emission is a strongly temperature dependent process. For films where the electron mean free path is lower than the film thickness the standard equation is replaced by a modified one [2]:

$$J = \alpha T^{3/2} E \mu \left(\frac{m^*}{m_0}\right) \exp\left[\frac{-q(\phi_b) - \sqrt{qE/4\pi\varepsilon_0 k_r}}{kT}\right] \tag{2}$$

where $\alpha = 3\times10^{-4}$ As/cm^3 K$^{3/2}$, μ is the electronic mobility in the insulator, m^* is the effective electron mass in dielectric and m_0 is the free electron mass.

Tunneling mechanisms

Tunneling can be divided in two cases – direct tunneling (i.e. tunneling through trapezoidal barrier) and Fowler-Nordheim tunneling (i.e. tunneling through triangular barrier). In the case of thicker films, the tunnelling becomes dominant at voltages where the barrier is approximately triangular and the electrons tunnel from the electrode to conduction band of dielectric. This process is described by Fowler-Nordheim equation:

$$J = AE^2 \exp(-\frac{B}{E}) \tag{3}$$

$$B = \frac{8\pi}{3h}(2qm^*)^{1/2}\phi_b^{3/2} = 6.83\times10^7\left(\frac{m^*}{m_0}\right)\phi_b^{3/2}[\text{V/cm}] \tag{3a}$$

$$A = \frac{q^3 m_0}{16\pi^2\hbar m^*\phi_b} = 1.54\times10^{-6}\left(\frac{m_0}{m^*}\right)\frac{1}{\phi_b}[\text{A/V}^2] \tag{3b}$$

Fowler-Nordheim tunnelling is generally considered to be temperature independent or very little temperature dependent mechanism, taking place at higher electric fields. If the dominant current transport mechanism is FN tunnelling, then the graph of $ln(J/E^2)$ versus $1/E$ will be a straight line and from its slope the barrier height could be extracted.
Direct tunneling (DT) current is expressed by [3]:

$$J = \frac{AE^2}{(\phi_b^{1/2} - (\phi_b - qV)^{1/2})^2}\exp\left(-\frac{B(\phi_b^{3/2} - (\phi_b - qV)^{3/2})}{E}\right) \tag{4}$$

Direct tunneling essentially operates in the low field (applied voltage) region $V<\phi_b/q$. For higher V conduction is via FN mechanism as the band bending under these applied voltages transforms the trapezoidal barrier into triangular one. DT is observed only for layers with d < 4-5 nm.

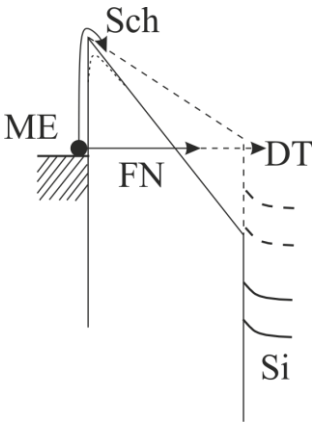

Fig. 2 Electrode limited conduction mechanisms: thermionic Schottkey emission, Fowler- Nordheim tunneling as well as direct tunneling (at low applied voltage – dashed line). Dotted line shows Schottkey barrier lowering.

2.2. Bulk-limited conduction mechanisms

Poole – Frenkel (PF) emission, trap-assisted tunneling mechanisms and hopping conduction

High-k dielectrics are trap-rich materials and conduction mechanisms, which govern the leakage current through them, are usually trap related. The trap states provide an alternative path for the charge carrier to pass from one electrode to the other. Depending on how this process is performed different kinds of trap-related mechanisms could be distinguished. The first step is tunneling of the charge carrier to the empty state and from there it can tunnel to the next trap of the same energy (hopping or multi-step tunneling). If the carrier energy is changed, then the process is inelastic tunneling. In this case the carrier looses energy and occupies a trap with different energy. Hopping and inelastic tunneling take place when the traps are distributed in a wide band of energies.
The current in hopping conduction is:

$$J = qan_c\nu \exp\left(\frac{qaE - \phi_t}{kT}\right) \tag{5}$$

where n_c is the density of the electrons in the conduction band, ν is the frequency of thermal vibration of electrons at trap sites, a is the mean hopping distance, (i.e., the mean spacing between trap sites) and ϕ_t the traps energy level measured from the bottom of the conduction band. Eq. 5 describes the tunneling of electron from a trap to adjacent one. However, if the density of the traps is not high enough so the mean hopping distance is large and the tunneling probability between two neighbor sites will be quite low. The hopping current then will result from the hopping of thermally excited electrons from one isolated site to another [4]:

$$J \propto E \exp\left(\frac{-\phi_t}{kT}\right) \tag{6}$$

So, in this case J obeys the Ohmic law with a temperature dependence defined by ϕ_t.

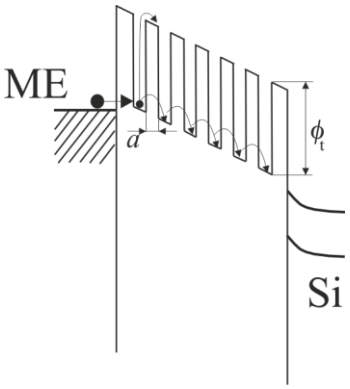

Fig. 3 Schematic representation of hopping conduction

Another possibility is to tunnel from a trap to conduction band of the other electrode, i.e. similar to direct tunneling the electron does not enter the conduction band of dielectric (Fig. 4). This process is usually referred to as a trap-assisted tunneling (TAT) and obeys the equation [5]:

$$J = q\int_0^d \frac{N_t(x)}{\tau_{in}(x)+\tau_{out}(x)}dx \tag{7}$$

where $N_t(x)$ is the trap density distribution, $\tau_{in}(x)$ and $\tau_{out}(x)$ tunneling time constants from the electrode to the trap and from the trap to the second electrode (these processes must happen sequentially) and d is the thickness of the layer, respectively. Depending of the chosen model for τ_{in} and τ_{out} calculation different expressions for J can be obtained, and some models involve numerical calculation. (τ_{in} in and τ_{out} are calculated directly from the Wentzel–Kramers–Brillouin approximation). The above equation can be written as [6]:

$$J = q\int \frac{C_t N_t P_1 P_2}{P_1+P_2}dx \tag{8}$$

Where P_1 and P_2 are the tunneling probabilities for electron tunneling into the traps and subsequently to the second electrode and C_t is a function of ϕ_t. The integration limits depend on the ϕ_b and ϕ_t, and it is from 0 to d if $\phi_t > \phi_b$ and X_t-d if $\phi_b > \phi_t$ ($X_t = (\phi_b-\phi_t-E_e)/E$, E_e is the total energy of the electron in the gate [7].

Using WKB approximation, assuming that $\phi_t + Ex >> E_e$, the following expression for J can be obtained [7]:

$$J = -\frac{2qC_tN_t}{3A\sqrt{\phi_t}}R_1\left(\tan^{-1}\left(\frac{R_2}{R_1}\right)-\tan^{-1}\left(\frac{\exp(-C_3+3\phi_t^{3/2}/2E)}{R_1}\right)\right) \tag{9}$$

with:

$$R_1=\exp(-C_3/2);\ R_2=\exp(C_3);\ C_3=\frac{3}{2}Ad\sqrt{\phi_t}\ ;\ A=\frac{4\sqrt{2qm_{ox}}}{3\hbar} \tag{9a}$$

or in more simplified equation [8]:

$$J=\alpha\frac{qN_t}{\tau}\exp\left(-\frac{4\sqrt{m_{ox}}}{3q\hbar E}\left(\phi_t^{3/2}-(\phi_t-qE(d-X_t))^{3/2}\right)\right) \tag{10}$$

where X_t is the most favorable position of trap in the dielectric, τ is the relaxation time of the trap.

M. Houssa et al. [9] have shown that in case of Si substrate injection through SiO_2/high-*k* stack, TAT current at low voltages can be approximated by:

$$J\propto N_t\exp\left(\frac{qV_{SiO2}-\phi_1+\phi_2+\phi_t}{kT}\right) \tag{11}$$

where V_{SiO2} is the voltage drop across SiO_2 layer, ϕ_1 (usually taken as 3.2 eV) is the barrier height at Si/SiO_2 interface and ϕ_2 is the barrier height at SiO_2/high-*k* interface. Since in most cases MIS structures with high-*k* layers actually are double layered (the high-*k* film and interfacial SiO_2 layer with thickness of 1÷2 nm generally), the TAT for the low voltage region will be proportional to exp(q*V*/k*T*).

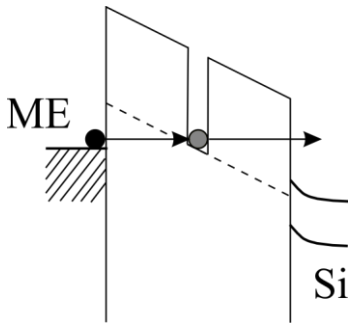

Fig. 4 Trap-assisted tunneling mechanism

When the applied field is high enough the electron enters the conduction band of dielectric through a triangular barrier (field-assisted tunneling, FAT) (Fig. 5). In this case by using (8) for the current in the two step tunneling process it can be obtained:

$$J=\frac{2C_tN_tq\phi_t}{3E}\exp\left(\frac{4\sqrt{2qm_{ox}}}{3\hbar E}\phi_t^{3/2}\right) \tag{12}$$

The last equation suggests that the process is quite similar to Fowler-Nordheim tunneling, but in this case the barrier height ϕ_b at the electrode/dielectric interface is replaced by the energy depth of trap ϕ_t.

Apart from the ground state (FAT), the electrons can tunnel also from a thermally excited state, and the conduction mechanism is referred to as thermionic FAT (T-FAT). T-FAT has been studied in detail by Sathayia and Karmalkar [10,11]. In this two-step process, thermally excited electrons tunnel from the metal into the trap level and then to the oxide conduction band through the triangular barrier.

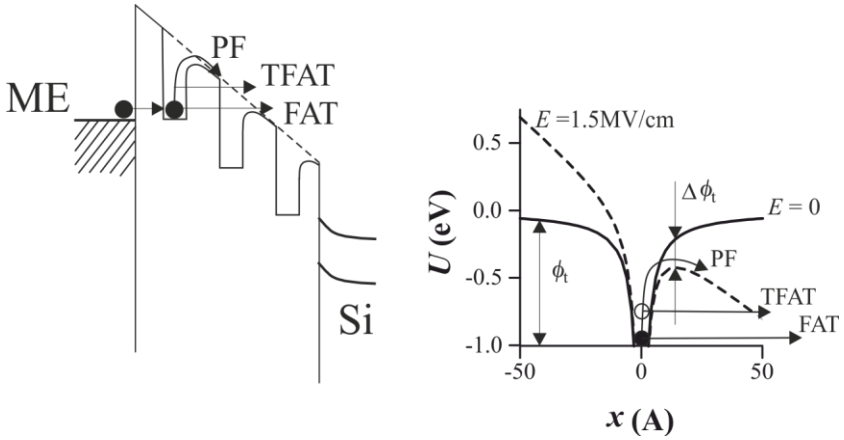

Fig. 5 Schematic representation and comparison of Poole–Frenkel, field-assisted tunneling and thermally stimulated field-assisted tunneling mechanisms along with the modification of the potential barriers of the trap as a result of coulombic interaction between the electron and charged trap core in the presence of electric field. The depth of the trap is 1 eV and the applied electric field is 1.5 MV/cm

The most widely reported conduction mechanism in high-*k* dielectrics is Poole-Frenkel (PF) emission effect. In the PF mechanism the electron tunnel from electrode to a trap in a forbidden gap of dielectric and then is thermally emitted to conduction band due to the lowering of the Coulombic potential barrier when a trap interacts with an electric field. The difference to FAT is represented in Fig.5, i.e. the electron enters the conduction band of dielectric through different processes – thermal emission and tunneling. PF effect will dominate when the tunneling probability is low: e.g. tunneling distances are long (TAT) or electric field is not high enough (FAT). Once emitted in the conduction band the carrier will be very likely captured again by another trap, so the conduction process will resemble hopping. The participating traps have to be Coulombic ones, i.e. neutral when the trap is occupied and charged when empty. The effect is similar to the Schottky emission, the electric field lowers the potential barrier for the trapped charge carrier thereby increasing the thermal ionization rate. The equation describing the current associated with field assisted thermal ionization of traps by Frenkel [12] treats the presence of only one type of trap in the band gap with the Fermi level laying in the middle between trap level and the conduction band edge. The original equation, however, often fails to describe the experimental *J-V* curves showing different slope than expected when plotted in PF scale ($\ln(J/E)$ vs. $E^{1/2}$). Simmons, Yeargan and Taylor, Mark and Hartman [13-15] have addressed the issue showing that if the dielectric besides the PF (donor-like)

trap contains also another type of traps (e.g. acceptor-like or neutral) reducing the density of the available electrons from the donor centers J_{PF} is defined as:

$$J_{PF} = C_{PF} E \exp\left(-\frac{\phi_t - \sqrt{q^3 E / \pi \varepsilon_0 \varepsilon_r}}{rkT} \right) \tag{13}$$

Here, C_{PF} is constant proportional to the donor trap density (N_d) and mobility and r is a coefficient reflecting the degree of compensation of the PF emitting traps by different trapping centers in the dielectric. There are two limiting cases for r: r=1 and r=2, i.e r have to be in the interval $1 \le r \le 2$. Eq. 13 predicts that plot $\ln(J/E)$ vs. $E^{1/2}$ is straight line from the slope of which high-frequency dielectric constant k_r [13] can be found and it is used to verify the operation of PF mechanism. Here we should mention that there is some discrepancy in the literature about the value of r concerning the original Frenkel formula (describing the case when only donor traps present). Some author assume r=1 for the original Frenkel expression eg. [13,16-21] while others as for example [22-24] show that in fact r=2 should be used. In the former case, commonly r=1 is denoted as a pure (or normal) PF effect, and r = 2 is referred as PF with compensation or modified PF [18-21]. In Frenkel's derivation [12] the density of electrons in the conduction band (CB) due to the emission is $\propto \exp(-\phi_t/2kT)$ which leads actually to r=2 in (13). As discussed, however, by J.G. Simmons in [20] and cited there reference, the abundance of shallow traps in the insulator is expected to increase the emission rate of electrons at high electric fields, and hence in case of thin films PF with r=1 is suggested. In this case, when shallow neutral traps lying above the Fermi level and donor sites are introduced in the layer [13] r = 2 is obtained providing the density of compensating traps is approximately equal to the donor ones. Note, that the existence of deep acceptor-like traps (below donor sites) will not change r while using the r=1 approach for a film with only donor traps present [13]. And vice versa if the donor only case is treated with r=2 then the deep acceptor-like traps will result in r=1 [14,15], but in the presence of shallow neutral traps it will remain 2. So, the outlined inconsistency in the "pure" PF model significantly embarrasses the interpretation of the experimental data. Additionally, as pointed out in [16] besides the presence of compensating traps r in (13) depends also on the electron density in CB. And the two limiting cases are r=1 if $n_c < N_{ct} << N_d$; and r = 2 when $N_{ct} < n_c << N_d$, (N_{ct} – density of the compensating traps). Since n_c changes with the applied voltage a transition from r=1 to r=2 could be observed in the PF plot (the transition region corresponds to $n_c \approx N_a$), i.e. the overall shape of $\log(J/E)$ vs. $E^{1/2}$ in the whole range of investigated E is not a single straight line, but can be divided on two straight line segments with different slopes. Hence, except the mere presence of some kind of compensating traps alongside with PF emitting sites, a little can be said about N_{ct} from the slope of J-E characteristics in PF scale. Moreover, it is actually not possible to discern unambiguously the nature of the compensating traps.

Similarly to Schottky emission, PF mechanism is a strongly temperature dependent process. The term $\phi_t - \sqrt{q^3 E/\pi\varepsilon_0 k_r}$ can be considered as an activation energy and is field-dependent. Hence, plotting E_a versus $E^{1/2}$ plot should be a straight line and from the intercept of this line with y-axis, the energy location of the traps ϕ_t (0 V) is obtained.

Eq. 13 was derived using Boltzmann approximation for the electron occupancy of PF traps. A consequence of this approach is that the current relations can be applied only for E bellow $\pi\varepsilon_0\varepsilon_r\phi_t^{\,2}/q$; at higher E the expressions do not have physical meaning inferring that J saturates. Using the Fermi-Dirac function for the electron population of the donor sites [23,25] leads to more complicated current expression but predicting the saturation at high E and also incorporating exact ratio of the donor and compensating traps densities.

Additional attempts have been made to extend the PF effect theory by considering effect of the barrier variation not only in forward but also in opposite to the E direction [26], three-dimensional (3D) treatment of the Coulomb potential in the uniform field [27], and energy distributed donors [28]. Nevertheless, eq. 13 is the most predominantly used for interpretation of the J-V data of dielectrics.

PF effect is observed when the density of ionized centres is low and the coulombic potentials of two adjacent sites do not overlap and the ionization barrier lowering for PF effect is affected only by the applied electric field. When the density of ionized traps is high enough the coulombic field between the adjacent sites overlaps resulting in a decrease of the potential barriers characterizing the system of traps. As a result, the leakage current obeys the simple exponential dependence on the electric field [29]. The mechanism is known as Poole hopping conduction as the thermally excited electron pass over the lowered potential barrier from one site to its adjacent. The Poole conduction current J_P for a 'symmetrical' two-centre system with the distance between centres d_t is given by [29]:

$$J_P = C_p \exp\left(-\frac{\phi'_t - s_p E}{kT}\right); \quad s_p = qd_t/2 \tag{14}$$

where C_P is the trap density-related proportionality constant, and ϕ_t' is the observed trap depth, which is the barrier height between the centres without external applied field. ϕ_t', however, differs from ϕ_t characteristic for non-interacting traps ($\phi_t' = \phi_t - q^2/(\pi\varepsilon_0 k_r d_t)$). Eq. 14 is obtained assuming that sites are grouped in pairs of nearest neighbors and the pairs are effectively insulated from one another. The minimal distance, $d_t^{\min}$ between traps at which the interaction between sites can be considered as negligible is $d_t^{\min} = \sqrt{q/\pi\varepsilon_0 k_r E}$. As PF and Poole conduction share very common nature (thermal excitation over a reduced by electric field potential barrier of trap) it is interesting to see the electric field range in which they are dominant. The deriving of the transitional field from Poole to PF regime, however, depends strongly on the model chosen to describe the Poole conduction. In the simplest case the transitional field is $E_{\text{trans}} = N_t^{2/3} q/\pi\varepsilon_0 k_r$, where the mean distance between traps $d_t \sim N_t^{-2/3}$. More exhaustive discussion of the relation between Poole and PF conductions can be found in [30].

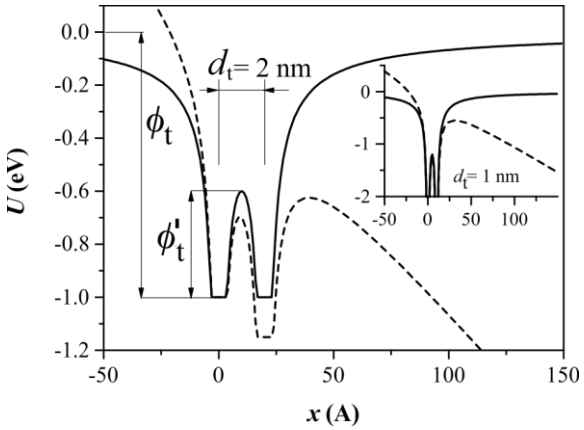

Fig. 6 Modification of the potential energy of two adjacent traps (distance between sites is 2 nm and 1 nm (inset)) without applied electric field (solid lines) and at E= 1.5 MV/cm (dashed lines).

Space charge limited current (SCLC)

SCLC are found in semiconductors and dielectrics under a strong carrier injection. The occurring space charge as a result of the injection of carriers generates additional electric field blocking the entrance of new carriers from the contact. J is defined by the matching of the space charge induced voltage drop inside the layer by applied external voltage. Due to the space charge the current does not obey Ohm's law and increases more rapidly than the applied V (i.e. J is not proportional on V). The space charge in dielectric/ semiconductor films is observed when the electron transition time became lower than dielectric relaxation time. The expression for SCLC is derived from the Poisson's equation and the continuity equation.

In case of ideal dielectric without any traps and no thermally generated carriers, J from single type of carriers is described by Mott-Gurney relation:

$$J = \frac{9}{8}\varepsilon\mu\frac{V^2}{d^3} \tag{15}$$

where ε is the permittivity of the layer. The presence of thermally generated carriers with concentration of n_0 leads to appearance of initial Ohmic part of the J-V characteristics where the injected carrier density is smaller than n_0. When the injected carrier density became equal to n_0 SCLC regime is on and J is given by (15), Fig. 7. The applied voltage at which Ohmic conduction is replaced by SCLC is:

$$V_{SCLC} = \frac{qn_0d^2}{\varepsilon} \tag{16}$$

The charge carrier traps are common feature in the real dielectrics and especially in the high-k materials. In terms of SCLC the traps are divided into two groups by their position in respect to the quasi Fermi level (in presence of electric field), E_{fq}. If the trap

energy level is above Fermi level the trap is denoted as shallow (E_t - E_{fq})/kT > 1, and if it is positioned below E_f it is a deep trap. When one type of single shallow trap exists in the material, J is given by:

$$J = \frac{9}{8}\theta\varepsilon\mu\frac{V^2}{d^3} \text{ with } \theta = \frac{N_c}{gN_t}\exp\left(\frac{E_t - E_f}{kT}\right) \tag{17}$$

where g is the degeneracy factor of the traps, N_c – effective density of states in the conduction band; N_t trap density. The deviation from the Ohm's law occurs at:

$$V_{SCLC} = \frac{qn_0d^2}{\theta\varepsilon} \tag{18}$$

(i.e. V_{SCLC} depends on N_t).

As E_{fq} rises with the increase of the injected carriers, gradually the trap level will come below E_{fq} and eventually all traps will be filled. Near the trap filled condition J begins to rise sharply for several orders of magnitude (represented on the log$J$-log$V$ plot by almost vertical, current jump). This increase continues till all the traps are filled at V_{TFL} after which there is not any trapping, all injected electrons are in conduction band and J is again proportional to V^2.

$$V_{TFL} \approx \frac{qN_td^2}{\varepsilon} \tag{19}$$

For the insulator with deep traps ($E_{fq} - E_t$)/kT > 1 the domination of SCLC begins when the number of total injected carriers (free and trapped) is equal to the empty traps in equilibrium and occurs at:

$$V_{SCLC} = \frac{qNtd^2}{g\varepsilon}\exp\left(\frac{E_t - E_f}{kT}\right) \tag{20}$$

Unlike the case of shallow traps or trap-free dielectric, the current after V_{SCLC} does not switch to square law. Instead a rapid increase of J is observed for $V > V_{SCLC}$. At sufficiently high $V > V_{TFL}$ when all the traps are filled J is again $\propto V^2$ (Fig. 7).

Thus, in the simple cases of trap-free dielectric or dielectric with traps represented by a single energy level in the bandgap, the operation of SCLC can be reliably verified by the presence of $J \propto V^2$ in the characteristics and additionally confirmed by the thickness dependence of J according to (15) and (17). The traps in real dielectrics could be characterized with rather more complex energy distribution than confinement in a discrete energy level. Several more complex distributions have been considered such as exponential, Gaussian and uniform distributions. It turns out that for these more complicated cases, J in SCLC regime is no longer $\propto V^2$. For traps with exponential distribution as well as deep traps distributed in Gaussian manner the current obeys [22,31,32]:

$$J \propto V^{l+1}/d^{2l+1} \tag{21}$$

Where l is higher than 1 and depends on the specific parameters of the particular distribution. (However, J for shallow traps with Gaussian distribution follows (17) but with different θ.).

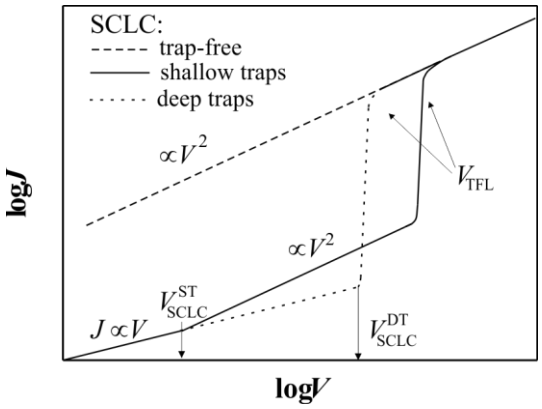

Fig. 7 Schematic *J*-*V* dependence of an insulator in the characteristic for SCLC log-log plot in case of trap-free material and dielectric with shallow and deep traps present. (V_{SCLC}^{ST} and V_{SCLC}^{DT} denotes the values of V_{SCLC} for shallow and deep traps, respectively)

If the traps are uniformly distributed within a narrow band in the forbidden gap (e.g. high impurity concentration) then *J* is represented by [33]:

$$J = 2q\mu N_c g^{-1} \frac{V}{d} \exp(-\Delta E / kT) \exp\left(\frac{2\varepsilon V}{qN_b kTd^2} \right) \tag{22}$$

where ΔE is the trap band width and N_b is the density of the traps per unit energy interval. The switch from Ohmic current to SCLC (V_{SCLC}) can be obtained by solving $J=qn\mu V/d$ where *J* is the current density in SCLC regime described by the above relations. The same approach is used to determine V_{TFL}, however, instead of Ohmic current eq. (15) have to be used.

3. Experimental Procedure

Investigation of current conduction mechanisms was performed on two kinds of test structures - metal-insulator-Si (MIS) or metal-insulator-metal (MIM) capacitors. Various dielectrics (ZrO_2, HfO_2, or Ta_2O_5 and their doped or mixed modifications) were used as insulator in these structures. Several techniques (rf magnetron sputtering, metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD)) were implemented to deposit these dielectrics. In addition, capacitor structures with various metal electrodes were prepared in order to investigate their influence on the conduction mechanisms. All details concerning technology of experimental structures could be found in the related publications cited in the text. Current flowing in the structures is measured in a wide voltage and temperature ranges and in both field polarities (i.e. in the case of MOS structures both at accumulation and inversion conditions) in order to perform complete analysis of current conduction mechanisms. It should be taken into account that when the MOS structure is in inversion due to insufficient amount of minority carriers the injection

current saturates already at low voltages which hinders investigation of conduction mechanisms at higher fields. To solve this problem *I –V* characteristics in inversion are usually measured under illumination to ensure a sufficient generation of minority carriers. Another issue to consider when analyzing I-V curves is the thermodynamic instability of high-k dielectrics when in contact with Si. As a result a thin SiO_2 interfacial layer is usually formed and the applied voltage V_a distributes between the two layers – the high-k dielectric and the interfacial SiO_2. Therefore, when considering the possible conduction mechanisms, the stacked structure of the dielectric layer should be taken into account. The voltage drops across the high-k dielectric – V_{hk}, and across the interfacial layer – V_{if}, can be obtained by the well-known equations [34]:

$$V_{hk} = \frac{V_a}{\frac{\varepsilon_{hk}}{\varepsilon_{if}}\frac{d_{if}}{d_{hk}}+1} = \text{ and } V_{if} = \frac{V_a}{\frac{\varepsilon_{if}}{\varepsilon_{hk}}\frac{d_{hk}}{d_{if}}+1} \tag{23}$$

where ε_{hk} and ε_{if} are the dielectric constants of high-k dielectric and the interface layer, d_{hk} and d_{if} – the thicknesses of the two layers.

4. Results and Discussion

4.1. Conduction mechanisms in SiO_2

Due to the nearly perfect defect free structure of SiO_2 the main conduction mechanisms which governs the current are the electrode-limited Fowler–Nordheim (FN) tunneling in thicker films and direct tunneling in layers thinner than about 3 nm. Lenzlinger and Snow [35] have shown that the conduction current in conventional SiO_2 films can be excellently described by the classical FN formula. Since thermally grown SiO_2 has an extremely wide bandgap and consequently a high energy barrier at its contact with an electrode, it is more likely to show electrode-limited conduction than other insulators. In addition, bulk-limited mechanisms are less likely to play a role because of the low trap density in the forbidden band of SiO_2. Direct tunneling is observed in very thin dielectric films (< 4 nm). In this case electrons tunnel from one electrode to the other through the dielectric film, i.e. this is a tunneling through trapezoidal barrier and the electron does not enter the conduction band of dielectric. Figure depicts typical *J-V* curves (gate injection mode) of MOS capacitors with thermal SiO_2 with thickness corresponding to DT and FN tunneling regimes, respectively. As seen the experimental data are very well fitted with eq. 3 and 4. Assuming that m^*/m_0 = 0.5the thickness of the SiO_2 layer and barrier height at Al/SiO_2 interface were found. The obtained results agree very well with the ellipsometrically measured thicknesses and widely accepted the values of ϕ_b for Al/SiO_2 interface.

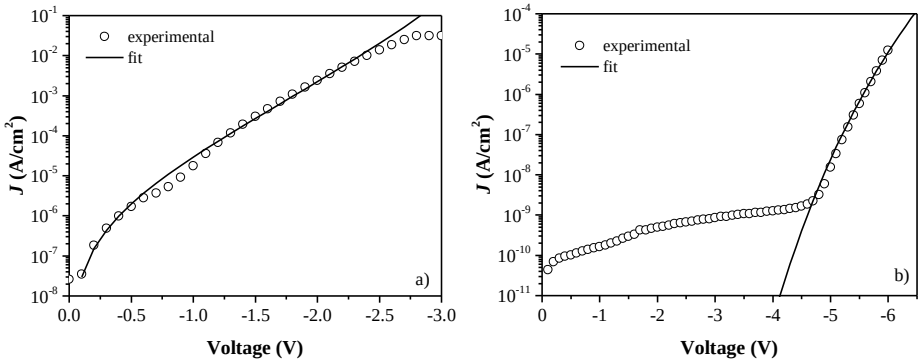

Fig. 8 Leakage currents of Al/SiO_2/p-Si capacitors with SiO_2 thickness of 2.3 nm (a) and 6.6 nm (b). The data is fitted to DT (a) and FN (b) mechanisms using $m^*/m_0 = 0.5$; $\phi_b = 3.05$ eV (a) and 3.1 eV (b).

4.2. Conduction mechanisms in high-*k* dielectrics

In high-*k* materials the conduction mechanisms are usually trap related and the domination of a certain mechanism depends on many parameters, which could be summarized in several groups: 1) parameters of intrinsic and process-induced traps (density, spatial and energy location, and charge state), which are directly related to the inherent electronic structure of the high-*k* material as well as to the technological processes used for their fabrication; 2) stack parameters including thickness of the dielectric and existence of interfacial layer, structural status of the films (amorphous or crystalline), type of metal electrode, etc.; and 3) measurement conditions—applied voltage and its polarity and temperature. Such a big set of parameters influencing the conduction process results in a wide diversity of mechanisms observed in high-*k* dielectric stacks.

Dependence on measurement conditions (bias, polarity, temperature)

It is clear that conduction mechanisms are strongly dependent and defined by the measurement conditions (bias, polarity, temperature). Respectively, the change of measurement conditions could result in a change of dominating conduction process in dielectric and this change could be used for better understanding of trap participation in conduction mechanisms as well as assessment of some structure parameters. The first example will demonstrate the possibility to obtain the barrier height at high-k dielectric/Si interface by measurement at low temperatures. Ti/Zr-silicate/Si MOS structures have been investigated [36] and we tried to obtain Fowler–Nordheim conduction in this structure. *I–V* measurements were performed under substrate injection at low temperatures (from room down to -185 °C). The measurements showed indeed that below about -120°C, the *I–V* curves are temperature independent and can be well fitted by Fowler–Nordheim equation (3). From the fitting, we obtained a value of 1.4 eV for the barrier height at the Zr-silicate/Si interface. This value is in agreement with the value of 1.4 eV given for zirconium dioxide [37].

Measurements at very low temperatures could give also valuable information about the traps because all temperature activated processes are suppressed, hence only temperature independent processes (e.g. Fowler-Nordheim, field-assisted tunneling etc.) may operate. In addition, at a certain temperature the trapping and detrapping are in a thermal equilibrium. As the trapping is slightly temperature dependent [38,39], while detrapping is strongly temperature stimulated process, it is expected that at very low temperatures detrapping does not occur, hence the influence on the leakage current of trapping with respect to detrapping will be maximized.

Following this idea the change of conduction mechanisms in $TiN/Zr_{1-x}Al_xO_2/TiN$ MIM structures (Al content less than 10%) measured in a wide bias and temperature range [40] has been investigated. The *J-V* curves of structures are measured down to very low (25 K) temperatures (Fig. 9). Despite of the symmetrical MIM structures there is a polarity asymmetry at 25 K, while at 300 K symmetrical curves have been obtained (Fig. 9a). At $T<175$ K the conduction process at both polarities is symmetric - it is FAT through one and the same bulk traps located at ~1.3-1.4 eV below CB of dielectric. The asymmetry of *J-V* curves and the stronger temperature dependence at positive bias resulted from the trapping/detrapping at the bottom TiN/high-k interface (where thin TiO_x–like layer is formed [41,42]) and the shift $\Delta V \sim 0.4$-0.5 V between the two *J-V* curves at 25 K corresponds to a trapped charge of $\sim 8 \times 10^{12}$ cm^{-2}. Consideration of possible conduction mechanisms at higher temperatures ($T \geq 25$ °C) (Fig. 9b) in negative polarity revealed that at low fields ($V < |-2|$ V) the current is due to trap assisted tunneling (TAT) through a trapezoidal barrier and the activation energy of the process is ~0.25 eV. The increase of voltage above $|-2|$ V changes the barrier for the tunneling electrons from trapezoidal to triangular, i.e. a change from TAT to FAT occurs, which results in a change of the field dependence of the current. The weak temperature dependence in the range 30-100 °C and the obtained activation energy of ~0.25 eV (same as that for $V < |-2|$ V) (Fig. 9b) is related to the thermal excitation of electrons at the first stage of the tunneling process (i.e. injection from electrode to the trap). With the increase of temperature above 100 °C the probability for thermal excitation from trap to the CB of dielectric increases and the PF process through traps located at ~1.3 eV (Fig. 10a) becomes the dominant mechanism. Therefore, the results reveal existence of a trap level at about 1.3 eV below the CB edge of dielectric, which fully controls the transport of electrons through the dielectric at negative polarity and gives rise to several conduction mechanisms that dominate at different conditions. This trap level is assigned to the first ionization level V^+ of O vacancy in ZrO_2 whose energy position has been calculated at 1.2-1.4 eV [43]. The conduction at positive polarity is substantially different and only one temperature activated process operates (Fig.10b), unlike the case at negative polarity. PF conduction is the dominating mechanism at these conditions and the energy location of traps is found to be at ~0.85 eV below the CB of the dielectric (i.e., it is substantially different from the values obtained at negative polarity). Therefore, the current transport at very low temperatures is realized through 1.3 eV traps, whereas at higher temperatures different traps govern the current at the two polarities. The feasible explanation is that 0.85 eV trap level is related to defects resulting from the reaction at the high-*k*/bottom TiN electrode. At very low temperatures these defects act as traps, while at high fields and temperatures they serve as transport sites, by this way controlling the current at positive polarity.

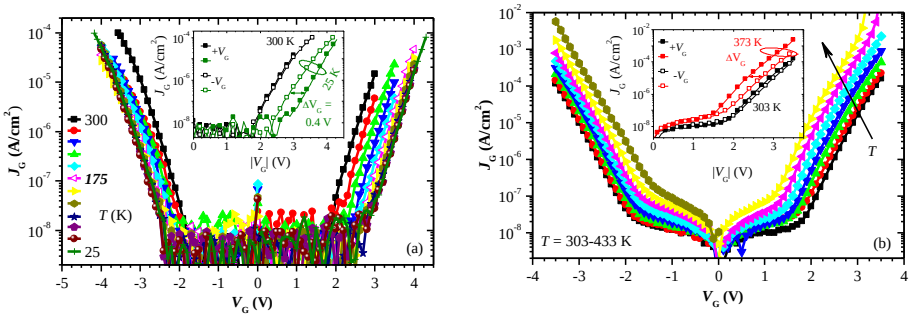

Fig. 9 *J-V* curves of TiN/$Zr_{1-x}Al_xO_2$/TiN capacitors measured (a) from 25 to 300 K, and (b) from 300 to 430 K. The insets compare the *J-V* curves at both top electrode polarities and different temperatures [40].

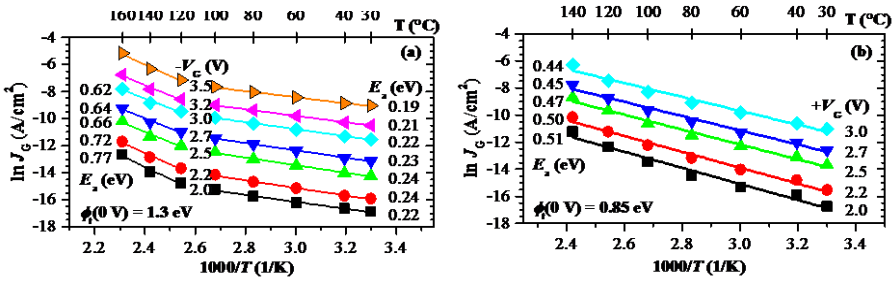

Fig. 10 Arrhenius plot of current density at (a) negative, and (b) positive top electrode polarity [40].

Dependence on thickness

Results obtained for Ru/Ta_2O_5/SiON/Si MOS structures will be used to demonstrate the dependence of conduction mechanisms on dielectric thickness [44]. Temperature dependent *I-V* (*I-V-T*) characteristics of structures with different Ta_2O_5 thickness in the range 1.85 – 13.5 nm measured at 25 and 100 °C are shown in Fig. 11. It is seen that *I-V-T* characteristics measured at negative voltages show stronger temperature dependence for the thicker dielectrics; this dependence weakens as the oxide thickness decreases and almost disappears for 1.85-nm-thick oxide film. For positive gate bias, *i.e.* substrate injection, *I-V-T* characteristics show a weak dependence on temperature for all thicknesses.

The considerations show that at low electric fields (Fig. 11), the logarithm of current density (J_g) changes linearly with gate voltage (V_g) for Ta_2O_5 with t_{ox} =13.5– 7.0 nm. This is consistent with the Poole hopping, eq (14) and can be explained with the higher defect density close to Ru electrode originating from the reaction at its interface with Ta_2O_5.

For higher electric fields under gate injection (V_g>|-3|, |-1.5|, and |-1| V for MOS capacitors with t_{ox}=13.5, 7.0, and 3.5 nm, respectively), observed behaviour indicates a gradual transition from temperature dependent conduction mechanism governing leakage current in the thicker layers to the mechanism with a weak temperature dependence in the thinner oxide layers. Among other conduction mechanisms examined, only transition from Poole-Frenkel (PF)

emission (eq. 13) through thermionic field assisted tunneling (T-FAT) to field-assisted tunneling (FAT) (eq. 3,12) can qualitatively reproduce *I-V-T* characteristics. For IF layer, direct tunneling through trapezoidal barrier is assumed. For MOS structure with t_{ox}=13.5 nm, PF emission (eq. 13) fits well *I-V-T* curves for V_g>|-3| V and ϕ_t=0.7 eV is extrapolated from eq. (13) (Fig. 12). Since electric field in the high-*k* oxides increases for thinner oxides, electron tunneling from the trap level to Ta_2O_5 conduction band through the triangular barrier (i.e. field-assisted emission) becomes dominant (Fig. 13). In thin layers tunneling is the more probable process. With increasing the thickness, the tunneling probability decreases and the PF emission from the traps becomes dominating.

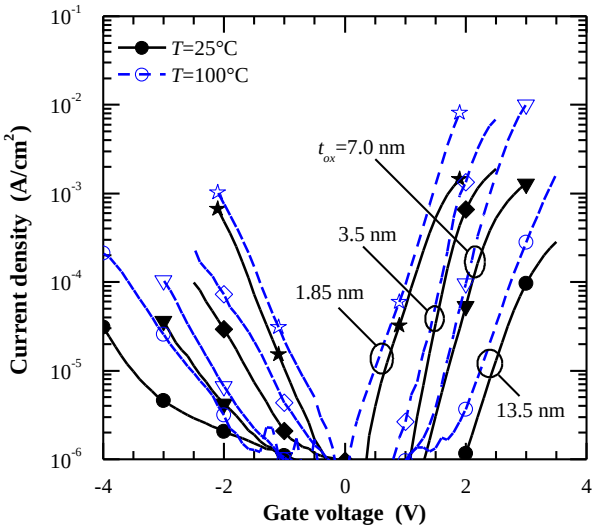

Fig. 11 Leakage current–voltage characteristics measured at 25 (solid symbols) and 100 °C (open symbols) on MOS structures with different oxide thickness. For clarity, the *I–V–T* characteristics of 10 nm thick oxide are not displayed [44].

The trap barrier heights for MOS structures with oxide thickness of 10.1, 7.0, and 3.5 nm have been calculated from *I-V* data measured at room temperature (RT) and 100 °C ($E_{high\text{-}k}$ is defined from eq. 23; m_{ox}=0.3m_e). The trap barrier heights measured at room temperature are in the range 0.29 - 0.31 eV for Ta_2O_5 with different thickness, while those extracted from the *I-V* curves measured at 100 C are systematically lower of about 10 meV. Although the difference between ϕ_t extracted at RT and 100°C is in the range of experimental error, observed behaviour suggests that conduction mechanism in the MOS capacitors with 3.5<t_{ox}<10 nm is dominated by T-FAT, *i.e.* trapped electrons are first thermally excited and then tunnel through the triangular barrier into the oxide conduction band.

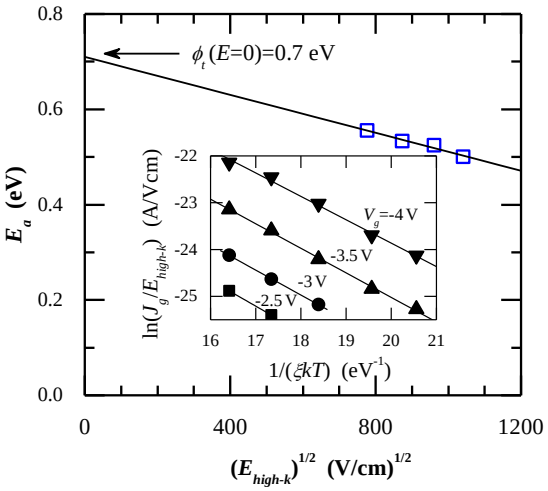

Fig. 12 The zero electric field trap barrier height extracted from the dependence of the activation energy (E_a) on $(E_{high-k})^{1/2}$ for 13.5 nm thick Ta_2O_5. Inset shows extraction of E_a from the slope of linear *I–V–T* characteristics at V_g =−2.5 (squares), −3 (circles), −3.5 (up triangles), and −4 V (down triangles) [44].

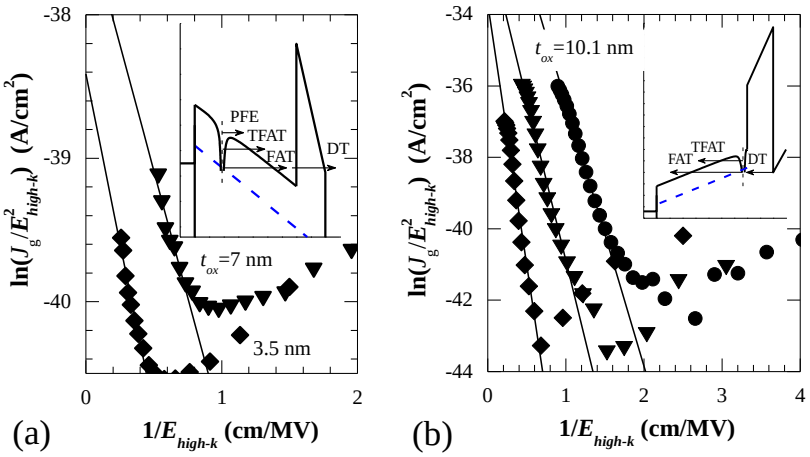

Fig. 13 a) FAT plot for the leakage current of MOS structures with thicknesses of 7.0 and 3.5 nm under gate injection; b) 10.1, 7.0 and 3.5 nm under substrate injection. Insets show schematic band diagrams illustrating the current mechanisms (*I–V* curves were measured at room temperature) [44].

For substrate injection, PF emission model did not fit *I-V-T* characteristics even for MOS structure with t_{ox}=13.5 nm, while good linearity of the FAT plot for oxide thickness ranging from 13.5 to 3.5 nm is observed (Fig. 13b). Calculated trap barrier heights extracted at RT range from 0.34 to 0.53 eV, i.e. the current is also governed by the T-FAT conduction

mechanism for MOS capacitors with t_{ox}=13.5, 10.1 and 7.0 nm. Gate leakage of the MOS capacitor with t_{ox} = 3.5 nm shows good linearity of the FAT plot, suggesting that FAT through the triangular barrier governs the conduction mechanism. Higher ϕ_t of 0.53 and 0.6 eV extracted at RT and 100 °C, respectively, is also consistent with emergence of the FAT conduction mechanism as these values approach that extrapolated at a zero electric field in Fig. 12. Trap barrier heights extracted from the FAT plot at 100 °C suggest gradual transition of conduction mechanism from T- FAT to FAT from the same trap level in Ta_2O_5. For the thicker oxides, thermally excited electrons tunnel through trapezoidal SiON IF layer into the Ta_2O_5 trap level and then through the triangular barrier into the conduction band (inset Fig. 13b). For the thinnest oxide, the high electric field in both interfacial layer and high-*k* oxide enables tunnelling of electrons directly from the Si conduction band into the Ta_2O_5 trap level and their subsequent tunnelling into the Ta_2O_5 conduction band.

Therefore, the results imply that for both the gate and the substrate injection, the same trap level located at about 0.7 eV below oxide conduction band edge and distributed throughout Ta_2O_5 bulk is involved in PF, T- FAT, and FAT conduction mechanisms. This trap level is in accordance with the theoretical predictions [45] and experimental observations (ϕ_t~0.8 eV) [46] of other authors which assign it to the first ionization level of the O vacancy double donor V^+ in Ta_2O_5.

Dependence on doping

Ti-doped Ta_2O_5: The effect of Ti dopant on the conduction mechanisms in sputtered Ta_2O_5 is considered in [47]. Ta_2O_5 films with overall thickness of 10 and 30 nm were subjected to Ti doping using two techniques: type-A ("surface doping") in which an ultra-thin Ti layer (0.7 and 2 nm) was sputtered on the top of the Ta_2O_5; and type-B ("bulk doping") where the Ti layer was sandwiched between two Ta_2O_5 sublayers with equal thicknesses (5 or 15 nm each). After the deposition the structures were subjected to PDA in N_2 at 400 °C for 30 min in order to obtain intermix of the resulting films. The obtained results show that Ti-doping can reduce the leakage currents of Ta_2O_5, but the outcome depends on both the amount of Ti (i.e. the thickness of Ti layer) and the method of doping. For 10 nm layers surface doping with minimum Ti is optimal, while for 30 nm films best results are obtained with type-B doping with 2 nm Ti sublayer. The conduction mechanisms of Ti-doped layers were interpreted in terms of Ohmic conduction and PF effect. *J-E* characteristics of type-B doped 10 nm Ta_2O_5 are linear up to ~1.2 MV/cm demonstrating Ohmic conduction. The observed change of the conduction mechanism from PF to Ohmic is most probably due to the introduction of significant amount of shallow traps during the type-B doping of the thin layers. We speculate that when Ta_2O_5 is thin enough the Ti intermixing with Ta_2O_5 through N_2 annealing leads to a stack having specific chemical bonds and high defect density which constitutes the detected conduction mechanism. In all other cases the conduction of Ti-doped is Ta_2O_5 described with Ohmic behavior at low electric fields and PF effect at E > 0.2 MV/cm Compared to the pure Ta_2O_5, the effect of the doping consist in a modification of the compensation factor of PF mechanism. The doping of thin Ta_2O_5 increases the value of *r* to 2, but for the thicker ones *r* is reduced compared to the pure Ta_2O_5 (Fig. 14). These results show that the type and the density of traps are changed as a result of the doping, but the details of this change depend on the film thickness rather than on the Ti incorporation method.

The analysis of the temperature dependence of the current in Ti:Ta_2O_5 layers [48] reveal that the energy levels of the defects participating in the conduction are in the range of 0.6-0.7 eV and do not depend on the method of Ti incorporation.

These values are close to the values typical for pure Ta_2O_5 suggesting that Ti-doping does not alter the dominant defect structure but only the traps density and the degree of compensation in the PF mechanism.

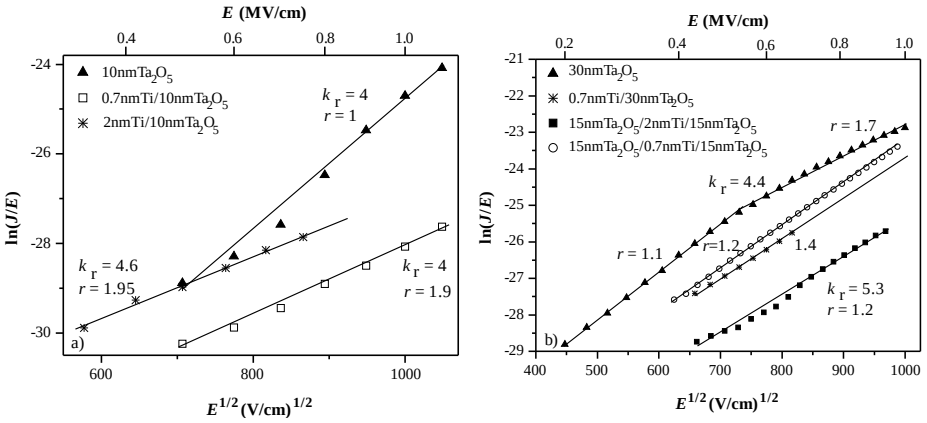

Fig. 14 Poole-Frenkel plot of *J–V* curves of the capacitors with pure and doped Ta_2O_5 with two levels of Ti incorporation and two thicknesses d of the stack: a) *d*∼10 nm, b) ∼30 nm. The values of k_r, *r* are given [47].

Hf-doped Ta_2O_5: The doping of Ta_2O_5 with Hf results in a significant alteration of the shape and temperature dependence of the leakage current (Fig.15) [49]. Generally, the current at room temperature in Hf-doped samples is higher than that in pure Ta_2O_5 and it is very weakly temperature dependent. The dominating conduction mechanisms and energy location of traps involved in them for samples with various thicknesses are summarized in Table 1. The results imply that a change of the conduction mechanism from field-assisted tunneling (FAT) to PF emission occurs with increasing the thickness of Hf-doped Ta_2O_5 which is in agreement with results obtained above for pure Ta_2O_5 with Ru electrode. However, the traps responsible for both processes are the same and they are located at ~0.35-0.45 eV below CB of dielectric. Therefore, the conduction in Hf-doped Ta_2O_5, either field-assisted tunneling, PF emission or even hopping, is governed by shallower traps (ϕ_t~0.35-0.45 eV). The deeper levels (~0.75-0.9 eV) typical of pure Ta_2O_5 (Table 1) are not observed in any of the doped samples. These results imply that Hf passivates the deeper traps (O vacancies) and the electron transport is performed through energetically shallower traps. The obvious consequences of the transport through shallower traps in the doped samples are the higher level of leakage current at room temperature and considerably weaker temperature dependence. The last result can have serious implementation as the increase of temperature during device operation will not change the leakage current in Hf-doped samples, hence more stable and predictable behavior and enhanced reliability could be anticipated. In fact, the leakage current at 100° C is already lower in the Hf-doped Ta_2O_5 as compared to the un-doped ones.

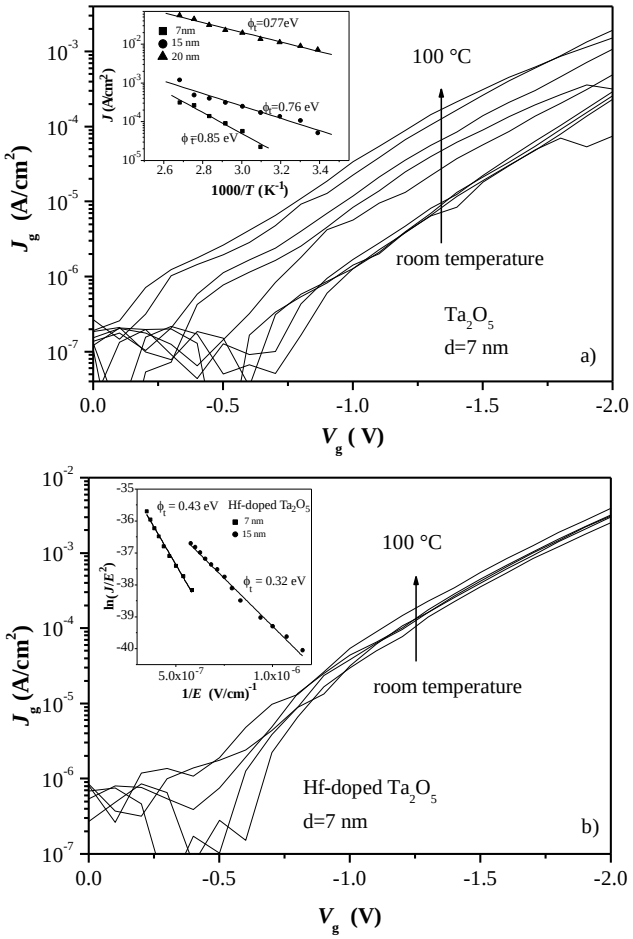

Fig. 15 Temperature dependent *J-V* curves of a) Al/pure Ta_2O_5/*p*-Si structures; the inset shows the Arrhenius plot of the current for three different film thicknesses and b) Al/Hf-doped Ta_2O_5/*p*-Si structures; the inset represents the results in FN coordinates [49].

Al-doped Ta_2O_5: Another doping agent studied to assess the possibility for improving the electrical properties of Ta_2O_5 is aluminum. Since Al atoms have lower valence than Ta ones it was expected that they could act as acceptors and compensate the oxygen vacancies in Ta_2O_5. Two Al-doping techniques were investigated. In the first approach, Al was introduced in Ta_2O_5 using the surface doping method (similarly as in the case of Ti- and Hf- doping) [50]. In the second approach, lightly Al-doped Ta_2O_5 layers were obtained by reactive sputtering in oxygen containing environment of TaAl target containing 5 at% aluminum [51]. For the first type of Al-doped stacks, the high field conductance was through PF effect, and similarly to the case of Ti-doping the effect of the dopant consists in a modification of the compensation factor *r*. The increase of Al content results in higher *r*.

The behavior of lightly Al-doped films fabricated by TaAl target sputtering is more complicated. Compared to the pure Ta_2O_5, the current in lightly Al-doped samples is higher. Furthermore, the temperature dependence of *J* seams to depend on the layer thickness as evidenced in Fig. 16, symptomatic of a significant difference in the dominant conduction mechanisms. Schottky emission and SCLC were ruled out as a possible origin of *J-V* characteristics in 10 nm films. PF mechanism can explain the characteristics at high fields (above 1.4 MV/cm). The obtained from the fits values of *r* exhibit a clear temperature dependence - it decreases with the temperature. *J-V* curves can be also well described by $J \propto \exp(E)$ (Fig. 17) which is consistent with Poole hopping (eq. 14). The two segments could be interpreted with two sets of traps defining the current at low and high fields respectively. The operation of Poole hopping (at gate injection) means the presence of high trap concentration close to the gate electrode. The Arrhenius plots of the current density at several applied voltages is depicted on Fig. 18 together with the calculated trap energies according to the considered conduction mechanisms.

Table 1 Summary of the dominant conduction mechanisms and the respective traps participating in them in dependence on the film composition and thickness

Samples	d, nm	Temperature of measurement	Dominant conduction mechanism	Trap energy position, eV
		20-50 °C	field assisted tunneling	0.4
Pure Ta_2O_5			Poole-Frenkel emission	
	7	60-100°C		0.85
Hf-doped Ta_2O_5		20-100°C	field assisted tunneling	0.43
Pure Ta_2O_5		20-100°C	Poole-Frenkel emission	0.76
			1.2<V<2.6 V	
			field assisted tunneling	0.32
Hf-doped	15			
Ta_2O_5		20-100°C	2.6<V<3.5 V	
			hopping	0.34
Pure Ta_2O_5		20-100°C	Poole-Frenkel emission	0.75-0.9
Hf-doped Ta_2O_5	20	20-100°C	Poole-Frenkel emission	0.45

The extracted value of ϕ_t^p in case of Poole process is 0.12 eV at high applied fields. Similar value (0.14 eV) is found also for traps participating in PF mechanism. This is again in contrast to pure Ta_2O_5 for which the current is governed by PF effect through the traps with energy depth of 0.7–0.8 eV. Therefore, the introduction of 5 at.% Al into Ta_2O_5 tends to create much more shallower traps compared to these of Ta_2O_5. Since *J* reflects mainly the changes in the cathode electrical field it seems that the traps involved in the conduction mechanism are located near the gate/doped Ta_2O_5 interface.

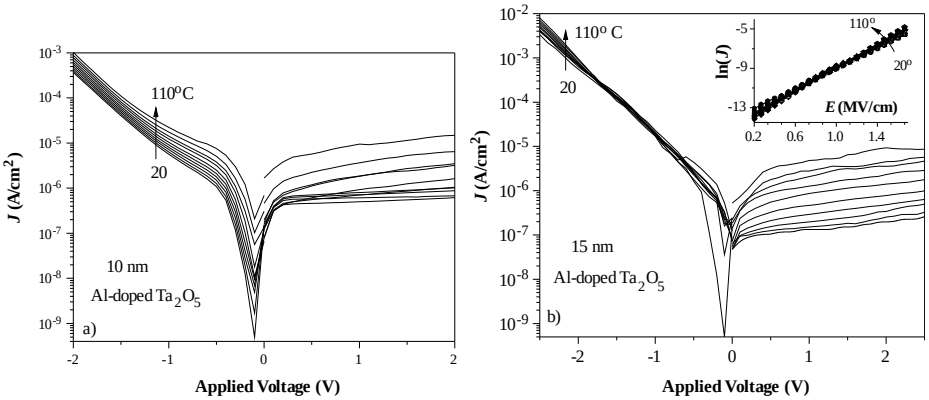

Fig. 16 Temperature dependent *J*–*V* curves for Al-doped Ta_2O_5, (a) *d* = 10 nm; (b) *d* = 15 nm [51].

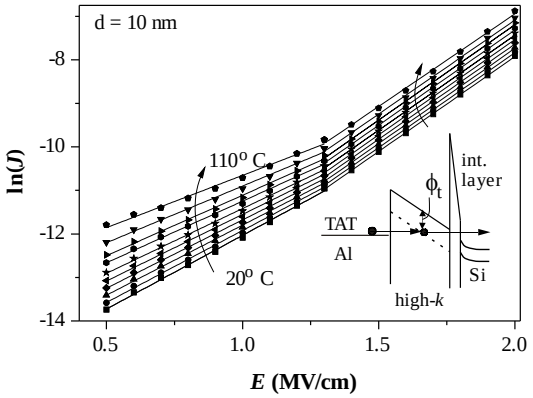

Fig. 17 ln*J* vs. *E* plot at different temperatures of 10 nm doped films. Symbols refer to the experimental data, solid lines to the fitting. Schematic energy band diagram of capacitor under a negative bias is also shown in the inset; ϕ_t is the trap energy depth [51].

The lack of temperature dependence of the current up to 1.3 MV/cm in 15 nm doped films suggests a domination of tunneling processes, but the layer's thickness obviously excludes the direct tunneling. Representation of the current characteristics in FN plot (Fig. 19) gives a barrier height ϕ_b ~ 0.16–0.18 eV for *T* varying between 20° and 100° C. The rough estimation of the band diagram of Al-Ta_2O_5 stacks gives ϕ_b ~ 1–1.2 eV. Therefore, it is more realistic to assume the domination of FAT and the obtained trap energy level ϕ_t ~ 0.16-0.18 eV is similar to that detected also for 10 nm films.

Therefore, the results imply that even very small (5 at.%) Al amount in the matrix of Ta_2O_5 can modify the mechanism of conductivity typical of undoped Ta_2O_5. Despite the difference in conduction mechanisms for sample with two thicknesses, the trap level observed is one and the same ϕ_t ~ 0.12–0.15 eV, i.e. the Al-doping suppresses deep defect states located at ϕ_t ~ 0.7–0.8

eV (governing the conductivity in pure Ta_2O_5) but creates new shallow traps which mediate the charge transport thereby changing the dominant conduction mechanism. The exact origin of these shallow traps is not known. A plausible explanation is that the passivation of O vacancy by Al results in a shift of its energy state up into the band gap of the dielectric.

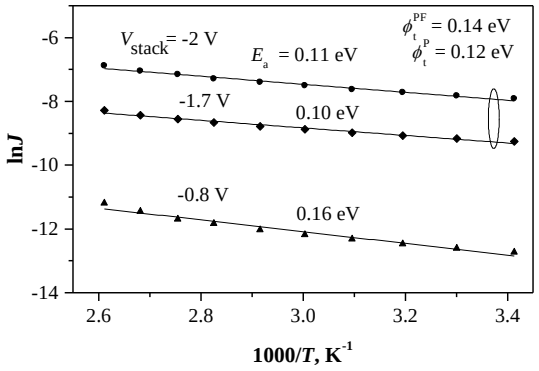

Fig. 18 Arrhenius plots of 10 nm Al-doped Ta_2O_5. The energy depth of electron traps participating in Poole–Frenkel or Poole effects, and the activation energies for TAT, extracted from the experimental fits are given [51].

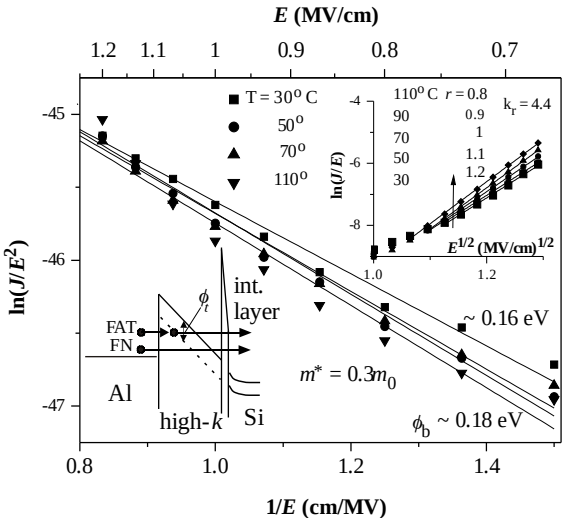

Fig. 19 Fowler–Nordheim plot of *J*–*V* curves at several temperatures for 15 nm doped films. Symbols refer to the experimental data and solid lines to FN simulation. Schematic energy band diagram for both FN and FAT process of a capacitor under negative bias is shown. ϕ_t is the trap energy below the conduction band of high-k film; ϕ_b is the Al/high-k barrier height. Inset: *J*–*V* curves at different temperatures, represented in PF coordinates [51].

Al-doped HfO_2: Next examples will demonstrate that the dominant conduction mechanism could be influenced not only by the type and amount of dopant but also by the way this dopant is introduced into the film. Three types of layers have been deposited on nitrided Si by atomic layer deposition (ALD) – pure HfO_2 (75 cy), HfO_2(36 cy)/Al_2O_3(5 cy)/HfO_2(36 cy) (HAH), and HfO_2(24 cy)/Al_2O_3(2 cy)/HfO_2(24 cy)/Al_2O_3(2 cy)/HfO_2(24 cy) (HAHAH). More details on deposition conditions and technology of structures could be found in [52]. Temperature dependent *I-V* measurements (Fig. 20) revealed significant differences between the samples, at negative biases. In positive polarity the leakage current is dominated by the conduction through the interfacial SiON layer which results in similar temperature behaviour of the *I-V* curves (for T<120 °C) for all the samples. Therefore, we will focus our attention on the behaviour of the *I-V* curves in negative polarity.

The very weak temperature dependence up to 60 °C for the pure HfO_2 film (Fig. 20a) implies the domination of some tunnelling processes. Fowler-Nordheim (FN) tunnelling is considered as the layers are relatively thick (~10 nm), hence the probability for direct tunnelling is low. The obtained barrier height for FN tunneling (E_{hk}>1.5 MV/cm) is $\phi_b \sim 0.7\pm0.1$ eV ($m^* = 0.1m_0$) [53]. As the barrier height at TiN/HfO_2 is expected to be much higher (~2.6 eV) [54], we conclude that the dominant mechanism is not Fowler-Nordheim tunnelling but field-assisted tunnelling (FAT).

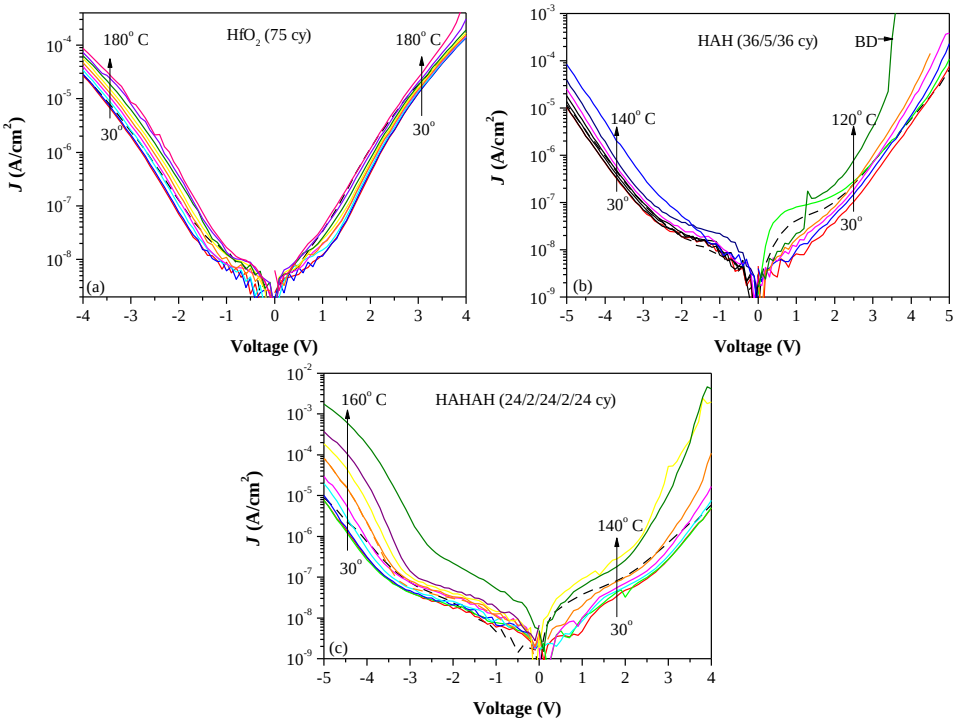

Fig. 20 Temperature-dependent I-V measurements for: (a) HfO_2 (75 cy); (b) HAH (36/5/36); and (c) HAHAH (24/2/24/2/24) samples [52].

Therefore, the obtained value of ~0.7 eV is the position of traps ϕ_t with respect to the CB of HfO_2 and it corresponds to the energy position of oxygen vacancies in HfO_2 [55,56]. The current is temperature dependent for T>60 °C, hence Poole-Frenkel mechanism (eq. 13) has been considered. The obtained values of r^2k_r (from the slope of the lines) are consistent with the refractive index of the dielectric and the limitation $1 \leq r \leq 2$ and it is concluded that PF is the dominant conduction mechanism and the energy position of traps ϕ_t ~0.72 eV was extracted, i.e. these are the same traps which govern the FAT process at lower temperatures. Therefore, the results imply that the conduction is performed through the traps situated at ~0.7 eV below the CB of HfO_2. FAT dominates at low T, while PF dominates at elevated temperatures. It is worth mentioning that FAT and PF conduction should co-exist in principle as they both represent the escape of an electron from a trap and the current is actually a sum of the currents from both mechanisms.

Similarly, the current in HAH (36/5/36) sample is nearly T-independent up to 60 °C (Fig. 20b) and the same mechanisms - FAT at T < 60 °C, and PF at T > 60 °C, (E_{hk} > 2 MV/cm) have been considered. The fitting gives a trap energy ϕ_t ~1.2-1.3 eV for FAT process and ϕ_t ~ 0.4 – 0.5 eV for PF process. In other words, unlike the pure HfO_2, in the HAH (36/5/36) sample the FAT and PF processes are mediated by two different trap levels. These results give evidence that Al-doping introduces deeper trap levels than these in pure HfO_2. Further considerations of the conduction mechanisms in the HAHAH(24/2/24/2/24) sample confirm this conclusion and reveal that the way of Al incorporation into HfO_2 is also of substantial importance. There is still a weak T-dependence up to 60 °C and above 60 °C the current increases more strongly compared to the HAH(36/5/36) sample (Fig. 20c). Consideration of FAT process as a dominant conduction mechanism at T < 60 °C, E_{hk} > 1.4 MV/cm gives a trap level ϕ_t ~ 1.4 eV, i.e. slightly deeper than that obtained for the HAH(36/5/36) sample. Poole-Frenkel does not fit the *I-V* curves well. Having in mind the peculiarity of the doping process of the HAHAH(24/2/24/2/24) sample, it is suggested that the conduction could be governed by Poole conduction (eq.13). Indeed, the Poole mechanism fits well the current at T≥100 °C (Fig. 21a) and the activation energy of the process controlling leakage current is found (Fig. 21b) - E_a ~ 0.2-0.3 eV for T<100 °C, while at T≥100 °C a larger activation energy of E_a ~ 0.6-0.7 eV is observed. For Poole conduction $E_a = \phi_t - s_pE_{hk,}$ i.e. the activation energy is linearly dependent on E_{hk} and the intercept of the line with the y-axis gives ϕ_t = 1.2 eV (Fig. 21a), i.e. very similar to the trap level which controls the FAT process at lower temperatures both in the HAH(36/5/36) and the HAHAH(24/2/24/2/24) samples. This result supports the conclusion that the 1.2 eV level is related to Al-doping. Therefore, the results obtained for this sample reveal that FAT is dominant at T<60°C; at 60°C < T < 100°C both FAT and Poole conduction are present. With increasing temperature the contribution of Poole conduction increases and at T>100°C it is the main mechanism which governs the current in HAHAH(24/2/24/2/24) sample. The specific way of Al incorporation in HAHAH(24/2/24/2/24) sample results in a more homogeneous distribution of traps and favours Poole conduction between them

The conduction mechanisms considered up-to-now dominate at relatively high fields E_{hk} > 1.5 MV/cm. As is seen in Fig. 20c there is a wide electrical field region (V< |-3| V, E_{hk} < 1.3 MV/cm.) where the current increases only slightly with applied voltage and temperature. It is suggested that in this region the conduction is governed by a space charge limited current (SCLC) mechanism [57]. The log$J$-log$E$ representation of *I-V*

curves gives a line with a slope of ~1 corresponding to Ohmic conduction, which increases to ~2 (Fig.22). This behavior is in accordance with the SCLC theory in the presence of discrete shallow traps (i.e. trap level above the Fermi level) (eq. 17). The voltage V_{TFL} in Fig. 22 is a trap-filled limit at which all the traps are filled. Therefore, in this field range SCLC is the dominant mechanism in the HAHAH(24/2/24/2/24) sample.

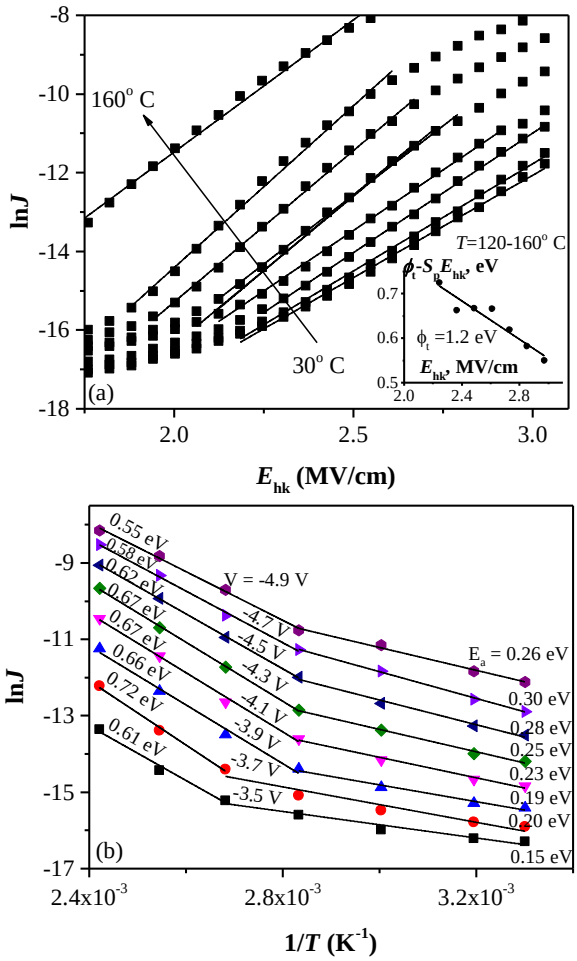

Fig. 21 (a) Representation of *I-V* curves in Poole coordinates (lnJ vs. E_{hk}) of HAHAH sample. The inset shows the dependence of activation energy $E_a = \phi_t - s_p E_{hk}$ of Poole conduction on the electric field. (b) Arrhenius plot of the current in HAHAH sample in the whole temperature range (30-100° C) and for different applied voltages [52].

Therefore, the detailed characterisation of conduction mechanisms in different stacks revealed the existence of traps with an energy level of 0.7 eV below the conduction band in pure HfO_2 which is consistent with the energy of an oxygen vacancy in HfO_2. The

conduction in HfO_2 is performed via these traps and the dominant conduction mechanism (FAT or PF emission) is defined by the measurement conditions (applied voltage and temperature). In all Al-doped samples the existence of a deeper level (1.2-1.4 eV below the conduction band) is undoubtedly revealed. The 0.7 eV level is not observed at all. The disappearance of the 0.7 eV trap level could be explained by a reduction of the concentration of oxygen vacancies in HfO_2 by Al-doping, which was observed also by other authors [58]. The increase of Al-doping obviously results in the formation of deeper traps, which have been observed also by Molas et. al. [59], who found a trap level at about 1.35 eV below the conduction band for HfAlO layers with Hf:Al(9:1) which is even deeper (1.55 eV) for samples with higher Al content (Hf:Al(1:9)).

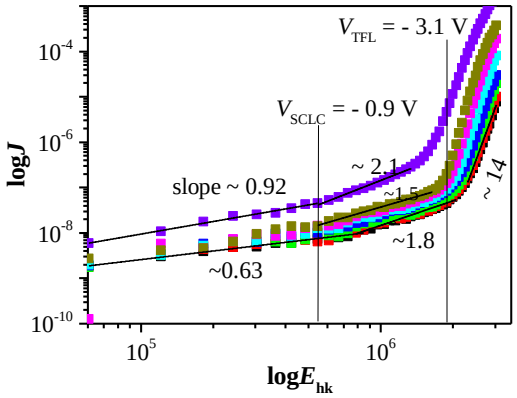

Fig. 22 logJ vs. $logE_{hk}$ curves representing the space-charge-limited conduction at low fields in HAHAH sample [52].

Dependence on composition

In the examples considered up to now the influence of small amount of a given element on conduction mechanisms of high-k dielectrics have been considered. The next example will demonstrate how the gradual change of Hf:Ti ratio (both Hf and Ti in significant amount) in the composition of high-k HfTi-silicate layers results in quite different field, temperature and polarity dependences of the leakage currents, hence in significant alteration of the dominating conduction mechanism (Fig. 23a-d) [60,61]. Five different compositions with Hf:Ti ratios in the films (100:0), (42:58), (27:73), (12:88), (0:100) have been investigated. The pure Hf-silicate ($Hf_{0.5}Si_{0.5}O_2$) (Fig. 23a) exhibits symmetrical *I-V* curves and conduction mechanisms suggesting deposition of single layers without formation of a significant interfacial layer. This also shows that the asymmetry of the band diagram does not influence the conduction mechanism, hence it is mostly bulk-limited. It is found that the conduction is governed by two different processes – PF emission dominates at lower fields, whereas FAT is the more probable process at higher fields. The trap level ϕ_t evaluated in both processes and both polarities is at 0.65-0.7 eV below the CB of dielectric (inset Fig. 23a). At T>100 °C for positive polarity another trap level ϕ_t~1.1 eV is also observed. This trap has been found to dominate also the PF conduction in Hf-silicate layers with larger Hf content ($Hf_{0.86}Si_{0.14}O_2$) [62]. The layers containing both Hf and Ti in significant amounts (Hf:Ti (42:58) and Hf:Ti

(27:73)) reveal a strong gate polarity asymmetry of the conduction process (Fig.3b,c). At negative polarity PF emission is again the dominating mechanism. However, two trap levels located at 0.7 eV and 0.9 eV below the CB of dielectric (insets Fig. 23b,c) participate in the conduction process. As with the increase of the Ti content the conduction through the 0.9 eV level prevails, this trap has been assigned to Ti-bonds. The later theoretical calculations of Muñoz-Ramo et al. [63] have indeed confirmed the existence of a 0.9 eV state caused by Ti incorporation into HfO layers. Therefore, these states are intrinsic traps related to the inherent electronic structure of the HfTiO dielectric. The analysis of the curves has also revealed that two phenomena give rise to the asymmetry. The first one is the enhanced trapping of negative charge near the Si/dielectric interface which modifies the field, hence the current. A significant trapping of negative charge occurs in the two samples at low positive voltages and lower temperatures. The trapped charge exists along the whole dielectric film and with the increase of Ti content its centroid moves farther away from the dielectric/Si interface. Here, the distinct difference between the traps participating in the conduction process and those causing asymmetry of the *I-V* curves should be mentioned. The former ones serve only as stepping sites for the carriers (i. e., the electrons are trapped there and released immediately thereafter). The later ones are states in which the carrier is trapped longer and could be detrapped at increased voltage and/or temperature. The asymmetry of electron conduction in the films cannot be explained only by charge trapping especially for the Hf:Ti (27:73) sample. A formation of an interfacial layer with a composition and/or structure different from the bulk film is also involved for the interpretation of the obtained results. It is suggested that the two phenomena (charge trapping and formation of a double layer structure) are manifestations of one and the same structural process, namely separation of phases and formation of TiO_2, HfO_2, and SiO_2 islands in the film. Depending on the degree of phase separation, these islands can act as trapping centers that only modify the Poole-Frenkel emission in the layer (Hf:Ti (42:58)) or can form a separate layer, in this way, causing a real asymmetry of the conduction process (Hf:Ti (27:73)). The conduction in the sample with the lowest Hf content (Hf:Ti(12:88)) (Fig. 23d) and the pure Ti-silicate (not shown) could not be fitted by any of the commonly considered conduction mechanisms. The low temperature (down to -193 °C) J-V measurements have revealed the participation of soft-optical phonons with an energy of ~20 meV in the conduction process and it was concluded that it is governed by a phonon-assisted tunneling between localized states (i.e. the current obeys the relation $J \sim \exp(A/E^{1/4})$ [65]) (insets Fig. 23d). The obvious consequence of this kind of process is that the electrons do not enter the conduction band of dielectric and the conduction takes place within the band gap. Another implication is that the conduction is governed by the intrinsic properties of the layers. The finding that soft optical phonons impact substantially the conduction gives some hints about the structural status of the films as the phonon modes depend on crystalline (amorphous) structure and local bonding [60,61]. The substantial contribution of the soft optical phonons to the intrinsic properties of HfTiO layers has been confirmed also by theoretical calculations [63] revealing that the increase in permittivity mainly originates from the changes in phonon spectrum induced by the presence of Ti.

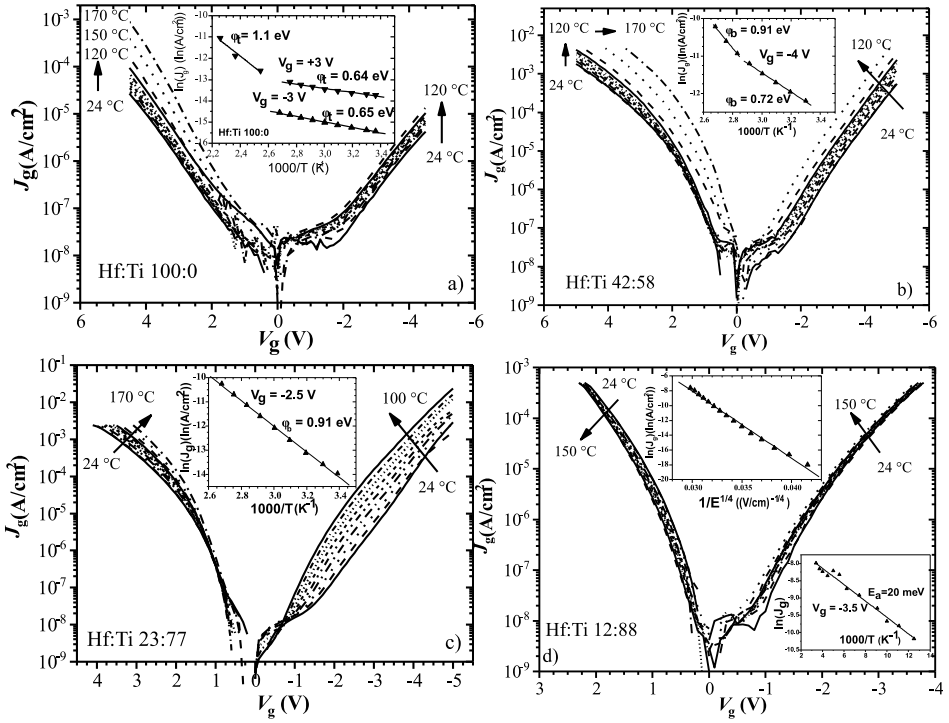

Fig. 23 Temperature dependent *J-V* curves of Al/Ti/HfTiSiO/*p*-Si structures with different dielectric layer compositions: a) Hf:Ti (100:0), b) Hf:Ti (42:58), and c) Hf:Ti (27:73); the insets show the Arrhenius plot of the current and the respective trap energy levels. d) Hf:Ti (12:88); the insets represent the Arrhenius plot of the current and *J-V* curves in phonon-assisted tunneling coordinates. All *J-V* characteristics in inversion are measured under illumination to ensure a sufficient generation of minority carriers. [64].

Effect of the top (gate) metal electrode

The influence of the gate electrode material on the leakage currents and conduction mechanisms in high-*k* dielectric stacks is of significant interest. Since the implementation of high-*k* dielectrics in microelectronics devices inculcate abandoning the poly-Si gates in order to avoid the creation of SiO_x interfacial layers compromising the overall capacitance, the gate material have to be carefully selected. Generally, the choice of gate metal is determined of its work function, as the higher work function will result in higher barrier height between the gate electrode and dielectric and hence lower leakage currents are envisaged. It turned out, however, that metal electrodes could also react with the underlying high-*k* film generating additional traps e.g. oxygen vacancies in the high-*k* [66]. In addition, the process of gate deposition has to be considered carefully, as it can also introduce defects in the dielectric and modify severely leakage and conduction mechanisms.

The effect of the metal gate on the conduction mechanisms is illustrated by the results obtain for Ta_2O_5 with Al, W and TiN gate electrode MIS capacitors. Two types of Ta_2O_5 layers were studied: reactively sputtered, and thermally oxidized Ta_2O_5 [67,68].

In case of sputtered Ta_2O_5 Al-gated structures exhibit highest leakage currents (Fig. 24).

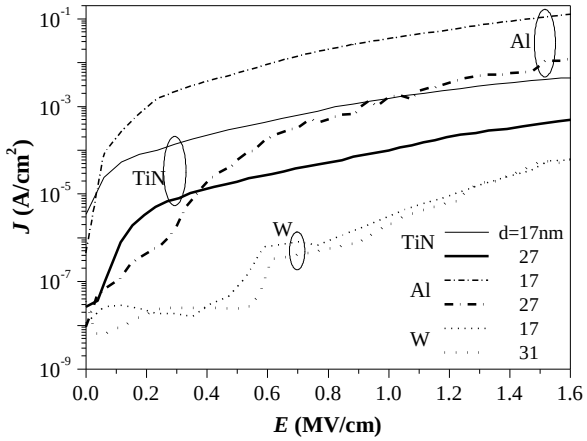

Fig. 24 *J-E* dependence at negative gate voltage for MOS capacitors two thickness of Ta_2O_5 and different gate electrodes [67].

Despite the higher work function (4.95 eV) capacitors with TiN electrodes were leakier than W-gated ones (4.55 eV was assumed as W work function). This behavior was attributed to a lowering of the barrier height at TiN/Ta_2O_5 interface, as a result of accumulation of radiation defects during electrode deposition. The conduction analysis showed that the current in the investigated capacitors is generally dominated by bulk limited conduction. PF effect governs the current in Al and W gated capacitors. Fig. 25 represents leakage characteristics in PF (a) and Schottky (b) plots. The dominant mechanism was defined by the level of agreement between k_r and their refractive index. The ellipsometry determined values of n were ~2.2, without a clear dependence on Ta_2O_5 thickness, hence the corresponding value of k_r is ~ 4.8. J of capacitors with W electrode is almost independent of E in the low field region (< 0.6MV/cm) suggesting a presence of transient currents. At higher fields (0.8–1.6MV/cm) the *J–E* curves are well fitted by a modified PF mechanism (with r=1.4) in case of 17 nm films and normal PF for the thicker (31 nm) ones indicating that they contain fewer traps. Al electroded structures are characterized with two regions: a low field region (~0.1–0.8 MV/cm) in which the conduction can be attributed to Schottky emission (Fig. 25b) although the obtained from the fit k_r values only roughly agree with ellipsometrically-measured refractive index. The conductivity in the second region can be described by the modified PF effect, (Fig. 25a) with r ≈ 2 with a weak trend of decreasing of r upon the increase of d. Neither the PF effect nor the Schottky emission can be invoked to explain the conduction for TiN capacitors (the values of k_r and r extracted from Schottky as well as PF plots do not agree with n). The $J(V)$ dependence (Fig. 26) at low voltages are linear, indicating Ohmic behavior, suggesting hopping conduction [69]. At applied $|V| > 0.5$ V the current becomes proportional to V^2 characteristic of space charge limited current. This

behavior is typical of dielectrics with substantial amount of shallow defects which affect the electric field in the film by charge carriers trapping.

Based on the results, it can be concluded that the type of the gate electrode affects the dominant conduction mechanism in reactively sputtered Ta_2O_5 layers on Si. The observed high leakage current for Al/Ta_2O_5 is a result from both lower barrier height and the larger defect density in Ta_2O_5. The former could be additionally reduced by a defects generation at the Al/Ta_2O_5 interface due to the reaction between Al and Ta_2O_5 causing appearance of thermionic emission in these capacitors [66,67,70]. The *J–V* behavior of TiN capacitors and corresponding conduction mechanisms is a manifestation of electrode deposition induced radiation defects affecting in some extend the electrical properties.

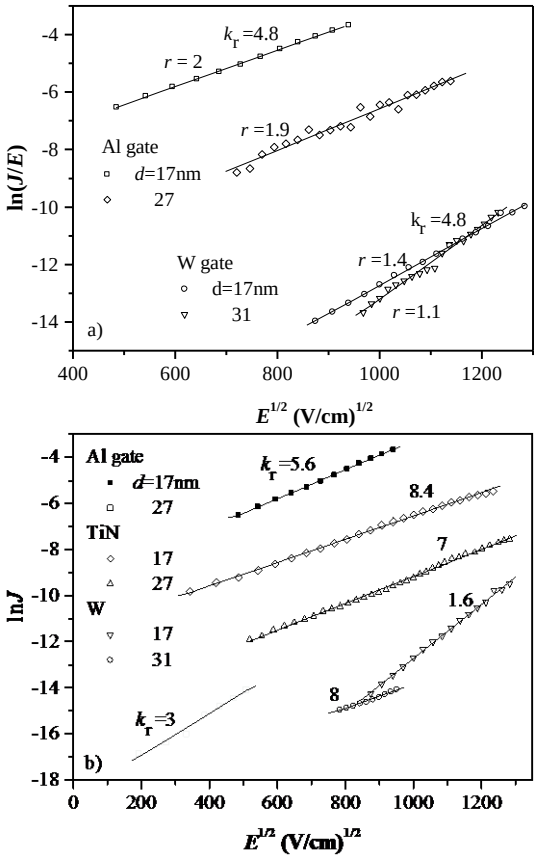

Fig. 25 *J–V* (forward bias) curves of capacitors with sputtered Ta_2O_5 and different gate electrodes in a Poole-Frenkel plot (a) and Schottky plot (b) [67].

The obtained results for MIS capacitors with thermal Ta_2O_5 and the same metal electrodes (Al, W and TiN) are in general agreement with the data for sputtered Ta_2O_5 [67]. The lowest leakage corresponds to W-gated capacitors, although in this case the conduction mechanism was not identified. Contrary to the structures with sputtered Ta_2O_5 highest *J* in

thermal Ta_2O_5 was observed for TiN electrodes, and the current of the capacitors with Al and TiN gates was substantially higher (up to 8 orders of magnitude) than *J* of W ones. The reason for such behavior was attributed to the possible reaction between Ta_2O_5 and Al or TiN electrodes producing near the gate interface AlO_x or TiO_x accompanied with unwanted traps probably in form of oxygen vacancies. The leakage characteristics of structures with Al and TiN electrodes in PF and Schottky plots are presented in Fig. 26. A nearly normal PF effect (r = 1.1 at k_r = 4.8) dominates the current at applied field of 0.3 to 1.7 MV/cm for the samples with Al electrode; Schottky conduction can be ruled out as evidenced in Fig 26b. PF effect can also be invoked for TiN gates at low electric fields (0.06 to 0.5 MV/cm). The obtained compensation factor is 1.2 close to the value proposed for normal PF. Hence, thermal Ta_2O_5 exhibits much lower (or negligible) density of compensating centers. The electrode material and deposition conditions only slightly alter the density of compensation traps causing small variations of degree of compensation. At higher fields the slope of PF plot is about 2.5 which is not fully consistent with the PF theory. In this field range J is described reasonably well by Schottky emission as the obtained from the plot value of k_r is in accordance with ellipsometrically determined refractive index.

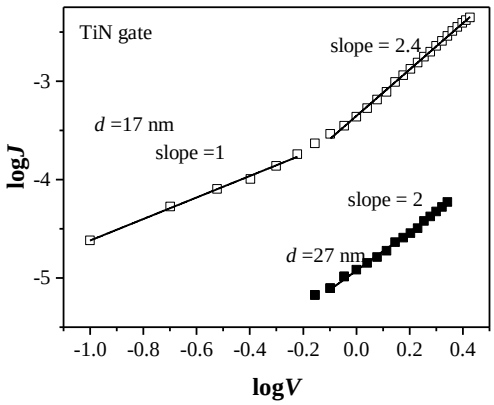

Fig. 26 logJ vs. logV for TiN/sputtered Ta_2O_5/Si capacitors [67].

This change of the mechanism from bulk (low and middle fields) to electrode limited (high fields) is strange and at a first glance it is not consistent with the indication for a noticeable generation of defects during TiN deposition. This behavior can be attributed to the quality of the top electrode-interface region itself (in one case electrons tunnel from the gate into the traps located close to/in this region and in another case they overcome the gate barrier by Schottky emission) defined by the density and energy distribution of the traps created during gate deposition. If the trap concentration close to the electrode is small the electrons could not tunnel through them in Ta_2O_5 conduction band. In this case Schottky emission is more relevant at high fields; especially for TiN case this means that the rf sputter-induced traps are not basically in the form of traps at the electrode but rather of interface states at Si with high density, as indicated by the *C–V* data. It should be mentioned however, that although *r* is slightly higher than theoretical limit of 2 in the high-filed region for TiN capacitors, the overall form of the PF plot is consistent with the

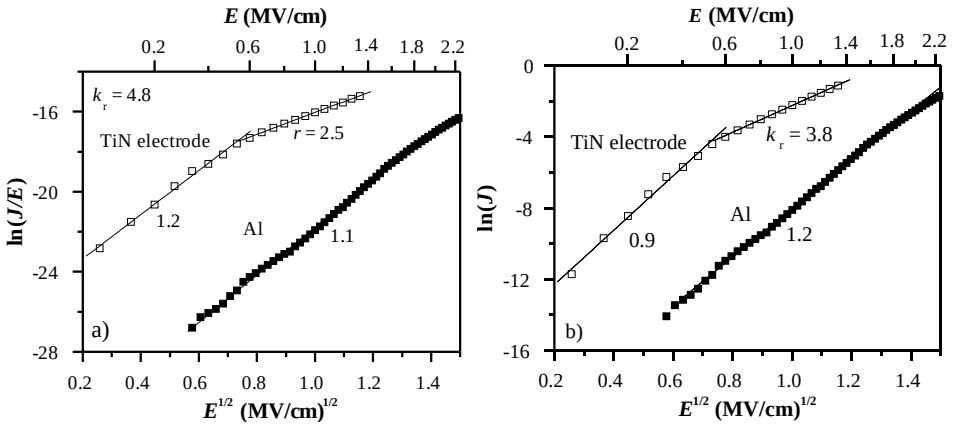

Fig. 26 (a) Poole–Frenkel and (b) Schottky plot of *I–V* characteristics for TiN and Al-electroded capacitors with thermal Ta_2O_5, d = 15 nm [68].

predicted in [16] one, suggesting a translation from r=1 to r=2 with the increase of E as a result of the growth of the electron density in the conduction band during the voltage ramp and change of inequity between the free electrons and donor and compensating traps. The observed slightly higher r may be a result from some uncertainty in the electric field determination typical for the structures with high-k dielectrics due to their double–layered nature and charge trapping. Moreover, the suggestion that conduction is governed by bulk-limited mechanism is further supported by the absence of a well pronounced effect of the gate material in accordance with its work function, although a special study of the work function especially of TiN deposited under conditions used here was not performed and the possibility that it differs from the literature values cannot be excluded.

4. CONCLUSION

In conclusion, a big diversity of conduction mechanisms - Poole–Frenkel emission, field-assisted tunneling, trap-assisted tunneling, phonon-assisted tunneling, etc., is demonstrated to operate in high-k dielectric materials. It is shown that by performing a detailed study and analysis of conduction mechanisms through metal gate/high-k dielectric stacks it is possible to obtain valuable information about the trap parameters as well as some stack parameters and structural alterations in these structures. It is also demonstrated that one and the same trap could mediate different conduction mechanisms in a given high-k dielectric depending on the specific stack parameters and measurement conditions. The doping/mixing of high-k dielectrics is revealed as an effective approach to change the energy location of traps in the bandgap of dielectric as well as their density in this way also changing the dominant conduction mechanism, hence electrical behavior of structures. The results also imply that in most of the cases investigated the oxygen vacancy is the main transport site

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