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EFFECTS OF PULSED NEGATIVE BIAS TEMPERATURE STRESSING IN P-CHANNEL POWER VDMOSFETS

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Abstract. *Our recent research of the effects of pulsed bias NBT stressing in p-channel power VDMOSFETs is reviewed in this paper. The reduced degradation normally observed under the pulsed stress bias conditions is discussed in terms of the dynamic recovery effects, which are further assessed by varying the duty cycle ratio and frequency of the pulsed stress voltage. The results are analyzed in terms of the effects on device lifetime as well. A tendency of stress induced degradation to decrease with lowering the duty cycle and/or increasing the frequency of the pulsed stress voltage, which leads to the increase in device lifetime, is explained in terms of enhanced dynamic recovery effects.*

Key words: VDMOSFET, NBTI, pulsed bias stress, threshold voltage, lifetime

1. INTRODUCTION

Negative bias temperature instability (NBTI) has been widely recognized as one of the crucial reliability issues in state-of-the art CMOS technology. Specifically, p-channel devices exposed to stress with negative gate bias at increased temperatures are susceptible to threshold voltage shift due to the complex physical mechanisms involving generation of bulk oxide charge and interface traps [1]-[6]. Magnitude of the observed shift strongly depends on stress parameters, such as the gate voltage, temperature, and stress time.

Most of the recent NBTI studies have been done on devices with very thin (less than few nanometres) gate oxide films, including SiO_2, SiON or high-k [1]-[6]. However, there is still high interest in ultra-thick oxides owing to widespread use of MOS technologies for the realisation of power devices. The electric fields and temperatures typical for NBT stress can be approached during the routine operation of power MOSFETs in many applications [7], so the investigation of NBTI in these devices, which may have gate oxide thickness ranging from several tens to 100 nm or even more, is of importance as

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well. Owing to its superior switching characteristics which enable operation in a megahertz frequency range, power VDMOSFET (Vertical Double Diffused MOSFET) is an attractive device for application in high-frequency switching power supplies, home appliances and automotive, industrial and military electronics [8], [9]. In these applications gate bias applied during the operation switches between the "high" and "low" voltage levels, thus creating the pulsed stress conditions. Earlier investigations have shown that the pulsed (also referred to as AC) NBT stress creates less significant degradation than the static (DC) stress owing to a dynamic recovery effect (a part of degradation created by the preceding stress voltage pulse is neutralized and/or annealed during the fraction of period corresponding to the "low" level of the pulsed stress voltage and has to be restored upon arrival of the next voltage pulse) [10]-[14]. Accordingly, the lifetime predictions based on static NBT stress [15], [16], where the transistor was continuously kept "on", might be wrong, and it is thus important to estimate device lifetime under the pulsed NBT stress conditions. This paper provides a review of our recent research of the effects of pulsed bias NBT stressing in p-channel power VDMOSFETs [17]-[20]. The dynamic recovery effects are assessed by varying the duty cycle and frequency of the pulsed stress voltage, and the results are further analyzed in terms of the effects on device lifetime.

2. Results and Discussion

Devices used in this study were commercial p-channel power VDMOSFETs IRF9520 with current/voltage ratings of 6.8 A/100 V, encapsulated in TO-220 plastic cases [21]. The devices were built in standard Si-gate technology with gate oxide thickness of 100 nm, and had the initial threshold voltage, V_{T0}, about −3.6 V. Owing to the thick gate oxide, accelerated NBT stressing of these devices requires gate stress voltage amplitudes even over -40 V, which exceed capabilities of commonly used signal voltage sources [22], [23]. For that reason we have developed a specific stress and measurement system suitable for NBTI testing in power MOS devices, which includes an external amplifier between the stress voltage source unit and the device under test (DUT) [24]. The system actually includes high voltage stress circuit and the low voltage measurement circuit, which are separated by two software-controlled switches. Gate stress voltage is supplied from Tektronix AFG3102 source unit acting either as a DC source or a pulse generator, for the static and pulsed NBT stressing, respectively, while the drain and source terminals are grounded. The measurements of transfer *I-V* characteristics of DUT are done by providing the sweeping gate bias from an Agilent 6645A source unit, while a source-measure unit from Agilent 4156C semiconductor parameter analyzer is used for drain biasing and drain current measurements. All the instrumentation and the temperature inside the Heraeus HEP2 chamber are computer controlled over IEEE-488 GPIB bus. This setup provides a complete measurement of *I-V* characteristic, with gate voltage swept from −4.75 V to −2 V in −50 mV steps, in about 235 ms (including the time required to switch the circuits from stress to measurement and back), which practically means that DUT remains unstressed at least 235 ms for each interim measurement performed [24].

We have first done a preliminary experiment, in which the two sets of devices were stressed for 36 hours under the static and pulsed NBT stress conditions, respectively. For the static NBT stress, negative DC voltages in the range 35 - 45 V were applied to the gate, whereas the drain and source terminals were grounded. For the pulsed bias stress, negative

gate voltage pulses (with base level of 0 V, frequency f = 10 kHz, and duty cycle DTC = 50%) of the same magnitudes were used instead. Stressing under both static and pulsed conditions was performed at temperatures ranging from 125 to 175 °C.

Typical subthreshold transfer *I-V* characteristics of p-channel power VDMOSFETs subjected to the static and pulsed NBT stressing are shown in Fig. 1, (a) and (b), respectively. The transfer *I-V* characteristics were measured at the drain voltage value of 100 mV, so the devices were kept in the linear region of operation. During the 36 hour stress, a total of 39 interim measurements were done according to a specified timeline, but for simplicity only the initial (before stress) and final (after stress) characteristics measured at room (27 °C) and stress temperature (175 °C) are shown. As can be seen, the characteristics are being shifted along the V_{GS} axis towards the higher V_{GS} voltages as a consequence of stress-induced build-up of oxide-trapped charge. At the same time, the slope of the characteristics slightly decreases, indicating that interface traps and/or near interface oxide traps, known as border traps or switching oxide traps, are generated as well. It also can be seen that the shifts caused by the pulsed NBT stressing are smaller than those found in the case of static NBT stressing.

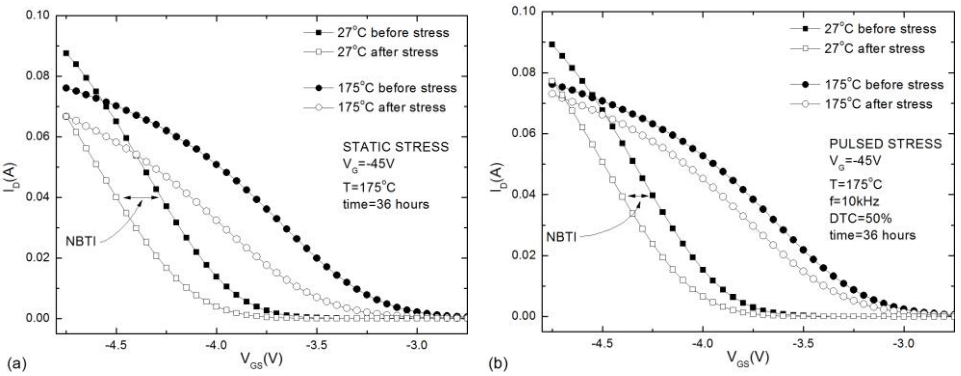

Fig. 1 Transfer *I-V* characteristics of p-channel power VDMOSFETs measured before and after (a) static and (b) pulsed (f=10kHz, DTC=50%) NBT stressing.

In line with observed shifts of transfer characteristics along the voltage axis, NBT stressing was found to cause significant threshold voltage shifts (ΔV_T). Threshold voltage values were calculated from the measured *I-V* characteristics using the second derivative method [25]. Two characteristic sets of data (for different stress voltages at 175 °C and at different temperatures for stress voltage of −45 V) for the stress-induced threshold voltage shifts found during the static and pulsed NBT stressing of IRF9520 p-channel VDMOSFETs are shown in Fig. 2. As can be seen, NBT stressing under both static and pulsed bias conditions was found to cause significant threshold voltage shifts, which were more pronounced at higher voltages and/or temperatures. In addition, it can be seen that the pulsed voltage stressing caused generally lower shifts as compared to static stressing performed at the same temperature with equal stress voltage magnitude.

The lower shifts observed in the case of the pulsed NBT stress can be explained by two factors associated with the nature of pulsed stressing itself. The first factor is assessed by taking into account that "stress time" in Fig. 2 refers to the total time, which includes fractions of the periods corresponding to both "high" and "low" levels of the pulsed gate voltage applied. However, the devices are actually stressed only during the fraction of period corresponding to the "high" voltage level (on-time), so the actual or net stress time is significantly shorter (and the resulting stress-induced threshold voltage shifts appear both slower and lower) in the cases of pulsed stress than in the case of static one. The other factor could be a partial recovery of threshold voltage during the period fractions corresponding to the "low" level of the pulsed stress voltage (off-time), which also contributes to the smaller shifts observed in the cases of pulsed bias stress. The partially recovered degradation is restored again on arrival of each new stress voltage pulse, so the phenomenon is referred to as dynamic recovery [26].

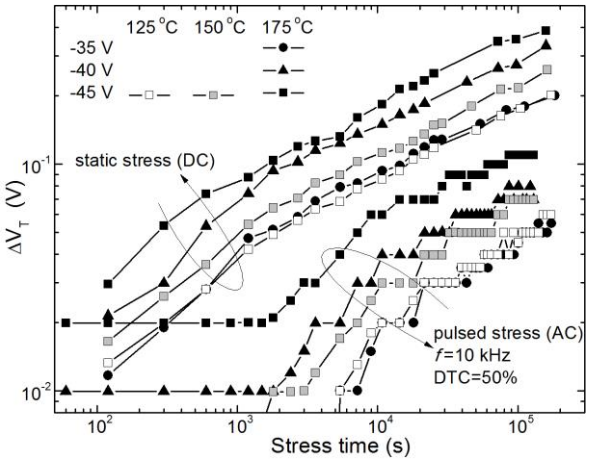

Fig. 2 Threshold voltage shifts in p-channel power VDMOSFETs during the static and pulsed (f = 10 kHz, DTC = 50%) NBT stressing.

To evaluate dynamic recovery effects during the pulsed bias stressing it is necessary to alleviate the first factor mentioned above, which is commonly done by plotting the threshold voltage shift as a function of the net stress time rather than the total time. Acordingly, Fig. 3 shows the results for threshold voltage shifts versus the net stress time, where the net stress time in the case of pulsed stressing was calculated by multiplying the total stress time with the value of duty cycle ratio (50% for the pulsed stress in this case). These results show that, for corresponding values of the net stress time, the stress induced threshold voltage shifts under the static stress remain much higher (approximately three times) than in the case of pulsed NBT stress. This clearly indicates that ΔV_T time dependencies in Figs. 2 and 3 have been affected by the partial recovery of threshold voltage during the period fractions corresponding to the "low" level of the pulsed stress voltage.

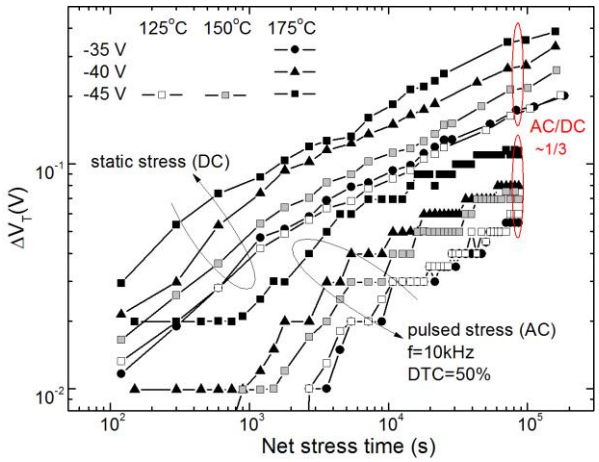

Fig. 3 Threshold voltage shifts in p-channel VDMOSFETs during the static and pulsed (f = 10 kHz, DTC = 50%) NBT stressing vs. the net stress time.

Further insight into the dynamic recovery effect was obtained by varying the duty cycle ratio and frequency of the pulsed voltage used for device stressing. The results of stressing with three different duty cycle pulses (75%, 50%, and 25%) at 10 kHz and those of static stress are shown in Fig. 4, where the net stress time in the cases of pulsed stressing was calculated by multiplying the total stress time with corresponding duty cycle value for each specific case. The overall net stress time was 6 h in all cases, and all devices were stressed with the same gate voltage magnitude (–45 V) at 175 °C. As can be seen, the NBT stress-induced threshold voltage shifts are most significant in the case of the static stress and clearly decrease with reducing the duty cycle in the cases of the pulsed bias stress. This is clear indication that dynamic recovery effects become more pronounced when the pulsed gate voltage with

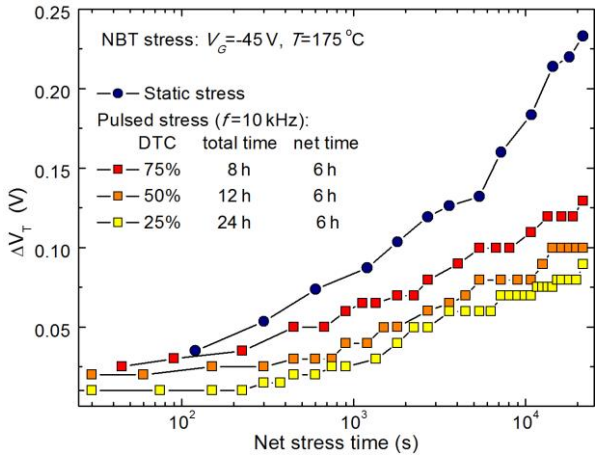

Fig. 4 Threshold voltage shifts in p-channel VDMOSFETs vs. net stress time at various duty cycles (NBT stress: V_G= –45 V, T = 175 °C, f = 10 kHz).

lower duty cycle ratio was applied. However, it should be noted that frequency remains constant, so variations in duty cycle change the ratio between the pulse and no-pulse fractions of the period: the lower duty cycle actually means shorter pulses and longer breaks in between the pulses, which further means shorter stress time and longer recovery time during each period of pulsed stress voltage applied. Accordingly, there is less time to create degradation during a single period and more time for recovery, so the overall resulting degradation found after stressing for equal net stress times tends to decrease with reducing the duty cycle. Therefore, it can be speculated that overall degradation tends to decrease with duty cycle reduction because of two combined effects: one is creation of lesser degradation because the pulses are getting shorter, while the other effect can be identified as the enhanced dynamic recovery because the period fractions between the two pulses are getting longer.

Threshold voltage shifts observed in devices stressed with three different frequency pulses (1, 10 and 100 kHz) in comparison with those obtained by static stress are shown in Fig. 5. All devices were stressed with the same gate voltage magnitude (−45 V) at 175 °C, and the overall net stress time was 6 h in all cases again. A duty cycle was kept at 50% for the pulsed stressing at all frequencies, so the net stress time in these cases was equal to a half of the total stress time. Again, the stress-induced threshold voltage shifts are most significant in the case of the static stress, and it is interesting to note that they clearly decrease with increasing the frequency in the cases of the pulsed bias stress. So, the dynamic recovery effects seem to become more pronounced with increasing the frequency of the gate voltage applied, even though the change of frequency at constant duty cycle practically does not affect the ratio between the pulse and no-pulse fractions of the period at all. However, the increase in frequency means that the pulses themselves and the fractions of period between the pulses simultaneously become shorter, which further means that there is less time to create degradation and also less time for recovery during each period of the pulsed voltage applied. Accordingly, one may expect the resulting degradation would be nearly independent of frequency, as reported in [27], [28], but in our case degradation apparently decreases with

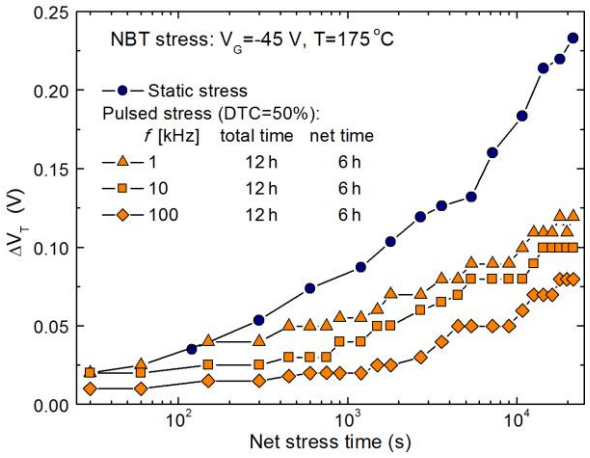

Fig. 5 Threshold voltage shifts in p-channel VDMOSFETs vs. net stress time at various frequencies (NBT stress: V_G=−45 V, T=175°C, DTC=50%).

increasing the frequency, as reported more recently in [29]. The advanced measurement techniques for NBTI characterization have been developed rather recently, which might be the reason for inconsistency of the data reported here and in [29] with those found in less recent publications [27], [28]. A possible explanation for why the degradation decreases with increasing the frequency could be as follows. The pulses at low frequencies are long enough to allow for creation of rather significant amount of the slow and/or non-recoverable component of degradation, which is hardly removed in the fraction of period between the pulses. The amount of this component decreases at higher frequencies, while that of the fast component increases, and the latter is more easily removed even though the fraction of period between the pulses becomes shorter. As a result, the dynamic recovery effects become more pronounced and overall degradation tends to decrease with increasing the frequency.

NBTI can put serious limit to a device lifetime, so one of the main goals of our NBTI studies was to estimate the normal operation lifetime of investigated p-channel power VDMOSFETs by using the experimental data obtained under the accelerated NBT stress conditions. Considering the above differences in the observed effects between the static and pulsed NBT stressing, the predictions based on the results of static NBT stressing [15], [16] may underestimate the lifetime, so the proper approach is to assess the lifetime under the pulsed NBT stress conditions, which are closer to those met by devices in real applications. Our experimental devices were the power transistors, so we could assume maximum normal bias and temperature to be, for example V_G = -20 V and T = 100 ^{o}C. Either of several device electrical parameters, such as threshold voltage, transconductance, or drain current, can be used as degradation monitor for the lifetime estimation [30], [31]. Threshold voltage is widely accepted as a well-suited parameter, so in our studies we have used the experimental results for the NBT stress-induced ΔV_T to estimate the device lifetime in practical operation.

The procedure of lifetime estimation consists of two steps: experimental values of the lifetime are extracted first, and these values are then used for extrapolation to normal conditions. Experimental lifetime is defined as the stress time required for the stress-induced ΔV_T to reach some predetermined value, which is called failure criterion (FC). In our case we defined FC as the threshold voltage shift of 50 mV. The extraction of experimental lifetime values from our data for stress voltage magnitude V_G = -45 V at different temperatures is illustrated in Fig. 6. As can be seen, lifetime values extracted from the static NBT stress data (τ1, τ2, τ3) are significantly shorter than those extracted from the corresponding pulsed stress data (τ4, τ5, τ6).

There are several well-established models for extrapolation along the voltage or electric field axis, such as "V_G", "$1/V_G$" and "power-law" models [32], [33], which are based on corresponding degradation models for the threshold voltage shifts. The "$1/V_G$" and other models for extrapolation along the voltage or electric field axis can be used to estimate the device lifetime and ten year operation voltage (the maximum operation voltage providing 10 years of device operation without failure) only at temperatures applied during accelerated stressing, which are generally higher than actual temperatures found in device normal operation mode. Estimates obtained by these models are very useful as the worst case expectations, but it could be even more useful if possible to have

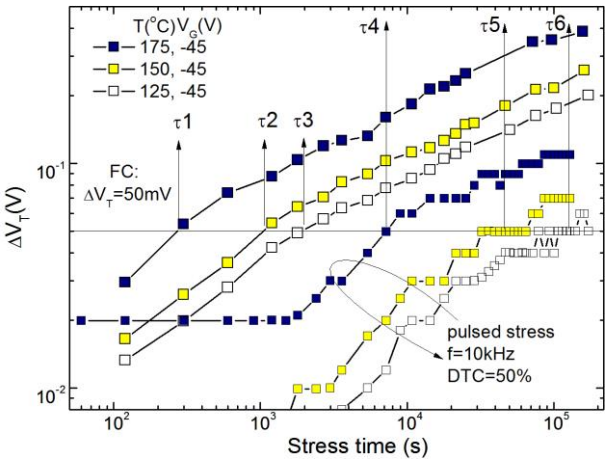

Fig. 6 Extraction of experimental lifetime from the threshold voltage shift time dependencies recorded during the NBT stressing with gate voltage V_G = - 45 V at different temperatures.

lifetime estimates for normal operation temperatures. Trying to resolve this issue, we have proposed extrapolation along the temperature axis [34]. A model for this extrapolation can be derived from any of several degradation models for NBT stress-induced threshold voltage shifts, which all include the Arrhenius temperature acceleration factor, and can be expressed as [34]:

$$\tau = A \cdot \exp(B/T), \tag{1}$$

where A and B are the fitting parameters taken from the initial degradation model. The above expression has the same mathematical form as the one describing the standard "$1/V_G$" model, so the proposed model was called "1/T" model. The "1/T" model requires experimental lifetime values extracted from the data for NBT stressing performed with the same voltage magnitude at several different temperatures, such as those plotted in Fig. 6. The lifetime estimation by means of this model is illustrated in Fig. 7. Only extrapolation to T = 100 °C (which seems rather realistic for operation of power devices) is shown, but the procedure can be used to estimate the lifetime by extrapolation to any other reasonable operation temperature. In analogy with the "$1/V_G$" model, extrapolation procedure employed by the "1/T" model additionally allows us to estimate a new reliability parameter, which is called a "ten year operation temperature", T_{10Y}, and is defined as maximum temperature that allows 10 years of device operation with stress-induced ΔV_T below FC. As can be seen in Fig. 7, "1/T" model yields significant differences between the effects of static and pulsed NBT stress. The lifetime at 100 °C is more than two orders of magnitude higher under the pulsed bias conditions (lifetime^P) than under the static ones (lifetime^S). Also, the ten year operation temperature is about 25 °C higher in the case of exposure to pulsed voltage stressing (T^P_{10Y}) than in the case of static one (T^S_{10Y}). These observations are completely in line with those obtained by means of "$1/V_G$" model [18].

An expectation based on the above results is that the use of lower duty cycle gate voltage pulses for switching (which of course has to conform to specific requirements of

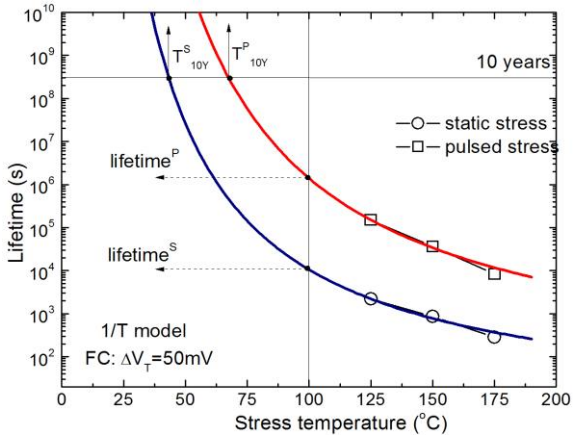

Fig. 7 Extrapolation to normal operation temperature by means of "1/T" model to estimate the lifetime and ten year operation temperature in p-channel power VDMOSFETs subjected to static and pulsed NBT stressing.

the circuit the investigated devices are to be used in) could lead to a longer device lifetime. This expectation is confirmed by the data in Fig. 8, which shows the NBT stress-induced threshold voltage shifts in devices subjected to the static and pulsed stressing under different duty cycles at f = 10 kHz. As can be seen, the pulsed NBT stress caused significant threshold voltage shifts, which were more pronounced at higher duty cycles, but still lower than those caused by the static stress. The figure additionally illustrates that stress time required for stress-induced threshold shift to reach the predetermined value of FC increases with decreasing the duty cycle, so the experimental values of device lifetime increase with decreasing the duty cycle as well ($\tau 1_S < \tau 1_{75\%} < \tau 1_{50\%} < \tau 1_{25\%}$), and the

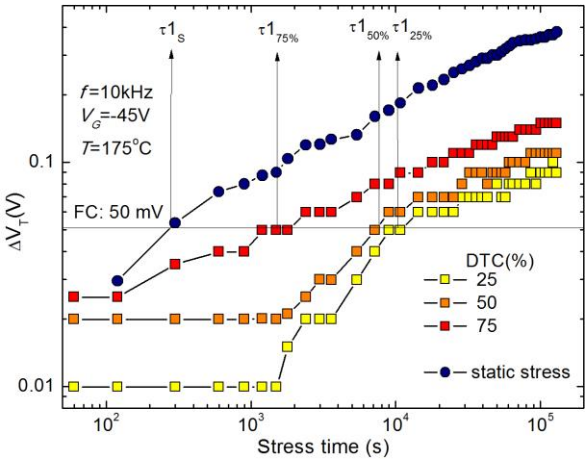

Fig. 8 Threshold voltage shifts in p-channel power VDMOSFETs subjected to the pulsed NBT stress at different duty cycles, f=10 kHz with corresponding experimental lifetime values indicated.

actual lifetime under the normal operation conditions is expected to increase likewise. This can be explained in terms of the mechanisms responsible for NBT stress-induced degradation. Threshold voltage shifts related to NBTI are known to originate from underlying buildup of oxide-trapped charge and interface traps due to stress-initiated electrochemical processes involving oxide and interface defects, holes, and various species associated with presence of hydrogen as a common impurity in MOS devices [1]-[6], [12]-[14], [35]-[37]. In the case of pulsed voltage applied to the gate, devices are sequentially subjected to stress and no-stress conditions, where the actual stress time depends on pulse frequency and duty cycle. The actual stress time apparently decreases with decreasing the duty cycle, so the resulting degradation associated with stress-induced generation of oxide-trapped charge and interface traps must decrease as well, whereas the device lifetime consequently increases.

3. CONCLUSION

The results of our recent research of the effects of pulsed bias NBT stressing in p-channel power VDMOSFETs have been reviewed in this paper. The reduced degradation normally observed under the pulsed stress bias conditions has been discussed in terms of the dynamic recovery effects, which are further assessed by varying the duty cycle ratio and frequency of the pulsed stress voltage. The stress-induced degradation was shown to decrease with reducing the duty cycle and increasing the frequency of the pulsed stress voltage. The results were analyzed in terms of the effects on device lifetime as well. A tendency of the stress induced degradation to decrease with lowering the duty cycle and/or increasing the frequency, which has resulted into the increase in device lifetime, was explained in terms of the enhanced dynamic recovery effects.

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REFERENCES

[1] D.K. Schroder, J.A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing", *J. Appl. Phys*., vol. 94, pp. 1–18, 2003.
[2] J.H. Stathis, S. Zafar, "The negative bias temperature instability in MOS devices: A Review", Microelectron. *Reliab.*, vol. 46, pp. 270–286, 2006.
[3] S. Ogawa, M. Shimaya, N. Shiono, "Interface-trap generation at ultrathin SiO2 (4–6 nm)-Si interfaces during negative-bias temperature aging", *J. Appl. Phys*., vol. 77, pp. 1137–1148, 1995.
[4] V. Huard, M. Denais, C. Parthasarathy, "NBTI degradation: From physical mechanisms to modeling", *Microelectron. Reliab*., vol. 46, pp. 1–23, 2006.
[5] M.A. Alam, S.A. Mahapatra, "A comprehensive model of PMOS NBTI degradation", *Microelectron. Reliab*., vol. 45, pp. 71–81, 2005.
[6] S. Mahapatra, N. Goel, S. Desai, S. Gupta, B. Jose, S. Mukhopadhyay, K. Joshi, A. Jain, A.E. Islam, M.A. Alam, "A Comparative Study of Different Physics-Based NBTI Models", *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 901–916, 2013.
[7] S. Gamerith, M. Pölzl, "Negative bias temperature stress in low voltage p-channel DMOS transistors and role of nitrogen", *Microelectron. Reliab*., vol. 42, pp. 1439–1443, 2002.

[8] B.J. Baliga, Fundamentals of Semiconductor Power Devices, New York: Springer, 2008.
[9] V. Benda, J. Gowar, D.A. Grant, *Power Semiconductor Devices*, New York: John Wiley, 1999.
[10] M.A. Alam, "A Critical Examination of the Mechanisms of Dynamic NBTI for PMOSFETs", in IEDM Techn. Dig., 2003, pp. 345-348.
[11] R. Fernández, B. Kaczer, A. Nackaerts, S. Demuynck, R. Rodríguez, M. Nafria, G. Groeseneken, "AC NBTI studied in the 1 Hz – 2 GHZ range on dedicated on-chip CMOS circuits", In IEDM Techn. Dig., 2006, pp. 1-4.
[12] S. Mahapatra, A. E. Islam, S. Deora, V. D. Maheta, K. Joshi, A. Jain, M. A. Alam, "A Critical Re-evaluation of the Usefulness of R-D Framework in Predicting NBTI Stress and Recovery", in Proc. International Reliability Physics Symposium (IRPS), 2011, pp. 614-623.
[13] H. Reisinger, T. Grasser, K. Ermisch, H. Nielen, W. Gustin, C. Schlünder, "Understanding and Modeling AC BTI", in Proc. International Reliability Physics Symposium (IRPS), 2011, pp. 597-603.
[14] S. Desai, S. Mukhopadhyay, N. Goel, N. Nanaware, B. Jose, K. Joshi, S. Mahapatra, "A Comprehensive AC/DC NBTI Model: Stress, Recovery, Frequency, Duty Cycle and Process Dependence", In Proc. International Reliability Physics Symposium (IRPS), 2013, pp. XT.2.1 – XT.2.11.
[15] D. Danković, I. Manić, S. Djorić-Veljković, V. Davidović, S. Golubović, N. Stojadinović, "NBT stress-induced degradation and lifetime estimation in p-channel power VDMOSFETs", *Microelectron. Reliab.* vol. 46, pp. 1828-1833, 2006.
[16] N. Stojadinović, D. Danković, I. Manić, V. Davidović, S. Djorić-Veljković, S. Golubović, "Impact of negative bias temperature instabilities on lifetime in p-channel power VDMOSFETs", In Proc. TELSIKS 2007 Conf., 2007, pp. 275-282.
[17] N. Stojadinović, D. Danković, I. Manić, A. Prijić, V. Davidović, S. Djorić-Veljković, S. Golubović, Z. Prijić, "Threshold voltage instabilities in p-channel power VDMOSFETs under pulsed NBT stress", *Microelectron. Reliab.* vol. 50, pp. 1278-1282, 2010.
[18] I. Manić, D. Danković, A. Prijić, V. Davidović, S. Djorić-Veljković, S. Golubović, Z. Prijić, N. Stojadinović, "NBTI related degradation and lifetime estimation in p-channel power VDMOSFETs under the static and pulsed NBT stress conditions", *Microelectron. Reliab.* vol. 51, pp. 1540-1543, 2011.
[19] D. Danković, I. Manić, V. Davidović, A. Prijić, S. Djorić-Veljković, S. Golubović, Z. Prijić, N. Stojadinović, "Lifetime estimation in NBT stressed p-channel power VDMOSFETs", *Facta Universitatis, Series: Automatic Control and Robotics*, vol. 11, pp. 15-23, 2012.
[20] I. Manić, D. Danković, A. Prijić, Z. Prijić, N. Stojadinović, "Measurement of NBTI Degradation in p-channel Power VDMOSFETs", *Informacije MIDEM, Journal of Microelectronics, Electronic Components and Materials.* vol. 44, pp. 280-287, 2014.
[21] "IRF9520N," Data sheet, International Rectifier, [Online]. Available: http://www.irf.com/product-info/datasheets/data/irf9520npbf.pdf
[22] Tektronix, Inc., "High amplitude arbitrary/function generator simplifies measurement in automotive, semiconductor, scientific and industrial applications," Application Note, [Online]. Available: http://www.tektronix.com/afg3000, 2008.
[23] Agilent Technologies Inc., "Agilent 4156C precision semiconductor parameter analyzer", Data sheet, p.5. [Online]. Available: http://www.agilent.com, 2009.
[24] A. Prijić, D. Danković, Lj. Vračar, I. Manić, Z. Prijić, N. Stojadinović, "A method for negative bias instability (NBTI) measurements on power VDMOS transistors", *Measure. Sci. and Technol*., vol.23, 085003 (8 pp.), 2012.
[25] A. Ortiz-Conde, F.-J. Garcıa Sanchez, J.J. Liou, A. Cerdeira, M. Estrada, Y. Yue, "A review of recent MOSFET threshold voltage extraction methods", *Microelectron. Reliab*., vol. 42, pp. 583–596, 2002.
[26] M.A. Alam, "A Critical Examination of the Mechanisms of Dynamic NBTI for PMOSFETs", In Technical Digest of the IEDM 2003, USA, pp. 345–348, 2003.
[27] G. Chen, M.F. Li, C.H. Ang, J.Z. Zheng, D.L. Kwong, "Dynamic NBTI of p-MOS transistors and its impact on MOSFET scaling", *IEEE Electron. Dev. Lett*., vol. 42, pp. 734–736, 2002.
[28] M.F. Li, G. Chen G, C. Shen, X.P. Wang, H.Y. Yu, Y.C Yeo et al., "Dynamic bias temperature instability in ultrathin SiO_2 and HfO_2 metal-oxide-semiconductor field effect transistor and its impact on device lifetime", *Jpn. J. Appl. Phys*., vol. 43(11B), pp. 7807–7814, 2004.
[29] T. Nigam, "Pulse-stress dependence of NBTI degradation and its impact on circuits", IEEE *Trans. Device Mater. Reliab*., vol. 9, pp. 72–78, 2008.
[30] C. Schlunder, R. Brederlow, B. Ankele, W. Gustin, K. Goser, R. Thewes, "Effects of inhomogeneous negative bias temperature stress on p-channel MOSFETs of analogue and RF circuits", *Microelectron. Reliab.*, vol. 45, pp. 39-46, 2005.

[31] S.S. Tan, T.P. Chen, C.H. Ang, L. Chan, "Mechanism of nitrogen-enhanced negative bias temperature instability in pMOSFET", *Microelectron. Reliab.*, vol. 45, pp. 19-30, 2005.

[32] M. Ershov, S. Saxena, S. Minehane, P. Clifton, M. Redford, R. Lindley, H. Karbasi, S. Graves, S. Winters, "Degradation dynamics, recovery, and characterization of negative bias temperature instability", *Microelectron. Reliab.*, vol. 45, pp. 99-105, 2005.

[33] H. Aono, E. Murakami, K. Okuyama, A. Nishida, M. Minami, Y. Ooji, K. Kubota, "Modeling of NBTI saturation effect and its impact on electric field dependence of the lifetime", *Microelectron. Reliab.*, vol. 45, pp. 1109-1114, 2005.

[34] D. Danković, I. Manić, V. Davidović, S. Djorić-Veljković, S. Golubović, N. Stojadinović, "New Approach in Estimating the Lifetime in NBT Stressed P-Channel Power VDMOSFETs", In Proc. MIEL 2008 Conference, 2008, pp. 599-602.

[35] N. Stojadinović, D. Danković, S. Djorić-Veljković, V. Davidović, I. Manić, S. Golubović, "Negative bias temperature instability mechanisms in p-channel power VDMOSFETs", *Microelectron. Reliab*., vol. 45, pp. 1343–1348, 2005.

[36] D. Danković, I. Manić, V. Davidović, S. Djorić-Veljković, S. Golubović, N. Stojadinović, "Negative bias temperature instabilities in sequentially stressed and annealed p-channel power VDMOSFETs", *Microelectron. Reliab*., vol. 47, pp. 1400–1405, 2007.

[37] I. Manić, D. Danković, S. Djorić-Veljković, V. Davidović, S. Golubović, N. Stojadinović, "Effects of low gate bias annealing in NBT stressed p-channel power VDMOSFETs", *Microelectron. Reliab*., vol. 49, pp. 1003–1007, 2009.