

FACTA UNIVERSITATIS

Series: **Electronics and Energetics** Vol. 30, N° 3, September 2017, pp. 375 - 382

DOI: 10.2298/FUEE1703375D

## MIXED MODE PERFORMANCE OF GAAS UTB-MOSFET WITH EXTRA INSULATOR REGION AND UNDOPED BURIED OXIDE REGION

Shiva Prasad Das<sup>1</sup>, Ananya Dastidar<sup>2</sup>,  
Partha Sarkar<sup>1</sup>, Sushanta K. Mohapatra<sup>3</sup>

<sup>1</sup>Department of Electronics and Communication Engineering, Centre for Advanced Post Graduate Studies, Biju Patnaik University of Technology, Odisha, India

<sup>2</sup>Department of Instrumentation and Electronics, College of Engineering and Technology, Bhubaneswar, BPUT, Odisha, India

<sup>3</sup>School of Electronics Engineering, KIIT University, Bhubaneswar, Odisha, India

**Abstract.** *Investigation of mixed mode performances for GaAs UTB-MOSFET at nanoscale regime keeping in view of “Beyond CMOS” is the current trend of semiconductor industry. Here it is proposed to modify conventional models by considering an extra Insulator Region (IR) and Undoped Buried oxide Region (UBR) to study the performance related to digital and analog/RF applications. Here a GaAs is considered as the channel material. The IR-UTB-SOI-n-MOSFET has shown promising results with respect to SS, DIBL,  $f_T$  and switching speed.*

**Key words:** *Silicon-On-Insulator, UTB MOSFET, GaAs, DIBL, Analog/RF Performance, Insulator Region.*

### 1. INTRODUCTION

In recent years, there has been a growing demand of Integrated Circuits (ICs) providing better analog/ RF applications as well as digital functionalities [1]–[3]. The Silicon-On-Insulator (SOI) technology [1], [4], [5] based Fully Depleted (FD) Silicon On Insulator MOSFETs are widely used for mixed mode application ICs as it offers sharp sub-threshold slope, high current drive, high transconductance, reduced parasitic capacitance, and absence of latch-up which are key parameters for digital applications [6]–[8]. Due to high transconductance to drain current ( $g_m/I_d$ ) ratio and low body factor, the FD-SOI-MOSFETs have been used to design low power circuits to operate at a high and low frequency as

---

Received September 17, 2016; received in revised form November 30, 2016

**Corresponding author:** Sushanta K. Mohapatra

School of Electronics Engineering, KIIT University, Bhubaneswar, Odisha, India

(E-mail: [skmctc74@gmail.com](mailto:skmctc74@gmail.com))

well as high temperature providing better performance than the conventional MOSFETs [9], [10].

The use of high electron mobility material like GaAs is promising as it has higher saturated electron velocity, higher electron mobility, allowing it to function at much higher frequencies, less noise and be operated at higher power levels than Silicon [11], [12].

Previously it has been shown by Orouji *et al.* [13] that SOI-MOSFETs with an extra Insulator Region (IR-SOI) in which the silicon active layer and drain region consists of an insulator region ( $\text{HfO}_2$ ) provides high electron reliability due to low gate leakage current and low critical electric field. The Self Heating Effect (SHE) which is one of the drawbacks of FD-SOI has been reduced by a new structure Undoped Buried Region MOSFET (UBR-MOSFET) [14].

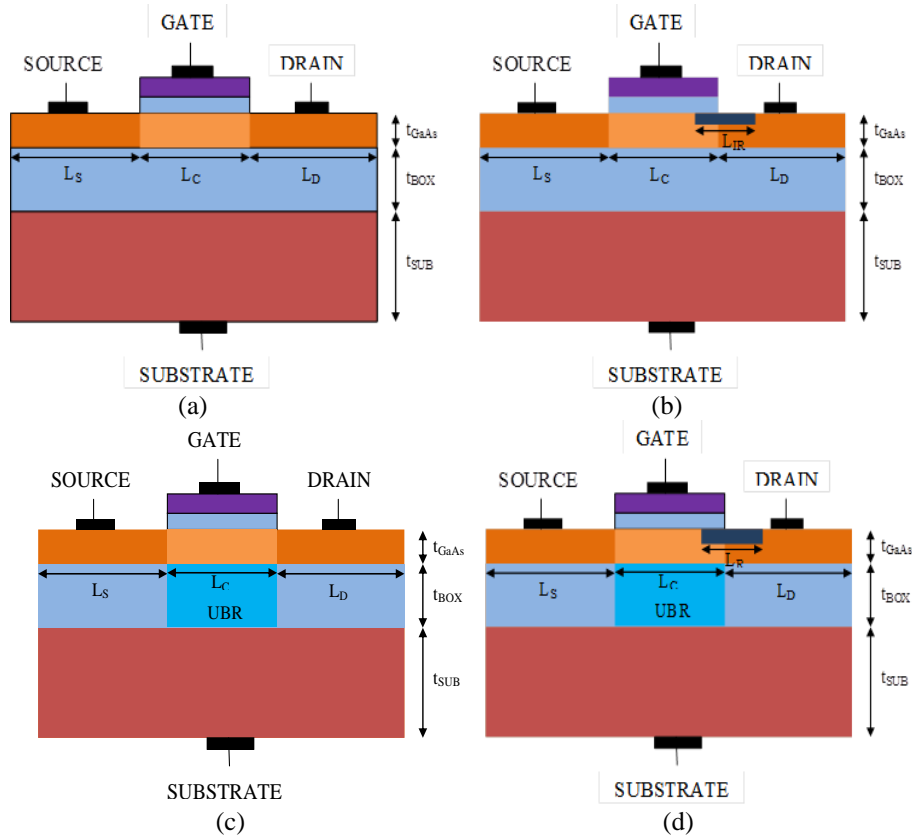
In this paper, the analog/ RF performance along with some scaling parameters of Ultra Thin Body (UTB) SOI n-channel MOSFET (UTB-SOI-n-MOSFET) has been examined along with UTB-SOI-MOSFET with extra Insulator Region (IR-UTB-SOI-n-MOSFET), UTB-n-MOSFET with Undoped Buried Region under channel (UBR-UTB-SOI-n-MOSFET) and a new structure UTB-SOI-n-MOSFET with extra insulator region and undoped buried region under channel (IR-UBR-UTB-SOI-n-MOSFET) with the help of the device simulator from SILVACO TCAD[15].

## 2. DEVICE STRUCTURE AND SIMULATION SETUP

The schematic representation of four different structures UTB-SOI-n-MOSFET, IR-UTB-SOI-n-MOSFET, UBR-UTB-SOI-n-MOSFET and IR-UBR-UTB-SOI-n-MOSFET, which was considered for the 2-D simulation is given in Fig.1. The Effective Oxide Thickness ( $EOT$ ), the gate length ( $L_G$ ), the GaAs body thickness ( $t_{\text{GaAs}}$ ), the  $\text{SiO}_2$  Buried Oxide Thickness ( $t_{\text{BOX}}$ ) and Si Substrate thickness ( $t_{\text{SUB}}$ ) have been taken of 1.1 nm, 60 nm, 10 nm, 50 nm and 100 nm respectively in all the four type of structures. The source extension ( $L_S$ ) and the drain extension ( $L_S$ ) have been taken as 70 nm each. The source and drain area are highly doped with n-type donor ions with concentration  $10^{20} / \text{cm}^3$  each to reduce the mobility degradation due to coulombs scattering. The silicon substrate is diffused with p-type acceptor ions with concentration  $10^{18} / \text{cm}^3$  and the GaAs channel region is doped with p-type acceptor ions with concentration  $10^{16} / \text{cm}^3$  to avoid threshold voltage variation[16]. The metal gate work function is set to 4.6 eV during simulation[17].

The structures are calibrated to meet the requirement of International Technology Roadmap for Semiconductors (ITRS) in 45 nm technology node [18]. The 2-D numerical device simulator [15] ATLAS is used for the simulation of the proposed structures. The drain bias is fixed to  $V_{\text{DD}} = 1.0$  V as per ITRS [19]. To study the Analog/ RF performance the simulation is carried out at the drain to source voltage  $V_{\text{DS}} = 0.5$  V (half of the supply voltage i.e.  $V_{\text{DD}}/2$ ) [20] with a variable gate to source voltage ( $V_{\text{GS}}$ ) 0 V to 1.0 V. The threshold voltage is obtained by using constant current  $I_{\text{D}} = 10^{-6}$  A/ $\mu\text{m}$ , from  $I_{\text{D}} \sim V_{\text{GS}}$  characteristic curve. In the channel region the electron and hole Shockley-Read-Hall [21],[22] generation and recombination lifetime,  $\tau_n$  and  $\tau_p$  are set to the value  $1 \times 10^{-8}$  sec each. In material models, Lombardi mobility model [23] is used which considers the effect of transverse electric fields along with doping and temperature dependent parameters

of mobility [24]. The numerical solution used here is based on the drift-diffusion approach [25]. Some other material models have also been used here like the concentration dependent (CONMOB), parallel electric field dependence (FLDMOB) which is required for measuring velocity saturation effect, Shockley-Read-Hall (SRH) and optical [15]. The Fermi-Dirac model helps to get the result close to ideal values by a Rational Chebyshev approximation [19].



**Fig. 1** Schematic Device structures (a) UTB-SOI-n-MOSFET (b) IR-UTB-SOI-n-MOSFET (c) UBR-UTB-SOI-n-MOSFET (d) IR-UBR-SOI-n-MOSFET

**Table 1** Structure notation

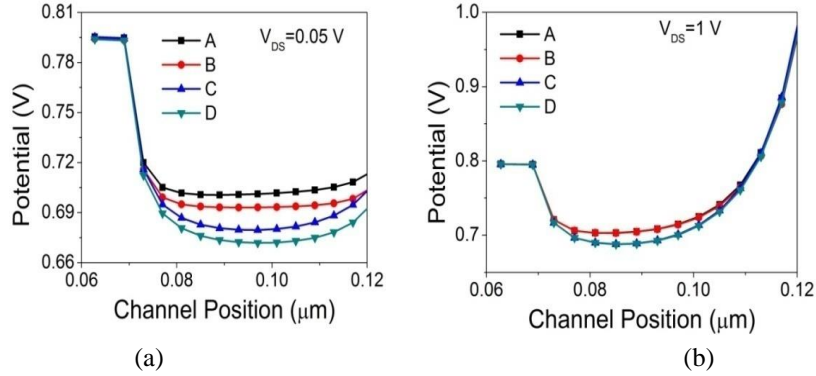
Notation used in this article	Structure
A	UTB-SOI-n-MOSFET
B	IR-UTB-SOI-n-MOSFET
C	UBR-UTB-SOI-n-MOSFET
D	IR-UBR-UTB-SOI-n-MOSFET

## 3. RESULT ANALYSIS

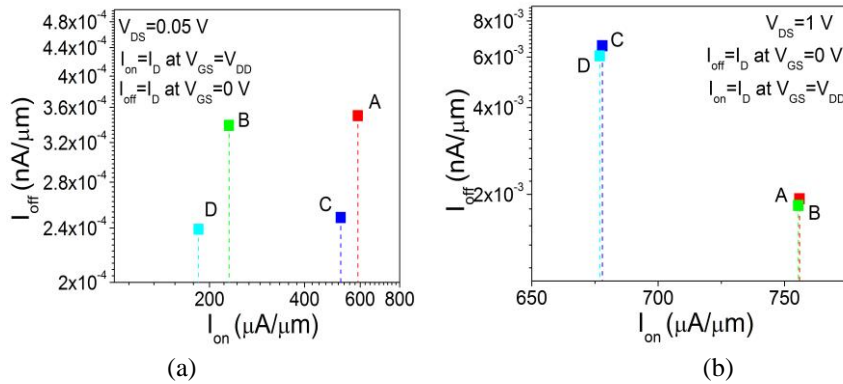
As described previously these four types of structures were simulated using 2-D numerical device simulator and the parameters like the on-state drive current ( $I_{ON}$ ), off-state leakage current ( $I_{OFF}$ ),  $I_{ON}/I_{OFF}$  ratio, threshold voltage ( $V_{th}$ ) and power dissipation variation were evaluated which are some of the factors affecting the scaling properties of the devices. The surface potential variation with respect to channel length was also observed. The RF/ Analog performance analysis was done by measuring the parameters like transconductance ( $g_m$ ), total capacitance ( $C_{Total}$ ), Q-factor and cut-off frequencies ( $f_T$ ) for the four different structures. A Sub-threshold Slope ( $SS$ ) was calculated by using the following equation [19].

$$SS(mV / dec) = \frac{\partial V_{GS}}{\partial(\log I_D)} \quad (1)$$

Another vital parameter responsible for scaling effect is the Drain Induced Barrier Lowering ( $DIBL$ ) which was also evaluated by the following equation[26].



**Fig. 2** Surface Potential Variation along channel for A, B, C and D at  $V_{GS} = 1$  V (a) at  $V_{DS} = 0.05$  V (b) at  $V_{DS} = 1$  V



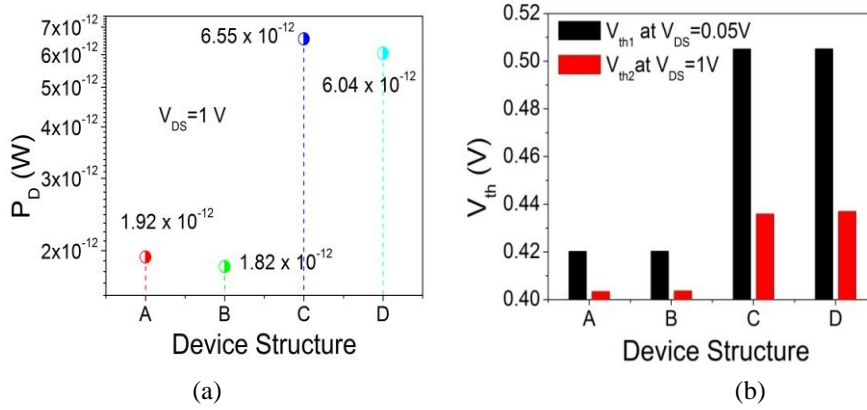
**Fig. 3**  $I_{ON}$  and  $I_{OFF}$  comparison for A, B, C and D (a) at  $V_{DS} = 0.05$  V (b) at  $V_{DS} = 1$  V

$$DIBL = \frac{V_{th1} - V_{th2}}{0.95} \quad (2)$$

Where  $V_{th1}$  and  $V_{th2}$  are threshold voltages at  $V_{DS} = 0.05$  V and  $V_{DS} = 1$  V.

Fig.2 shows the surface potential variation along the channel of the structures A, B, C and D, where Fig. 2 (a) shows the variation of surface potential along the channel for the four structures at drain to source voltage  $V_{DS} = 0.05$  V and Fig. 2 (b) shows the surface potential variation along the channel for the four structures when  $V_{DS} = 1$  V.

The trade-off between  $I_{OFF}$  and  $I_{ON}$  has been shown in the Fig. 3 for different structures. Fig. 3(a) shows the  $I_{ON}$  and  $I_{OFF}$  comparison between A, B, C and D at  $V_{DS} = 0.05$  V and Fig. 3(b) shows the  $I_{ON}$  and  $I_{OFF}$  comparison between A, B, C and D at  $V_{DS} = 1$  V. At  $V_{DS} = 0.05$  V structure C gives better  $I_{ON}/I_{OFF}$  ratio and at  $V_{DS} = 1$  V, structure B shows significant improvement in  $I_{ON}/I_{OFF}$  ratio.



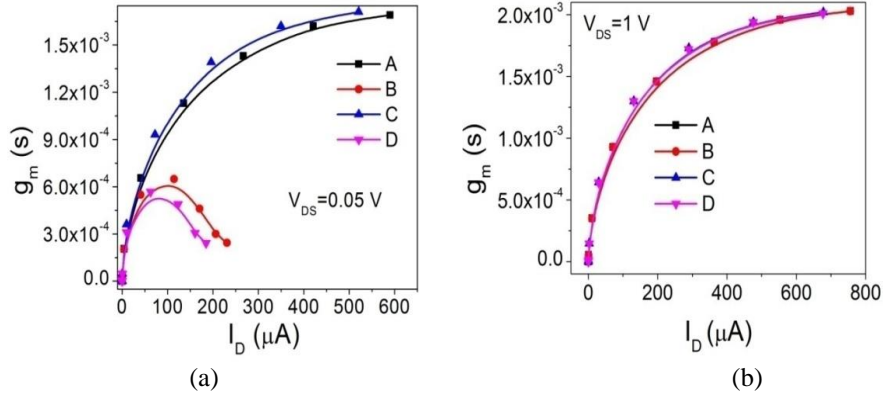
**Fig. 4** (a) Static Power Dissipation for A, B, C, and D,  
(b) Threshold Voltage Variation at  $V_{DS} = 0.05$  V and  $V_{DS} = 1$  V

In the Fig. 4(a), the static power dissipation ( $P_D = I_{OFF} \times V_{DD}$ ) [27] variation with respect to the four type of structures is presented. The structure B provides lower static power dissipation than the other three structures. The Fig. 4(b) provides the threshold voltage variation of the four structures at  $V_{DS} = 0.05$  and  $V_{DS} = 1$  V. The extracted value of threshold voltage, sub-threshold slope, DIBL and static power dissipation are tabulated for all device structures in table 2.

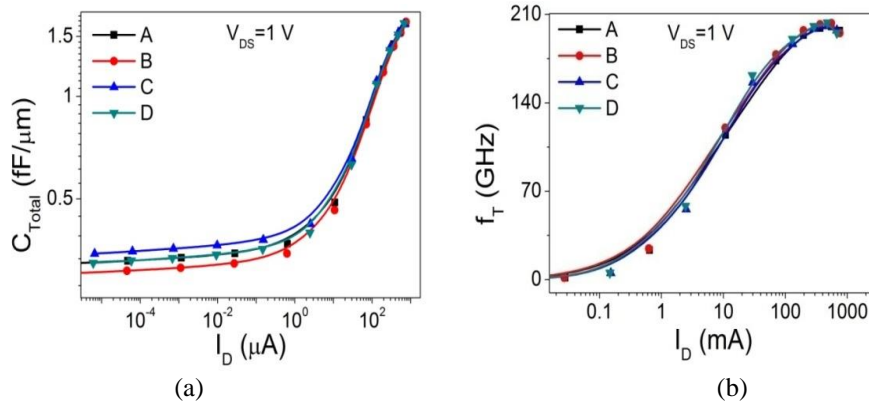
In Fig. 5, the trans-conductance i.e.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (3)$$

for different A, B, C and D has been given. The Fig. 5(a) and Fig. 5(b) show the  $g_m$  variation with  $I_D$  for the given four structures at  $V_{DS} = 0.05$  V and  $V_{DS} = 1$  V respectively.



**Fig. 5** Trans-conductance ( $g_m$ ) variation with  $I_D$  for A, B, C and D  
(a) at  $V_{DS} = 0.05$  V (b) at  $V_{DS} = 1$  V



**Fig. 6** (a) Total Capacitance ( $C_{Total}$ ) with  $I_D$  for A, B, C and D at  $V_{DS} = 1$  V  
(b) a Cut-off Frequency ( $f_T$ ) variation with  $I_D$  for A, B, C and D at  $V_{DS} = 1$  V

In Fig. 6(a), the variation of total capacitance ( $C_{Total} = C_{gd} + C_{gs}$ ) for A, B, C and D has been given at  $V_{DS} = 1$  V where  $C_{gd}$  is parasitic gate to drain capacitance and  $C_{gs}$  is the parasitic gate to source capacitance.

Another important parameter, a cutoff frequency ( $f_T$ ) has been plotted in Fig. 6(b)

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (4)$$

The  $Q$ -Factor ( $g_m/SS$ ) has been calculated for the four device structures and given in the Table 3.

**Table 2** Performance parameters-1

Structure	$V_{th1}$ (V)	$V_{th2}$ (V)	SS1 (mV/dec)	SS2 (mV/dec)	DIBL (mV/V)	$P_D$ ( $\times 10^{-12}$ W)
A	0.420	0.403	69.81	71.95	17.678	1.92
B	0.420	0.404	69.68	71.83	17.589	1.82
C	0.505	0.436	74.11	82.21	72.923	6.55
D	0.505	0.437	74.01	81.90	71.872	6.04

**Table 3** Performance parameters-2

Structure	$I_{ON1}/I_{OFF1}$ ( $\times 10^{-9}$ )	$I_{ON2}/I_{OFF2}$ ( $\times 10^{-8}$ )	$C_{Total}$ (fF/ $\mu$ m)	$f_T$ ( $\times 10^{-11}$ Hz)	$Q$ -Factor
A	1.686	3.920	1.639	2.00	24.21
B	0.681	4.132	1.655	2.03	9.32
C	2.095	1.034	1.629	2.00	23.07
D	0.773	1.120	1.639	2.03	7.68

#### 4. CONCLUSIONS

A comparative performance analysis of a new structure was presented namely a IR-UBR-UTB-SOI-n-MOSFET which contains an extra Insulator Region (IR) at the channel source junction, Undoped Buried Region and having a GaAs under the channel region. The scaling and RF parameters of IR-UBR-UTB-SOI-n-MOSFET have been obtained along with conventional UTB-SOI-n-MOSFET. From the analysis, it has been obtained that the Sub-threshold slope, DIBL, and the static power dissipation are lower for IR-UTB-SOI-n-MOSFET than the other three structures and it also provides better  $I_{ON}/I_{OFF}$  ratio. So the above structural change in the device can be a good candidate for switching and low standby operating power application.

#### REFERENCES

- [1] S. Cristoloveanu, "Silicon on insulator technologies and devices: from present to future," *Solid. State. Electron.*, vol. 45, no. 8, pp. 1403–1411, 2001.
- [2] M. A. Pavanello, J. A. Martino, V. Dessard, and D. Flandre, "Analog performance and application of graded-channel fully depleted SOI MOSFETs," *Solid. State. Electron.*, vol. 44, no. 7, pp. 1219–1222, 2000.
- [3] K. Kim, "1.1 Silicon technologies and solutions for the data-driven world," In Digest of Technical Papers 2015 IEEE International Solid-State Circuits Conference-(ISSCC), 2015, pp. 1–7.
- [4] J.-T. Park and J.-P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines," *Electron Devices, IEEE Trans.*, vol. 49, no. 12, pp. 2222–2229, 2002.
- [5] A. Chaudhry and M. J. Kumar, "Investigation of the novel attributes of a fully depleted dual-material gate SOI MOSFET," *Electron Devices, IEEE Trans.*, vol. 51, no. 9, pp. 1463–1467, 2004.
- [6] S. Cristoloveanu and S. Li, *Electrical characterization of silicon-on-insulator materials and devices*, vol. 305. Springer Science & Business Media, 2013.
- [7] B. Vandana, "Study of Floating Body Effect in SOI Technology," *Int. J. Mod. Eng. Res.*, vol. 3, no. June, pp. 1817–1824, 2013.
- [8] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "ZTC bias point of advanced fin based device: The importance and exploration," *Facta Univversitatis: Series, Electronics and Energetics*, vol. 28, no. 3, pp. 393–405, 2015.
- [9] Q. Xie, C.-J. Lee, J. Xu, C. Wann, J. Y.-C. Sun, and Y. Taur, "Comprehensive Analysis of Short-Channel Effects in Ultrathin SOI MOSFETs," *Electron Devices, IEEE Trans.*, vol. 60, no. 6, pp. 1814–1819, 2013.
- [10] H.-S. Wong, "Beyond the conventional transistor," *IBM J. Res. Dev.*, vol. 46, no. 2.3, pp. 133–168, 2002.

- [11] R. H. Reuss *et al.*, "Macroelectronics: Perspectives on technology and applications," *Proc. IEEE*, vol. 93, no. 7, pp. 1239–1256, 2005.
- [12] J. Yoon *et al.*, "GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies," *Nature*, vol. 465, no. 7296, pp. 329–333, 2010.
- [13] A. A. Orouji and M. K. Anvarifard, "SOI MOSFET with an insulator region (IR-SOI): A novel device for reliable nanoscale CMOS circuits," *Mater. Sci. Eng. B*, pp. 1–7, 2013.
- [14] M. Rahimian and A. A. Orouji, "A novel nanoscale MOSFET with modified buried layer for improving of AC performance and self-heating effect," *Mater. Sci. Semicond. Process.*, vol. 15, no. 4, pp. 445–454, 2012.
- [15] *Atlas User Manual*. Silvaco International, Santa Clara, 2012.
- [16] H. A. El Hamid, J. R. Guitart, and B. Iñiguez, "Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric double-gate MOSFETs," *Electron Devices, IEEE Trans.*, vol. 54(6), p. 1402–1408., 2007.
- [17] J. P. Colinge, "Multiple-gate SOI MOSFETs," *Solid State Electron*, vol. 48 (6), pp. 897–905, 2004.
- [18] "The International Technology Roadmap for Semiconductors," 2011.
- [19] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, "Temperature dependence inflection point in Ultra-Thin Si directly on Insulator (SDOI) MOSFETs: An influence to key performance metrics," *Superlattices Microstruct.*, vol. 78, pp. 134–143, 2015.
- [20] S. Chakraborty, A. Mallik, and C. K. Sarkar, "Subthreshold performance of dual-material gate CMOS devices and circuits for ultralow power analog/mixed-signal applications," *Electron Devices, IEEE Trans.*, vol. 55 (3), pp. 827–832, 2008.
- [21] W. Shockley and W. T. Read, "Statistics of the recombination of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, 1952.
- [22] R. N. Hall, "Electron-hole recombination in germanium," *Phys. Rev.*, vol. Phys. Rev., p. 387, 1952.
- [23] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Trans. Comput. Des. Integr. Circ. Syst.*, vol. 7 (11), pp. 1164–1171, 1988.
- [24] P. K. Sahu, S. K. Mohapatra, and K. P. Pradhan, "Zero temperature-coefficient bias point over wide range of temperatures for single- and double-gate UTB-SOI n-MOSFETs with trapped charges," *Mater. Sci. Semicond. Process.*, vol. 31, pp. 175–183, 2015.
- [25] S. Selberherr, "Analysis and Simulation of Semiconductor Devices," *Springer-Verlag, Wien-NewYork*, 1984.
- [26] G. C. Patil and S. Qureshi, "Impact of Segregation Layer on Scalability and Analog / RF Performance of Nanoscale Schottky Barrier," *J. Semicond. Technol. Sci.*, vol. 12, no. 1, pp. 66–74, 2012.
- [27] K. P. Pradhan, D. Singh, S. K. Mohapatra, and P. K. Sahu, "Assessment of III-V FinFETs at 20 nm node: A Process variation analysis," *Procedia Comput. Sci.*, vol. 57, pp. 454–459, 2015.