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TOTAL IONIZING DOSE EFFECTS AND RADIATION TESTING OF COMPLEX MULTIFUNCTIONAL VLSI DEVICES

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Abstract. *Total ionizing dose (TID) effects and radiation tests of complex multifunctional Very-large-scale integration (VLSI) integrated circuits (ICs) rise up some particularities as compared to conventional "simple" ICs. The main difficulty is to organize informative and quick functional tests directly under irradiation. Functional tests approach specified for complex multifunctional VLSI devices is presented and the basic radiation test procedure is discussed in application to some typical examples.*

Key words: *Total ionizing dose (TID) effect, radiation test, functional failure, operating mode*

1. INTRODUCTION

Radiation hardness requirements are typical for all kinds of microelectronic parts for space, avionics, military and nuclear physics applications. Radiation tests have to be performed to qualify each type of IC within its design, manufacturing or application steps [1], [2]. The infinite number of various radiation test results have been published recently but most of them are concentrated on rather simple devices under test – transistors, digital or analog ICs with rather simple radiation sensitive parameters set and well developed measurement procedures [3]-[5]. In case of modern complex VLSI ICs the same test approach is widely used, based on choosing modes and conditions of IC's operation under irradiation to be as simple as possible and measuring the simplest electric parameters, for example output voltages and power supply or input currents. At the same time, most of radiation test facilities initially are not adopted for IC radiation tests and have rather long signal cables – about ten meters and more, that excludes the real functional test possibility under irradiation for high-frequency and precision devices.

The aim of this research is to prove the necessity and demonstrate the possibility of complex functional testing (FT) of VLSI ICs under TID irradiation, and to show the existence of critical electrical and functional modes of IC operation. We have reviewed the most typical problems of multifunctional VLSI ICs TID testing which are illustrated

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by different ICs radiation behavior [6]-[16]. We also provide typical guidelines for FT procedure (both hardware and software) and present the proper gamma irradiation facility. In this paper we concentrate on TID effects experimental research, but all main results and conclusions can be spread to transient radiation effects (TRE), displacement damage (DD) and single event effects (SEE) [17]-[20].

2. Functional and Parametric Failures

TID behavior of complex VLSI ICs is usually non-trivial. It means that simultaneous total dose degradation of different elements and their mutual influence often lead to mixed parametric-functional IC failures. The results of 32-bit RISC-processor IDT79R3081-25MJ testing are shown in Fig. 1 as an example [6]. Processor malfunction (internal cache memory errors) is accompanied by parametric failure (supply current increase).

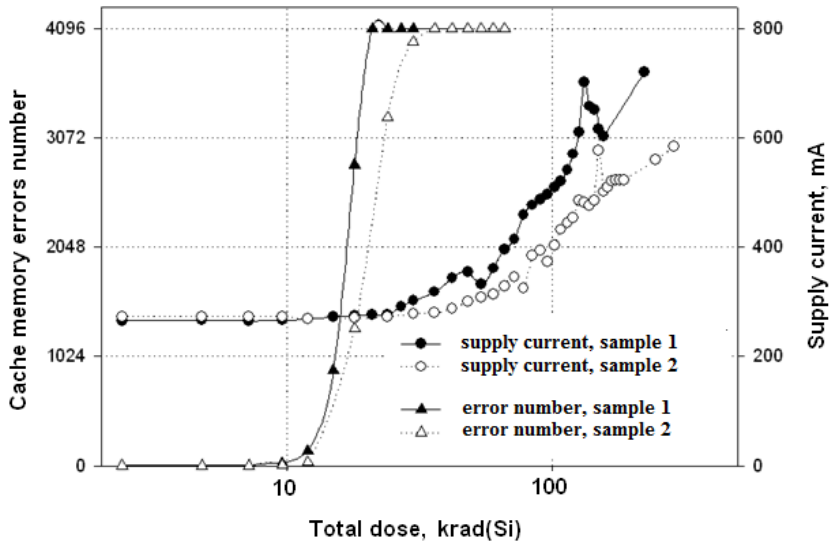

Fig. 1 Processor cache memory errors number and supply current vs. total dose.

It is difficult to separate parametric and functional TID failures for some types of complex ICs, such as ADCs and DACs. Parametric degradation leads to functional failures of these ICs. In Fig. 2 the set of ADC parameters is presented as a function of total dose [7]. The increase of gain error and nonlinearity is derived from the ADC transfer function degradation (Fig. 3) at 200 krad, when the ADC actually does not operate.

The similar radiation behavior is observed at flash memory SLCF128MM1UI (STEC) testing (Fig. 4). The read speed extreme fall means in fact that the flash memory cannot operate properly [8].

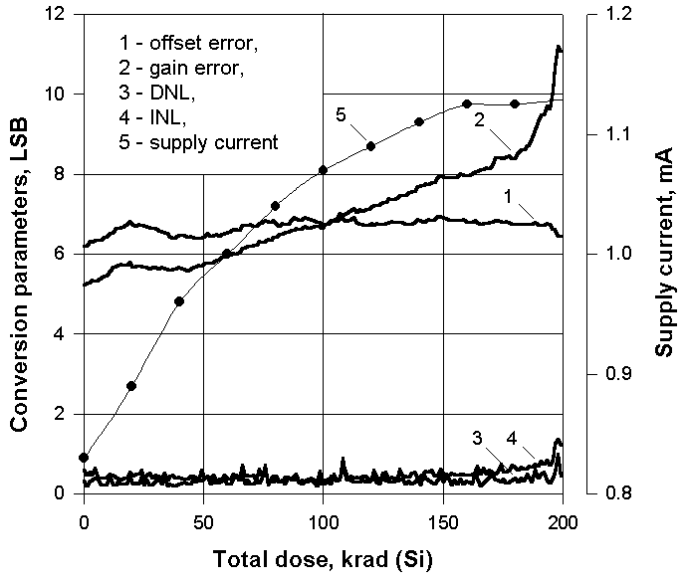

Fig. 2 TID degradation of ADC conversion parameters and supply current.

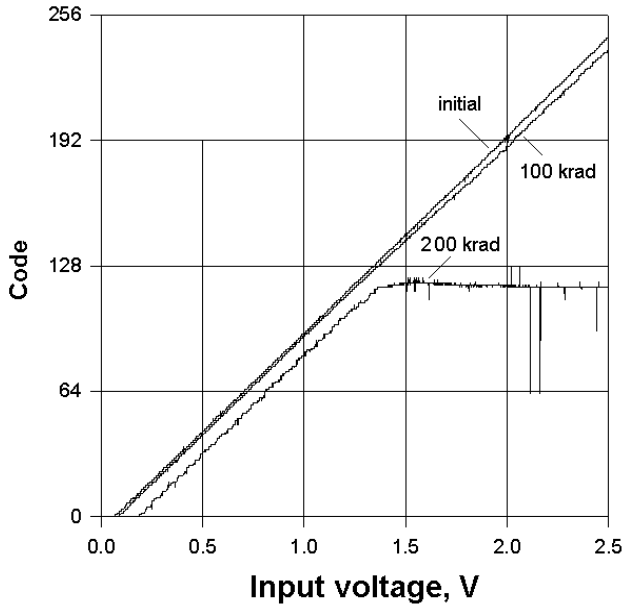

Fig. 3 TID degradation of ADC transfer function.

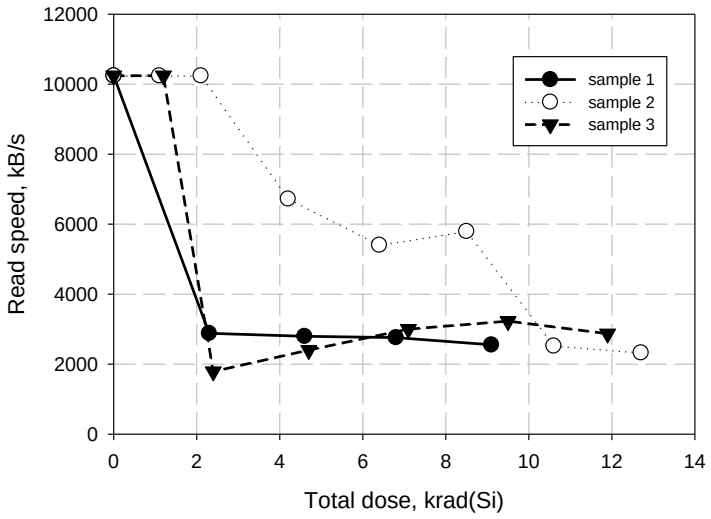

Fig. 4 Read speed vs. TID level for SLCF128MM1UI.

The analysis of TID test data for different IC types demonstrates the critical importance of FT during complex multifunctional VLSI ICs radiation test. ICs dominant TID failure mechanism (parametric or functional) statistics from our test center is presented in Fig. 5.

One can see the essential prevalence of TID failures for simple logic while other (complex) types of ICs are characterized by subsequent or even dominant functional failures [9].

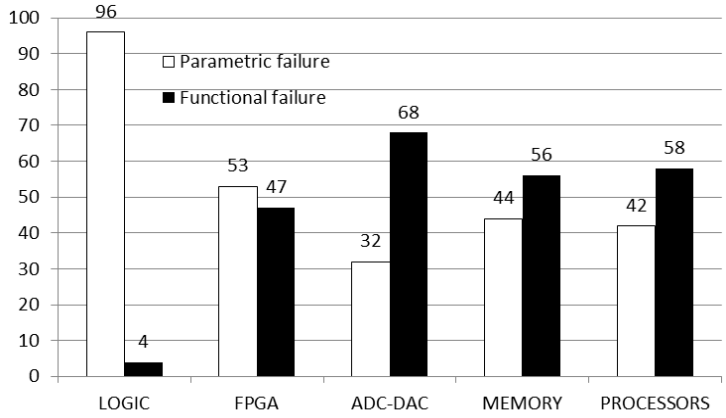

Fig. 5 Functional vs. parametric TID failures quantities for various ICs classes.

The essential problem of FT design is the proper selection of ICs operating modes under irradiation. It is known that TID hardness usually depends strongly on the electric bias and operating mode under irradiation [10]. The hardness level difference between the best and the worst case modes for a particular IC may be several times.

Radiation sensitivity of IC's different units can vary significantly, since the elements operate at different electrical modes under irradiation. Fig. 6 shows that SOI RISC microprocessor PowerPC7448 (E2V) demonstrates no uniformity in TID hardness.

In 'normal' mode (processor executes a test program under irradiation) the failure dose is much higher (6–10 times) than in 'periodical restarts' mode under irradiation. It was found that the boot unit of the microprocessor is the most TID sensitive [12].

Static and dynamic operation modes of IC under irradiation usually lead to very different estimations of hardness levels. For example, the total dose graphs presented in Fig. 7 demonstrate the extreme increase of RAM supply current at static irradiation mode, while the samples irradiated at dynamic mode are much harder [13].

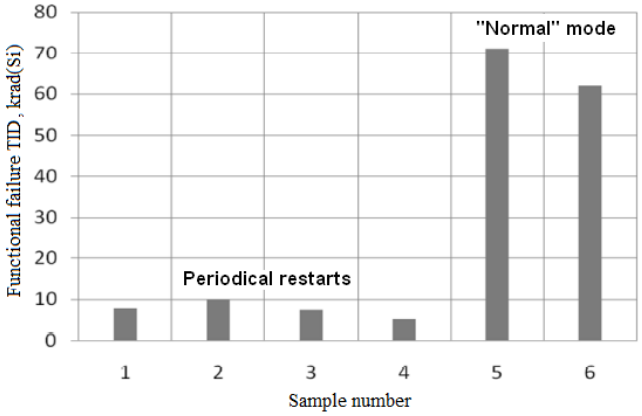

Fig. 6 Functional failureTID for different irradiation modes of PowerPC7448 microprocessor.

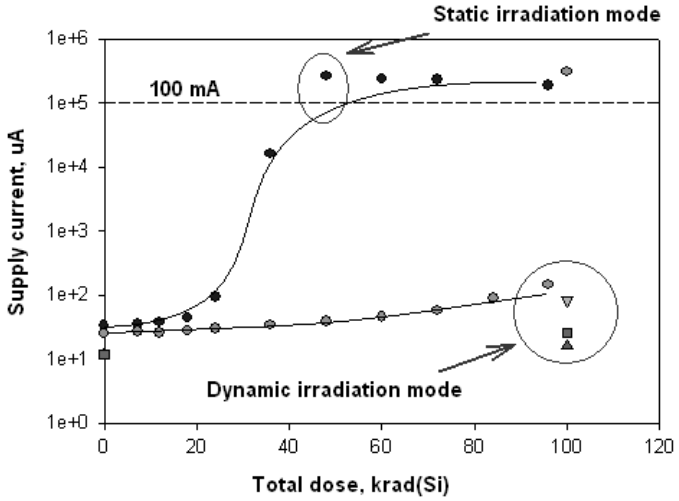

Fig. 7 RAM supply current vs. total dose at static and dynamic operation modes under irradiation.

3. ICs OPERATING MODE UNDER IRRADIATION

In some cases TID hardness difference of samples irradiated in various operating modes leads to the situation when the samples irradiated in one mode do not fail at all, whereas the hardness level of the samples irradiated in another mode is rather low. For example, in Fig. 8 the results of MIL-STD-1553B receiver BUS-65163-220Y (DDC) TID testing are presented [14]. Some samples have been irradiated in data transfer mode and the others – in 'silent' mode (without data transfer). One can see that the second part of samples did not fail at all.

These examples demonstrate the importance of ICs operating mode under irradiation correct selection. In most cases the purpose of the test is to determine the IC hardness level in the worst case mode. Complex multifunctional VLSI ICs can often operate in dozens of modes, that is why the preliminary analysis and research should be carried out to find such mode.

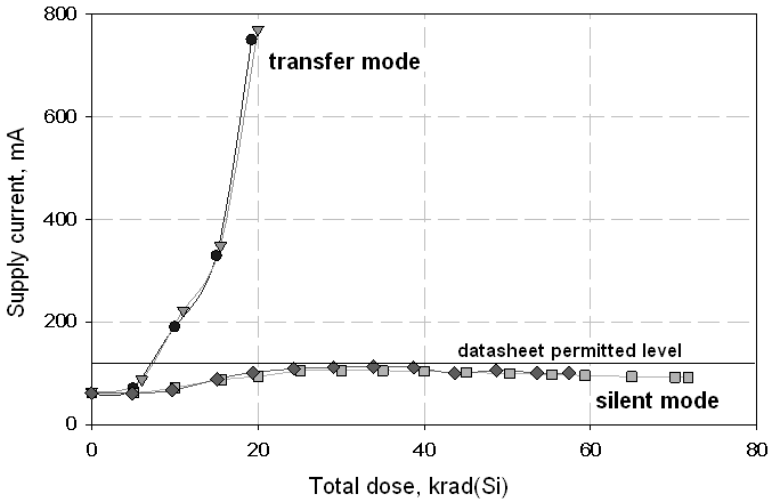

Fig. 8 Supply current vs. TID level for BUS-65163-220Y samples irradiated in transfer mode and "silent" mode.

4. TESTING DURING AND AFTER IRRADIATION

As it has been mentioned before, sometimes radiation test procedure is based on measurements of only the most primitive electrical parameters under irradiation. The complete functional testing, if any, is performed with a delay of several hours or even days after irradiation. This is due to the inability of a radiation test center to carry out an informative test under irradiation. The test procedure is often based on special equipment (industrial IC testers) which is not adapted to radiation test environment, nor is compatible with irradiation facilities and does not support remote testing. But according to our experience and data, it is really very important to execute FT directly during irradiation. Testing IC samples after irradiation would distort the real radiation behavior picture and hardness level because of annealing that can result even in full operation recovery.

In Fig. 9 two graphs of CMOS ADC INL are shown: the first is measured immediately after the 100 krad (Si) irradiation and the second 12 hours later (T = +25ºC) [15]. One can see that 12-hours annealing leads to an ADC's operation recovery.

Fig. 10 demonstrates another example of TID hardness level distortion because of annealing [8]. Annealing was carried out at a temperature of +25ºC. The samples of 4 Mbit static RAM have been irradiated to 60-120 krad (Si) and were tested both during irradiation and after 24-hours annealing. The second part of this procedure demonstrated full functional recovery and significant supply current drop.

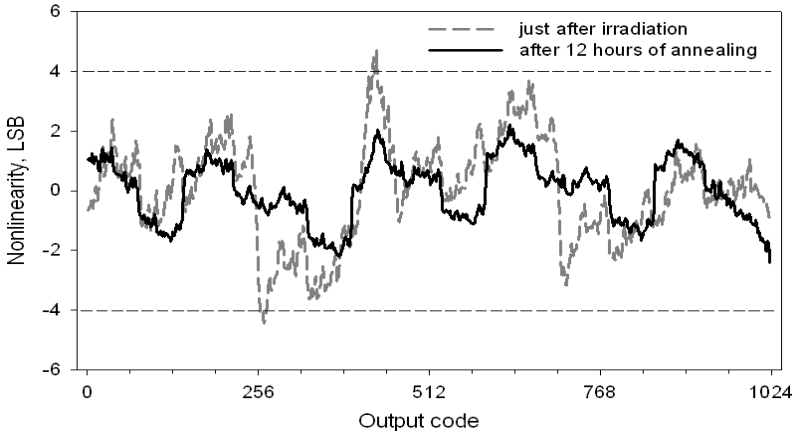

Fig. 9 ADC INL measured immediately after 100 krad (Si) irradiation and 12 hours later(T = +25ºC) (datasheet margins are shown by dashed lines at ±4 LSB).

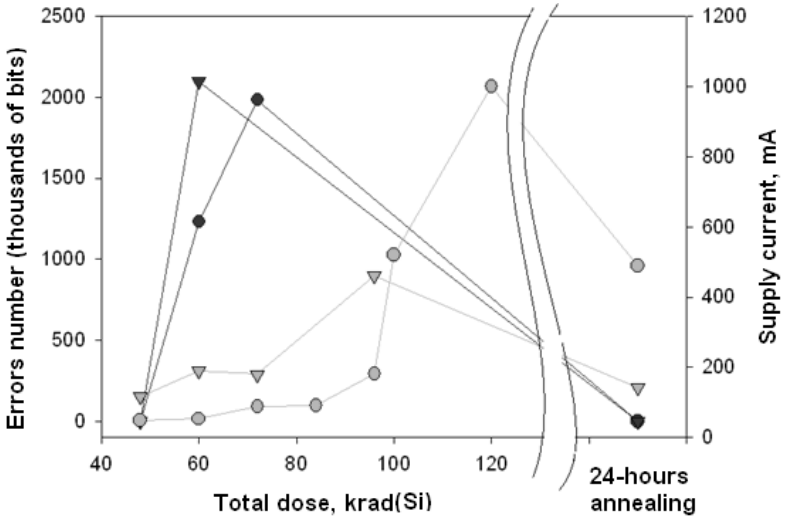

Fig. 10 RAM errors number (black symbols) and supply current (gray symbols) vs. TID during irradiation and after annealing(T = +25ºC).

5. Low Dose Rate Effects

The important specifics of space applications is its low intensity (dose rate) in the range of 10^{-3} ... 10^{-4} rad (Si)/s, and it is well known that the low dose rate effects can affect ICs total dose hardness [3], [21]. It should be noted that in most cases radiation tests are carried out in the dose rate range 10 ... 1000 rad (Si)/s.

Low dose rate effects are especially important for bipolar ICs, which are often characterized by increasing parameters' degradation and low TID hardness at low dose rate, the so-called ELDRS (Enhanced Low Dose Rate Sensitivity) effect [22], [23]. This effect has to be taken into account when planning bipolar ICs testing procedure for space applications.

At the same time, for CMOS ICs dose rate influences on the hardness in the opposite way – the hardness levels are usually higher at low dose rates [24], [25]. The example in Fig. 11 demonstrates the influence of radiation dose rate on CMOS flash-memory WF1M32B (White Electronic Designs) TID hardness. Low dose rate conditions proved to be about 1,5 times better than high dose rate [26].

For complex devices the low dose rate effects may be more complicated. Both parameters degradation and functional performance of such ICs often demonstrate different behavior at low and average radiation intensities. In Fig. 12 the nonlinearity of ADC AD7890 (Analog Devices) vs. total dose at two dose rates is presented.

Since radiation tests are usually carried out at the average dose rates, the real on-board CMOS ICs TID hardness may be higher than it has been determined in laboratory radiation tests. Direct low dose rate testing is usually hard to fulfil because of the long time required. There are many techniques of accelerated testing usually based on irradiation at average intensity and following annealing (see [27] – the well known MIL-STD-883H test method), but all of them have restrictions and adequacy problems.

We suggested and implemented the 'engineering' technique for low dose rate effects estimation. This technique is based on the combination of dose rates under testing and allows obtaining real TID hardness levels without great time loss. The basic structure of the technique for CMOS ICs is as follows:

(1) radiation testing of some samples (about half of a lot) at average dose rate (10 ... 100 rad (Si)/s) to estimate TID failure level;

(2) comparison of this level with the required hardness level;

(3) if the determined TID failure level is above the requirements we do not need to take the low dose rate effect into account, because this effect can only improve the CMOC ICs TID hardness;

(4) if the determined TID failure level is below than the requirements for more than 3 times we also do not need to test the low dose rate conditions, because according to our experience, this effect cannot improve the hardness level estimation for more than 2-2,5 times;

(5) and if the failure level is below the requirements less than 3 times, we test the rest samples of a lot at low dose rate (0,005 ... 0,05 rad (Si)/s) to determine the TID failure level for the real space conditions.

This rational technique reduces the low dose rate testing amount in several times [28].

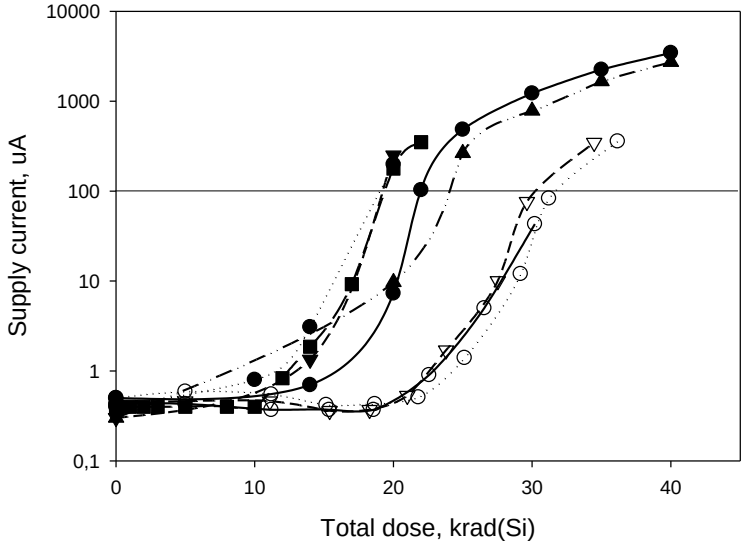

Fig. 11 Total dose degradation of WF1M32B supply current: black symbols – 10 rad(Si)/s, white symbols – 0.04 rad(Si)/s.

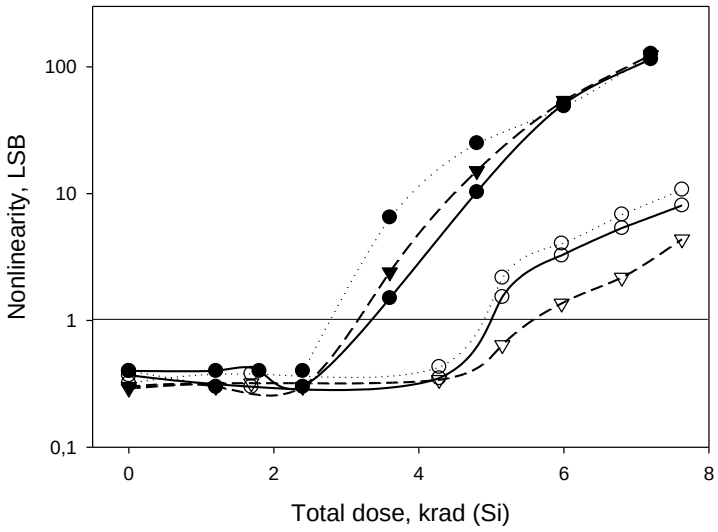

Fig. 12 Total dose degradation of AD7890 nonlinearity: black symbols – 5 rad(Si)/s, white symbols – 0.01 rad(Si)/s.

6. RADIATION TEST FACILITIES

The experimental results presented in the previous section demonstrate the necessity of special test equipment for complex multifunctional VLSI ICs radiation testing. As a rule, industrial IC testers are not optimal for radiation test procedure. That is why specialized technical solutions have been designed, in order to combine complex FT of different VLSI ICs with restrictions of modern irradiation facilities.

Therefore, universal VLSI ICs test system have been designed based on the National Instruments hardware, LabView software and the set of test plates, adapted and specified to the variety of complex multifunctional ICs under test [29]. The general system structure is presented in Fig. 13.

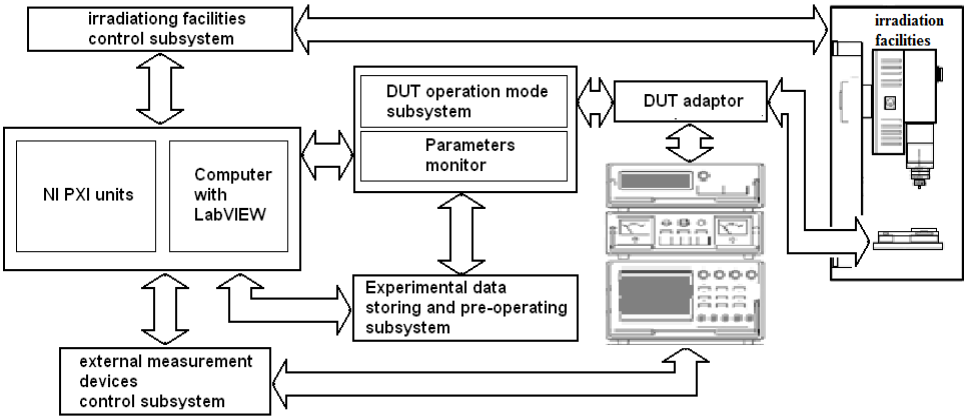

Fig 13 General structure of the NI-based VLSI ICs radiation test system.

Radiation testing of VLSI ICs also requires convenient irradiating facilities. The basic requirements are low electromagnetic interference and short signal lines. The original dual-zone Co-60 (energy 1,25 MeV, dose rate 0,01...1 rad/s) and Cs-137 (energy 0,66 MeV, dose rate 0,2...20 rad/s) gamma facilities have been especially designed and installed in NRNU MEPHI – SPELS test center. The unique feature is about 1m distance between FT equipment and device under test. Being used in coincidence with compact X-ray tester (energy up to 0,1 MeV, dose rate 1...500 rad/s) and pulsed linear electron accelerator in X-ray mode (LINAC – energy 2 MeV, dose rate 0,5...100 rad/s) these facilities allow to carry out complex multifunctional VLSI ICs TID-radiation tests in practical range of irradiation intensities, that is necessary to estimate TID hardness for all kinds of applications – [30],[31],[32].

7. CONCLUSION

As a conclusion we can note that radiation behavior of multifunctional VLSI ICs differs from radiation behavior of ‘simple’ ICs by significant features, causing specifics in test procedure. It is necessary to take it into account when planning and preparing the test experiment.

According to the practical TID test experience one can summarize the following features of complex multifunctional VLSI ICs radiation test procedure:

- it is important to research and select correctly worst-case IC bias conditions and operating modes under irradiation;
- functional and parametric tests should accompany each other in coincidence;
- tests should be executed directly under irradiation;
- low dose rate effects influence should be taken into consideration during testing.

These principles form the foundation of basic test technique and equipment which are used in Radiation Test Center of NRNU MEPHI-SPELS. The test system and procedure presented have been checked and verified in hundreds of real radiation tests of complex multifunctional VLSI devices.

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