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MEMORY CHIPS AND UNITS RADIATION TOLERANCE DEPENDENCE ON SUPPLY VOLTAGE DURING IRRADIATION AND TEST

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Abstract. *In this work we investigate the influence of various memory chips supply voltage on their sensitivity to the radiation environment. The main physical mechanisms responsible for radiation-induced degradation at nominal, increased, and decreased supply voltage values are discussed. It is demonstrated that, depending on supply voltage value during irradiation and subsequent testing, device's tolerance to data corruption effects in memory circuits, single event latch-up (SEL) and hard errors induced by ionizing radiation can vary significantly. We also give some recommendations to perform radiation tests.*

Key words: *space radiation, memory, digital integrated circuits, flash, SRAM, SEU, total dose*

1. INTRODUCTION

The typical variation of allowable supply voltage values for complex digital CMOS integrated circuits (microprocessors, microcontrollers, memory chips, etc.) is within 5 to 10 percent of the nominal one. The device in application can work at any supply voltage within this range. According to data from previous works, the total dose hardness and single event sensitivity can vary significantly depending on the operation conditions [1]-[9]. This fact must be taken into account when assessing radiation tolerance of microcircuits. In this work we concentrated our investigations on radiation tolerance dependence with supply voltage for memory segment of digital ICs. Memory cells or units are a part of the vast majority of digital ICs. In some cases memory is the most critical unit of digital ICs due to its sensitivity to radiation [1], [10]-[11]. Radiation environment (space, various ground sources, etc.) can have a negative impact on electrical parameters of memory chips

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and units, such as supply current, output voltage levels, timing parameters, etc. However, the most negative consequences are associated with radiation effects leading to functional failures, such as corruption of data stored in memory or inability to rewrite data. The radiation tolerance level to these functional and parametric failures can significantly depend on the supply voltage of ICs and particularly for memory devices. The radiation behavior of memory devices and units must be taken into account while providing radiation qualification of digital ICs.

The aim of this work is to demonstrate how the influence of supply voltage applied during irradiation and testing can influence the radiation response of memory microcircuits, and to determine the worst-case supply voltages for various critical microcircuit parameters. We will describe the main mechanisms that determine the dependency of radiation response to supply voltage and work out some recommendations for proper selection of supply voltage during radiation tests of various memory devices and digital ICs containing memory units.

2. The Influence of Supply Voltage on Total Dose Hardness of Memory Integrated Circuits

Previous works have shown that total dose hardness levels of complex multifunctional very large scale integration (VLSI) devices strongly depend on operating conditions during radiation tests [12]-[14]. In this work we consider in more detail total dose tolerance dependence of various memory ICs on their supply voltages not only during irradiation but also during functional tests.

The amount of radiation-generated carriers escaping initial recombination increases with applied electric field, as shown in Figure 1 [15]. The application of supply voltage on the IC during irradiation leads to the presence of a higher electric field in oxides, and induces a higher density of charge trapped in oxides. Thus, applying the maximum allowed supply voltage during irradiation is the most critical parameter for the estimation of total dose tolerance of digital ICs (in particular memory devices) estimation.

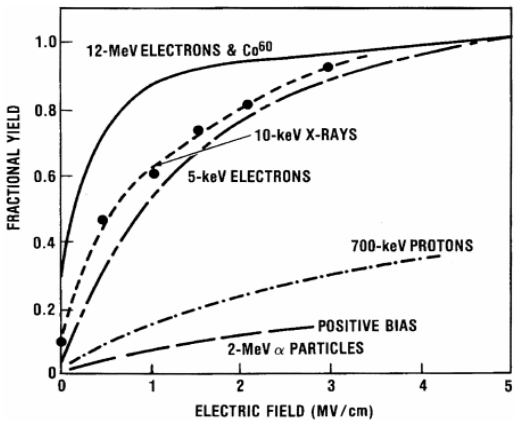

Fig. 1 Experimentally measured fractional hole yield as a function of applied electric field, for a number of incident particles [15]

At the same time, as will be shown below, applying the maximum supply voltage during functional tests after irradiation is not always critical for memory total dose tolerance estimation.

We experimentally compared TID levels when applying minimum, nominal and maximum allowed supply voltages during functional tests of SRAM microcircuits. These SRAMs were manufactured on various CMOS processes, supply voltages vary from 2,7 V to 5,5 V. Device irradiation was performed at maximum supply voltage. This experimental comparison (figure 2) shows that applying the minimum allowed supply voltage during functional test (writing and reading test operations) is the most critical mode for SRAM functional failure total dose level estimations. Such behavior is due to the fact that an IC in this mode exhibits the maximum sensitivity to threshold voltage shift and leakage caused by the trapping of the radiation-induced charge in the oxide.

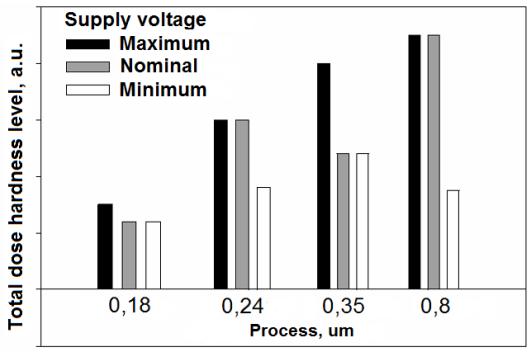

Fig. 2 Total dose hardness dependence on supply voltage applied during functional tests for various SRAMs

A different behavior was observed for flash and EEPROM memories. We investigated functional failure dependence on supply voltage during test after irradiation for flash memory S29GL064N manufactured on 110 nm CMOS process. Before irradiation, the test pattern was stored into the memory array. During irradiation the device was kept in storage mode at nominal supply voltage. Periodically irradiation was paused and a reading operation was performed on the memory array at minimum, nominal and maximum allowed supply voltages. The first differences between write (stored) and read data were observed for the maximum supply voltage (figure 3).

All observed errors were bit upsets from programmed state (charge stored into cell gate, “0” logical level) to erased state (charge removed from cell gate, “1”logical level). Thus, it can be argued that bit upsets were caused by the loss of charge stored into the cell during irradiation. When the radiation-induced charge loss is total, stored information is upset from the programmed state to the erased state. When the loss of charge is only partial, it leads to a threshold voltage shift of the flash memory cell, as illustrated by the dashed curves in Figure 4. During the reading operation of the memory, the voltage on cells gate has the same value as the supply voltage. Therefore, as illustrated in figure 4, applying the maximum supply voltage during irradiation and test will be the most critical for total dose tolerance estimation.

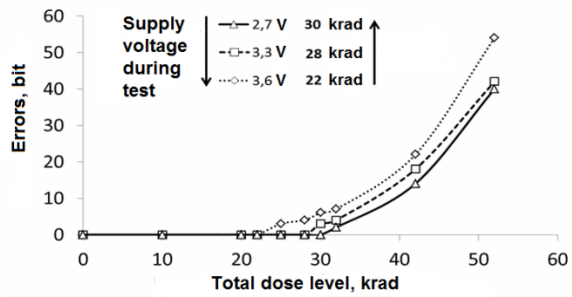

Fig. 3 Number of flash memory read error bits vs total dose level for various supply voltage applied during test

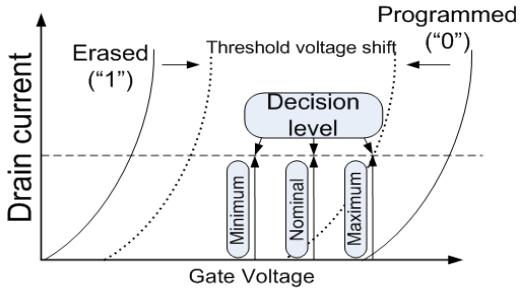

Fig. 4 Drain current vs gate voltage for programmed ("0") and erased ("1") cell states and cell with some charge (dotted curve)

3. The Influence of Supply Voltage on Single Event Sensitivity of Digital Integrated Circuits

Two main single event effects in digital ICs are single event latchup (SEL) and single event upsets (SEU) in memory units, control and data registers. Single event upsets in registers can cause single event functional interrupt (SEFI). We provide estimation of SEU sensitivity dependence on supply voltage for different types of memory devices and units.

3.1. SEU sensitivity dependence on supply voltage for SRAM memory.

In a memory cell, the area sensitive to single event upsets is the drain of off-state transistors in [16]-[21]. According to [21], the critical charge for SRAM cell upset depends on static noise margin of the device and can be estimated as:

$$Q_c = C_{OX} V_{SNM} \tag{1}$$

where C_{OX} – the capacitance of gate oxide, V_{SNM} is the static noise margin of memory cell. Static noise margin decreases with supply voltage. Therefore, the sensitivity of SRAM memory ICs and units to single event upsets increases with the decrease in supply voltage. Such behavior was observed for XC7Z020 configuration memory, as shown in the results presented below.

However, the critical charge for cell upset does not always show a linear dependence on supply voltage level. For this reason, experimental results obtained for one supply voltage cannot be extrapolated to another level without experimental estimation [22]. Investigation of single event upsets in SRAM due to neutrons [23] shows that simple cross section estimation based on critical charge in some cases can give underestimated results.

The results of investigation on the XC7Z020 configuration memory are shown in Figure 5, where the SEU cross section increases with the decrease in supply voltage during test. For this type of memory, applying the minimum supply voltage during irradiation is the most critical mode for SEU.

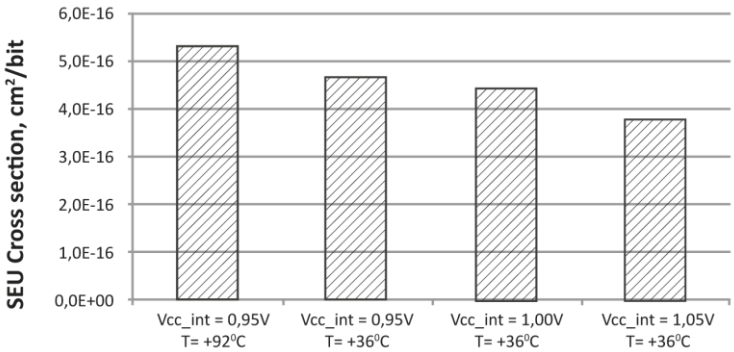

Fig. 5 SEU cross section dependences vs supply voltage during test and temperature for 120 MeV protons irradiation (cm^2/bit), (MeVcm^2/mg)

At the same time SEU investigation results for CMOS 0,25 μm SRAM 512K×8 (Figure 6) and XC5VLX50 block and configuration memory (Figure 7) show no significant difference in SEU cross section at different supply voltages during irradiation. However, it should be noted that a difference in sensitivity of SRAM at different voltages can be observed in the LET threshold region of the effect. Experimental data for linear energy transfer (LET) values in near-threshold have not been obtained in this case.

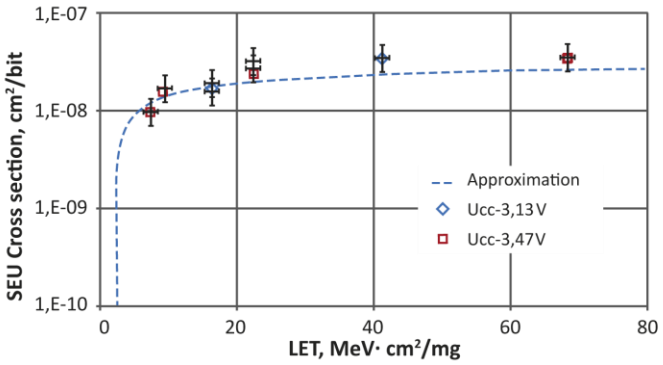

Fig. 6 CMOS 0,25 um SRAM 512K×8. SEU cross section vs heavy ion LET for various supply voltages applied during irradiation

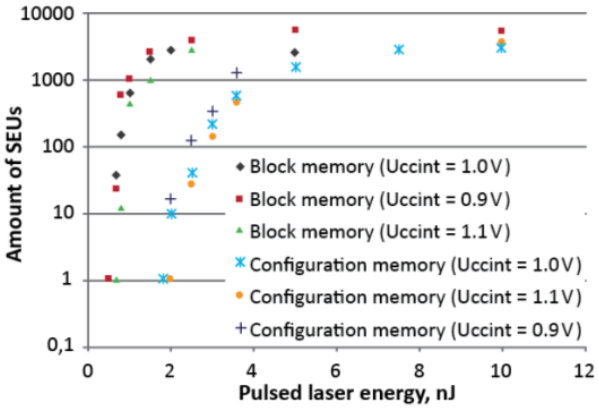

Fig. 7 Amount of SEUs in block and configuration memory vs pulsed laser energy for various supply voltages

3.2. SEU sensitivity dependence on supply voltage for charge storage memory.

Another dependence of the sensitivity to SEUs is observed for charge storage memories (Flash, EEPROM). We provide data on the irradiation of flash memory S29GL064N manufactured on 110 nm CMOS process by Ne ions with an LET near 7 MeV·cm2/mg at various supply voltages. After irradiation, information stored was read from the array at minimum, nominal and maximum allowed supply voltages for this device (figure 8) and compared with the data written before irradiation. As shown by the experimental results in Figure 8, the device cross section does not depend on supply voltage during irradiation. At the same time, an increase in SEU cross section with supply voltage during test after irradiation has been observed. SEUs in this flash memory result from partial charge loss stored in memory cell [24] and increase in cross section with supply voltage can be explained similarly to total dose. In this case the maximum supply voltage during test will be the most critical mode for SEU sensitivity estimation.

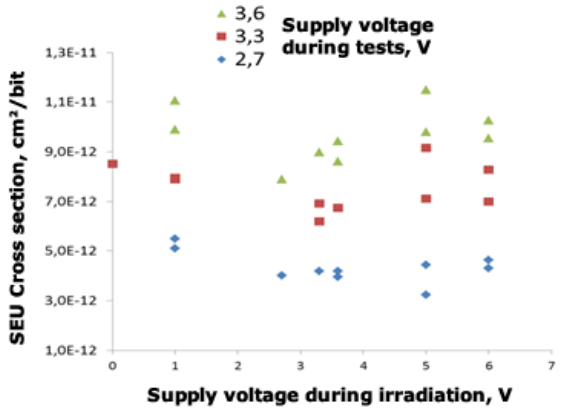

Fig. 8 SEU cross section vs supply voltage during test and irradiation Ne ions at normal incidence for S29GL064N

3.3. SEL sensitivity dependence on supply voltage for digital ICs.

Memory ICs and units have no difference in single event latchup mechanisms and sensitivity dependence on supply voltage in comparison with other digital ICs. Our experimental results obtained for CMOS SRAM memories CY62256 (Figure 9) and 90nm CMOS SRAM 1Mx8 (Figure 10) show that the worst-case for SEL sensitivity is to apply the maximum supply voltage during irradiation.

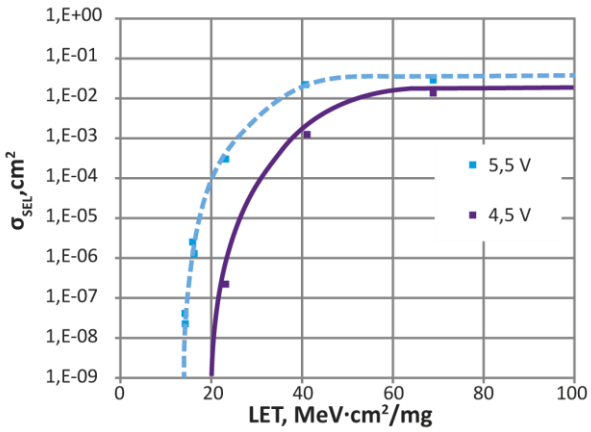

Fig. 9 CY62256. SEL cross section (σ_{SEL}) vs heavy ions LET for different supply voltages

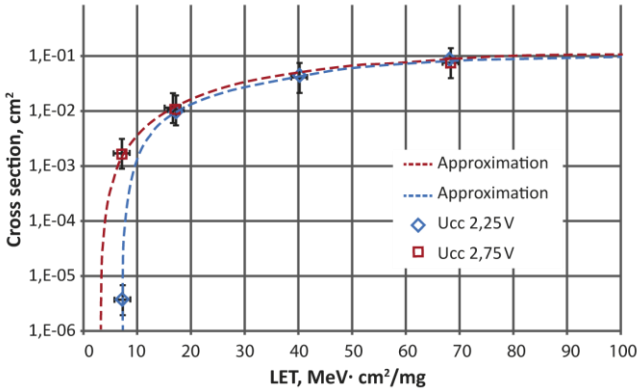

Fig. 10 90nm CMOS SRAM 1Mx8. SEL cross section(σ_{SEL}) vs heavy ions LET for different supply voltages

There is no influence of ICs scaling on the parameters of the parasitic thyristor structure at the origin of the SEL mechanism. Switch-on current does not vary significantly for CMOS processes with design rules from 180 nm to 65 nm. Operating temperature and supply voltage mainly affect ICs SEL sensitivity [25]. Sensitivity to SEL decreases with supply voltage, which is explained by a decrease in the gain of the parasitic bipolar transistor and a decrease in the collected charge with a lower electric

field strength [26].The influence of the supply voltage is mainly manifested near the SEL threshold LET. It can be clearly seen from our experimental results presented above in Figures 9 and 10. The SEL saturation cross section is almost unchanged with supply voltage, while the SEL threshold LET varies significantly. In addition, a higher supply voltage can be more likely to exceed the SEL holding voltage, which increases the probability of maintaining SEL condition. Results presented in work [26] show a sharp increase in sensitivity to SEL at supply voltages greater than 1.5 V (figure 11). Therefore the maximum supply voltage is the most critical mode for SEL sensitivity estimations.

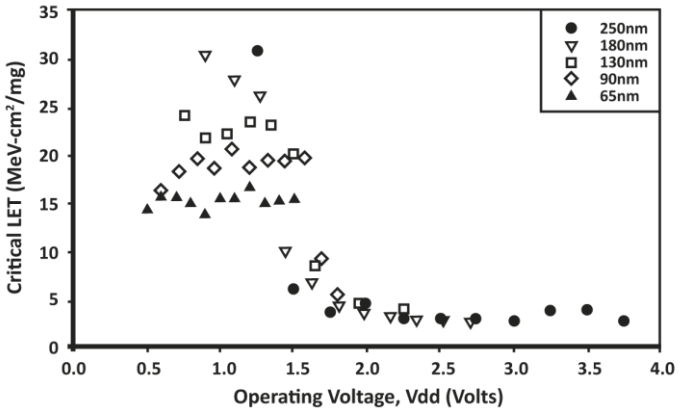

Fig. 11 Dependence of the SEL threshold LET on the supply voltage for various design rules

4. Recommendations on Selection of Supply Voltage for Different Types of Memory Integrated Circuits and Units during Radiation Tests

When performing radiation qualification of ICs, it is necessary to correctly select the worst-case supply voltage to give conservative estimations of radiation hardness level. Incorrect selection of supply voltage can lead to overestimation of radiation hardness level. It is important to take into account that the worst-case supply voltage to use during test and during irradiation may be different. Based on the results of the investigation and their analysis presented above, we can give recommendations for an appropriate selection of the worst-case supply voltage during certification of memory ICs and units. These recommendations are presented in table 1.

Table 1 Worst-case supply voltages during ICs radiation certification

Type of memory	Total dose		Single events		
	During irradiation	During test	SEL	SEU	
				During irradiation	During test
SRAM	Maximum	Minimum	Maximum	Minimum	Any
Charge storage memory	Maximum	Minimum and maximum	Maximum	Any	Minimum and maximum

5. CONCLUSION

In this work we have shown significant influence of memory ICs and units supply voltage on their sensitivity to total dose and single event upsets. We identified the worst-case supply voltage for total dose and single event upsets memory ICs sensitivity during irradiation and test, and we have shown that they can be different in some cases. Consequently, recommendations are also provided to properly select the supply voltage to use during memory ICs and units radiation qualification.

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