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HIGH PERFORMANCE DIGITAL CURRENT CONTROL IN THREE PHASE ELECTRICAL DRIVES

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Abstract. *Majority of contemporary static power converters makes use of three-phase, PWM controlled IGBT inverters. Typical applications include electrical drives and grid connected converters. In both cases, a high closed loop bandwidth is highly desirable. The bandwidth is constrained by the problems of the feedback acquisition. The feedback errors are caused by the noise, parasitic phenomena and by the current ripple at the PWM frequency. The errors can be reduced by considering deriving the average value of the output current within the past PWM period. This feedback acquisition method reduces the noise, but it also introduces delay into the feedback lines. Along with delays brought in by digital PWM, the feedback delay reduces the range of stable gains and limits the closed loop bandwidth. Effects of the delay can be reduced by conveniently placing the control interrupt and adopting an optimum parameter setting which meets both the bandwidth requirements and the robustness against the noise and the parameter changes. Experimental verification proves that the proposed current controller achieves the response speed and the robustness against the noise which outperforms the competitive solutions.*

Key words: *Current control, High-performance control, Signal acquisition, Ac motor drives, Three phase inverters*

1. INTRODUCTION

Electrical drives are frequently used to control the speed or the position of the work piece or the tool. In such cases, the speed and position controllers are used as the outer control loop, which provide the torque reference. The later determines desired currents that have to be injected into the stator windings in order to obtain the desired torque. Digital current controllers are the inner loop of the drive, [1], [2]. The bandwidth of the current loop determines the torque response time. Therefore, it determines the overall performance of the drive [3], [4], such as the closed loop bandwidth of the speed or position loop. For the proper operation of the drive, it is essential to decouple the flux control loop and the torque control loop. The basic prerequisite for the decoupled flux and torque control is a fast and robust current controller [5]-[7]. In high speed drives, the

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fundamental frequency f_F of the stator currents and voltages can reach considerable values. In some cases, f_F can reach a considerable fraction of the sampling frequency f_{SPL} of the current controller [8]-[11]. In such cases, it is of particular importance to have a high closed loop bandwidth of the digital current controller. Although the objective of this paper is to maximize the closed loop performances in the presence of delays, and it is reasonable to expect that the devised control measures would also improve the closed loop performances with very high fundamental-to-switching-frequency ratios, we did not discuss nor did we verify such performances in this paper.

A high bandwidth of the current controller is also important in grid-connected static power converters, such as the three phase inverters that regenerate into the grid, used in conjunction with wind-power plants and solar-power plants. In order to inject undistorted, sinusoidal currents into the grid, the closed loop current controllers have to overcome the nonlinearities such as the lockout time, reduce the line harmonics, and to secure a very low factor of total harmonic distortions (THD). For this to achieve, digital current controllers should have a quick response and a high disturbance rejection. Several imperfections and nonlinearities make this requirement difficult to achieve. Performance enhancement requires the proper modeling and accounting for such imperfections and nonlinearities [8], [10], [11]. Certain popularity is gained by the dead-beat and predictive controllers [13], due to their capacity to cope with transport delays, but their wider use is hindered by pronounced sensitivity to changes in system parameters.

Digital current controllers are frequently located in synchronous *dq* frame. This is done in order to achieve constant steady-state references, instead of sinusoidal steady-state references, that would have to be tracked with the controllers located in stationary coordinate frame. Synchronous controllers have the possibility to achieve the steady state performance with zero phase error and zero amplitude error. Controller structure includes proportional and integral action. When used with elevated fundamental frequencies f_F, the current controller has to be enhanced by the *dq* decoupling actions [10], [11], [14]. In cases where the PWM delays and imperfections are negligible, and where the current ripple does not impair the feedback acquisition process, conventional PI controllers can be tuned by using well known tuning procedures [11], [12], [14], derived by applying the IMC concept [5]. Neglecting the imperfections, the synchronous frame current controllers can reach the bandwidth frequency of $0.11 \cdot f_{SPL}$. With stationary frame controllers, it is possible to achieve the bandwidth frequency of $0.07 \cdot f_{SPL}$ [12]. In cases where the PWM ripple of the output current is not negligible, as well as in cases where the PWM delays and lockout time delays impair the sampling process and contribute to parasitic alias components, it is not possible to use the conventional structure and parameter setting of digital current controllers.

The current controller designed in this paper reduces the sampling errors by taking the average value of the feedback signals over the past PWM period. In essence, the well known technique of oversampling is applied within the current controller environment, paced by the PWM carrier, and implemented on an industrial DSP as a time-skewed one-PWM-period-averaging. The method uses an automated, DMA-driven oversampling. The feedback signal is calculated from a large number of equally spaced samples collected within the past two sampling periods. With double-update mode, the two sampling periods correspond to one PWM period. Although this approach reduces the feedback errors caused by the noise and the ripple, it also introduces delay into the feedback lines. The feedback delay adds to the delay contributed by the digital PWM. In a conventional

implementation, where the control interrupt gets triggered by the zero-count and the period-count of the PWM carrier, the equivalent transport delay encountered with the proposed one-PWM-period-averaging reaches 2.5 sampling periods, thus reducing the range of stable gains and limiting the closed loop bandwidth. Effects of the delay can be reduced by conveniently shifting the control interrupt and adopting an optimum parameter setting which meets both the bandwidth requirements and the robustness against the noise and the parameter changes.

In order to deal with transport delays in digital current controllers, and to provide and error-free feedback acquisition, the authors recently designed and tested several solutions. The most important previous results are given in [20] and [21]. As well as this paper, [20], [21] deal with digital current controllers. Therefore, it is of interest to clarify what has been done in [20], [21], and what is the contribution proposed in this paper.

In [20], delay compensation is performed by introducing a differential control action with the proper *d*-gain setting. In this paper, we took a different approach. We do not use the differential action. Instead, we rely on the time-skewed acquisition window of Fig. 9, which permits rescheduling of the interrupt as an effective way of coping with delays.

It is also of interest to compare the feedback acquisition technique used in [20], [21], and in this paper. The approach used in this paper is similar, but not identical to the one used in [20], while the approach of [21] is quite different than both. In [20], the impact of the lockout time, the motor cable capacitance and the switching noise on the feedback errors incurred with conventional regular-sampling-double-update approach are experimentally verified, suggesting the need for the use of the oversampling. Thorough experimental evidence of [20] is obtained with variable length of the motor cable, and it proves that the PWM-period-based oversampling and decimation results in considerable reduction of the sampling errors. The method is coined into *one-PWM-period-averaging*, and it takes the average of the samples acquired within one T_{PWM} window encircled by the interrupt ticks. While the method used in this paper also uses the oversampling-decimation, the current samples are acquired within a different acquisition window. In Fig. 9, the new acquisition window is shifted by Δt_{EXE} with respect to the interrupt ticks. The time shift Δt_{EXE} corresponds to the execution time of the control interrupt. The skew between the corresponding sampling windows can be observed by comparing [20, Fig. 5] and Fig. 9.

In [21], the authors deal with the current controllers which do not use the oversampling/ decimation, but rely instead on the conventional regular-sampling-double-update approach. This approach is applicable to noise-free sampling cases, such as the one where the inverter is integrated within the motor housing. The structure of the current controller of [21] uses *p*, *i*, and *d* actions, and it is different that the controller considered in this paper. In [21], the parameter setting deals with the three gains, and it takes into account the controller capability to suppress the impact of the electromotive-force disturbances. In this paper, the parameter setting focuses on *p* and *i* gains, and it does not consider the disturbance rejection capability. The objective of parameter setting rules in [21, page 7, criterion function *Q*] is different than the objective of the parameter setting rules in Section 5 of this paper. The former results in an optimum *p*-*i*-*d* gains, while the later deals with a *p*-*i* controller and it searches for the optimum *p* gain while maintaining a constant *p*/*i* ratio. The feedback acquisition technique, the structure of the current controller, and the goal of the parameter setting procedure in [21] are different that those proposed in this paper.

This paper is organized as follows. The system with three phase IGBT-based inverter, the typical load and the digital controller are reinstated in Section 2. The feedback

acquisition system is discussed in Section 3, with the proposal of the error-free sampling scheme which operates with a minimum indispensable delay. In Section 4, the two competitive structures of the digital current controller are analyzed and discussed. The optimum parameter setting is proposed in Section 5, focused of achieving quick response, robustness, and high rejection of the input disturbances. Experimental results obtained with the proposed current controller are included in Section 6. Conclusions are given in Section 7.

2. SYNCHRONOUS-FRAME DIGITAL CURRENT CONTROLLER

Most 3-phase digital current controllers are either employed in electrical drives or in grid connected static power converters. The former have the task of controlling the stator currents of 3-phase ac machines, while the later control the current injected into the 3-phase ac grids. An IGBT inverter, used to supply an ac machine, is shown in Fig. 1. The ac line voltage is rectified to obtain the dc voltage E. The voltage E feeds the 3-phase inverter. By means of the pulse width modulation (PWM), the inverter generates variable frequency, variable amplitude voltages, required for the proper current control. In Fig. 2, the two IGBT inverters are used to take the energy from the wind turbine and pass it into the ac grid. One of the inverters (on the right) has the function rather similar to the one in ac drives, and it controls the stator current of the ac generator, thus controlling the flux and torque of the machine. The inverter on the left in Fig. 2 takes over the energy that comes through the dc link circuit and passes the energy into the grid. It has to control the current injected into the grid. The grid current has to be sinusoidal, with a low THD, and with the power factor which depends on the active power and reactive power commands. In both Fig. 1 and Fig. 2, the three phase inverters are used as the voltage actuators, which supply the voltages required for the proper current control.

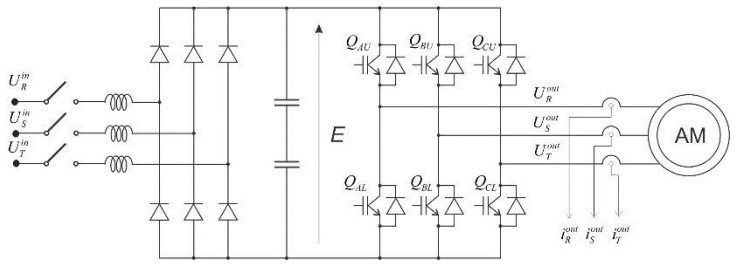

Fig. 1 Three phase inverter as the voltage actuator within an electrical drive.

The three phase inverters of Figs. 1 and 2 are nonlinear voltage actuators that cannot supply a continuously changing voltage. They are linearized by means of the pulse width modulation, illustrated in Fig. 3. In each switching period T_{PWM}, the output phases are connected to the upper rail of the dc bus during t_{ON} conduction interval, and then switched to the lower rail of the dc bus during $t_{OFF} = T_{PWM} - t_{ON}$ conduction interval. In this way, the average value within the switching period is $U_{av} = E \cdot t_{ON}/T_{PWM}$, where E is the dc voltage across the dc bus, while the voltage U_{av} is referred to the minus rail of the dc bus. In the prescribed way, the switching bridge as a voltage actuator is linearized. In each switching interval T_{PWM}, it provides the average voltage which can be adjusted by altering the value of t_{ON}.

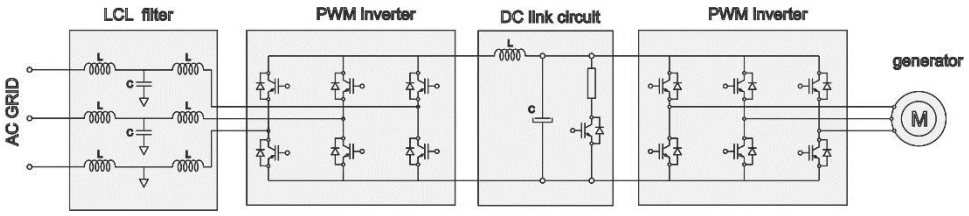

Fig. 2 The use of the 3-phase inverters as the voltage actuators within the power conversion system which takes over the energy from a variable speed generator (right) and recuperates the energy into the ac grid.

The left side of Fig. 3 illustrates asymmetrical PWM technique, while symmetrical PWM is given in the right. Due to the inferior performances, asymmetrical PWM is not used in 3-phase inverters. In both electrical drives and grid side power converters, the 3-phase inverters use the symmetrical PWM technique. Other techniques which are also used have the same sequences as the carrier-based symmetrical PWM. In cases where the output voltage of the 2-level 3-phase inverter is generated by the space vector modulation, the resulting PWM pattern can be proved equal to the pattern obtained with symmetrical PWM where the modulating signal is conveniently changed.

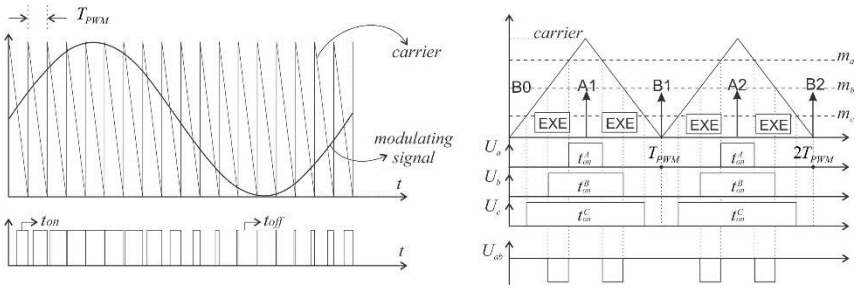

Fig. 3 Pulse width modulation with asymmetrical (left) and symmetrical carrier. The waveform of the line-to-line voltage U_{ab} is given in lower right.

In Fig. 3, the intervals where the digital controller executes the control algorithm are designated by EXE. One execution occurs during the rising edge of the carrier, while the successive execution takes place during the falling edge. In other words, there are two executions in each T_{PWM}. Therefore, the sampling time of the current controller is $T_{SPL} = T_{PWM}/2$.

Each execution instants calculates a new value for the conduction intervals t_{ON} for the phases A, B, and C. Due to $U_{av} = E \cdot t_{ON}/T_{PWM}$, calculated intervals t_{ON} actually represent the voltage commands. The ratio $m=t_{ON}/T_{PWM}$ represents the modulation index. In Fig. 3, the modulation indices are denoted by m_a, m_b, and m_c.

Considering the execution instant between B0 and A1 in Fig. 3, it calculates the values of t_{ON} (m) that cannot be applied before the instant A1, when the carrier reaches the period count and starts do decline. Therefore, the effects of the calculated t_{ON} (m) take place between A1 and B1, thus affecting the falling edges of the phase voltage pulses.

The same way, the execution instant between A1 and B1 produce t_{ON} and m that would be applied only after the instant B1, when the carrier reaches zero, thus affecting the rising edge of the phase voltage pulses between B1 and A2.

Delays are introduced due to the hardware properties of the PWM peripheral units. In order to avoid multiple commutations within a single period T_{PWM}, the values of modulation signals m_a, m_b, and m_c are reloaded into the PWM comparators only at instants where the PWM carrier reaches either zero or the period count. Intrinsic delay of the PWM peripheral unit introduces a transport delay of $T_{SPL}/2$ into the voltage actuator. This delay has to be taken into account when designing the structure and deciding parameters of the digital current controller.

A simplified schematic of the inverter supplied stator winding is given in Fig. 4, made by adopting the subsequent assumptions. For both the induction motors and synchronous motors, it is reasonable to assume that the magnetic flux within the machine exhibits very slow changes, compared to the desired dynamics of the loop. The same assumption holds for the rotor speed. At the same time, the electromotive force E_{MF} is the product of the flux and the rotor speed. Therefore, it is reasonable to assume that the electromotive force E_{MF} has the role of a slow, external disturbance within the current control system.

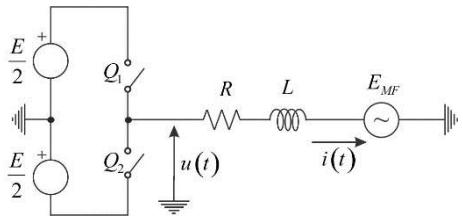

Fig. 4 Simplified schematic of the inverter supplied stator winding. This schematic does not reflect the coupling between phases in an electric machine.

In cases where the inverter of Fig. 1 generates the three phase system of symmetrical, sinusoidal voltages, the average value of the three output phase voltages corresponds to the center-point of the dc bus, denoted by the ground symbol in Fig. 4. If the three phase winding of the ac machine is symmetrical, and the electromotive forces are symmetrical and balanced, then the star connection of the stator winding remains at the potential of the ground, as denoted in Fig. 4. In such cases, the stator winding can be represented by simplified schematic of Fig. 4. Similar considerations can be drawn for grid side connected power converters with series L filter. The only difference is that the phase voltages of the ac grid replace the electromotive forces of the stator winding, while RL parameters of the output filter and the grid replace the elements R and L in Fig. 4.

In order to perform the current control task, it is necessary to acquire the feedback signals, namely, the value of the stator current. Characteristic waveforms are given in Fig. 5. Due to the pulsed nature of the stator voltage, the current has the fundamental component and a superimposed ripple. The ripple comprises the spectral component at the PWM frequency f_{PWM} and a certain spectral content at f_{PWM} integer multiples. With $T_{SPL} = T_{PWM}/2$, the most of the ripple energy resides at the Nyquist frequency and impairs the sampling process. With assumed linear change of the ripple (curve A in Fig. 5), it would be possible

to acquire the samples at the center of each voltage pulse, whether positive or negative, and obtain a ripple free feedback (i_1) (regular-sampling-double-update). Due to *RL* nature of the winding impedance, the waveform of the ripple assumes the form of the curve B in Fig. 5. Moreover, the center of the voltage pulses gets affected by unpredictable effects of the lockout time and gating signal delays. Therefore, an attempt to acquire a single sample in each half-period of the PWM would result in sampling errors, denoted by i_2 in Fig. 5.

One of the ways is to respect the limits imposed by Kotelnikov sampling theorem, that is, to filter out any spectral content above $f_{SPL}/2 = f_{PWM}$. Considering a limited resolution of the analog-to-digital converter, it is usually considered quite sufficient to reduce any spectral content in the *forbidden* area below the level of 1 LSB of the ADC. Even so, a heavy low pass filtering would be required to complete the task, thus introducing unacceptable delays, phase errors and amplitude errors. Alternative ways of securing an error-free sampling without introducing considerable delays is explained in the following Section.

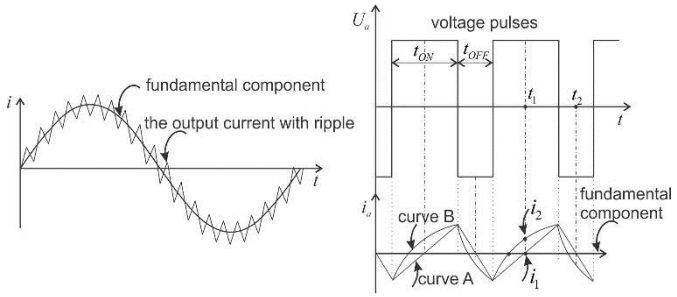

Fig. 5 PWM-related ripple and the fundamental component of the stator current.

3. An Advanced Feedback Acquisition System

The main problem in acquiring the current feedback is the presence of the current ripple, caused by the pulsed nature of the inverter voltages. The ripple has a triangular form, illustrated in Fig. 6. Most of the spectral energy of the ripple resides at the PWM frequency, with some minor components located at integer multiples of f_{PWM}. The consequential sampling errors, illustrated in Fig. 5 can cause considerable performance deterioration of the current controller performance.

In ac drives environment, single-sample feedback acquisition of Fig. 5 is prone to sampling errors [17], [18]. With relatively large d*V*/d*t* values at the inverter output, the switching causes parasitic oscillations of the voltage and current [17]. The frequency of such oscillations is well above the Nyquist frequency. The parasitic *LC* elements that give rise to poorly damped parasitic oscillations are present even with a rather short inverter-motor cable [17]. In all the sampling schemes where the feedback is obtained from a single sample in each sampling period, the oscillations above the Nyquist frequency introduce the sampling errors. In a 3-phase ac controller, the switching instants continuously change according to the voltage command, and their position relative to the sampling instant is variable. The consequential sampling noise is larger when the switching comes close to the sampling instants, where the switching-excited parasitic oscillations may contribute to considerable feedback errors [18]. Regular-sampling-double-update approach introduces the sampling errors even in cases where

the switching-noise-oscillations are much lower, such as the case with ac drives with integrated motor-inverter and no cable. The feedback errors are introduced whenever the sampling instants slide away from the zero-crossing instants of the current ripple. Any imperfection, parasitic effect or delay that moves the ripple-zero-crossing from the sampling instant introduces the sampling errors. One way of reducing the such errors is finding the average value of the current in each PWM period by oversampling.

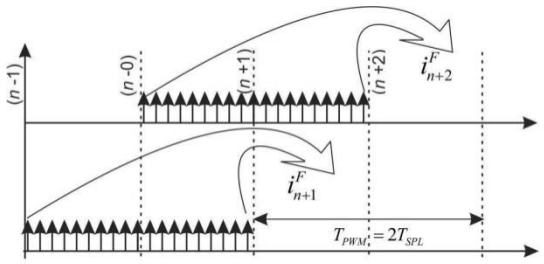

Fig. 6 Sampling scheme with PWM-period averaging.

The oversampling technique aided with digital filtering/averaging is well known and widely used [16], [20]. In order to reduce the measurement errors in an industrial current control environment, we implemented the oversampling to perform time-skewed one-PWM-period averaging of the feedback signals on an industrial DSP. Devised technique is rather simple. A similar technique has been introduced and tested in [20]. Thorough experimental evidence of [20] proves that the proposed oversampling and decimation technique, also called *one-PWM-period-averaging* results in considerable reduction of the sampling errors. While the feedback acquisition proposed in [20] takes the average of the samples acquired between the interrupt events, the acquisition window proposed in this paper (Fig. 9) uses another acquisition window. It is skewed by Δt_{EXE}, where Δt_{EXE} corresponds to the execution time of the control interrupt. In [20], the feedback delay is compensated by extending the controller with a differential control action. In this paper, we avoid the differential action and rely on the time-skewed acquisition window (Fig. 9) which enables an effective reduction of time delays.

The basic approach taken is [20, Fig. 5] is similar, but not identical to the time-skewed approach illustrated in Fig. 9, where the oversampling window is shifted by Δt_{EXE}. The general description of the oversampling/decimation is found in [20] in a brief, eight lines paragraph above (12). At the same time, neither this specific implementation nor the analysis of consequential delays were published by other authors. A more detailed description of the one-period-averaging is reinstated in this Section, along with the necessary information and the model of the transport delay, which is required for the proper understanding of the next steps and for the further analysis. Later on, the time-skewed sampling window of Fig. 9 is emphasized and discussed, as it represents the difference between the feedback acquisition of [20] and the feedback acquisition used in this paper.

The feedback averaging is implemented on a low cost DSP controller. The implementation of the time-skewed one-PWM-period averaging on an industrial DSP requires some skill, as the resources are cost-limited and the programming is not trivial. We are also aware of the possibility to implement the relevant algorithm on the

laboratory control platform dSPACE MicroAutobox II, which has the hardware support for the synchronization of A/D and PWM processes, and it also supports the oversampling. This opens the possibility to implement and verify the time-skewed one-PWM-period averaging in laboratory environment, with much lower effort, and without the need to change the DSP code of the actual industrial drive.

The current ripple can be reduced by the sampling scheme outlined in Fig. 6. The feedback signal at instant $(n+1)T_{SPL}$ is calculated from a number of equidistant samples, acquired within the past PWM period, starting from $(n-1)T_{SPL}$ and ending with $(n+1)T_{SPL}$. The number of equidistant samples acquired within each $T_{PWM} = 2T_{SPL}$ interval can be very large. With contemporary digital signal processors, it is possible to scan all the ADC channels each 1μs. Hence, with a typical f_{PWM} = 10 kHz, it is possible to acquire up to 100 successive samples of all the analog channels. For practical reasons, the number of samples is usually adjusted to 2^n, hence, either 32 or 64 samples. The samples are collected automatically, by an internal DMA machine, without an additional overload of the CPU. Collected samples are automatically stored in a designated region of the internal RAM, thus made ready for further processing. During each control interrupt, it is necessary to find the sum of the samples acquired over the past PWM period, and to calculate their average value by dividing the sum by the number of samples. In cases where the oversampling factor is equal to the power of two (2^n), division can be replaced by simple right-shifting of the sum. The sum of the samples corresponds to the average value of the output current in stationary coordinate frame. Transformation into the stationary frame requires the proper angle between the two frames. The averaged feedback signals have to be transferred into the synchronous frame by using the average angle within the same PWM period where the actual samples have been acquired. In both direct and inverse Park transformations, the angle has to be time-synchronized with the samples that are being transformed.

With a considerable number of samples, it is reasonable to assume that the average value of the collected samples corresponds to the average value of the sampled current within the preceding T_{PWM} period. Therefore, value of i^F_{n+1} at instant $(n+1)T_{SPL}$ can be expressed in terms of the current samples i_{n-1}, i_n and i_{n+1}, representing the instantaneous value of the output current at instants $(n-1)T_{SPL}$, nT_{SPL}, and $(n+1)T_{SPL}$. It is of interest to notice that the samples i_{n-1}, i_n and i_{n+1} are not actually acquired, and they are not available in the DSP RAM. They are mentioned in an effort to relate the feedback signals to the output response of the actual system. Namely, the DSP controller does not acquire the samples at instants $(n-1)T$, nT, and $(n+1)T$, and it does not have the information on the actual output (i^{dq} in Fig. 7). The feedback loop is closed by using the signal $i_F{}^{dq}$ in Fig. 7, obtain by one-PWM-period averaging. For the purposes of the subsequent analysis, it is necessary to find appropriate model of the delay, and to express the feedback i^F_{n+1} in terms of the samples i_{n-1}, i_n and i_{n+1}. The samples i_{n-1}, i_n and i_{n+1} coincide with the zero-count and the period-count of the PWM carrier (Figs. 3 and 5). With regular-sampling-double-update, $T_{PWM}=2T_{SPL}$, and the average value of the inverter voltage is changed in each $T_{PWM}/2$. With $L/R >> T_{SPL}$, and neglecting the current ripple, the remaining ripple-free component of the output current has a quasi-linear change between $(n-1)T_{SPL}$ and nT_{SPL}, as well as between nT_{SPL} and $(n+1)T_{SPL}$. With this assumption, the average value of the output current from $(n-1)T_{SPL}$ to nT_{SPL} is roughly equal to $(i_{n-1}+i_n)/2$, while the average value from nT_{SPL} to $(n+1)T_{SPL}$ is equal to $(i_n+i_{n+1})/2$. Therefore, the average value on the interval $[(n-1)T_{SPL} .. (n+1)T_{SPL}]$ becomes the average value of $(i_{n-1}+i_n)/2$ and $(i_n+i_{n+1})/2$,

$$i_{n+1}^{F} = \frac{i_{n+1} + 2 \cdot i_n + i_{n-1}}{4}. \tag{1}$$

Both the samples of the stator current, such as $(n\text{-}1)T_{SPL}$, nT_{SPL}, and $(n\text{+}1)T_{SPL}$, and the samples of the feedback i^F can be transformed into z domain and represented by corresponding complex images $i^F(z)$ and $i(z)$. The former and the later are related by the transfer function of the feedback path W_F,

$$W_F(z) = \frac{i^F(z)}{i(z)} = \frac{z^2 + 2 \cdot z + 1}{4z^2}. \tag{2}$$

With $T_{SPL} = T_{PWM}/2$, the transfer function W_F has an infinite attenuation at the switching frequency f_{PWM}. The attenuation is also infinite at integer multiples of f_{PWM}. Therefore, the feedback signal acquired from (1) does not get affected by the ripple. An average transport delay introduced by (1) and (2) is equal to T_{SPL}, hence, considerably lower than the delay of conventional anti-aliasing filters that can be used instead of the proposed averaging.

It is of interest to compare the frequency response of the pulse transfer function (2) and the actual one-PWM-period-averaging. With a large number of current samples within each period, the transfer function of the feedback acquisition system is very close to the analog-implemented average over the past T_{PWM}, which has an infinite attenuation at the switching frequency and its integer multiples. Delay model of one-PWM-period averaging with N samples requires modified z-transform with the fractional sampling period ratio of N=32 or N=64, which is less convenient, less instructive, and hardly suitable for the analysis, design and the parameter setting of the controller. For that reason, we adopted the approximation (2). This approximation is verified by considerable similarity between simulations and the experimental results. Thus, all the further design phases and parameter setting procedures use delay approximation of (2).

The purpose of $W_F(z)$ approximation is to model the transient phenomena below the Nyquist frequency, which is the frequency range of interest when it comes to designing and tuning the digital current controller. In the frequency range well above the Nyquist frequency, there are differences between one-PWM-period-averaging and the transfer function (2), but they do not have any meaningful influence on the setting of the feedback gains. Validity of the above approximations are justified by the experiment.

4. THE STRUCTURE OF THE CURRENT CONTROLLER

The current controller provides the two voltages (u_d and u_q) supplied to the three phase ac machine, where they affect the two output currents (i_d and i_q). Whether represented in synchronous or in stationary frame, the plant has two inputs and two outputs. The transient phenomena in orthogonal axis are coupled. The coupling depends on the revolving speed of the dq frame, that is, on the revolving speed of the electrical machine. The coupling is also affected by the transport delays. Direct digital design (DDC) with the IMC applied in z domain [11] decouples the transient phenomena in orthogonal axes by means of the controller with conveniently embedded proportional and integral actions. The pulse transfer of such controller gets multiplied by the pulse transfer function of the plant (Fig. 7) to obtain the open loop transfer function which does not have any coupling terms [11, IV.E]. Relying on this result, it is possible to add the filtering terms in the feedback path and

perform the gain setting assuming that the coupling between the orthogonal axis does not exist; namely, assuming that the current controlled system is a single input - single output system (SISO). The analysis given in subsections 4.1 and 4.2 are performed under this assumption. More detailed support for such a claim is given in subsections 4.3-4.5.

The current controller executes in each T_{SPL} interval, that is, two times in each PWM period. The current controller tasks include the acquisition of the feedback signal, the execution of the control algorithm, and writing the voltage references, in the form of t_{ON} commands, into the corresponding registers of the PWM peripheral. The exact sequence of events has considerable effects on the consequential transport delay and it determines the closed loop performance.

The execution of the current control tasks takes place within an interrupt, triggered by a programmable event. The interrupts have to repeat twice in each PWM period. In Fig. 8, the interrupt events are created whenever the PWM carrier reaches either zero or the period count. One such execution account is denoted in Fig. 8. It takes place after the period count of the PWM carrier, at $t = (n-1)T_{SPL}$. The interrupt calculates the feedback signal i^F_{n-1} as the average value of successive current samples within the past PWM period. It can be approximated by the function of the samples i_{n-3}, i_{n-2}, and i_{n-1}, as $i^F_{n-1} = 0.25(i_{n-3}+2i_{n-2}+ i_{n-1})$. Based upon such feedback, the current controller derives the current error, and it calculates the voltage command u_{n-1}, suited to drive the current error back to zero. Once calculated, the voltage command u_{n-1} is expressed in terms of the pulse width t_{ON} for each of the three inverter phases. The pulse width values are reloaded into the PWM peripheral at instant $t = nT_{SPL}$. Therefore, the voltage command u_{n-1} determines the average voltage on an interval $[nT_{SPL} .. (n+1)T_{SPL}]$. This implies another transport delay that has to be taken into account in the controller design.

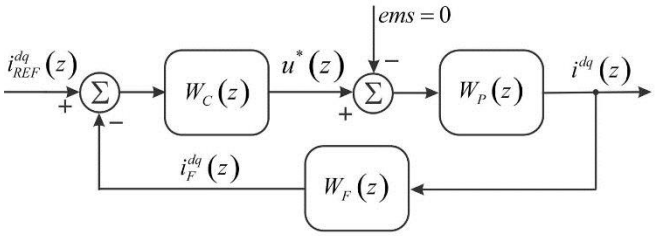

Fig. 7 Block diagram of the digital current controller.

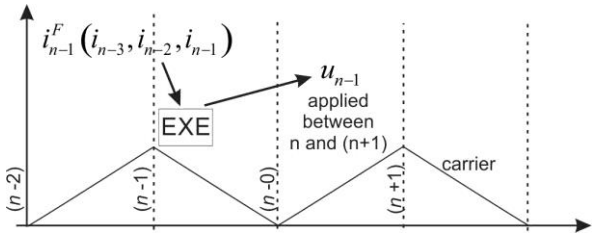

Fig. 8 Execution of the control interrupt immediately after the PWM carrier reaches zero-count or period-count.

The transport delays can be reduced by using the multisampling technique of [18]. Instead of executing the control interrupt twice per each PWM period T_{PWM}, as is the case in most dual-update-mode solutions, the interrupt can be executed $N > 1$ times in each half-period $T_{PWM}/2$. Each time the interrupt is triggered, a new feedback sample is acquired and a new voltage reference calculated. The voltage references affect the modulating signals that change N times in each half-period. Most of these references do not get implemented, as the PWM process permits only one switching per half-period, as it accepts only one crossing of the modulation signal and the PWM carrier. Therefore, the PWM unit uses only one of the voltage references in each $T_{PWM}/2$, while the multisampling generates considerably more references. One of the consequential drawbacks is a nonlinear relation between the voltage command and the actual output voltage. Positive side of the multisampling approach is reduction of the transport delay. Besides the nonlinear input-output relation, caused by specific insensitivity at vertical transitions, the multisampling picks up the current ripple, which has to be reduced by introducing a dedicated digital filtering, proposed in [18]. In order to suppress the impact of the switching transients on critical samples, it is of vital interest to avoid and skip any sampling after the PWM switching. In order to avoid possible multi-switching conditions, the multisampling requires specialized PWM logic which prevents the system from making more than one commutation in each half-period of the PWM.

Another possibility of sequencing the current control tasks is denoted in Fig. 9, where the zero-count events and period-count-events of the PWM carrier take place at $(n-1)T_{SPL}$, $(n\text{-}0)T_{SPL}$, and $(n+1)T_{SPL}$. The interrupts occur Δt_{EXE} before each counter event. The value of Δt_{EXE} should be larger than the worst-case execution time of the control interrupt. In this case, the control interrupt would complete before the successive event of the PWM counter. With recent DSP controllers, the interrupt execution time does not exceed 4μs. Hence, the interval Δt_{EXE} is considerably shorter than the sampling period T_{SPL}. The interrupt which completes just before $t = nT_{SPL}$ calculates the feedback signal i^F_n as the average value of successive current samples within the past PWM period. With $\Delta t_{EXE} << T_{SPL}$, the feedback signal can be approximated by the function of the samples i_{n-2}, i_{n-1}, and i_{n-0}, as $i^F_n = 0.25(i_{n-2}+2i_{n-1}+i_n)$. The current controller derives the current error and calculates the voltage command u_n, expressed in terms of the pulse widths t_{ON} in corresponding phases. The values are ready before nT_{SPL}, and they are reloaded into the PWM peripheral at instant $t = nT_{SPL}$. In this way, transport delay is reduced as u_n determines the average voltage on an interval $[nT_{SPL} .. (n+1)T_{SPL}]$. Both the schedule of Fig. 8 and the schedule of Fig. 9 are considered in this Section.

4.1. The schedule with the control interrupt executed after the counter event.

In this Section, the schedule of Fig. 8 is considered, where the current controller collects the feedback i^F_{n-1} as $0.25(i_{n-3}+2i_{n-2}+ i_{n-1})$, calculates the voltage command u_{n-1}, which, in turn, determines the average voltage on an interval $[nT_{SPL} .. (n+1)T_{SPL}]$.

The 3 output currents (i_a, i_b, and i_c) can be converted into $\alpha\beta$ frame of reference and expressed in terms of their components i_α and i_β. The current can be expressed as a vector $i^{\alpha\beta}=i_\alpha + ji_\beta$. By introducing $\lambda =\exp(-RT_{SPL}/L)$, and assuming that the slowly changing E_{MF} can be neglected, the difference equation which describes the change of the output current becomes

$$i_{n+1}^{\alpha\beta} = i_n^{\alpha\beta}\lambda + \frac{1-\lambda}{R}u_{n-1}^{\alpha\beta}. \tag{3}$$

Introducing the complex images $i(z)$ and $u(z)$ by

$$i(z) = \sum_{k=0}^{+\infty} i_k, \quad u(z) = \sum_{k=0}^{+\infty} u_k,$$

the transfer function $W_P(z)$ of the plant can be obtained by

$$W_P(z) = \left.\frac{i(z)}{u(z)}\right|_{E_{MF}=0} = \frac{1-\lambda}{R}\frac{1}{z\cdot(z-\lambda)}. \tag{4}$$

The structure of the current controller can be determined by applying the IMC principle on W_P,

$$W_C(z) = \alpha\frac{z}{z-1}W_P^{-1}\cdot\frac{1}{z^q},$$

where q is adjusted to make W_C feasible, while α is design parameter that determines the response speed. Applied to (4), the IMC concept results in a PI controller, with both P- and I-gains determined by α. Decoupled variation of the gains provides an additional degree of freedom which helps meeting the desired performances. The current controller with proportional action K_P and the integral action K_I can be described by the following transfer function,

$$W_C(z) = K_P + K_I\frac{z}{z-1}. \tag{5}$$

With transfer functions (2)-(5), the block diagram of the current controller is given in Fig. 7, where E_{MF} is assumed to a slow, external disturbance, the effects of which are reduced by the integral action of the controller.

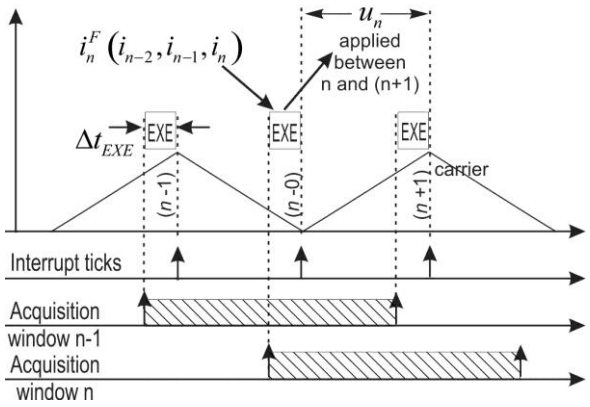

Fig. 9 Execution of the control interrupt just before the PWM carrier reaches the next zero-count or period-count. The interrupt must start at least Δt_{EXE} before the rollover of the PWM carrier. The worst case execution of the interrupt should not exceed Δt_{EXE}.

The open loop transfer function $W_{OL} = W_C W_P W_F$ is equal to

$$W_{OL}(z) = \frac{(K_P + K_I)z - K_P}{z-1} \frac{z^2+2z+1}{4z^2} \frac{1-\lambda}{R} \frac{1}{z\cdot(z-\lambda)}. \tag{6}$$

Introducing the relative gains p and i,

$$p = K_P \frac{1-\lambda}{4R}, \; i = K_I \frac{1-\lambda}{4R}, \tag{7}$$

$$W_{OL}(z) = \frac{[(p+i)z - p](z^2+2z+1)}{z^3(z-1)(z-\lambda)}. \tag{8}$$

The closed loop transfer function is

$$\begin{aligned} W_{CL}(z) &= \frac{i(z)}{i^*(z)} = \frac{W_C W_P}{1+W_{OL}} = \\ &= \frac{4(p+i)z^3 - 4pz^2}{z^5 + z^4(-1-\lambda) + z^3(p+i+\lambda) + z^2(p+2i) + z(i-p) - p}. \end{aligned} \tag{9}$$

The optimum gain setting and the resulting performances are discussed in Section 5.

4.2. The schedule with the control interrupt executed before the counter event

If the execution time of the control interrupt represents a negligible fraction of the sampling time, than the delay of Δt_{EXE} can be neglected in Fig. 9. In this case, the feedback signal i^F_n is obtained as $0.25(i_{n-2}+2i_{n-1}+ i_n)$, and it is used to obtain the voltage command u_n, which gets applied on the interval $[nT_{SPL} .. (n+1)T_{SPL}]$. In this case,

$$i^{\alpha\beta}_{n+1} = i^{\alpha\beta}_n \lambda + \frac{1-\lambda}{R} u^{\alpha\beta}_n, \tag{10}$$

which leads to the transfer function $W_P(z)$ of the plant

$$W_P(z) = \left.\frac{i(z)}{u(z)}\right|_{E_{MF}=0} = \frac{1-\lambda}{R} \frac{1}{z-\lambda}. \tag{11}$$

The open loop transfer function $W_{OL} = W_C W_P W_F$ of the system in Fig. 9 becomes

$$W_{OL}(z) = \frac{[(p+i)z - p](z^2+2z+1)}{z^2(z-1)(z-\lambda)}. \tag{12}$$

The closed loop transfer function becomes

$$\begin{aligned} W_{CL}(z) &= \frac{i(z)}{i^*(z)} = \frac{W_C W_P}{1+W_{OL}} = \\ &= \frac{4(p+i)z^3 - 4pz^2}{z^4 + z^3(p+i-1-\lambda) + z^2(p+2i+\lambda) + z(i-p) - p}. \end{aligned} \tag{13}$$

Due to reduced delays, the order of the system is reduced from the 5th down to the 4th, providing the potential to improve the bandwidth and robustness of the system.

4.3. Decoupling of d-axis and q-axis

The plant has two inputs, the voltages in *d*-axis and *q*–axis. The two outputs are the corresponding currents. Therefore, it is a multi input, multi output system (MIMO). In cases where the transient phenomena in orthogonal axis are decoupled, it is possible to design and tune the current controller in a simplified way, considering a single input, single output system (SISO). Adopting the complex vector notation, where the current error is expressed as $\Delta i=\Delta i_d+j\Delta i_q$, while the output current is $i=i_d+ji_q$, the product $W_C W_P = i(z)/\Delta i(z)$ in Fig. 9 is a complex number. In cases where the axes are coupled, this number has a non-zero imaginary part. In cases where the controller W_C cancels the undesired dynamics of the plant W_P and achieves complete decoupling, the transfer function $W_C(z)W_P(z)$, as well as the closed loop transfer function $i(z)/i^*(z)$ do not have an imaginary part. One such example is given in [11, IV.E], where the equation (12) represents the resulting closed loop transfer function. In such cases, it is possible to adopt SISO approach in parameter tuning. Some key considerations on decoupling and tuning of the current controllers are given in [8], [11], [12], [14], and [19].

The axis decoupling can be obtained by using the *s*-domain IMC approach, as shown in [5-7]. In absence of additional delays, the approaches of [5-7] would provide a decoupled operation of the current controller. Yet, any digital implementation of the current controller is time-discrete, and it involves additional time delays.

There is a number of valuable contributions that deal with the current controller in *s*-domain, and they provide a useful insights to readers [12], [14], [19]. In *s*-domain, the transport delays have to be modeled by rational approximation, and most frequently by Pade approximation. At the same time, discrete-time integrators are represented by Tustin approximation. Designing and tuning digital current controllers in *s*-domain has a limited accuracy of representing the discrete-time phenomena in *s*-domain. Consequential errors are more emphasized in the frequency range next to the desired bandwidth. The errors get more visible as the frequency comes close to the desired bandwidth, which is close to 20% of the PWM frequency in cases with regular-sampling-double-update. In addition, rational approximation of delays also introduces the non-minimum phase phenomena that do not correspond to the behavior of the actual system. The above mentioned problems do not exist in cases where the controller design relies on direct digital design, and in particular on the implementation of the IMC concept in *z*-domain. In such cases, the errors introduced by *s*-model representation of discrete-time phenomena are absent.

In [19], the current controller is designed in *s*-domain, with approximation of discrete-time phenomena. The transport delay is equal to 3/2 of the sampling period, and it is approximated by Pade delay. This approximation has the phase error of 1 degree at 10% of the sampling frequency. The error rises to 8 degrees at 20% of the sampling frequency. The phase shift of the relevant vectors due to delay is compensated by introducing a "lead" compensation which rotates the vectors by an angle of $\omega\cdot\Delta t_{delay}$. The integrators are represented by Tustin approximation. Notwithstanding the decoupling measures, some cross-coupling effects remain due to delays. Remaining cross coupling is seen from non-diagonal elements. These cross coupling effects are seen in differential equation [19, Eq. 17] and the plant transfer function [19, Eq. 18]. The cross coupling is greatly reduced by MIMO design and a systematic procedure for an accurate tuning of the PI controller. The non-minimal phase due to numerator of [19, Eq. 23] causes some inaccuracy at the very beginning of transients.

4.4. Direct digital design with z-domain IMC

The effects caused by approximations inherent to *s*-domain design are also seen in the first four controllers considered in [11]. In the design IV.E of [11], where the approximations are not used and the IMC design is applied in *z*-domain, the open loop transfer function $W_{OL}(z) = i_{dq}(z)/\Delta i_{dq}(z)$ and the closed loop transfer function $W_{CL}(z) = i_{dq}(z)/i^{*}_{dq}(z)$ do not have the cross coupling terms, and do not include delay-dependent factors. The function $W_{CL}(z)$ in [11, Eq. 12] represents the ratio between the output current $I_{dq}(z) = I_d(z) + j\, I_q(z)$ and the corresponding reference. The imaginary part of this $W_{CL}(z)$ is equal to zero. Therefore, the *q* axis output current is not affected by the *d* axis reference, and vice versa. The input step response obtained with the current controller of [11, IV.E] does not depend on the excitation frequency, proving the effective decoupling. It has to be noticed at this point that the above conclusions consider the closed loop transfer function. The same does not hold for the disturbance transfer function, which relates the output to the voltage disturbance. While the IMC-designed controller W_C of Fig. 9 gets multiplied with W_P to obtained ($W_P W_C$), the product free from any coupling terms; the electromotive force in Fig. 9 acts between W_P and W_C. This results in the disturbance transfer function which comprises the factor W_P on its own, without getting multiplied by W_C. Thus, the undesired coupling does not get canceled in disturbance transfer function, which depends on the fundamental frequency even in systems with DDC-IMC designed controllers. The same holds in all the competitive current controllers [14], where the response of the output current to changes in the electromotive force depends on the fundamental frequency. Disturbance response of the current controller is of considerable importance, but it falls out of the scope of this paper. At the same time, the electromotive force in synchronous permanent magnet motors comes as a product of the constant flux of the magnets and the revolving speed. Therefore, the changes in the electromotive force are determined by the speed changes, which are considerably slower than the current loop transients. In grid connected inverters, where the electromotive force gets substituted by the mains voltage, disturbance transfer function is of particular importance. Namely, it describes the capability of the current loop to reject the low order harmonics of the grid and prevent them from introducing distortion in the output current.

4.5. The ratio between proportional and integral gains

The IMC design in *s*-domain results in $W_C(s) = \alpha R/s + \alpha L + j\alpha\omega L/s$. The ratio between the proportional gain αL and the integral gain αR is defined by the electrical time constant, and it has to be maintained in order to cancel the undesired plant dynamics. Direct digital design and the use of the IMC method in *z*-domain results in the current controller given in [11, Fig. 10] and [11, Eq. 11]. It has the proportional gain of $\alpha L/T_{SPL}$ and the integral gain of αR. Hence, the ratio between the proportional and integral gain has to remain equal to $(1/T_{SPL})(L/R)$ in order to maintain the desired decoupled operation.

Within the closed loop transfer function W_{CL}, the pulse transfer of the controller W_C is multiplied by the plant W_P to obtain the product $W_C W_P = i_{dq}(z)/\Delta i_{dq}(z)$. With DDC-IMC design [11, IV.E], $W_C W_P$ does not have any coupling terms. Relying on that, it is possible to add the term $W_F(z)$ in the feedback path and to perform the gain setting assuming that the coupling between the orthogonal axis does not exist. As long as the function $W_F(z)$ does not introduce the coupling terms of its own, the closed loop gain $W_C W_P W_F$ and the closed loop transfer function $W_C W_P/(1+W_C W_P W_F)$ will remain coupling-free.

The previous conclusions can be applied to Fig. 9, where DDC-IMC designed controller W_C multiplies the plant transfer function W_P and provides the direct-path gain $W_P W_C$ with no diagonal elements. With proper implementation, the transfer function W_F of (2) does not introduce any coupling elements. Therefore, the analysis and the parameter setting of the system with one-PWM-period averaging in the feedback path can be performed by adopting SISO approach, as already done in previous subsections.

While applying the SISO design procedure, a particular attention has to be paid to the parameter setting procedure. Namely, the choice of the proportional and integral gains is not free. In order to maintain the decoupled operation, the gains have to maintain the ratio $(1/T_{SPL})(L/R)$.

5. THE OPTIMUM PARAMETER SETTING

Design and tuning of digital current controllers has attracted considerable attention. A comprehensive and instructive summary of most relevant controllers is given in [11]. It includes several *s*-domain approaches to designing and tuning the digital current controllers, as well as the case with direct digital control (DDC) with z-domain implementation of the IMC concept. While the other approaches introduce a number of *s*-domain approximations of discrete-time features, and therefore introduce additional coupling terms, the approximation-free DDC-IMC concept provides a flawless decoupling. The controller W_C comprises the basic proportional and integral actions along with several decoupling terms that include $\exp(j\omega T_{SPL})$ elements. Therefore, parameter tuning procedure has to establish the proportional and integral gains that provide the desired response. In current controller design IV.E of [11], the open loop transfer function and the closed loop transfer function do not have the cross coupling terms, and they do not include delay-dependent factors. Based upon that, we concluded that in the systems with DDC-IMC designed controller, the feedback filtering and the parameter setting procedure can be performed on a simplified, more transparent and more intuitive bases. In order to keep decoupled response, it is necessary to maintain the ratio between the proportional and integral gains, which reduces the gain tuning to selecting one single parameter.

Performance of both closed loop transfer functions (9) and (13) depends on the closed loop gains p and i. With characteristic polynomials of the 4^{th} and the 5^{th} order, it is difficult to find analytical relation between the gains and the closed loop performance. Parameter setting procedure proposed in this Section envisages

(a) Definition of the performance criterion,

(b) The search of the *p*-*i* plane for the point which offers the best performance.

In order to obtain a fast, high-bandwidth response with well damped waveforms, the performance criterion includes the settling time t_{01}. The value of t_{01} has to do with the closed loop step response. Following the input step, the output of the system moves towards the target, and it settles on the target exponentially, or with some damped oscillations. After the time delay t_{01}, the output error falls into +/-1% wide strip. Following t_{01}, the error does not leave the strip, unless another input disturbance is received. The interval t_{01} is called "1% settling time", and it is of interest to keep it as small as possible. The settling time as performance criterion is an effective way of discarding the reponses which have a high bandwidth and a short rise time, but at the same time exhibit poorely damped response with oscillatory approach to the target value.

In addition to the settling time, it is also of interest to evaluate the robustness of the controller. Due to on-line changes in the system parmeters, such as the ac grid impedances in a grid connected power converter, it is of interest to maintain the stability and the response characters in the presence of variable parameters. The robustness of the system can be measured by the vector margin (VM), as effectively used in [11].

The vector margin is usually calculated from the open loop transfer function $W_{OL}(z)$. For the given excitation frequency ω, the argument z is $\exp(j\omega T_{SPL})$. While ω sweeps from 0 up to the Nyquist frequency, the values of $W_{OL}(z)$ are complex numbers which move in the complex plane and draw a graph. For the system stability, this graph must not pass through the point (-1, j0). The robustness can be judged from the the minimum distance (radius) between the graph and the point (-1, j0). The value of the radius is called the vector margin. With VM < 0.5, one would expect an oscillatory response that is likely to pass into instability in the case of a significant parameter change. The motivation of using a larger VM comes from the fact that magnetic saturation in electrical machines has considerable effect on the equivalent inductance of the stator winding. In this paper, there are two search runs for the optimum parameters. The first search assumes that the feedback gains p and i can be changed independently, while the second search respects the need to maintain a constant p/i ratio.

5.1. Parameter search in p-i plane

Parameter search performed in this subsection assumes that the feedback gains p and i can be changed independently. In other words, it is assumed that the ratio p/i does not have to be kept constant. The optimum gains p and i are searched for the closed loop transfer functions of (9) and (13). The space where the optimum gains are searched is a domain in the 2-dimensional p-i space, limited by $p > 0$, $i > 0$, and by $p < 1$, $i < 1$. The search method is rather simple, it starts by selecting a large number of equally spaced discrete gains along both axes, it proceeds by calculating the performances for each pair of the gains (p, i), and ends by selecting best pair of gains according to design criteria. The optimum gains are searched for the execution schedule of Figs. 7 and 8. In both cases, the search method provided the optimum gains (p, i), the frequency f_{45} where the phase of W_{CL} drops to -45°, the frequency f_{bw} where the amplitude of W_{CL} drops to -3dB, the vector margin VM, and the overshoot of the step response. All the results are obtained with f_{PWM} = 10kHz. The results are summarized in Table 1. In cases with VM > 2/3 (p < 0.0777 in Table 1), the character of the closed loop response is maintained for a wide range of parameter changes. The step responses are compared in Fig. 10.

It has to be noted in Table 1 that, although the ratio p/i is not fixed, the ratio between the optimum gains remains close to $(1/T_{SPL})(L/R)$. The ratio p/i is equal to 119 for the schedule of Fig. 8, and 131 for the schedule of Fig. 9. For the given motor, the ratio $(1/T_{SPL})(L/R)$, required for the decoupled operation is equal to 144. Hence, in a way, the search procedure finds the optimum close to the area which secures decoupled operation. It is of interest to perform the search procedure where the ratio p/i is kept constant and equal to $(1/T_{SPL})(L/R)$.

5.2. Parameter search with constant p/i ratio

Although there are two gains, p and i, they have to maintain the same ratio, determined by parameters L and R, in order to preserve the proper decoupling between d and q axis [11], [14]. Therefore, it is of interest to consider the changes of the gain p, assuming that the ratio p/i remains unaltered and equal to $(1/T_{SPL})(L/R)$. In this case, the search results are

given in Table 2. With an overshoot of 2.64%, the closed loop bandwidth reaches 20% of the switching frequency.

In Table 2, the gain p sweep from 100% to 150% of the optimum value makes the overshoot increase from 3.4% up to 22%, while the closed loop bandwidth increases from 21% up to 33% of the switching frequency. Starting with the optimum gain setting, the gain reduction of 50% leads to an overshoot of 0%, while the closed loop bandwidth drops to 7% of the switching frequency. Stability limit is reached with the gain equal to 410% of the optimum value.

Comparable state-of-the-art solutions are summarized in [11] and [14]. They do not use one-period-averaging, and rely instead on regular-sampling-double-update with one sample in each $T_{PWM}/2$. In Table 1 of [11], the closed loop bandwidth of a well damped, low overshoot response reaches 10% of the sampling frequency (20% of the switching frequency). In Figs. 12-14 of [14], a well damped, low overshoot response has the rise time of 5-6 sampling times. The corresponding bandwidth is, roughly, $0.35/(5 \cdot T_S) = 0.07 \cdot f_S$, (14% of the switching frequency). Solution devised in this paper has an additional delay, caused by the feedback averaging. With devised control methods, the consequential closed loop bandwidth of Table 2 is better than with comparable solutions.

Table 1 Performance factors obtained with the optimum gains and with the execution schedule of Figs. 7 and 8. Parameter search is performed in two dimensional space, with unconstrained proportional and integral gains.

Schedule	p	i	f_{45} [Hz]	f_{bw} [Hz]	VM	Overshoot [%]	t_{01}
Fig. 8	0.0442	0.00037	541	1177	0.677	0.84	21
Fig. 9	0.0708	0.00054	994	1882	0.705	0.67	9

Table 2 Parameter search is performed for the schedule of Fig. 9, and for fixed ratio between the proportional and integral gains.

Schedule	p	f_{bw} [Hz]	VM	Overshoot [%]
Fig. 9	0.065	1607	0.722	0.42
Fig. 9	0.067	1687	0.715	0.75
Fig. 9	0.071	1862	0.701	1.61
Fig. 9	0.075	2005	0.689	2.64
Fig. 9	0.077	2116	0.679	3.45
Fig. 9	0.081	2252	0.668	4.8
Fig. 9	0.086	2474	0.648	6.8
Fig. 9	0.091	2618	0.636	8.4
Fig. 9	0.095	2753	0.623	10.2
Fig. 9	0.1	2912	0.607	12.1
Fig. 9	0.116	3382	0.553	22

6. EXPERIMENTAL RESULTS

The experimental verification of the two current controllers is performed on an experimental setup which comprises a synchronous motor with surface mounted magnets, a PWM inverter and a digital control platform. The stack length of the motor is L = 128mm, and it has 6 poles. The rated torque is 7.3 Nm while the rated current is 7.3 Arms. The motor has stator resistance of 0.47Ω and the inductance of 3.4 mH. The PWM inverter has the dc-bus voltage of E_{DC} = 520V, and it has the switching frequency of 10kHz. The rated

lockout time is set to 3μs. The digital control platform uses TMS320F28335 DSP. It has the ADC unit with 12-bit resolution and with 16 input channels. The oversampling mechanism acquires 32 samples per base period. The sampling and storing is automated by embedded DMA machine. The anti-aliasing filters are designed as passive *RC* filters, using the standard procedures, and also taking into account the fact that the effective sampling frequency is 32 time larger. With one-PWM-period-averaging, the effective Nyquist frequency is increased 32 times, as well as the desired cutoff frequency of the analog anti-aliasing filters. Therefore, it is possible to design a passive anti-aliasing filter that would remove any residual noise, while having the cutoff frequency considerably above the desired bandwidth. Thus, the impact of such anti-aliasing filter on phase lag, delays and the closed loop dynamics is negligible, and it has no detrimental effects on the closed loop response.

In most reports on digital ac current controllers, the experimental waveforms of the output current in *dq* frame are calculated by the DSP controller, and then written on a DAC or copied into a PC. Similar procedure is not feasible with the present system of Fig. 9, where the output current $i^{dq}(z)$ gets filtered through the block $W_F(z)$ to obtain the feedback signal $i_F{}^{dq}(z)$. It has to be noted at this point that the only signal available to the DSP controller is the feedback signal. For that reason, the output current $i^{dq}(z)$ cannot be observed from the registers of the DSP controller. The only way to access the output current instead of the average feedback is direct measurement of the actual motor current. The phase current does reflect the changes in $i_d(t)$ and $i_q(t)$, but it is also affected by the rotor position. Therefore, experimental traces in Fig. 11 are obtained with the rotor locked in position where the measured phase current gets equal to the *q*-axis current. It has to be notice though that this approach does not allow the experimental verification of the axes decoupling at high speeds. In this regard, the authors rely on the analytical and experimental findings of [11], which considers the direct digital design and the implementation of the IMC approach in *z*-domain, the approach also used in this paper. Results of [11] prove that any coupling is removed, while the input-step response does not depend on the excitation (fundamental) frequency.

The execution of the control interrupt takes 3.5μs on the selected DSP platform. Therefore, for the scheduling scheme of Fig. 9, the interrupts were triggered 4μs prior to each PWM counter event. Experimental traces are obtained in Fig. 11, showing a reasonable similarity with the simulation results shown in Fig. 10. All the measurements were done at the zero speed, with the rotor locked in position where the measured phase current corresponds to the *q* axis current.

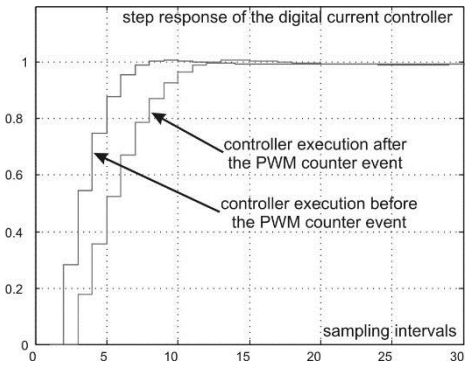

Fig. 10 Step response with execution schedules outlined in Figs. 7 and 8.

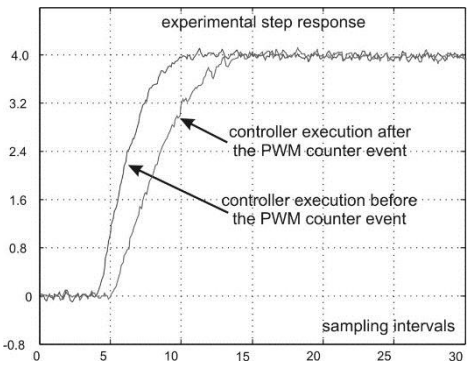

Fig. 11 Experimental step responses with schedules of Figs. 7 and 8.

7. CONCLUSIONS

This paper deals with practical implementation of digital current controllers, which represent the key elements in majority of contemporary static power converters. High performance current controllers are required in the electrical drives and also in grid connected converters. A high bandwidth and considerable robustness are of uttermost importance in all applications of digital current controllers. In this paper, a novel approach to acquiring and filtering the feedback signal is proposed. Devised approach is free from sampling errors and it introduces only a minimum delay into the feedback path. We also consider the transport delays in the voltage actuation path and the transport delays in the feedback path. Proposed parameter setting procedures takes into account the delays, and it meets both the bandwidth requirements and the robustness against the noise and the parameter changes. Proposed results are verified by simulation and also on an experimental setup comprising a brushless dc motor, a PWM inverter and a DSP-based control platform. For the relative gain $p = 0.075$, and for gain ratio p/i determined by the IMC procedure, the closed loop bandwidth reaches 20% of the switching frequency (that is, 10% of the sampling frequency) with an overshoot of 2.64% and with a vector margin of 0.689. The system parameters can to change more than 4 times before entering the instability region. Devised control solutions have the potential of reducing the noise sensitivity and improving the closed loop performance of digital current controllers applied in 3 phase ac drives and in grid connected power converters.

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