FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 28, N^o 4, December 2015, pp. 507 - 525
DOI: 10.2298/FUEE1504507S

HORIZONTAL CURRENT BIPOLAR TRANSISTOR (HCBT) – A LOW-COST, HIGH-PERFORMANCE FLEXIBLE BICMOS TECHNOLOGY FOR RF COMMUNICATION APPLICATIONS

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Abstract. *In an overview of Horizontal Current Bipolar Transistor (HCBT) technology, the state-of-the-art integrated silicon bipolar transistors are described which exhibit f_T and f_{max} of 51 GHz and 61 GHz and f_TBV_{CEO} product of 173 GHzV that are among the highest-performance implanted-base, silicon bipolar transistors. HBCT is integrated with CMOS in a considerably lower-cost fabrication sequence as compared to standard vertical-current bipolar transistors with only 2 or 3 additional masks and fewer process steps. Due to its specific structure, the charge sharing effect can be employed to increase BV_{CEO} without sacrificing f_T and f_{max}. Moreover, the electric field can be engineered just by manipulating the lithography masks achieving the high-voltage HCBTs with breakdowns up to 36 V integrated in the same process flow with high-speed devices, i.e. at zero additional costs. Double-balanced active mixer circuit is designed and fabricated in HCBT technology. The maximum IIP3 of 17.7 dBm at mixer current of 9.2 mA and conversion gain of -5 dB are achieved.*

Key words: *BiCMOS technology, Bipolar transistors, Horizontal Current Bipolar Transistor, Radio frequency integrated circuits, Mixer, High-voltage bipolar transistors.*

1. INTRODUCTION

In the highly competitive wireless communication markets, the RF circuits and systems are fabricated in the technologies that are very cost-sensitive. In order to minimize the fabrication costs, the sub-10 GHz applications can be processed by using the high-volume silicon technologies. It has been identified that the optimum solution might

Received March 15, 2015
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be to use a coarser-lithography BiCMOS technology [1, 2], instead of an advanced-lithography pure CMOS technology [3]. Moreover, the bipolar part should be integrated with CMOS with a minimum addition to process complexity, which could make the high-performance Si/SiGe BiCMOS technologies [4] prohibitively expensive.

On the other hand, Horizontal Current Bipolar Transistor (HCBT) [5, 6] is a very compact structure, outperforming all the existing Lateral Bipolar Transistors (LBTs) [7, 8]. HCBT is fabricated in a simple technology without the need for the steps that are standard in the vertical-current bipolar structures, i.e. without n^+ buried layer, epitaxial growth, base polysilicon layer, emitter-base spacers, collector plug implantation, deep trench isolation etc., which makes it attractive for the very low-cost, high-performance BiCMOS technology.

HCBT is invented at the Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia, [9, 10] and its characteristics has been improved over 3 generations of transistors. At first, the technology concept has been demonstrated by using coarse contact lithography having transistors of with cutoff frequency (f_T) of 4.4 GHz and collector-emitter breakdown voltage (BV_{CEO}) of 15.8 V [11]. In the second generation of HCBT, the 0.5 μm stepper lithography has been used reaching f_T=30.4 GHz and BV_{CEO}=4.2 V which became the fastest lateral bipolar transistor [12, 13]. Finally, HCBT has been integrated with CMOS and further optimized having f_T=51 GHz and BV_{CEO}=3.4 V [5, 14], which is among the fastest pure-silicon bipolar transistors reported [15].

In this paper, an overview of the most advanced HCBT technology is given, showing all the innovative technology steps and specific device effects that have enabled the record-breaking electrical characteristics. Furthermore, the mixer is demonstrated as an RF circuit fabricated in HCBT technology [16], together with high-voltage HCBT structures [17-19], which broaden the application spectrum of HCBT BiCMOS technology platform.

2. HCBT FABRICATION

The HCBT structure with a single polysilicon region is fabricated by using a commercial 180 nm CMOS process, which features dual gate oxide thicknesses of 3 nm and 7 nm for 1.8 V and 3.3 V supply voltages, respectively. Both nMOS and pMOS transistors are made with 2 versions of threshold voltages (V_{th}), optimized for high-speed and low stand-by power consumption at 1.8 V supply voltage. The CMOS process features 6 aluminum layers and poly-poly and metal-metal capacitor modules.

The HCBT fabrication sequence is depicted in Fig.1. The active transistor region is processed in the silicon sidewall defined by the Shallow Trench Isolation (STI), which is 350 nm deep with the sidewall at approximately 80° angle relative to the surface. The active sidewalls of HCBT are aligned to (100) crystal direction. After the implantation of the CMOS n- and p-wells, the 1st HCBT mask is used for the implantation of the n-hill collector region as shown in Fig. 1.a. The n-hill is implanted by phosphorus and consists of 3 steps with the energies of 340 keV, 220 keV and 110 keV. Alternatively, the CMOS n-well can be used for the collector n-region and the 1st HCBT mask is not needed, resulting in the even lower-cost process.

The CMOS gate polysilicon layer is left at the emitter side of the n-hill at the distance of 500 nm (Fig. 1.b), in order to obtain the desirable final shape of the emitter n^+ polysilicon region. After the gate polysilicon etching, re-oxidation and source/drain

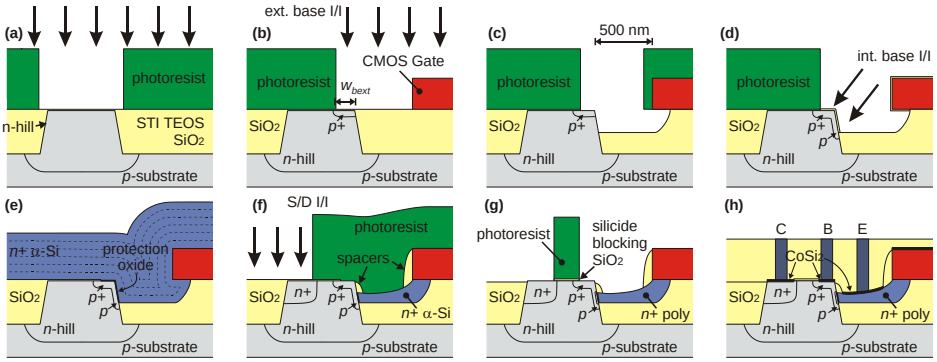


Fig. 1 Fabrication sequence of HCBT with a single polysilicon region.

extension implantation for MOS transistors, the extrinsic base is implanted by using the 2nd HCBT mask (or the 1st, if the n-well collector is used), as shown in Fig. 1.b. The edge of the mask across the n-hill determines the extrinsic base width (w_{bext}) and the distance between the extrinsic base and the n^+ collector region. The extrinsic base is annealed together with the source/drain extensions, which is a CMOS baseline process step.

The 3rd HCBT mask (or the 2nd in the case of the n-well collector) is used for STI oxide etching after the source/drain annealing. The STI oxide is timed etched, as shown in Fig. 1.c, defining the trench for the emitter polysilicon region. The thickness of the remaining oxide at the n-hill sidewall is around 100 nm. The 10 nm of TEOS oxide is deposited next and the 2nd HCBT mask (or the 1st in the case of the n-well collector) is used again for the intrinsic base implantation, which is performed at a tilt angle of 30° using BF_2, as shown in Fig. 1.d.

The RTA process at 800°C is carried out, followed by the deposition of 450 nm of *in situ* doped amorphous silicon (α-Si) layer as shown in Fig. 1.e. The n^+ α-Si layer fills the emitter trench near the active sidewall and under the CMOS gate. The α-Si is then timed etched by Tetramethyl Ammonium Hydroxide (TMAH) and is removed across the wafer except in the emitter trench (Fig. 1.f). Since the TMAH etchant is very selective to the oxide, the n-hill is protected from etching by a thin layer of oxide grown during the pre-deposition RTA step, as shown in Fig. 1.e. In this way, the emitter n^+ region is formed, while the base and the n-hill are protected by the thin oxide layer. The CMOS gates are protected from TMAH etching by the oxide encapsulation, grown during gate re-oxidation process.

The CMOS gate at the emitter side of the n-hill makes it possible to obtain the shape of emitter n^+ α-Si layer with the minimum thickness very close to the active sidewall, as can be seen in the TEM cross-sections in Figs. 2.a and 2.b. If the CMOS gate is not used (Fig. 3), the emitter α-Si is the thinnest in the middle of the trench, which limits its thickness at the active sidewall. Fig. 3.a depicts the marginal case of HCBT without CMOS gate, where the emitter contact barely sits on polysilicon, but its thickness at the active sidewall is 125 nm. By using the CMOS gate, the emitter polysilicon thickness at the active sidewall is 85 nm (Fig. 2.b) and it increases toward the contact. Additionally, the use of CMOS gate requires a deposition of thinner polysilicon layer to fill the emitter trench, which improves the controllability of the final polysilicon thickness.

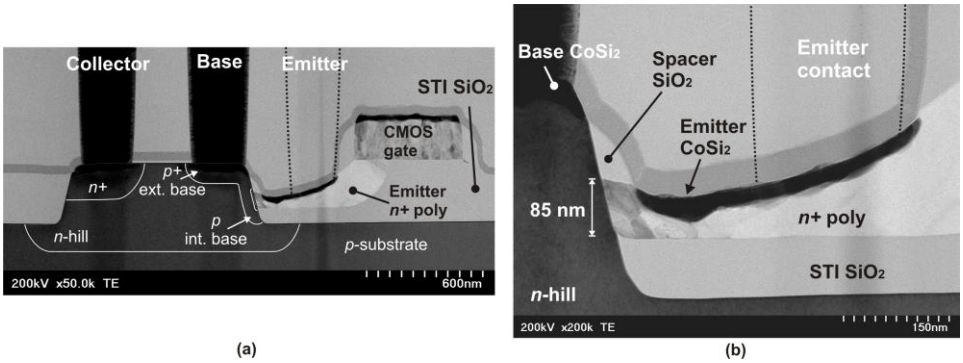


Fig. 2 TEM cross-section of the processed HCBT structures with a single polysilicon region: (a) the whole transistor structure with CMOS gate, (b) close-up of the active sidewall. The emitter contact is out of the image plane and is hand-sketched.

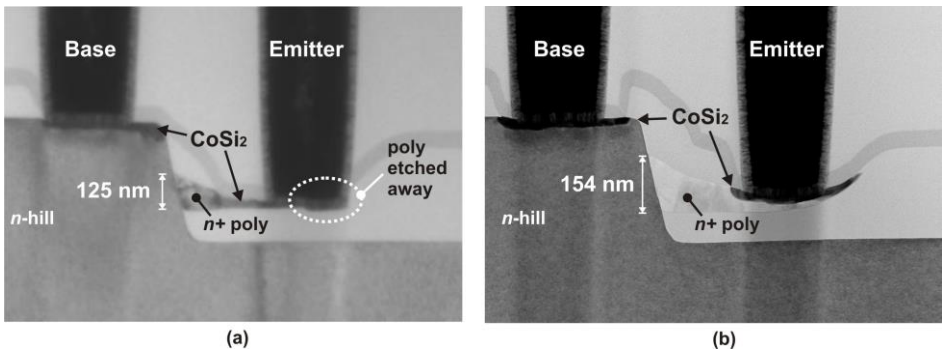


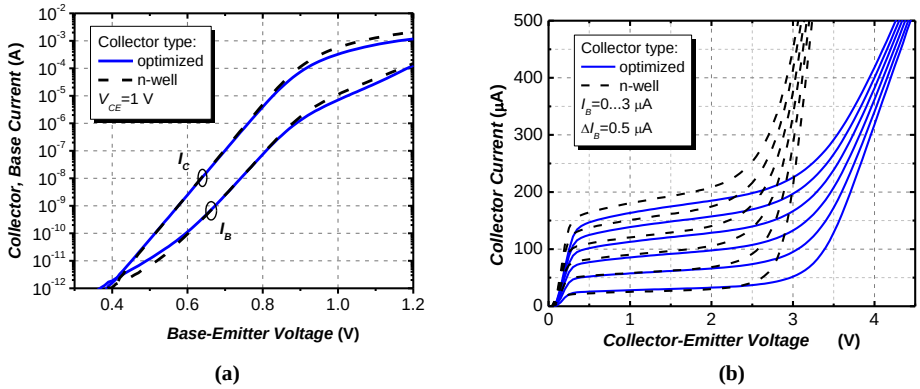
Fig. 3 TEM cross-section of the processed HCBT structures without CMOS gate: (a) excessive n^+ amorphous silicon etching and removed n^+ polysilicon under the emitter contact, (b) exact n^+ amorphous silicon etching, but too thick n^+ polysilicon (154 nm) at the n-hill sidewall.

The CMOS spacers are formed at the n-hill sidewalls above the n^+ α-Si layer and serve to isolate the emitter and base silicides from each other, as shown in Fig. 1.f. Next, the source/drain implantation mask of the nMOS transistor is also opened above the n-hill and the collector n^+ region is obtained (Fig. 1.f). The source/drain junction depth is around 200 nm, reaching deeper than the extrinsic base junction. The emitter drive-in diffusion is performed during source/drain annealing and α-Si layer crystallizes forming the emitter n^+ polysilicon region. The silicide-blocking oxide layer has to be left between the extrinsic base and the implanted n^+ collector in order to prevent the collector base shorts, also used in standard CMOS contact processing (Fig. 1.g). The final HCBT structure with a single polysilicon layer is shown in Fig. 1.h.

3. HCBT ELECTRICAL CHARACTERISTICS

The electrical characteristics of the HCBT with the optimized collector fabricated by a separate implantation are compared with the lower-cost HCBT with CMOS n-well region used as collector. The collector profile of the optimized HCBT is designed to obtain a uniform electric field in the collector-base depletion region resulting in an optimum trade-off between the f_T and f_{max} and collector-emitter breakdown voltage (BV_{CEO}). This effect is specific to HCBT structure and can be used as an additional technological step to optimize transistor characteristics, which will be analyzed further in Section 4.

The Gummel plots and output characteristics of the optimized and n-well HCBTs are shown in Fig. 4 and the electrical parameters are summarized in Table 1. Both transistors are optimized for maximum f_T and f_{max} and have a modest current gain (β) of around 70. The n-well HCBT has a higher extrinsic base doping level reducing the electron component of the base current. The n-well HCBT has BV_{CEO} = 2.8 V, whereas the optimized HCBT has BV_{CEO} = 3.4 V, which makes it more suitable for the use in the circuit applications with voltage supply of 3.3 V.



(a) **(b)**

Fig. 4 Measured DC characteristics of HCBT with a single polysilicon region with emitter area 0.1×1.8 μm^2 with the optimized collector and n-well collector: a) Gummel plots, i.e. I_B and I_C vs V_{BE}, and b) output characteristics, i.e. I_C vs V_{CE}.

Table 1 Electrical parameters of HCBT with the optimized collector and n-well collector

	optimized	n-well
Emitter area	0.1 x 1.8 μm^2	
Peak β	72	76
BV_{CBO} (V)	9.5	8.3
BV_{CEO} (V)	3.4	2.8
V_A (V), V_{BE}=0.85 V	16	15
V_A (V), I_B=5 μA	10	11
C_{BC} (fF) @ V_{CB}= 1 V	1.1	1.6
R_B (Ω), circle imp.	480	430
f_T (GHz) @ V_{CE}= 2V	51	43
f_{max} (GHz) @ V_{CE}= 2V	61	56
$f_T BV_{CEO}$(GHzV)	173	120

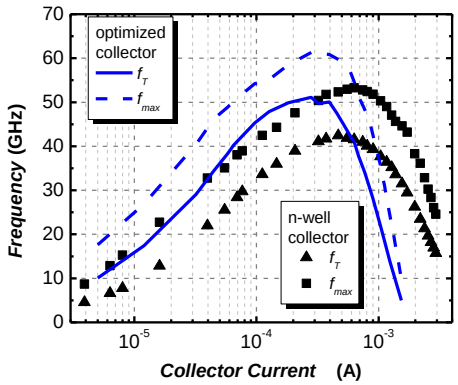


Fig. 5 Cutoff frequency (f_T), and maximum frequency of oscillations (f_{max}) vs. collector current (I_C), of HCBT with emitter area 0.1×1.8 μm^2 with the optimized collector and the n-well collector, at V_{CE}=2 V.

The high-frequency characteristics of the optimized and n-well HCBTs are shown in Fig. 5. The optimized HCBT has f_T and f_{max} of 51 GHz and 61 GHz, respectively, and $f_T BV_{CEO}$ product equals 173 GHzV, which is among the highest reported for the implanted-base Si BJTs and very close to the theoretical Johnson's limit [20]. The n-well HCBT has f_T and f_{max} of 43 GHz and 56 GHz, respectively. The f_T and f_{max} of n-well HCBT fall off at higher currents due to the increased collector concentration. However, the peak values are lower for n-well HCBT due to the increased neutral base width and due to the effect of charge sharing between the extrinsic and intrinsic base regions, which will be explained in more details in Section 4. Peak f_T and f_{max} of n-well HCBT are still high enough for wireless applications and it can be used as a low-cost technology. Both HCBTs have a small collector-base capacitance (C_{BC}) per emitter length of less than 0.8 fF/μm, which makes them attractive for low-power circuit applications.

The Early voltages (V_A) of the optimized HCBT are equal to 16 V and 10 V for constant V_{BE} and for constant I_B, respectively, and 15 V and 11 V for n-well HCBT. Since both transistors are optimized for maximum speed, V_A for constant I_B are relatively low, but it can be improved by reducing collector doping level and traded for f_T in such a case.

4. COLLECTOR DOPING PROFILE EFFECT ON ELECTRICAL CHARACTERISTICS

In standard vertical-current bipolar transistors, the intrinsic and extrinsic base regions are formed at the wafer surface next to each other, resulting in classical planar collector-base pn-junction. On the other hand, in HCBT structure, the extrinsic base p^+-region and the intrinsic base p-region form the angle of approximately 100°, because the extrinsic base is implanted at the wafer surface, whereas the intrinsic base is implanted at the n-hill sidewall. Hence, the ionized donor charge on the n-collector side of the collector-base pn-junction is shared between the intrinsic and the extrinsic base acceptors, since the collector is surrounded by the extrinsic and intrinsic base regions. Therefore, the depletion region has to extend to the collector side and to shrink at the base side to reach the charge balance [21], as shown in Fig. 6, reducing the electric field as a result. As a

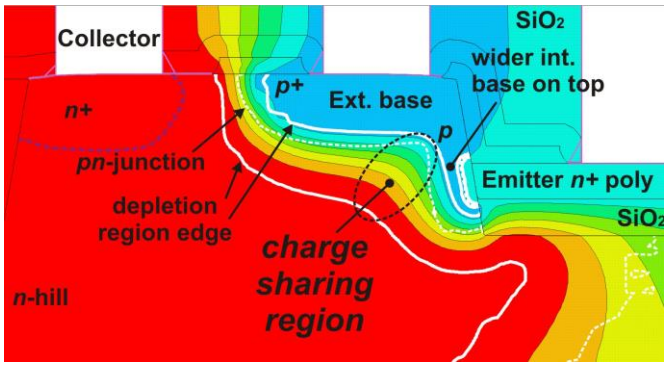


Fig. 6 Simulations of HCBT cross-section showing the potential distribution in the collector-base depletion region.

consequence, the intrinsic base is locally wider at the top of emitter reducing the I_C, β and f_T. Hence, the collector doping must be increased just under the extrinsic base to suppress the charge sharing effect, i.e. to reduce the neutral base widening and the extension of the depletion region.

In order to examine the effect of collector design and to optimize the HCBT characteristics, two structures with different collector doping profiles, as shown in Fig. 7, are compared [22]. HCBT with Collector 1 has a steeper doping profile than HCBT with Collector 2, i.e. a higher doping concentration at the top of the intrinsic base, just under the extrinsic base, where the charge sharing effect is mostly pronounced. A distribution of impact ionization rates are simulated and shown in Fig. 8. Non-local impact ionization based on lucky electron model with hard threshold energy is used. The peak impact ionization rates are $1.4 \cdot 10^{24}$ $cm^{-3}s^{-1}$ and $7.9 \cdot 10^{24}$ $cm^{-3}s^{-1}$ for collector 1 (steep n-hill) and collector 2 (uniform n-hill), respectively. The HCBT with collector 2 (uniform n-hill) has a higher impact ionization rate and it occurs at the bottom of the base, because the current density is the highest in this region due to the narrowest neutral base there. Moreover, the electric field is reduced at the top of the base due to the charge sharing effect reducing the impact ionization rate there. Additionally, the rounded shape of the collector-base

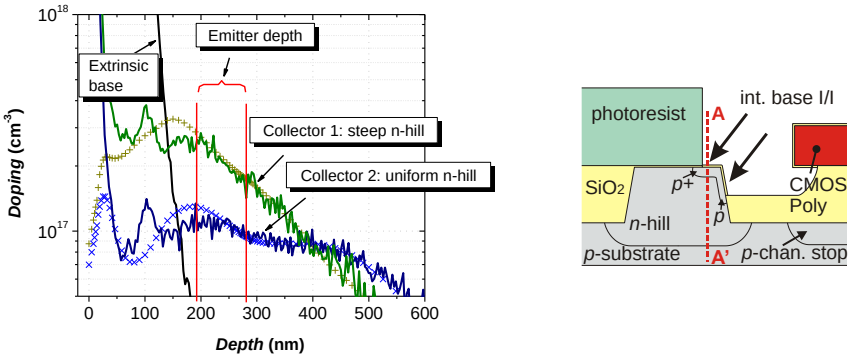
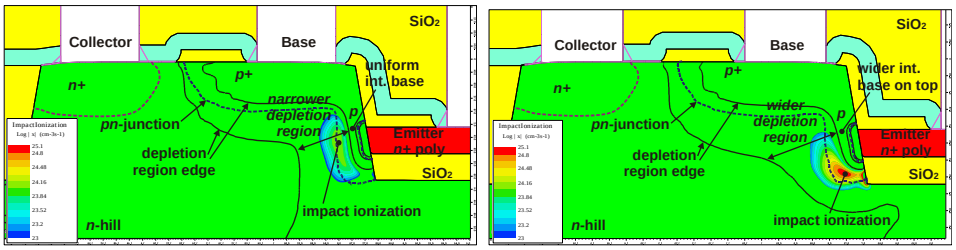


Fig. 7 Measured SIMS (lines) and simulated (symbols) doping profiles of collector region along the cross-section AA', after all of the CMOS annealing steps.

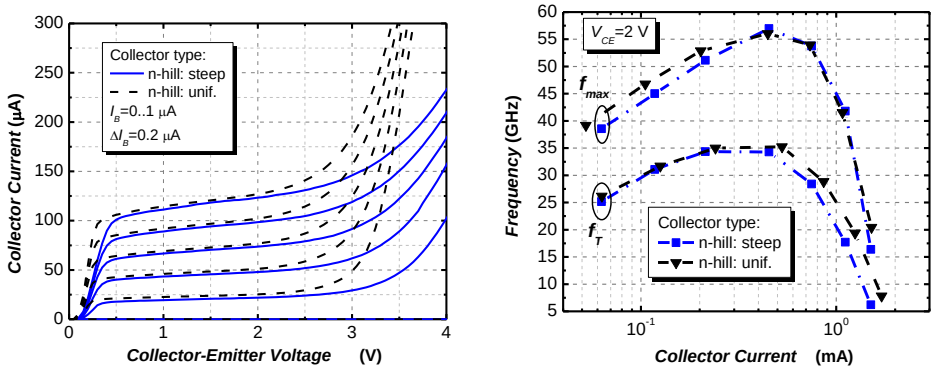


(a) (b)

Fig. 8 Cross-sections of the simulated impact ionization rate distribution of HCBT structures with: (a) Collector 1 (steep n-hill), (b) Collector 2 (uniform n-hill), at V_{BE}=0.7 V and V_{CE}=2 V.

depletion region at the bottom of the base causes the reverse charge sharing effect increasing the local electric field there. The HCBT with collector 1 (steep n-hill) has a smaller impact ionization rate since the doping profile reduces charge sharing effect, and also decreases electric field at the bottom of the base. Therefore, impact ionization rate does not have a peak as sharp as in uniform collector, but is more uniformly distributed along the intrinsic transistor.

The output characteristics depicted in Fig. 9.a show a lower BV_{CEO} for HCBT with Collector 2 (uniform n-hill) corresponding to the higher peak impact ionization shown in Fig. 8., and a higher BV_{CEO} for HCBT with steep collector profile due to the more uniform electric field and current flow distributions in the collector-base depletion region, and reduced impact ionization rate. As shown in Fig. 9.b, f_T and f_{max} are basically equal for two collector doping profiles. Therefore, due to the higher BV_{CEO} and equal f_T the HCBT with collector 1 (steep n-hill) has a higher $f_T BV_{CEO}$ product and represents an optimum HCBT design. The measured characteristics of HCBT with two different collectors are summarized in Table 2. Both transistors are designed to have a higher β comparing to the transistors described in Section 3 [5], by reducing the doping levels in the intrinsic base



(a) (b)

Fig. 9 Measured (a) output and (b) high-frequency characteristics of HCBT with a single polysilicon region with emitter area 0.1×1.8 μm^2 with Collector 1 (steep n-hill), with Collector 2 (uniform n-hill).

and collector and consequently resulting in a lower f_T. The HCBT with collector 1 (steep n-hill) has a higher collector resistance (R_C) due to the lower average collector doping level, but it still has a rather small effect on f_T and f_{max} as compared to the neutral base and collector-base depletion region time constants.

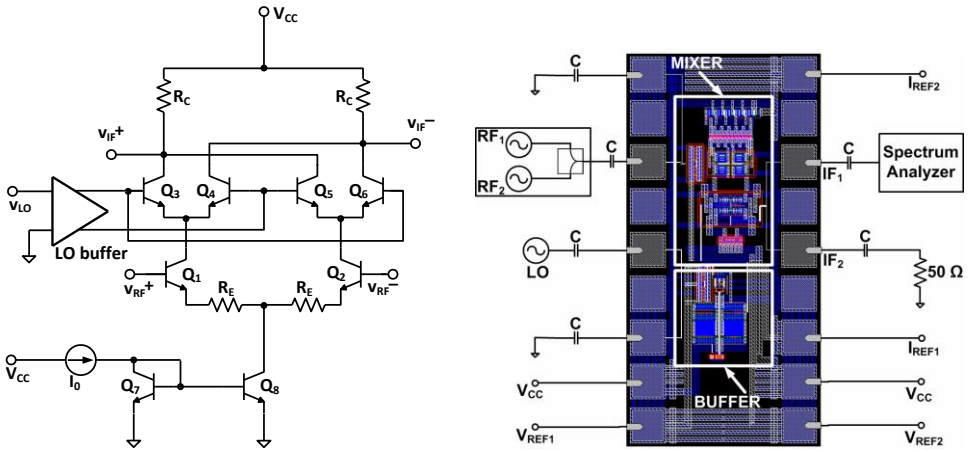
Table 2 Measured electrical parameters of HCBT with Collector 1 (steep n-hill), Collector 2 (uniform n-hill).

	Collector 1	Collector 2
Emitter area	0.1 x 1.8 μm^2	
Peak β	118	126
f_T (GHz)	34	35
f_{max} (GHz)	57	56
BV_{CEO} (V)	3.6	3.1
$f_T BV_{CEO}$(GHzV)	122	109
C_{BC}(fF) V_{CB}=1V	1.8	1.8
R_C (Ω), sat.	590	320

5. HCBT CIRCUIT DESIGN

Beside the characterization of transistor-level electrical characteristics, the HCBTs' performance is examined by using them in circuits. For this purpose, a down-converting mixer is designed and measured as the first RF circuit fabricated in HCBT technology [13]. Mixers are RF building blocks widely used in heterodyne transceivers [23]. Since most communication protocols involve an increasing number of users, the frequency spectrum is shared by multiple channels. In order to minimize the intermodulation distortion, the linearity is a critical parameter of wireless transceivers. Moreover, the linearity of radio receivers (also including bandpass filters and low-noise amplifier) are typically limited by the IM distortion of the first downconverting mixer [24]. Hence, mixer linearity must be as high as possible at a given power consumption, since many of applications include portable battery-supplied devices.

Double-balanced active mixer based on a Gilbert cell shown in Fig. 10.a is designed in three different HCBT technologies by using different collector doping profiles: HCBT 1 (steep n-hill), HCBT 2 (uniform n-hill) and HCBT 3 (CMOS n-well). Gilbert cell mixer consists of differential input amplifier (Q1, Q2) cascoded by a commutating circuit (quad) made by 4 transistors (Q3 – Q6). Since the IM distortion in such mixer is mainly caused by the input differential pair, degeneration resistances (R_E) are used to improve the linearity. The Local Oscillator (LO) buffer is used to convert the single-ended input to the differential signal for Gilbert cell and to provide the voltage swing high enough to switch the quad transistors on and off. All subcircuits (Gilbert cell, LO buffer, current source) are made with the same HCBTs in 3 different technology versions with different collector doping profiles. Power supply voltage is 5 V. All passive components are kept constant in all versions of circuits, such that the difference in the circuit performance can be attributed to the difference of the used transistors.



(a) (b)

Fig. 10 Double-balanced active mixer based on a Gilbert cell designed and fabricated in HCBT technology: (a) mixer schematic, (b) chip layout and test setup.

Mixers are measured on-wafer by using multi-contact probes with the setup shown in Fig. 10.b. The RF and LO ports are driven by a single-ended RF signal generator without any matching networks. The input impedances are designed to be 50 Ω, but the exact values are measured separately by using Vector Network Analyzer (VNA) and the input losses due to the impedance mismatch are taken into account. However, they are below 1 dB due to the small reflexion coefficient at both inputs. The output power is measured by spectrum analyzer connected asymmetrically to one output (collectors of Q3 and Q5), whereas the other output port is terminated by 50 Ω. The output impedance is also measured by VNA and the impedance mismatch loss together with the loss due to the single ended output is added to the measured output power.

The 3rd order input intercept point (IIP3) and conversion gain of mixers with 3 different HCBTs are measured at 1 GHz RF frequency and -10 dBm input power. The LO buffer is driven by RF generator with 0 dBm output power. The output frequency is 10 MHz and the two-tone spacing used in IIP3 measurement is 10 kHz. The measured IIP3 and conversion gain dependence on the mixer current (I_{mix}) (without the LO buffer current) are shown in Fig. 11. The maximum IIP3 of 17.7 dBm is achieved by mixer with HCBT 2 at I_{mix}= 9.2 mA, which is a small current for a given IIP3 as compared to the available mixers, e.g. [25]. The peak IIP3 of HCBT 1 and HCBT 3 are 10.9 dBm, and 14.7 dBm at currents 6.7 mA and 9.5 mA, respectively. If the power consumption of the mixer is critical, the IIP3 above 10 dBm can be obtained at current consumption between 5 mA and 6 mA by all three mixer designs, resulting in the power consumption between 25 and 30 mW. The conversion gains are rather constant with current (above 4 mA) with the maximum values of -4.2 dB, -5 dB and -5.5 dB for HCBT 1, HCBT 2, and HCBT 3, respectively. The maximum conversion gains are obtained at approximately the same current as the maximum IIP3. Such conversion gains are expected and are due to the use of emitter degeneracy and are traded for high IIP3s.

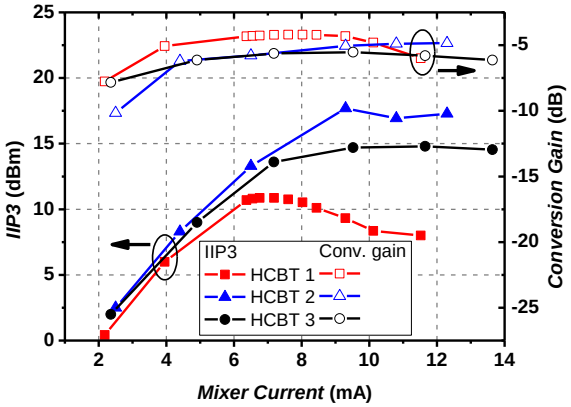


Fig. 11 Measured 3rd order Input Intercept Point (IIP3) and Conversion Gain vs. mixer current (I_{mix}) of mixers in three different technologies: HCBT 1 (steep n-hill), HCBT 2 (uniform n-hill) and HCBT 3 (CMOS n-well). Measurement setup: P_{RF}= -10 dBm, P_{LO}= 0 dBm, f_{RF}= 1 GHz, f_{IF}= 10 MHz, two-tone Δf= 10 kHz, V_{CC}= 5 V.

All three mixers have approximately the same linearity at low currents (below 6 mA), whereas the difference appears at higher currents, where the quad transistors (Q3 – Q6) operate near the high-current drop-off region, i.e. at or above the currents of peak f_T. The linearity of transistors in high-current regime is affected by the slope of f_T vs I_C characteristics at high currents, influenced by the charge sharing effect discussed in Section 4. It can be explained by the rate of base charge (Q_b) increase with I_C, which is the smallest for HCBT 2 with uniform n-hill collector profile. More detailed explanation is provided in [16]. High-current linearity can be improved for all collector doping profiles by increasing the size of quad transistors resulting in the operation at the lower current density avoiding the high-current drop-off region. However, the transistor operation below the current densities around peak f_T implies the increase of layout area.

6. High-Voltage HCBT Devices

6.1. Double-emitter (DE) HCBT

The HCBT structures described so far are optimized for high-frequency characteristics targeting RF communication circuit applications. In order to broaden the application spectrum of HCBT BiCMOS technology, i.e. for automotive, instrumentation and biomedical electronics, transistors with higher breakdown voltages are highly desirable. In standard vertical-current bipolar transistor structures based on the super-self-aligned transistor (SST), different breakdown voltage devices are typically obtained by the different parameters of Selectively Implanted Collector (SIC) [26], which usually requires additional lithography masks and increases the fabrication costs.

A high-breakdown voltage HCBT can be fabricated by placing two active transistor regions at the silicon sidewalls opposite to each other, such that their collector-base

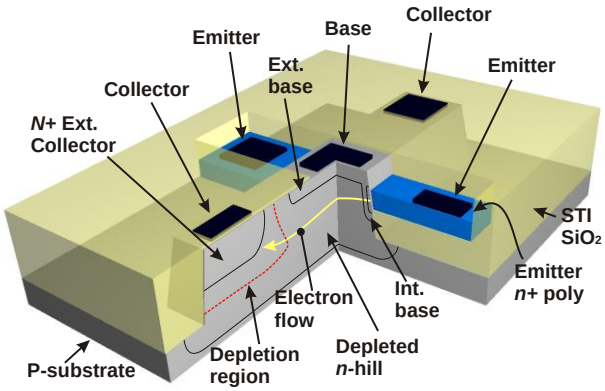


Fig. 12 3D schematic of double-emitter (DE) HCBT structure formed by merging two HCBTs in opposite directions resulting in the reduced electric field.

depletion regions merge, resulting in the reduced electric field. Such structure has two emitters opposite to each other and two collector contacts in the plane perpendicular to the direction that connects emitters, as shown in Fig. 12. The structure is named double-emitter (DE) HCBT [17, 18]. Since the two emitters of DE HCBT are placed at the opposite sidewalls of the silicon *n*-hill, extrinsic bases overlap on the top and intrinsic collector between two intrinsic bases is shared, as can be seen in Fig. 13.

The extrinsic collector is fabricated laterally in front and back of the intrinsic transistor. In such a way, the intrinsic collector is surrounded by p^+ extrinsic base from the top, two intrinsic bases from left and right and by the *p*-substrate from the bottom (Fig. 12). Since collector charge is shared between surrounding acceptors, collector is fully depleted by reverse collector-base voltage, if transistor operates in the forward active region. Once collector is fully depleted by collector-base reverse voltage (V_{CB}), the potential is pinned in the middle of the *n*-hill between two intrinsic bases, as shown in

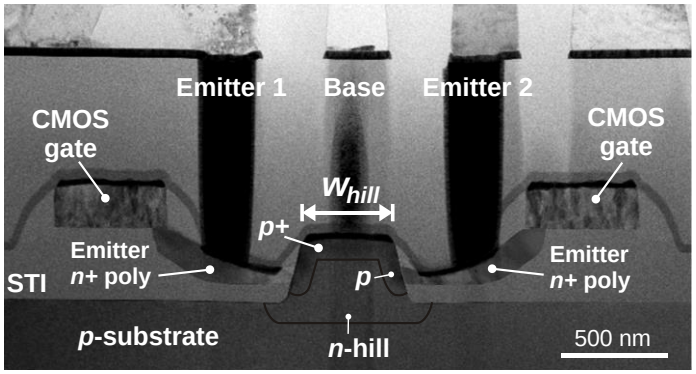


Fig. 13 TEM cross-section along the emitters of the fabricated double-emitter (DE) HCBT structure. Extrinsic collectors are in the front and the back.

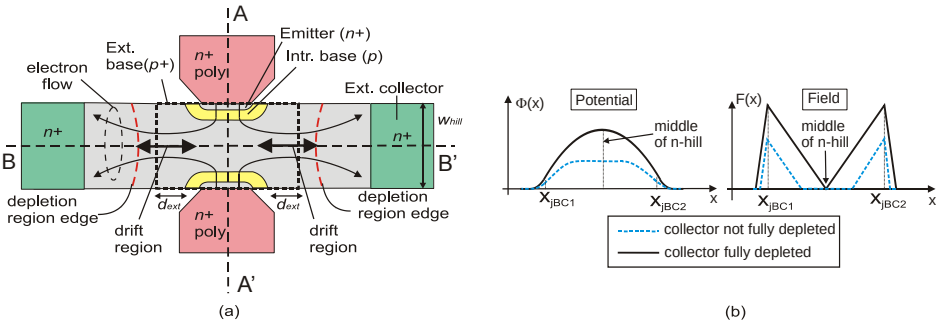


Fig. 14 (a) Schematic cross-section at the middle of the intrinsic transistor parallel with the wafer surface (top view). (b) Potential and electric field at the symmetry line along the middle of emitters (AA' line). In case of fully depleted collector maximum potential and electric field are limited due to limited amount of collector fixed charges. The rest of the voltage is dropped laterally across the drift region.

Fig. 14. Further increase in V_{CB} causes the potential drop laterally across the drift regions, which are formed toward the extrinsic collector, whereas the potential drop across the intrinsic base-collector junction remains roughly constant. Additional shielding of the intrinsic bases from the collector voltage is obtained by the extension of the extrinsic base on the top of the drift region, which is wider than the intrinsic base (Fig. 12), as well as by the substrate, which is connected to the ground potential in order to isolate the device. Eventual current leakage into the substrate might occur at very high current densities, but this is beyond the useable bias conditions.

Double-emitter HCBT is fabricated in the same fabrication flow as standard single polysilicon region HCBT with the steep collector profile [22], described in Sections 4 and 5. The only additional process step is eventually the ion implantation of the intrinsic base at the opposite side of the *n*-hill. No additional lithography masks are needed to integrate DE HCBT with standard HCBT BiCMOS.

The measured DC characteristics of DE HCBT are presented in Fig. 15. The Gummel characteristics (Fig. 15.a) show satisfactory quality of fabricated junctions. In the output characteristics (Fig. 15.b) with different *n*-hill widths (w_{hill}) it is obvious that DE HCBT has a higher BV_{CEO} and Early voltage (V_A) comparing to standard single-poly HCBT. The measured electrical parameters of two DE HCBTs and single-poly HCBT are summarized in Table 3. In order to take the full advantage of BV_{CEO} improvement and to maximize V_A for a given collector profile, transistors should be fabricated with a narrow n-hill, i.e. w_{hill} should be 0.5 µm or smaller. A hard breakdown cannot be observed in Fig. 15.b for V_{CE} lower than 10 V for all DE HCBT structures. In case of the transistor with w_{hill}=0.6 µm, the change in the slope indicates the start of the avalanche process, which is then limited by the base shielding effect at higher V_{CE}.

The BV_{CEO} is measured in forced V_{BE} configuration, where V_{BE} is set to 0.7 V and V_{CB} is swept. BV_{CEO} is determined as the V_{CB} where the base current (I_B) turns from positive to negative, increased by V_{BE}=0.7 V. For the transistor with w_{hill}=0.6 µm substantial avalanche current is generated for V_{CB} > 2.5 V reducing I_B and eventually reversing its direction. However, the slope of I_B characteristics becomes smaller for V_{CB} > 4 V

indicating that collector is fully depleted and electric field across the intrinsic base-collector junction as well as avalanche multiplication are limited. Even though I_B turns to negative, hard breakdown does not occur and the output characteristics in Fig. 15.b become flat. In case of the transistor with w_{hill}=0.5 μm, characteristics in Fig. 15.b show similar behavior. However, since w_{hill} is decreased, a smaller V_{CB} is needed to fully deplete collector and the base shielding effect is more efficient. Therefore, the electric field across the intrinsic base-collector junction is limited to lower value compared to the transistor with w_{hill}=0.6 μm. In case of the transistor with w_{hill}=0.36 μm, base shielding is the most efficient. The output characteristics in Fig. 15.b are flat, indicating that potential drop over the intrinsic base-collector junction does not increase substantially with V_{CB}, meaning that base width modulation is suppressed. Indeed, extrapolated Early voltage from the output characteristics between V_{CE}=5 V and V_{CE}=8 V for I_B=0.5 μA equals V_A=301 V. Giving the fact that the current gain at V_{CE}=5 V is β=95.4 this gives the $\beta \cdot V_A$ product as high as 28700 V.

Table 3 Measured electrical parameters of single-poly HCBT and double-emitter (DE) HCBTs with different width of the n-hill

	Single-poly	DE, w_{hill}=0.5 μm	DE, w_{hill}=0.36 μm
Emitter area (μm^2)	0.1 x 1.8	2 x (0.1 x 1.3)	
β_{max} (V_{CE}=2 V)	124	104	94
V_A, (V)	9.5	75	301
BV_{CBO} (V)	8.3	11.2	12.9
BV_{CEO} (V)	3.6	11.6	12.6
$V_{CB}@BV_{CEO}$ (V)	2.9	10.9	11.9
f_T (GHz)	37.6	13.6	12.7
f_{max} (GHz)	67	29.5	28
$I_C@f_{Tmax}$ (μA)	220	100	77
f_TBV_{CEO}(GHzV)	135	158	160
$\beta \cdot V_A$, (V),	1178 (V_{CE}=2 V)	7800 (V_{CE}=5 V)	28700 (V_{CE}=5 V)

It can be seen in Table 3 that the DE HCBT with narrower n-hill has a reduced f_T of 13.6 and 12.7 GHz for transistors with w_{hill} of 0.5 μm and 0.36 μm, respectively. Dominant cause of the lower f_T is the increase in the base-collector depletion region transit time, because electrons flow through the depleted n-hill region, which is approximately 1 μm long. Moreover, since w_{hill} is smaller than the emitter width (w_E), the current is crowded near the middle of the *n*-hill increasing the local current density and causing the Kirk effect to occur at lower values of I_C. Therefore, f_T peaks at lower I_C in DE HCBT. For transistors with smaller w_{hill}, BV_{CBO} is increased, meaning that electric field is reduced at the peripheral part of the extrinsic base toward the extrinsic collector. Interestingly, measured BV_{CEO} and BV_{CBO} given in Table 3 are almost equal, but V_{CB} at which BV_{CEO} occurs (i.e. I_B changes the sign) is slightly smaller than BV_{CBO}.

6.2. Double-emitter (DE) reduced-surface-field (RESURF) HCBT

In DE HCBTs the breakdown voltage can be increased above 12 V by merging the n-collector regions of two transistors, due to the fact that the n-collectors are at the active region surface in the compact HCBT structure and not at the bottom of the intrinsic device as in the conventional vertical-current transistors. The breakdown voltage can be increased further, up to 36 V, by shielding the electric field in the drift region resulting in the reduced-surface-field (RESURF) DE HCBT [19]. This is done by using a CMOS p-well implant and by the design of lithography masks (i.e. without any additional costs). Having a high-speed, as well as 12 V and 36 V high-voltage bipolar transistors along with the CMOS increases the flexibility and application spectrum of HCBT BiCMOS technology further, making it attractive both for RF and other analog applications. Since high-voltage bipolar transistors are integrated at zero-cost, the technology is suitable for integration of low-cost smarter systems including higher-power and human-interface sensor circuits, which makes it a contender for the future Internet of Everything (IoE) applications.

Cross-sections at the symmetry lines of the DE HCBT with RESURF region are shown in Figs. 16.a and 16.b. In double-emitter configuration, a C_EB^EC layout is used with extrinsic collectors folded to front and back of the intrinsic transistor. Compared to the standard DE HCBT, this one has an extended extrinsic collector with CMOS p-well implanted underneath to obtain local substrate with increased concentration. The basic idea is that the n-hill above the p-well region is fully depleted if collector voltage is increased and that the second RESURF drift region is formed.

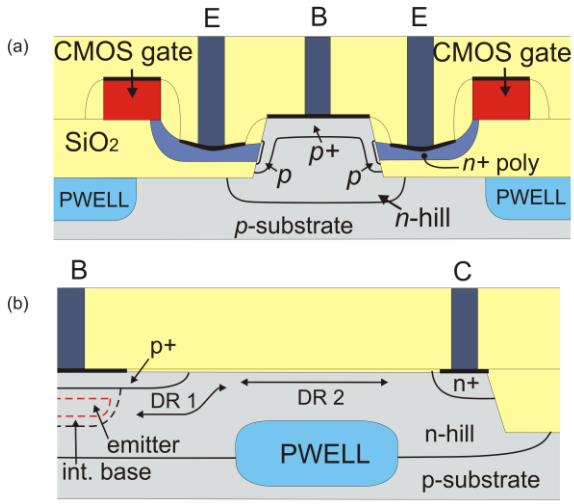


Fig. 16 Schematic cross-sections of the fabricated DE RESURF HCBT structure having C_EB^EC layout. (a) EBE cross-section along the emitters. (b) CBC cross-section along the middle of the *n*-hill. Due to the symmetry, only one half is shown. Compared to standard DE HCBT structure, CMOS p-well is implanted in the n-hill between the collector contact region and the intrinsic transistor. In the forward active region, portion of the n-hill above the p-well is fully depleted and the 2nd drift region (DR 2) is formed.

The change of the electric field with the increase of the collector-emitter voltage (V_{CE}) is shown in Fig. 17. For small V_{CE}, the peak electric field at the intrinsic base-collector junction increases with V_{CE} as shown in Fig. 17.a and depletion regions spread into the intrinsic collector. After intrinsic collector is fully depleted, there is no available donor charge in this cross-section (Fig. 16.a) and the maximum electric field at the junctions remains unchanged. The voltage is dropped in the perpendicular cross-section across the 1st drift region (DR 1 in Fig. 16.b) toward the extrinsic collector.

Electric field along the current path in the middle of the n-hill is shown in Fig. 17.b. As V_{CE} is increased, the 2nd peak of the electric field appears at the end of DR 1, whereas the 1st peak at the intrinsic base-collector junction remains the same, because collector voltage is blocked by the extrinsic base extensions above DR 1. Further increase in V_{CE} increases the 2nd peak up to the voltage where the extrinsic collector above the p-well region becomes fully depleted and the 2nd drift region (DR 2) is formed. Additional increase in V_{CE} causes the voltage drop across the DR 2. Collector voltage is partially blocked by the p-well region reducing its impact on the value of the electric field 2nd peak. Since there is enough available charge in the extrinsic collector, the 3rd peak of the electric field appears at the end of the DR 2. The ability of the p-well region to block the collector voltage determines whether the critical field is first reached in the 2nd or the 3rd peak of the electric field. This can be controlled by the length of DR 2.

DE RESURF HCBTs are fabricated on the same dies as high-speed HCBTs and DE HCBTs with BV_{CEO}=12 V. The steep n-collector doping profile described in Section 4 is used. Measured common emitter output characteristics of fabricated transistors with different l_{pw} are shown in Fig. 18.a. Breakdown occurs around 26 V for the transistor with l_{pw}=0.5 µm and around 36 V for the transistor with l_{pw}=3 µm. Summary of electrical characteristics is given in Table 4.

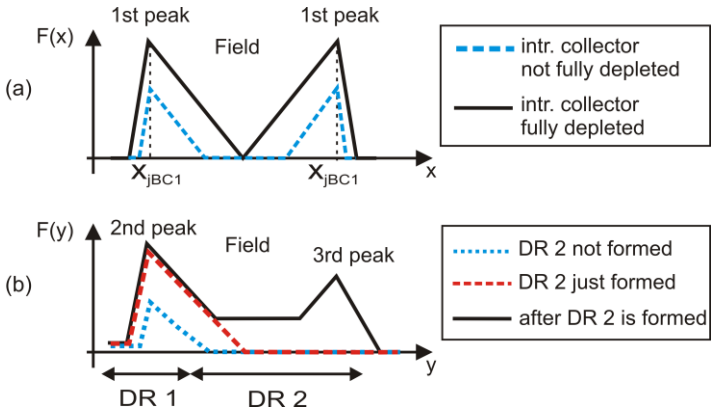


Fig. 17 Electric field with the increasing V_{CE}: (a) along the middle of the emitters (EBE cross-section of Fig. 16.a), (b) along the current path in the CBC cross-section from Fig. 16.b.

Table 4 Measured electrical parameters of double-emitter (DE) HCBT with n-hill width of 0.36 μm and different length l_{pw}.

	l_{pw}=0.5 μm	l_{pw}=3 μm
Emitter area (μm^2)	2 x (0.1 x 1)	2 x (0.1 x 1)
β_{max}	123	129
V_A, (V), (I_B=15 nA, V_{CE}=6~7 V)	1928	2233
BV_{CEO} (V), output char.	26	36 (=BV_{CS})
BV_{CS} (V)	33	36
f_T (GHz)	5.3	2.7
f_{max} (GHz)	10.6	4.6
$f_T BV_{CEO}$ (GHzV)	137	97
$\beta \cdot V_A$, (kV),	237	288

In the case of transistor with l_{pw}=0.5 μm, the classical common-emitter breakdown mechanism occurs, meaning that the critical field appears along the current path and that a positive feedback loop due to transistor current gain is closed. For the transistor with l_{pw}=3 μm, breakdown occurs between the local p-well substrate and the n-hill. This means that neither the 2nd nor the 3rd peak from Fig. 17.b generate holes, which can close the positive feedback loop. The 2nd peak is limited below the critical value for avalanche, whereas the holes generated at the 3rd peak are collected by the substrate instead of the extrinsic base. For the transistor with l_{pw}=3 μm, it is more effective than for the transistor with l_{pw}=0.5 μm, because holes have to travel longer distance to reach the extrinsic base in the presence of strong vertical electric field component in the DR 2. This is confirmed by the measurements of the collector-substrate breakdown voltage (BV_{CS}), which equals the BV_{CEO} measured in the output characteristics for the structure with l_{pw}=3 μm. Avalanche current generated at breakdown flows between the collector and the substrate, whereas the base and the emitter currents are not changed, which is not the case in the standard bipolar transistors. As a result we have BV_{CEO}=BV_{CBO}=BV_{CS}.

Due to the E-field shielding of the intrinsic base-collector junction, the base-width modulation is suppressed, resulting in very high Early voltage, which equals around 1.93 kV and 2.23 kV for the transistors with l_{pw}=0.5 μm and l_{pw}=3 μm, respectively. This reflects to almost 100 dB of intrinsic gain (V_A/V_T) at room temperature for both devices. Since the value of current gain β is high, considering that the transistor has implanted base, the $\beta \cdot V_A$ product is remarkable indicating good analog performance. Dependence of the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) on collector current are shown in Fig. 18.b. In this structure, the high-frequency performance is traded for higher BV and f_T and f_{max} are reduced accordingly. Nevertheless, $f_T \cdot BV_{CEO}$ products show results very close to the Johnson's limit [20].

7. CONCLUSION

The HCBT is based on a new concept of bipolar transistor technology resulting in a low-cost fabrication, but with many innovative steps. The optimized-collector HCBT is fabricated with 3 additional masks to CMOS process, resulting in an optimum trade-off between the f_T, f_{max} and BV_{CEO}. The HCBT with the n-well collector requires 2 additional

masks to CMOS process and has lower f_T, f_{max} and BV_{CEO}, but still high enough for wireless communications circuits in the frequency range between 0.9 and 5 GHz. The optimized-collector HCBT targets the applications with supply voltages of 3.3 V, whereas the HCBT with the n-well collector has BV_{CEO} below 3 V, which has to be taken into account in circuit design.

Since f_T and f_{max} peak at low currents, i.e. at 200-300 μA in HCBT with optimized collector, HCBT is very attractive for low-power battery-supplied wireless communications circuit blocks. Furthermore, such small currents allow for an increase of emitter length in order to reduce R_B for low-noise applications, while maintaining a reasonably low I_C. The demonstrated double-balanced active mixers based on a Gilbert cell show that the high-current linearity of HCBTs are affected by n-collector doping profile and are optimized such that transistors can operate in high-current regime saving the layout area.

The n-collector doping profile also impacts the degree of the charge sharing between the extrinsic and intrinsic bases, which determines the value and distribution of the electric field defining the transistor breakdown voltage. Therefore, the breakdown voltage can be increased without affecting the high-frequency characteristics.

By using the charge sharing effect and HCBT geometry where all intrinsic transistor regions (emitter, base and collector) are along the horizontal line of current flow, it is possible to merge 2 devices and fully deplete n-collector. In this way, the electric field can be shielded and the breakdown voltage is engineered. By adding the p-well region underneath n-collector, the electric field shielding effect is extended further and the breakdown voltage can be increased to 36 V. The breakdown voltage can be adjusted just by changing the lithography masks. Hence, HCBT makes it possible to have a flexible BiCMOS technology platform with high-speed devices for RF circuits and high-voltage devices for very diverse system on-a-chip applications.

Acknowledgement: *This work has been supported in part by Asahi Kasei Microdevices Co., by the Croatian Science Foundation under the Project no. 9006, and by the Ministry of Science, Education and Sports of the Republic of Croatia, under Contracts No. 036-0361566-1567 and No. 036-0982904-1642.*

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