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SHORT-CIRCUIT ROBUSTNESS ASSESSMENT IN POWER ELECTRONIC MODULES FOR MEGAWATT APPLICATIONS

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Abstract. *In this paper, threats and opportunities in testing of megawatt power electronic modules under short circuit are presented and discussed, together with the introduction of some basic principles of non-destructive testing, a key technique to allow post-failure analysis. The non-destructive testing equipment at CORPE, center of reliable power electronics, Aalborg University, Denmark, is presented and its features are discussed in detail, together with some relevant results. Limitations of experimental analysis have also been addressed, together with the introduction of a mixed thermal-electrical simulation tool originally developed to study abnormal conditions and helping to predict very fast and dangerous thermal transient especially in case of worn out devices. The paper is concluded with an overview on present challenges in next-generation semiconductors for such high power ranges – basically silicon carbide – and new concepts for non-destructive testing of ultrafast power modules adopting such a technology.*

Key words: *IGBT, robustness, reliability, short circuit, instabilities, SiC power modules*

1. INTRODUCTION

Main renewable energy sources, e.g. photovoltaic (PV) and wind, require larger and larger initial investments, so that the breakeven point reaching risks to be considerably delayed. Ten years seems to be a reasonable time for the next-generation power plants, but this interval is strictly connected to the expected useful lifetime of the generation plant, which presently is being pushed towards twenty years and over [1]. For this reason, reliability has become very crucial to save money and moving one step forward to make possible the big challenge of 100% renewable energy sources for the mankind. In the above time horizon, random failures cannot be neglected, and the scenario is still somehow chaotic: on the one hand, industries observe unexpected failures happening

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much earlier than the schedule maintenance; on the other hand, very often power electronic components are replaced in advance with respect to their useful life time, with obvious loss of money and useless downtime.

A recent FP7 project (European Framework Programme 7) named Reliawind [2] pointed out the main causes of failure and maintenance requests over a large number of operating wind turbines (about 300). Referring to Fig. 1, the first three groups of causes for wind turbine off times are, in descending order: 1) power module; 2) rotor module and 3) control. Looking inside these groups, the scenario is even more critical from the power electronic standing point. In fact, the main power converter is responsible for more than 15 % of the overall causes of failure, which is even bigger than the fragile pitch system (14 %) and the main generator itself (13 %). The previous amount worsens considerably if one includes control faults in the overall power electronic failures amount.

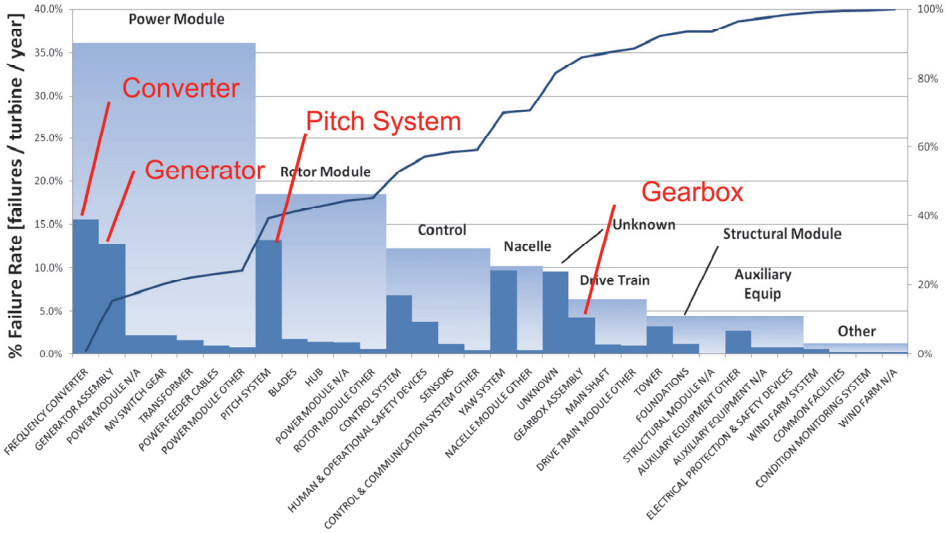


Fig. 1 Field experience of failure in wind turbines (normalized failure rate) [2]. The curve superimposed is the cumulative failure rate.

The main reason for such a big lack of reliability is the strong unpredictability of many failures occurring in power electronics. In fact, referring to Fig. 2, failures can be roughly classified into two categories: aging failures and catastrophic failures. Looking at root causes, aging failures are basically due to wear out of electronic parts, mostly at package level, whereas catastrophic failures basically come from severe overloads or instabilities. Along with root cause, though, it is interesting to point out the degree of predictability of such failures. Whilst wear-out failures can be predicted in a good approximation, severe overloads occur intrinsically random and their prediction becomes quite hard. Prediction of instabilities is even harder as they arise from a complex combination of several parameters, like: temperature, EMI (electromagnetic interference), impedance variations, gate driving circuit behavior, etc. For this reason, different approaches must be used to face different failure mechanisms.

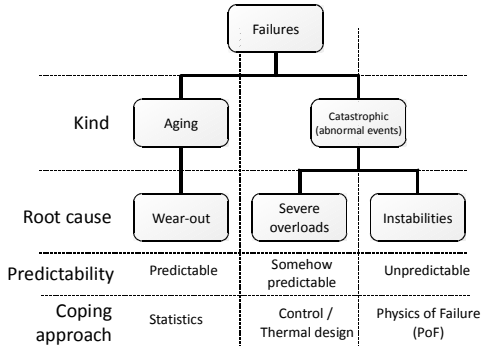


Fig. 2 Classification of failures in Power Electronics based on root causes [3].

Statistics is the key approach to cope with wear-out failures, especially when a large amount of field data is available, whereas physics-of-failure (PoF) approach is the only possible when dealing with severe overloads and instabilities.

As a matter of fact, the scenario becomes even more complicated in case of interaction, i.e. when severe overloads trigger instabilities. As will be discussed later on, in modern high-performing IGBT power modules amplification mechanisms can take place in short circuit conditions leading to gate-side oscillations, which are extremely dangerous for the device safety. On top of that, such a kind of phenomenon occurs very fast and no intervention can be made at gate level to save the device.

The aim of this article is to present and discuss modern techniques used for assessing the device response to short circuit events, especially with respect to instabilities. The remaining part of the paper is structured as follows: section 2 introduces the utilized test approach to study the device behavior during short circuit and some experimental results. Section 3 shows and describes a novel simulation approach utilized by the research group led by the author to investigate the role of electro-thermal interactions in instabilities at chip-package level. Some challenges about incoming technologies, namely Silicon Carbide MOSFETs will be pointed out in Section 4, whereas section 5 will draw some conclusions and perspective work.

2. ROBUSTNESS TESTING

Typical devices for megawatt-scale inverters, like PV plants or wind turbines, are rated in the range of kilovolt and kiloampere. In Fig. 3a, an Infineon PrimePack™ IGBT module is shown whose rating is 1.7 kV, 1.0 kA. In Fig. 3b, a sample assembly of a power stack for wind turbine applications has been reported including seven devices on the same fluid-cooled heat sink.

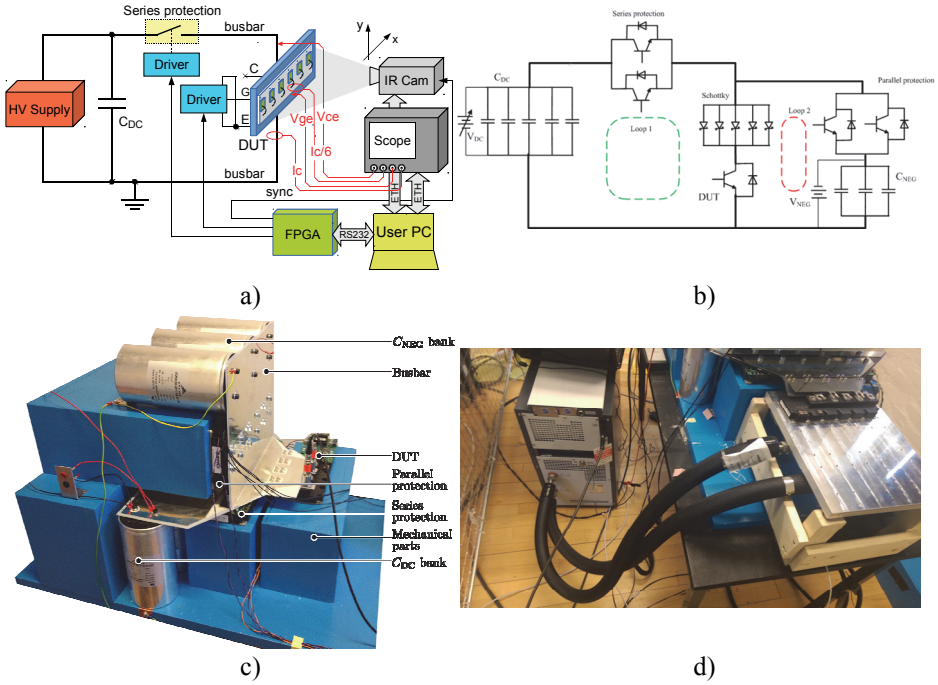
Non-destructive short-circuit testing principles have already been introduced in [4] for past-generation IGBT modules, where basic principles and limitations of such a testing technique were pointed out. To test modern power devices, though, besides established characteristics like: protection switches to avoid explosion in case of failure, low-inductance busbar and single-shot capability, several additional requirements have to be strictly fulfilled at the same time:

a) b)

Fig. 3 a) a PrimePak™ 3 IGBT module, which is widely used in wind power applications [5]; b) CAD model of a power stack assembly for wind turbine inverters including fluid heat sink [6].

- Large current design, typically 5 kA and over;
- Even lower busbar stray inductance, according to commutation speed of last-generation IGBT modules;
- Digital timing control;
- Personal-Computer supervising system, in order to perform automatic and safe experiments;
- Overall geometry compatible with infrared camera shooting.

It is worth to note that the above characteristics are quite hard to be obtained altogether, as many of them conflict with each other. For instance, to comply with a very low busbar inductance requirement is not easy because of the presence of protection switches in the circuit.



a) b)

c) d)

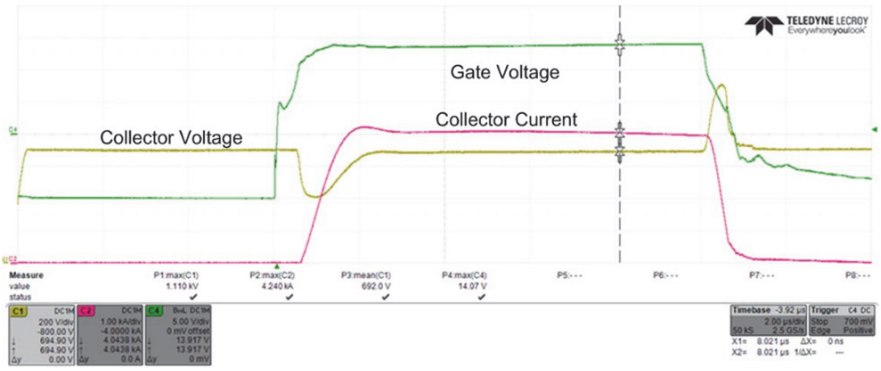
Fig. 4 a) Principle schematic of the Non-Destructive Tester in CORPE [7]; b) detailed electrical schematic; c) picture of the equipment; d) detail of the heating/cooling system.

In Fig. 4a, the principle schematic of the Non-Destructive Tester (NDT) recently developed in CORPE – Center of Reliable Power Electronics at Aalborg University, Denmark, has been reported. The equipment is operated in single-shot mode. The device under test (DUT) is connected to a capacitor C_{DC} providing the energy needed for the test through a busbar connection. A series protection is initially closed and opens right after the test, in order to break the circuit in case of failure occurrence. The DUT is driven by a commercial IGBT driver, which has been modified on purpose in order to deactivate its embedded short-circuit protection (desaturation detection). The DUT driver and the series protection driver are synchronized accurately by means of a user-PC-configured FPGA-based hardware, which also provides the trigger signals to the rest of the equipment. An oscilloscope (Scope) is synchronized with the test sequence and acquires the electrical waveforms Vce, Vge and Ic. In case an open device is available, the current flowing through each single section of the IGBT module (Ic/6) can be also measured. An infrared camera (IR cam) shoots at the device once it has been opened and opportunely treated for increasing emissivity in order to monitor possible thermal imbalances occurring during the tests. The mentioned user PC (personal computer) also provides testing parameter setting and waveform processing. In Fig. 4b, a detailed electrical schematic has been reported. The capacitor C_{DC} has been obtained by putting five capacitors in parallel to reduce the stray inductance. The series protection has been made with two large IGBT modules in parallel whose total current capability is 6 kA. A second loop is also present in the schematic of Fig. 4b, where a parallel protection made up of two further IGBT modules has been included in order to support the main (series) protection in zeroing the current through the DUT. The parallel protection is fired contemporarily to the series one. The emitters of the parallel protection IGBT are connected to a negative voltage, sustained by three further capacitors C_{NEG}, in order to enhance the overall effect of the protection, as demonstrated in [8]. To avoid negative voltage on the DUT, a set of five Schottky diodes has been put in series to the DUT. Fig. 4c depicts the experimental apparatus, where every part described in Fig. 4b can be easily recognized. The geometry has been designed in order to be able to shoot at the DUT from close distance from the top by means of an infrared camera. The apparatus also includes a cooling/heating plate as shown in Fig. 4d, ranging from -40 °C to + 250 °C. Of course, such an extended range can be only achieved by proper thermal and humidity isolation. At present, the apparatus can only be operated from room temperature to 150 °C.

The NDT can be used for a number of different tests. Fig. 5a shows a typical short-circuit commutation performed on the IGBT module of Fig. 3a under the following electrical and thermal conditions: DC-link voltage V_{DC} = 700V, gate voltage V_{GE} = 14V, $t_{short\ circuit}$ = 10ms, T_{test} = 25°C. An undershoot and an overshoot corresponding to the current rise and fall can be respectively observed on the collector voltage waveform, which are caused by the circuit stray inductance. In the test of Fig. 5a, the measured stray inductance was about 40nH. In the same figure a slight decrease in the current waveform can be also noted which is typical of device heating during the test. The same equipment can be profitably used for assessing the stability behavior of experimental prototypes. In Fig. 5b an unstable behavior has been observed on a laboratory-constructed module, whose layout has been designed in order to optimize the commutation energy. In the test, the external circuit inductance has been increased in order to simulate electrical conditions much closer to real short circuit events occurring between two inverter output phases. The waveforms evidence a limit-of-stability behavior, in which the gate voltage is affected by

permanent oscillations. Synchronous oscillations are observed on the collector voltage as well, evidencing a strong amplification behavior in these extreme conditions. In such a case, the NDT has been profitably used to investigate the unstable behavior step by step, increasing the on-time interval with steps of few tens of nanoseconds and firing the protections right after the device turn off, in order to remove the power in case of possible failures. The procedure would have immediately been stopped in case of appearance of any kind of instability, so that the device under test could be saved from possible ruptures [9].

One more way to profitably exploit the NDT is to perform synchronized infrared acquisitions during short circuit. In such a case, the sample has to be prepared by removing the external enclosure and the silicone gel the module is internally filled with.



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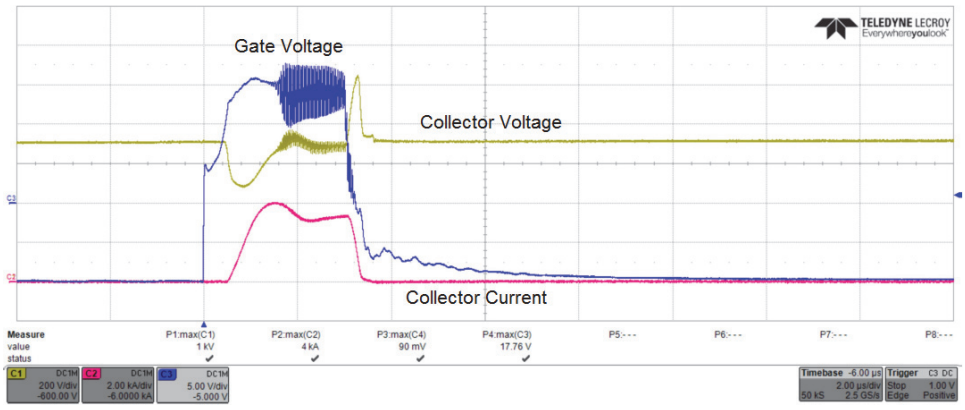
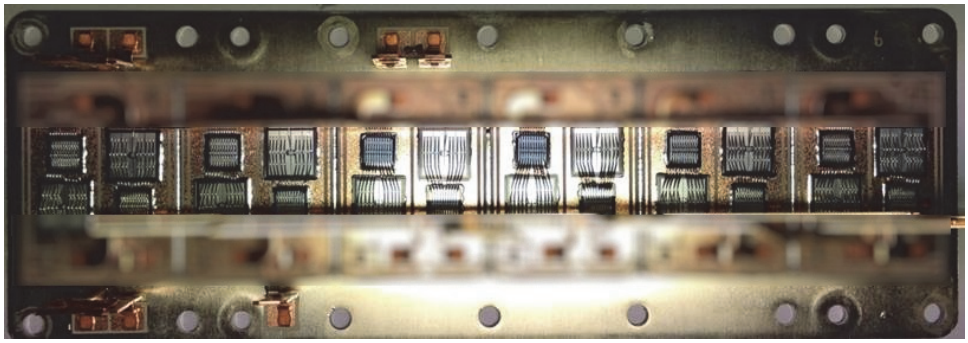


b)

Fig. 5 Short circuit experiments performed on a test module at 700V. a) safe commutation; b) commutation evidencing gate oscillations typical of unstable behavior. Collector voltage: 200 V/div; Gate Voltage: 5 V/div; Collector Current: a) 1 kA/div b) 2 kA/div.

In Fig. 6a, a picture of an experimental open module is reported, in which some non-relevant details of the internal layout have been blurred. On its surface, six sections can be easily recognized, each of which has got two IGBT chips (the big ones) and two freewheeling diodes (the small ones). The module has been painted with a few-micrometers-thick, black-paint layer in order to enhance the emissivity, which is necessary to improve the IR camera performance. The IR camera shooting instant is set by the FPGA hardware described in Fig. 4a, according to the parameters set from the user Personal Computer prior to the test. Fig. 6b reports an IR image acquired during a short-circuit test performed at room temperature T_{room} = 25°C. The six squares corresponding to the IGBT chips can be recognized, whose temperature is significantly higher than the rest of the module. A very meaningful result is that an evident temperature imbalance can be observed in the experiment of Fig. 6b, pointing out how much relevant is the internal layout in the current balancing in abnormal (in particular, short-circuit) conditions.



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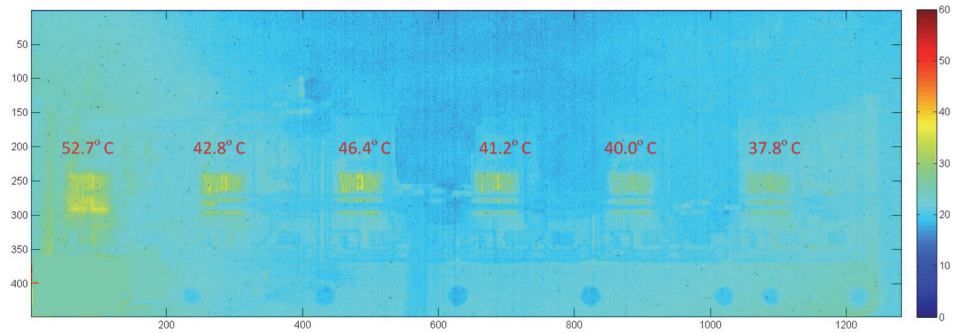


b)

Fig. 6 a) an experimental black-painted open module developed for testing. The non-relevant parts of the layout have been blurred;
b) Infrared shot of the same module taken during a short circuit test.

A short summary can be drawn from the observed results. Instabilities in IGBT power modules have been observed on laboratory prototypes in several cases. According to [7], some conditions to trigger such instabilities are:

- **Non-negligible circuit stray inductance**. It has been observed that the inductance involved in the short-circuit loop worsens the stability of the device, showing some oscillations. Such a condition is very typical of phase-to-phase short circuit in industrial inverters.
- **RF amplifying behavior**. The device exhibits an amplifying behavior so that an oscillation on the gate side produces a synchronous oscillation on the collector side.
- **Module internal layout**. It is very difficult to design a module whose layout exhibit good current balance during abnormal conditions, like short-circuit. IR tests evidenced a significant heating imbalance among the different chips.

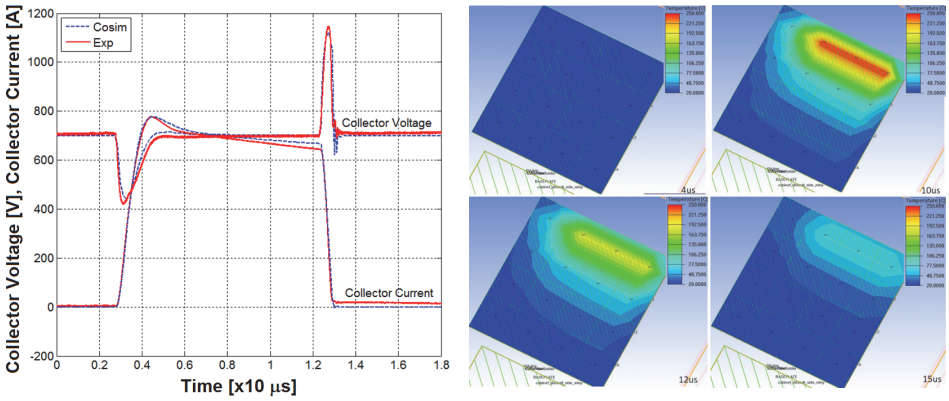
3. Modelling Abnormal Conditions

In the previous section, a testing approach has been discussed in detail including IR camera shooting, pointing out its key benefits. Nevertheless, there are a number of practical limitations arising from the used technique which considerably limit the feasibility of some extreme tests, namely:

- Gate-voltage instabilities are very dangerous, as the overvoltage on the gate terminal can provoke a dielectric breakdown of the gate oxide. This means that no longer investigations are possible in case a gate instability takes place;
- The thermal evolution of the system, in particular of the IGBT dies, is significantly slowed down by the thermal inertia of the metal layer on top of the chips and also of the black paint. This means that, even if an uneven current sharing can confidently be observed, the real junction temperature in a given chip is not measurable;
- The effects of the stray elements of the module internal layout are not easily measurable, as new prototypes have to be built up to study a different configuration.

The above bullets lead obviously to the need for an accurate and reliable simulation tool. As a matter of fact, such a tool necessarily has to include multi-domain physics, as short circuit behavior strongly depends both on electrical and thermal aspects. In fact, the IGBT saturation current is significantly affected by the thermal evolution (i.e. it decreases with time because the device warms up very fast) and the thermal evolution is directly dependent on the electrical power generated in the semiconductor junction. Many simulation tools have been presented over the last two decades, with various trade-offs between accuracy and time efficiency [10]–[16], but a still quite unexploited approach is to connect a finite-element method (FEM) simulator of the thermal part to a light and versatile model on the electrical part. This co-simulation approach has been possible thanks to a sophisticate MATLAB®-based approach introduced recently in [17] that interfaces the ANSYS Icepak world [18] with the ORCAD PSpice one [19]. The electrical part implements a well-established IGBT model for PSpice [20] with a very good trade-off between accuracy and simulation speed. Fig. 7a qualitatively shows the performance of such a mixed approach. Short-circuit experimental waveforms obtained at 700V, room temperature, have been compared with the one obtained thanks to the discussed co-simulation approach. The simulation waveforms are in excellent agreement with the

experimental one. In particular, the hard-to-predict current waveform is very accurately described, which is strongly dependent on the thermal evolution. What's more, the simulation helps also in detecting possible measurement mistakes, like the non-zero current at the end of the test of Fig. 7a, which is due to a non-ideal behavior of the adopted current probe. The FEM part of the discussed co-simulation approach gives even more interesting results on the thermal aspects: Fig. 7b shows a simulation output of a short circuit in presence of a reconstruction phenomenon [21] of the device metal surface. The device warms up much more underneath the bond wire attach area because of the non-negligible lateral voltage drop across the degraded chip metallization. Moreover, a direct consequence is that the on-state voltage drop is considerably increased and this easily ends up in current imbalance phenomena.



a) b)

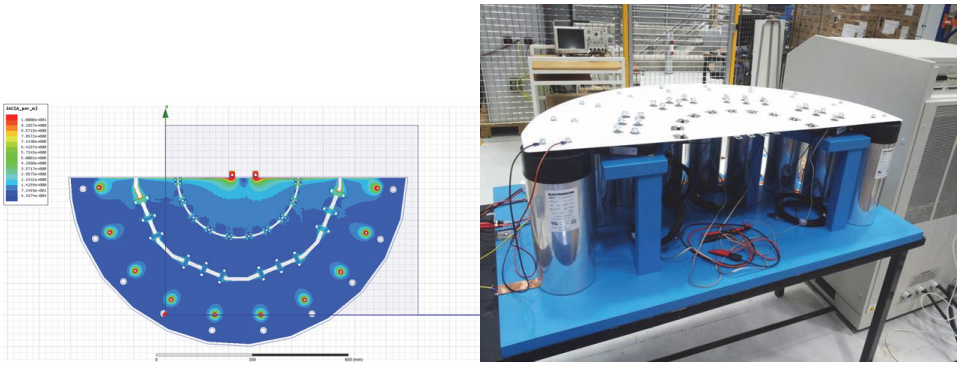
Fig. 7 a) comparison between short circuit experimental and simulated waveforms by means of the mixed ANSYS-PSpice approach introduced in [17]; b) significant shots of the simulated sequence. Time instants: 4µs, 10µs, 12µs and 15µs. Temperature scale: 20°C – 250°C.

4. Silicon Carbide Testing Requirements

On the one hand, silicon is nowadays a well-established technology and its reliability and robustness issues are widely shared in the power electronics community. On the other hand, new and promising technologies have appeared in the last ten years enabling the efficient and relatively cheap growth of new semiconductor materials, like Silicon Carbide (SiC) and Gallium Nitride (GaN). Those materials exhibit outstanding figures from the power electronics' standpoint, as they combine much higher critical electric field with higher mobility and higher thermal conductivity with respect to traditional silicon technology. Such characteristics lead to significantly better performances, especially in terms of switching speed, which is key for increasing operating frequency and, in turn, reducing converters' weight, volume and cost. Said new materials, though, open once again typical challenges of non-mature technologies, i.e. reliability estimation, lifetime prediction and, not least, robustness.

As matter of fact, SiC technology is very promising from the robustness point of view as many recent works demonstrated outstanding performances of JFET discrete devices [22]–[24] and MOSFET discrete devices [25]–[27]. Nevertheless, robustness of SiC power modules is more challenging with respect to traditional silicon, for three main reasons:

1. faster switching speed opens new problems in terms of current balancing in transients, both at normal and abnormal conditions;
2. intrinsic higher operating temperature capability complicates significantly the thermal balancing;
3. since chip area of present SiC technology node is limited by yield constraints at foundry level, more chips have to be put in parallel to achieve the same current capability with respect to silicon IGBTs.



a) b)

Fig. 8 a) round-shaped busbar design for ultra-low stray inductance testing [28]. Simulation of current density is reported in arbitrary units; b) picture of the final assembly of the Non-Destructive Tester NDT2 at CORPE, Center of Reliable Power Electronics, Aalborg University, Denmark.

The considerable limitations pointed out above require an extremely careful design at both layout level and circuit level, therefore: internal stray parameters need to be accurately equalized to reduce current imbalance as much as possible; circuit stray parameters – especially stray inductance – need to be further minimized to reduce dangerous voltage overshoots, typical of turn-off commutations, which could lead to a number of unstable secondary phenomena.

Of course, circuit stray parameters need to be even more minimized when designing a testing apparatus for short-circuit assessment, where 5x - 10x larger currents have to be switched on and off in times comparable to normal switching. This strict requirement calls for the adoption of special busbar design concepts, including negative coupling inductance and uniform current sharing. In fact, one of the major challenges in large-current busbar designs is that wide parallel current flowlines lead to a significant auto-inductance which cannot be reduced below an intrinsic minimum. A special design geometry showing negative coupling inductance between adjacent current paths helps in further reducing the inductance below the limit. Concerning the uniform current sharing, CAD simulations (ANSYS Q3D [29]) should be used to ensure that current spreads uniformly instead of focusing on a preferred

path. This latter effect would eventually increase the equivalent stray inductance as well. A study including all the optimization concepts discussed so far has been presented recently [28], where an innovative CAD-designed, round-shaped busbar to achieve a very low inductance (few nanohenries) has been successfully developed. In Fig. 8a, a Q3D simulation from that paper evidencing the uniform current distribution inside the designed busbar is shown. Current moves from the periphery (where capacitors are placed) to the center of the circle (where the DUT is connected) and vice versa through the below layer of the busbar. Fig. 8b depicts the constructed NDT2 setup, where a round professionally-made busbar can be recognized and ten massive capacitors are placed at the periphery of it. With reference to the schematic of NDT of Fig. 4b, the series protection switches have been increased to four; they can be recognized by the four groups of six bolts each laying at about half radius distance from the center. A little closer to the center, ten Schottky diodes can be recognized as well. The parallel protection loop is made up of another similar round busbar which will be installed vertically at an angle of 90 degrees with respect to the series one and connected to the DUT as well. For the sake of clarity, the parallel protection busbar has not been included in the picture.

5. Conclusion and Perspectives

Big efforts are being done in power electronics nowadays, particularly driven by renewables, like photovoltaic and wind power generation. In this scenario, robustness validation is a non-negligible part of confident reliability evaluation, especially regarding power electronic modules, which ends up in lowering costs and enabling larger and larger investments. In this paper, the state of the art about one of the most important robustness assessments, i.e. with respect to short circuit, has been discussed for power modules in the range of megawatt, where challenges are significantly bigger than in the discrete components' world.

The non-destructive testing technique has been presented and discussed in deep details, in order to share best practices and threats. In particular, the important of accurate time synchronization, physical layout, overall stray inductance, current sharing problems have been presented, providing some useful solutions.

The advent of new semiconductors in this power range, in particular silicon carbide, is definitely paving the way to a new revolution in terms of size, cost and efficiency. On the other hand, it challenges robustness expert from new and more complex point of views, basically related to extremely high gradients of current and voltage during commutations, ending up in need for non-conventional design of the testing setup. The paper concludes introducing new concepts for ultra-low inductance design to be adopted for such technologies. Work on the way of robustness assessment of so promising technologies is still in progress.

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