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TRANSIENT VOLTAGE SUPPRESSOR BASED ON DIODE-TRIGGERED LOW-VOLTAGE SILICON CONTROLLED RECTIFIER

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Abstract. *Transient voltage suppressor (TVS) has been widely used for electronic system ESD protection. A good TVS is usually costive as it needs some special processes and extra masking layers for fabrication. A novel TVS design based on the standard CMOS process will be much more attractive. This work proposes a new TVS device using a CMOS compatible diode-triggered silicon controlled rectifier (DLVTSCR) as the core device. Due to the availability of multiple trigger mechanisms and the dual current paths for bypassing the ESD current, the newly proposed device is able to sink an ESD current of over 10 A. In addition, the holding voltage is promoted up to 6.83 V and the trigger voltage is lowered down to 10.8 V which is well suited for most portable device applications.*

Key words: TVS, ESD, LVTSCR

1. INTRODUCTION

The integrated circuits (ICs) used in modern mobile electronic devices are faster, more powerful, less power consumptive, and are much smaller than ever before. However, they are more vulnerable to reliability issues, not only due to the small device size and the use of ultrathin gate oxide, but also due to their applications which make the devices more frequently exposed to electrostatic discharge events produced during the frequent human interfacing, and often plugging and disconnecting the USB devices and HDMI port. On-chip protection is now of vital importance for system reliability. However, conventional protection scheme is not only costive and bulky, but also leads to the system performance degradation [1]-[5].

Transient Voltage Suppressor (TVS) diodes have long been used to provide a high robustness system level ESD protection [6-8]. Under normal operating conditions, the TVS diode maintains in a high impedance state. During a transient discharge event, the TVS breaks down electrically and yields a low impedance shunt path to bypass the transient current. A

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good TVS protection circuit must be able to divert the transient current and to clamp transient voltage below the threshold value before the failure of the protected IC.

A TVS structure includes a core device and some steer diodes. The clamping voltage usually depends on the core device, and the steer diodes can divert the ESD current to the core device and can reduce the overall capacitance of the structure. However, to obtain a good TVS diode, some special processes, such as deep trench isolation or additional processing masking layers, are required. This work attempts to develop a CMOS compatible TVS device. FIG. 1 shows the conventional TVS based on a Zener diode (a) and the newly proposed TVS structure.

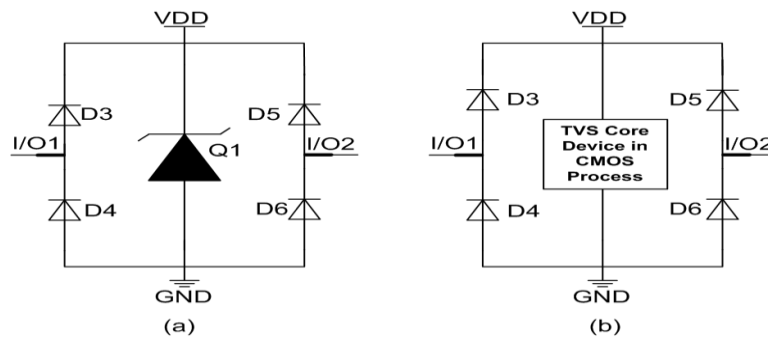


Fig. 1 Conventional TVS structure based on Zener diode and the proposed TVS structure based on the standard CMOS process.

For protecting the interface for data line communications, a good TVS device must possess some special features. First, a low working voltage is crucial for safeguarding the submicron integrated circuits. The maximum reverse working voltage, V_{rwm} , which is the largest allowable DC voltage that can maintain the TVS in non-conducting state, is the key parameter for specifying the working voltage. When the transient voltage exceeds V_{rwm} , the TVS turns on quickly and a low impedance path will be established to divert the transient current. Hence, a low working voltage is essential for clamping the transient voltage to a level well below the threshold value. Second, the equivalent capacitance of TVS should be low enough in order to preserve signal integrity at the high-speed interface. If the capacitance of the TVS diodes is too high, it will cause excessive load to the circuit and then signal distortion and data errors will result.

2. STRUCTURE AND PERFORMANCE

The schematic equivalent circuit and the cross-sectional view of the diode-triggered LVTSCR structure are shown in Fig. 2. LVTSCR, using the gated p-well structure, has been widely used as ESD protection devices because of its suitable values of holding voltage and the low trigger voltage. However, the gate structure also plays an important role in the reliability of the device. By adding an extra diode connecting the anode and cathode of the conventional LVTSCR, the structure can be triggered by an ESD event more easily. When an ESD event occurs, the drain PN junction and the substrate of the GGNMOS will be first driven into an avalanche breakdown and the voltage drop across

the diode increases as the avalanche current increases. Meanwhile, the electrons in the N+ (the one between the N-well and P substrate) will diffuse into the N-well. When the voltage drop across the diode rises above 0.7 V, the bipolar transistor (Q1) will be turned on. And that makes the SCR to be turned on later owing to the positive feedback in the transistors Q1 and Q2.

This device has been taped out in 0.18 μ m CMOS process. To study the characteristic of this new structure, transmission line pulse (TLP) measurements using pulses with a rise time of 10 ns and a pulse width of 100 ns were conducted. Fig. 3 shows the comparison of TLP characteristics for conventional and diode triggered LVTSCR. As compared with the conventional LVTSCR, the new diode-triggered LVTSCR structure exhibits a low parasitic resistance (calculated by dv/di), because the current conduction path in the newly proposed structure is now formed by the GGNMOS together with the SCR. As shown in F, the trigger voltage decreases from 8.94 V to 7.82 V; whereas the holding voltage increases from 2.01 V to 3.21 V. In addition, the failure current, I_{t2} , also increases from 3.17 A to 4.05 A because of the availability of two current conduction paths.

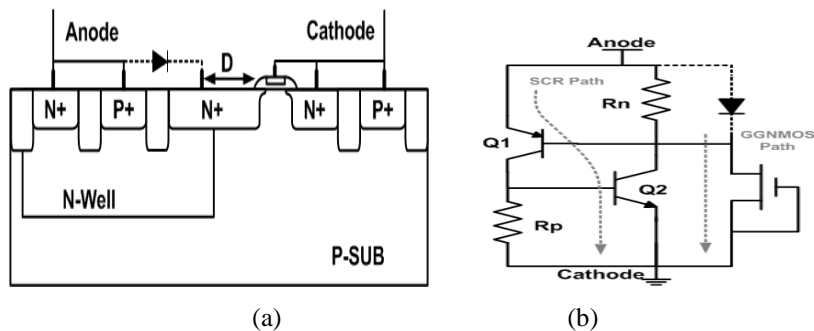


Fig. 2 Cross-sectional view (a) and the schematic equivalent circuit (b) of diode-triggered LVTSCR.

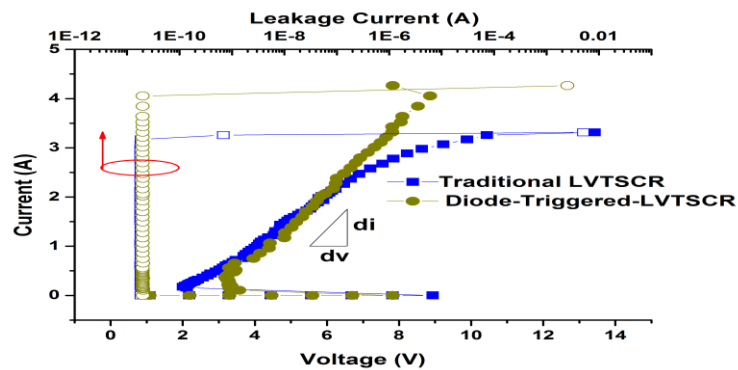


Fig. 3 TLP results of conventional LVTSCR and diode-triggered LVTSCR.

As shown in Fig. 4, when the value of D (the distance between the drain side of gate to contact of gate, see Fig. 2(a)) increases from $0.85\ \mu\text{m}$ to $2.35\ \mu\text{m}$, I_{t2} increases from $2.05\ \text{A}$ to $3.1\ \text{A}$. When the drain contact is close to the poly gate (when D is small), the heat produced at the drain junction spreads isotropically to the contact metal and results in a lower failure current level [8]. Hence, a larger separation between the contact and the poly gate will help to increase the failure current level. On the other hand, this device behaves like a diode when adding reverse voltage on it.

After investigating the standalone DLVTSCR, a TVS using the DLVTSCR as the core device was realized and the TLP test result is shown in Fig. 5. Taking I/O1 as an example, when adding ESD strike on I/O1 to GND, the ESD current will be released by the steer diode D1, through the DLVTSCR and then going to GND. As shown in Fig.5, the TVS structure presents a higher holding voltage of about $6.83\ \text{V}$ and an acceptable trigger voltage of about $10.8\ \text{V}$. These values should be acceptable for ESD protection applications for high-speed digital interfaces such as USB2.0, HDMI, AVI ports etc, in portable equipments.

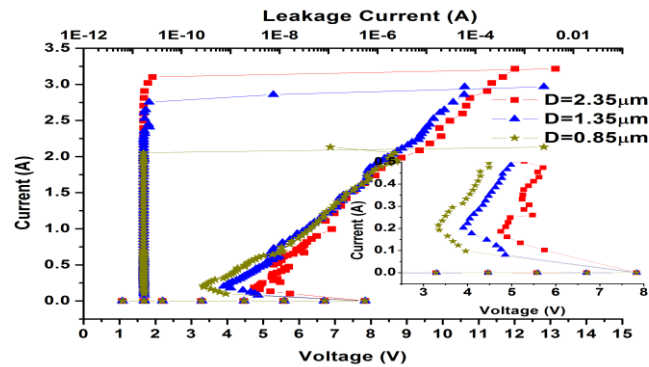


Fig. 4 TLP characteristics of diode-triggered LVTSCR as a function of device spacing (D) between the gate and drain contact of GG MOS of the LVTSCR.

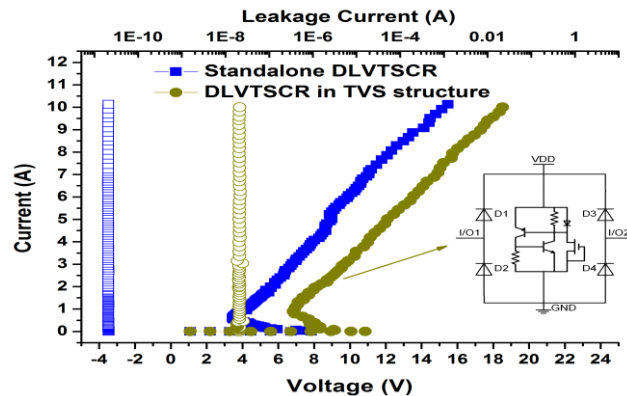


Fig. 5 Comparison of TLP characteristics of a standalone DLVTSCR and a TVS device embedded with a DLVTSCR.

3. CONCLUSION

This paper attempts to incorporate a diode-triggered low-voltage silicon controlled rectifier into a TVS. The results show that the larger distance between the gate edge and the drain contact, the higher ESD current (I_{t2}) can be obtained. The TVS structure was further verified with the standard CMOS process and good robustness was obtained. This structure can be used for system level ESD protections for high speed digital interfaces such as USB2.0, HDMI, AVI ports, and so on.

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