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HIGH-BANDWIDTH BUFFER AMPLIFIER FOR LIQUID CRYSTAL DISPLAY APPLICATIONS

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Abstract. *In this paper, a novel high-bandwidth and low-power buffer amplifier is presented for the liquid crystal display applications. This buffer amplifier consists of a folded cascade differential amplifier in the input and a class-AB amplifier in the output, which are designed carefully. The proposed buffer amplifier utilizes a high-performance feedback circuit to increase the bandwidth. It also utilizes a comparator circuit to avoid wasting power. The designed circuit has been simulated in 180nm technology using HSPICE 2008.3. The simulation results show that the bandwidth, power consumption and power supply of the designed circuit are 1.14MHz, 1.64mW and 1.8V, respectively.*

Key words: *buffer amplifier, liquid crystal displays, low-power amplifier, high-bandwidth amplifier*

1. INTRODUCTION

The increasing development of electronics made living in nowadays almost impossible without electronic devices such as cell phone, television, and tablet. Progress in demands of human nature has forced science to grow up in this field [1, 2]. Display is a common factor among these devices, which helps so much in improving the progress of them. The main reason for users and market attractiveness of progress in this field is that the display devices directly interface with the users.

There are several improvements in this field, which can be categorized in two groups: (a) improvement in the circuit components, and (b) improvement in the hardware of displays. Buffer amplifiers are main part of the screens. They directly affect power consumption, settling time, speed, bandwidth and other parameters [3-5].

Developments in integrated circuit technology, particularly circuits related to displays and their improvements, indicate that there is a need to have a high-quality and high-speed circuit under low voltage source and low power consumption [3-5]. Recently, the technology and consumer tendency are portable devices such as cell phone and tablet. In this process, many attempts have been done to improve the circuits to achieve the objectives that

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generally focus on parameters such as the slew rate, voltage swing, bandwidth, maximum load current and low power consumption [3-5].

There are many attempts to increase the performance of displays such as [6-10]. In [6], the designed circuit works well in terms of charging and discharging speed of large capacitors, but it has low bandwidth. In [7] and [8], the designed circuits have a good bandwidth, but they do not have the ability to charge large capacitors well. In [9] developed circuit works well in terms of charging and discharging speed for relatively large capacitors, but it has a relatively high power consumption. The developed circuit in [10] works well in terms of charging and discharging speed of large capacitors. The power consumption is also relatively good, but it has low bandwidth.

This paper presents a novel and efficient buffer amplifier. The proposed circuit consists of four parts, which are designed carefully. The proposed circuit has been simulated using HSPICE. The simulation results show that the proposed circuit provides an improvement in terms of bandwidth, slew rate and power consumption compared to other buffer amplifiers.

The remaining of this paper is organized as follows: general description of the proposed buffer amplifier circuit is described in section 2. Circuit design techniques are discussed in section 3. In section 4, the simulation results of the proposed buffer amplifier are compared with other buffer amplifiers. Finally, section 5 concludes this paper.

2. BUFFER AMPLIFIER

The buffer amplifiers generally consist of several parts: an input amplifier, an intermediate amplifier, a feedback network and output stage for drives capacitive loads [11]. As it is presented in Figure 1, the first block is a differential amplifier. The folded cascade amplifier is a commonly used amplifier in this stage; it is because in this amplifier due to differential inputs and outputs, the noise is eliminated. So, it has a better swing compared to telescopic amplifier. In the next block, in the output stage of class AB, the output circuit in [11] is utilized. Since two comparators are used behind the output transistors, the output efficiency is considerably increased, which prevents the static power dissipation. Figure 2 shows a schematic of the output circuit [11].

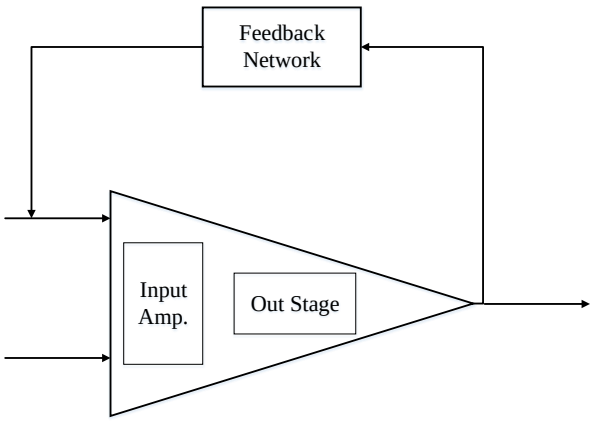

Fig. 1 A simplified buffer circuit schematic

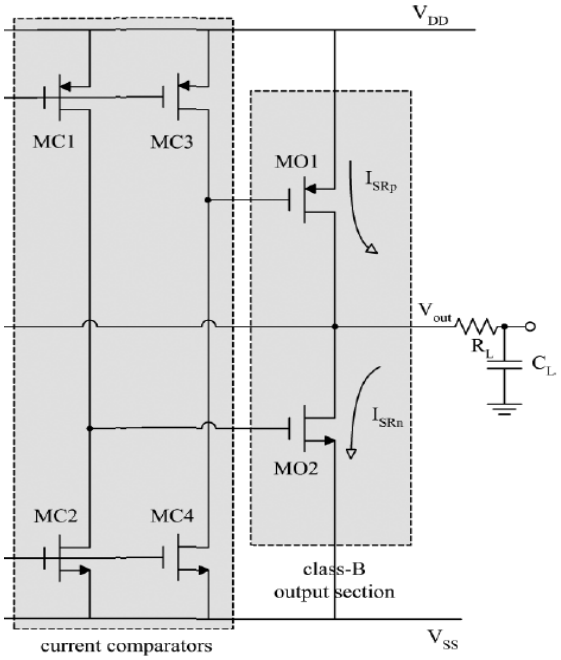

Fig. 2 The circuit of the output stage

In the third part, a feedback circuit is used. As it is shown in (1), using this feedback network, the bandwidth of the buffer amplifier is increased. Figure 3 shows a schematic of feedback network [8].

$$BW_{(new)} = BW_{(old)}(1+AB) \quad (1)$$

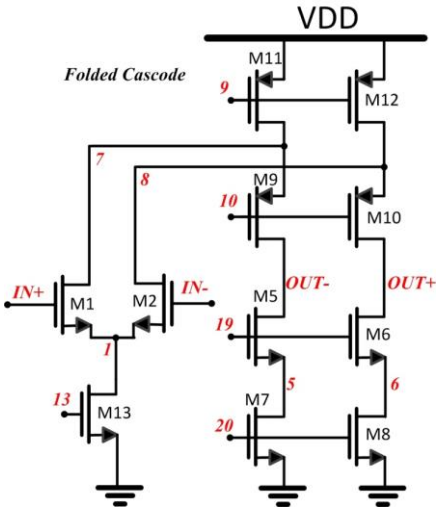

Fig. 3 The feedback network schematic

3. CIRCUIT DESIGN

To implement the proposed buffer amplifier circuit, the design must begin by designing circuit of folded cascade differential amplifier. Then, the common mode feedback circuit should be added. Moreover, the g_m constant circuit and the level shifter should be designed and added. To design the circuit, g_m/I_d method is used as shown in [11].

Circuit design is done using the graph of g_m/I_d in relation with V_{ov} [11]. In g_m/I_d design methodology, the circuit is designed using a curve dependent on the utilized technology. So, the possibility to choose appropriate dimensions of transistors is provided more efficiently. This curve is independent of the dimensions, and it is relevant to all areas of the transistors. In addition, it can be used to design the dimensions of all transistors in the utilized technology. It should be noted that this ratio is directly related to the coefficient of carrier mobility in transistors. According to differences in the n-type transistors, the p-type transistors are used. Thus, in designing swing with respect to transistor and the utilized technology, v_{ov} must be considered differently.

Figure 4 shows the g_m/I_d -v_{ov} according to [11] for n-type transistors.

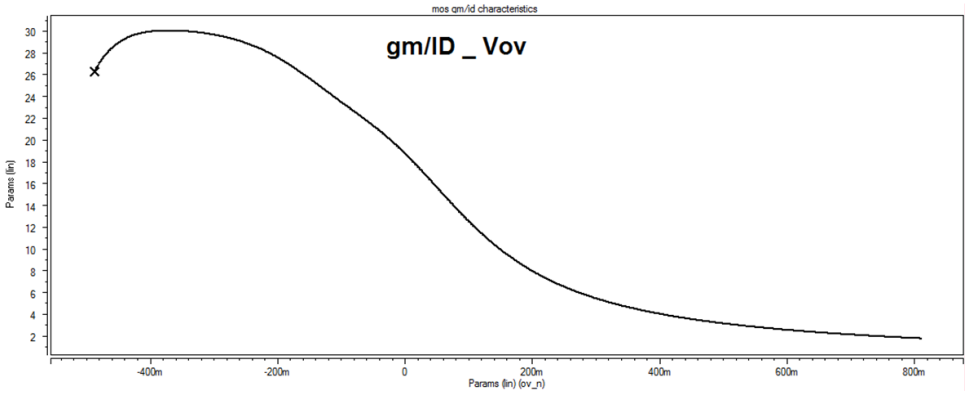

Fig. 4 The simulation results for g_m/I_d to v_{ov} for n-type transistors

In this circuit, swing voltage is 1.2Volt. With this limitation, over drive voltages are selected as shown in (2) and (3):

$$V_{ovn}=0.13Volt \tag{2}$$

$$V_{ovp}=0.17Volt \tag{3}$$

Using the same way, p-type transistors and feedback circuit are designed. In the feedback circuit design, one thing is necessary: the low current branches should be considered. So, the power consumption of the entire circuit does not increase. Feedback circuit is shown in Figure 5.

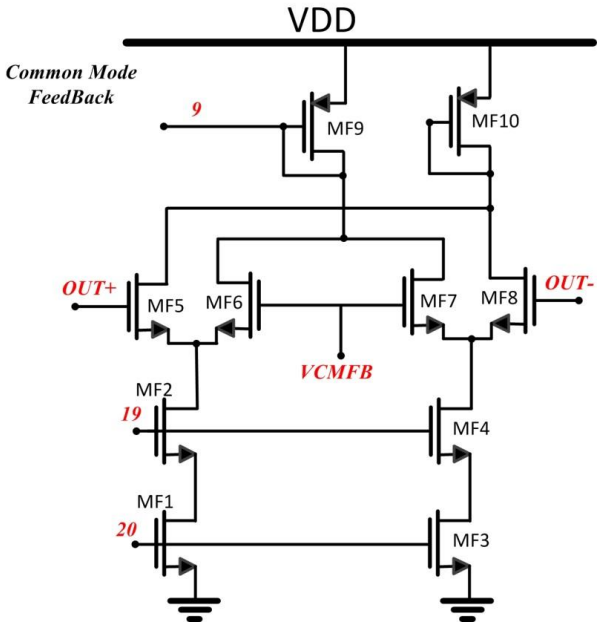

Fig. 5 The utilized circuit for the feedback in the proposed buffer amplifier

The general circuit of the proposed buffer amplifier without output stage is shown in figure 6. that utilizes two circuits as shown in Figures 2 and 3.

It should be noted that figure 2 depicts output power stage. To ensure the other driving devices MO1 and MO2 to stay off during static operation and to save power consumption, the DC currents of MC1 and MC4 are designed to be slightly lower than the nominal currents of MC2 and MC3, respectively. The above specification is fulfilled by the following design conditions:

$$\frac{(\frac{W}{L})_{MC1}}{(\frac{W}{L})bias_p} = \frac{(\frac{W}{L})_{MC2} - \Delta(\frac{W}{L})}{(\frac{W}{L})bias_n} \tag{4}$$

$$\frac{(\frac{W}{L})_{MC4}}{(\frac{W}{L})bias_n} = \frac{(\frac{W}{L})_{MC3} - \Delta(\frac{W}{L})}{(\frac{W}{L})bias_p} \tag{5}$$

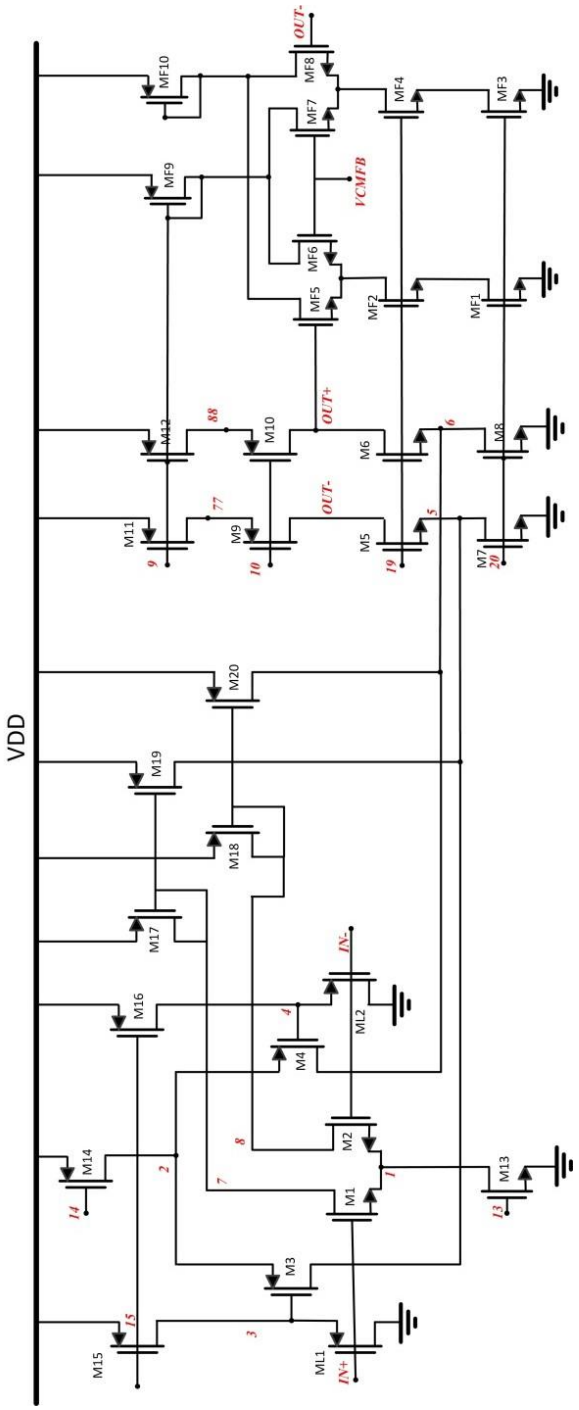

Fig. 6 The general circuit of the proposed buffer amplifier

4. SIMULATION RESULTS

The designed circuit that is shown in figure 6 is simulated in 180nm technology using HSPICE 2008.3 with 1.8 volt power supply. The simulation results for the slew rate and bandwidth are shown in Fig. 7 and Fig. 8, respectively.

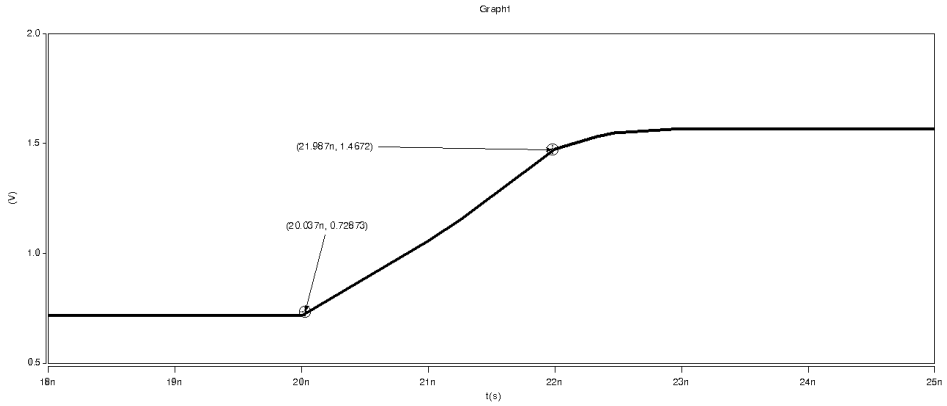

Fig. 7 The simulation results for the slew rate of the proposed circuit

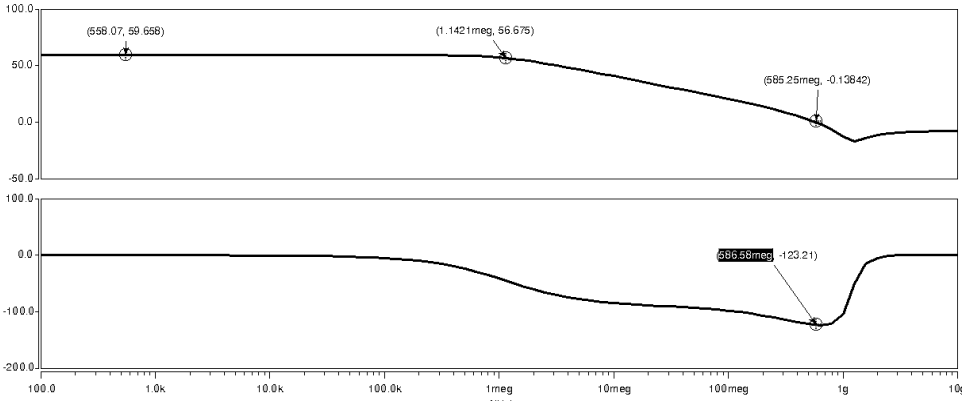

Fig. 8 The simulation results for the bandwidth of the proposed circuit

Table 1 summarizes the simulation results of the proposed buffer amplifier in HSPICE in comparison with other buffer amplifiers [6-10].

Based on our simulation results, which are shown in table 1, the developed circuit provides an improvement in comparison with [6-10] in terms of bandwidth, power consumption and slew rate.

Table 1 The comparative table for amplifiers

Reference	Power consumption (mw)	Maximum capacitive load (pF)	CMOS technology (nm)	Supply voltage (v)	Bandwidth (MHz)	Slew rate (v/μs)
[6]	1	680	600	4	0.1	--
[7]	--	15	350	2	2.3	--
[8]	--	200	500	3.3	--	--
[9]	--	20000	130	--	1	0.083
[10]	6.47	1000	500	5	0.503	5.7
This paper	1.64	1000	180	1.8	1.14	378

5. CONCLUSION

Low-power and high-bandwidth design are trends in the circuit design [4-5]. In this paper, a novel buffer amplifier has been proposed to be used in the liquid crystal display applications. The proposed buffer amplifier is composed of four parts, which have been designed carefully. The proposed circuit has been simulated using HSPICE. The simulation results showed that the proposed circuit provides an improvement in terms of bandwidth, power consumption and slew rate compared to [6-10]. Therefore, the proposed buffer amplifier architecture has a huge potential to be an efficient architecture for hardware implementation of buffer amplifier.

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