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SELF-TUNING LOW-NOISE AMPLIFIER*

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Abstract. *A low-noise amplifier with a phase control loop is described in this paper. In the proposed circuit, the resonant frequency is auto-tuned to the input signal frequency. In that way, high gain (20 dB), a phase shift of -180o between input and output signals, and good selective characteristics are obtained. The amplifier is robust to parameter variations, ensuring maximal amplification of the input signal regardless of its frequency as long as it is within a specified frequency range (880-950 MHz). Hence, the proposed circuit possesses self-tuning properties. The stability of the phase loop is analyzed by using Lyapunov's control theory.*

Key words: *Low-noise amplifier, Band-pass filter, Phase control loop, Self-tuning, Sability analysis*

1. INTRODUCTION

The rapid growth in RF CMOS circuit design techniques has made it possible to integrate the RF frontends, baseband transceivers, and digital circuitry on a single chip. However, modern CMOS manufacturing technologies show large process parameters, supply voltage, and temperature (PVT) variations. The main design goal now is to maintain circuit performance non-sensitive in all possible manufacturing and environmental situations. Traditionally, temperature, voltage/current and process variability have been addressed separately during the design process. Temperature variations are usually compensated using temperature independent biasing circuits that provide constant voltage/current within the defined temperature range [1, 2]. The compensation of process variations in RF circuits is usually implemented as on-chip self-calibration approach [3, 4], meaning that self-calibration appears to be a necessary need for contemporary RF chips. To cope with the abovementioned problems, the solutions, based on digitally con-

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trolled binary-weighted capacitor- or current mirror-array [5], master-slave [6] or self-tuning [7-9] design principles, are used.

Low-Noise Amplifier (LNA) is one of the basic building blocks in the receiving end of wireless communication system. The purpose of LNA is to amplify very weak received signal to the acceptable level, while, at the same time, adding as little additional noise as possible. In general, if CMOS technology is used, apart from low noise, high linearity, sufficient gain, low power consumption and well defined resistive input impedance are important design requirements that LNA has to fulfill. More details concerning input impedance matching of the LNA are given in [10, 11]. Methods for reducing the effect of gate-drain overlap capacitance Cgd in CMOS RF LNAs are presented in [10, 12]. Among them cascode configuration is one of the most widely used techniques.

In this paper, we propose cascode common source LNA with a phase control loop forming self-tuning LNA (STLNA). STLNA has a defined phase shift at central (resonant) frequency, so the phase comparison of input and output signals is used for detection of amplifier characteristics mismatch. The phase control loop utilizes a phase shift value to adjust STLNA to maximal gain. In the proposed STLNA, we use a phase detector for phase measurements and MOS varicap for LNA frequency tuning. There are at least two benefits from the proposed design: (a) in the presence of parameter perturbations, STLNA is always tuned to the input signal frequency, and (b), since it has maximal gain at input signal frequency, STLNA could be utilized as a selective amplifier in a wide frequency range.

The paper is organized as follows. In Section 2, STLNA principle of operation is discussed. Then, the amplitude and phase characteristics of LNA are given. The details on the basic constituents of STLNA are also presented in this Section. The stability analysis of STLNA phase control loop is treated in Section 3. To verify the proposed design solution, simulation results are given in Section 4. Section 5 contains some concluding remarks.

2. STLNA PRINCIPLE OF OPERATION

The design of STLNA is based on phase control principle similar to the one used in [7]. The block diagram of the proposed circuit is presented in Fig. 1.

As constituent of STLNA, we use LNA implemented in inductively degenerated common source topology [13]. LNA is loaded by L_1, C_1 and MOS varicap, as a voltage controlled capacitor [14], forming resonant circuit whose resonant frequency is:

$$f_r = \frac{1}{2\pi\sqrt{L_1(C_1 + C_{MVar})}}, \tag{1}$$

with the capacitance [14]:

$$C_{MVar} = \frac{C^*_{MVar}}{\sqrt{1+V_{ctrl}/V_\rho}}, \tag{2}$$

where C^*_{MVar} and V_ρ are positive constants, and V_{crtl} is a MOS varicap control voltage. The phase shift of LNA is:

$$\theta = -180^{o} - \text{atan}\left(2Q\frac{f_s - f_r}{f_r}\right), \tag{3}$$

where f_s is a frequency of input signal V_{in} and Q is a quality factor.

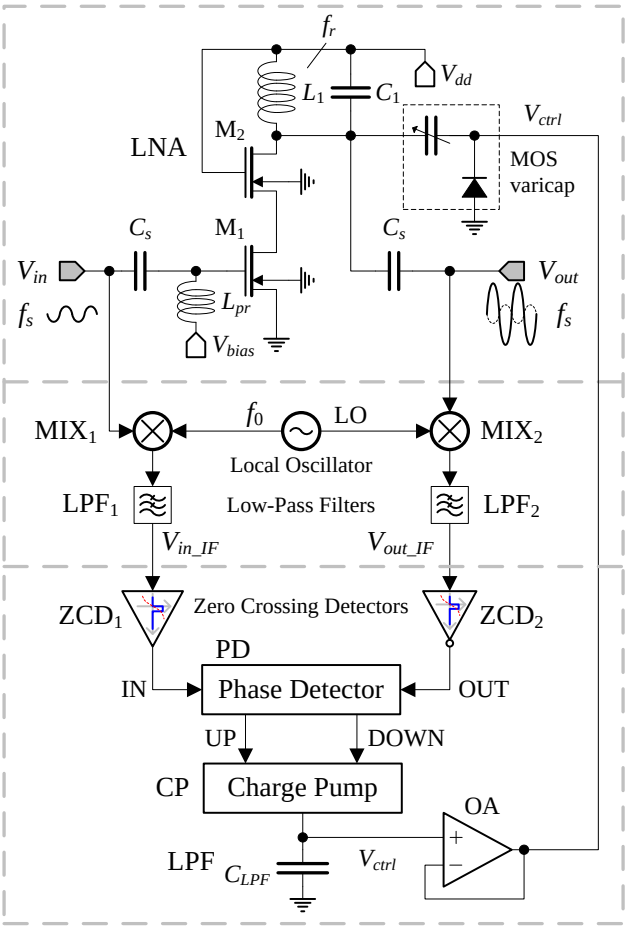

Fig. 1 Block diagram of STLNA circuit.

The gain and phase characteristics of LNA are depicted in Fig. 2 for V_{ctrl} within the interval 1.7 - 2.7 V, giving resonant frequencies in the range from 880 up to 950 MHz. Maximal gain is obtained for the phase shift of -180° with $f_s = f_r$.

Since it is difficult to realize a correct operation of a phase detector at high RF/MW frequency, the frequency down conversion of signals V_{in} and V_{out} is done by using two mixers (MIX$_1$, MIX$_2$), local oscillator (LO) with frequency f_0, and two low-pass filters (LPF$_1$, LPF$_2$). The results of conversion are signals, V_{in_IF} and V_{out_IF}, at lower frequency $f_0 - f_s$. The frequencies $f_0 + f_s$ are eliminated by LPF$_1$ and LPF$_2$. These signals are

amplified first and, then, shaped to rectangular form by zero crossing detectors (ZCD_1, ZCD_2), composed of CMOS inverter stages. In order to ensure proper operation of phase detector (PD), ZCD_2 has one inverter stage more than ZCD_1, introducing an additional -180° phase shift to the output signal. In that way, the phase error, estimated by PD, is:

$$\theta_{PD} = -\text{atan}\left(2Q\frac{f_s - f_r}{f_r}\right). \tag{4}$$

PD compares IN and OUT, generating UP and DOWN signals, whose widths are proportional to θ_{PD}. UP (DOWN) signal is high, and DOWN (UP) signal is low, when the phase of IN (OUT) leads with respect to the phase of OUT (IN). UP and DOWN signals drive a charge pump (CP). By charging and discharging the load capacitor C_{LPF}, CP provides V_{ctrl}, which tunes the LNA resonant frequency, so when $f_s = f_r$, $\theta_{PD} = 0^o$ and $\theta = -180^o$, V_{in} and V_{out} signals are synchronized but in an opposite phase, and V_{out} is significantly amplified. An operational amplifier (OA) with the unity gain decouples the influence of C_{LPF} to MOS varicap capacitance. The control voltage V_{ctrl} is defined as:

$$V_{ctrl} = -k_{cp}\int_{-\infty}^{t}\theta_{PD}\,\mathrm{d}\tau \tag{5}$$

where k_{cp} is a CP gain.

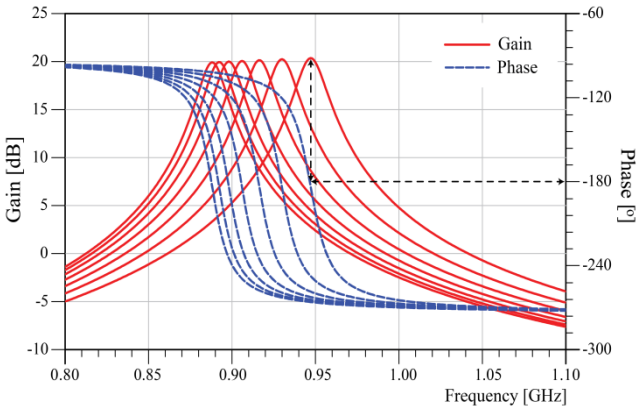

Fig. 2 LNA gain and phase characteristics

3. STABILITY ANALYSIS

Taking into account (1), (2) and (5), the phase loop dynamics can be obtained by time-differencing (4):

$$\dot{\theta} = -\frac{2k\pi QLC\_ff}{V(C\_)(f\_ + 4Q(f - f))}\theta. \tag{6}$$

To prove the phase loop stability, we use the Lyapunov's theorem [15], where the Lyapunov's function candidate is selected as $V = \theta_{PD}^2 / 2$. V is positive definite function $V > 0$ for $\forall\, \theta_{PD} \neq 0^o$, $V = 0$ for $\theta_{PD} = 0^o$ and $V \to \infty$ when $\theta_{PD} \to \infty$. The time–derivative of V is given by $\dot{V} = \theta_{PD}\dot{\theta}_{PD}$, and it is negative definite function $\dot{V} < 0$ for $\forall\, \theta_{PD} \neq 0^o$. According to the Lyapunov's theorem, the phase loop dynamics is globally asymptotically stable, i.e. $\theta_{PD} \to 0^o$, $\theta \to -180^o$ and $f_s = f_r$.

4. Simulation Results

Verification of the proposed STLNA is performed by Spice simulation with the IHP design kit for 0.25 μm SiGe BiCMOS [14], and supply voltage V_{dd} = 3 V. STLNA has the following characteristics: gain 20 dB, resonant frequency range from 880 up to 950 MHz, f_0 =940 MHz, bandwidth $BW \in$ (24.4, 26.4) MHz, Q= 36, noise figure 1.28 dB, and –1 dB compression point -9.8 dBm. Tab. 1 shows the simulation results of this proposal and other similar works, which relate to self-tuning LNA. As indicated in Table 1, power consumption and noise figure have been reduced, while the other characteristics are in acceptable range comparing with [8,9].

Table 1 Simulation results of the proposed LNA and other works

LNA	[This paper]	Ref. [8]	Ref. [9]
Technology	0.25 μm SiGe	0.18 μm CMOS	0.2 μm GaAs
Gain	20 dB	26.7 – 30 dB	15.1 – 21.6 dB
Resonant frequency range	880 – 950 MHz	0.8 – 1.5 GHz	2.4 – 5.2 GHz
Bandwidth	24.4 – 26.4 MHz	–	25 MHz
Quality factor	36	–	20 – 88
IIP3	3.7 dBm	–9.9 / +10.6 dBm	–3 dBm
Total noise / NF	1.28 dB	3.9 – 4.3 dB	2.8 – 3.8 dB
–1 dB compression point	–9.8 dBm	–	–8 dBm
P_{total} (LNA core)	2.34 mW	5.4 – 10.8 mW	–

The phase control loop adjusts circuit resonant frequency by varying V_{ctrl} until $f_r = f_s$ is fulfilled, thus providing maximal gain at the resonant frequency. Time responses of STLNA for f_s = 915 MHz are given in Fig. 3. As it is presented in Fig. 3(a), V_{in_IF} *and* V_{out_IF} signals are synchronized and in opposite phase as expected. We can see from Fig. 3(b) that the steady-state ($\theta_{PD} = 0^o$) is reached within 1 μs. The proposed STLNA can be also utilized for realization of robust band-pass active filters, based on master-slave architecture [7].

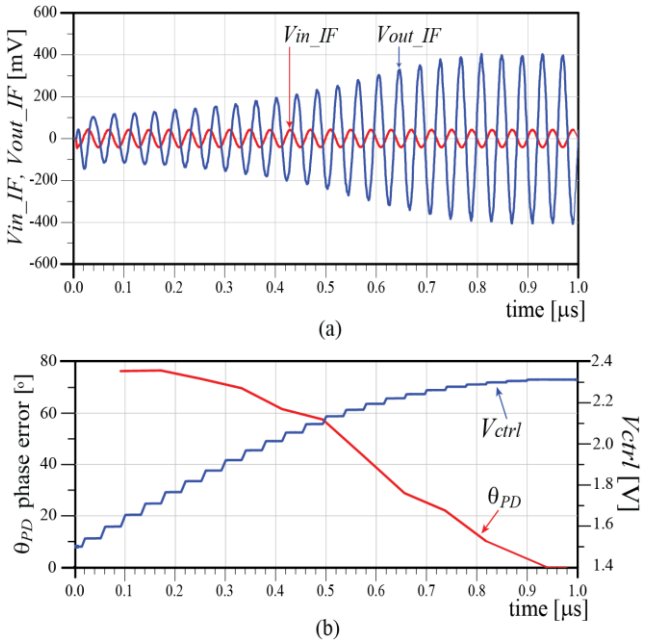

Fig. 3 Time responses of STLNA (a) V_{in_IF} and V_{out_IF} signals (b) Phase error θ_{PD} and control voltage V_{ctrl}

5. CONCLUSION

Selective low-noise amplifier (LNA) with self-tuning properties, suitable for VLSI implementation, is presented in this paper. Unlike self-tuning solutions based on sensing of power [8] or voltage [9] level, the phase control loop is introduced herein to tune the circuit resonant frequency to the frequency of input signal. This is done by changing MOS varicap capacitance with control voltage, which is proportional to the integral of phase error, estimated by phase detector. The self-tuning LNA is working within a frequency range from 880 up to 950 MHz, and it has high quality factor Q, and high gain (20 dB). The duration of the entire self-tuning process is less than 1 μs in full frequency range of STLNA operation. The proposed circuit is useful for realization of narrow-band amplifiers implemented in heterodyne receivers. Simulation results are promising for practical implementation of the described solution.

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