Design of MAC With Improvement in Performance

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Abstract: - **In this paper a new technique is proposed and implemented by the help of the accumulator oriented multiplier and termed as the protocol of the MAC with the improved performance of the storage of the 64 bit data. The performance of the unit related to the MAC protocol is integrated by the help of the processor of the digital signal for the evaluation of the operation related to the unit of MAC plays a crucial role in its analysis point of view respectively. Here the design of the multiplier based on the modified multiplier wallace adder of the carry save is used as the adder operationality respectively. The implementation of the proposed system is in the language of the source code of the VHDL and the compiler of the RTL cadence is used for the synthesis effectivity under the technology of the TSMC of the included library functions in a typical fashion. Here implementation is in such a way that there is a reduced dissipation of the power at the time of the analysis and the implementation structure and design based criteria. Experiments have been conducted on the present method where there is a lot of analysis takes place on the present method in which a huge number of test beds have been conducted for the calculation of the performance of the system in a well oriented fashion respectively.**

Keywords: **MAC Design, Improved performance, Real time logic cadence, Adder of carry save, Multiplier, Accumulator, Modified multiplier of Wallace and Processor of digital signal respectively.**

I. INTRODUCTION

As moving in to the everyday life there is a lot of advancement takes place in the system in terms of the utilization and it should be reliable followed the accurate synthesis and the order of integration in a well oriented fashion. Under the applicability of the processing unit of the signals based on the digitized condition there is a mandatory integration of the unit of MAC which plays a crucial role for the operation in the basic terminology and the needs of the implementation respectively [1][2]. Here the applicability operations includes additions and multiplications etc. For the further improvement in the performance of the system in the processing of the signal relative to the digital environment MAC layer plays a crucial role in its analytics skills respectively. Some of the applications of the processing of the signal in the digitized environment includes cosine transformation in the discrete environment, Transformation with respect to the wavelet based features and also the functions of the non linear characteristics respectively [5]. Here the applications oriented are repetitive in nature by the proper integration of the accumulator followed by the operation related to the arithmetic scenario respectively. Here it is mainly used for the flexible analysis and also the reduced time and reduced complexity finally accurate processing speed for the proper maintenance of the module respectively.

BLOCK DIAGRAM

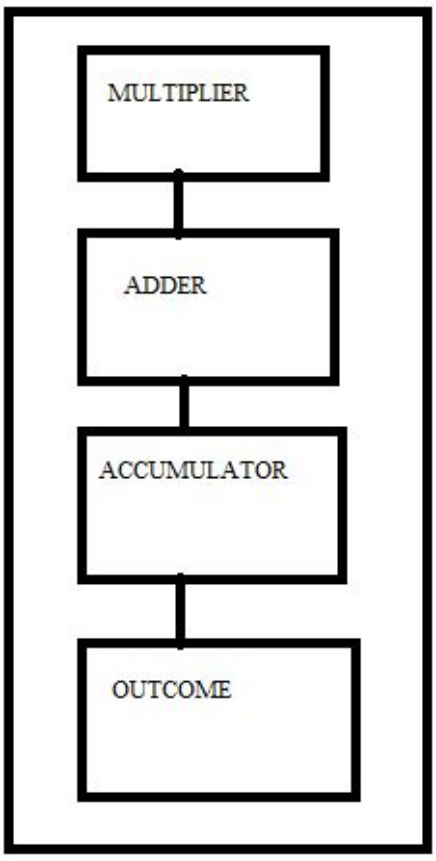

Fig 1: Shows the block diagram of the present method respectively

II. METHODOLOGY

In this paper a new technique is propose under the algorithm of the protocol related to the MAC is a major concern which is used in the integrated fashion with respect to the processor of the signal based on the digitized environment respectively. Here the proper implementation of the system is shown by the above block diagram and is also explained in the summarized fashion respectively. Here the operation of the MAC includes (accumulator multiplier) used for the applications of the DSP followed by the processing information the multimedia and other [6][7][8]. Here the integration of the adder followed by a multiplier and and accumulator in the integrated fashion forms the MAC protocol respectively. Here in the implementation of the present strategy there is a utilization of the accumulator of the multiplier of the 64 bit storage of the Wallace scenario where from the location of the memory the inputs are obtained from the block of the multiplication respectively.

III. EXPECTED RESULTS

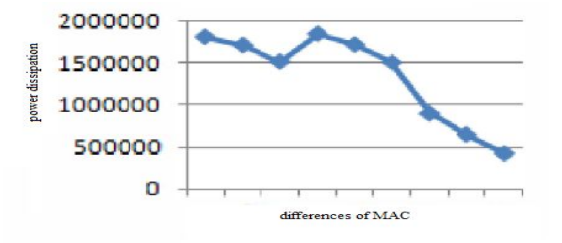

Fig 2: Shows the graphical representation of the present method respectively

Here the present method is effective and efficient in terms of the performance followed by the outcome of the entire system in a well oriented fashion as comparing to that of the several previous methods and are shown by the above diagram in the comparative fashion respectively. A lot of analysis and the large number of the test beds have been conducted in order to evaluate the results and also the performance evaluation takes place in terms of the data storage and the efficiency under the scenario of the reliability and the sped of the process and the task implementation and also fulfilling the integration part with respect to the processor of the signal related to the digital environment respectively. Here we finally conclude that the present method is effective and efficient in terms of the entire aspect of the system as per the all parameters plays a crucial role.

IV. CONCLUSION

In this paper a new technique is proposed by the accumulation of the protocol of the 64 bit Wallace accumulator in order to improve the performance of the system. Here for the further improvement of the performance of the entire system there is a requirement or the utilization of the accumulator and the multiplier of the size of the bit 64 for the further improvement in the performance of the entire system. Here the operation of the MAC includes 217 mega hertz of the frequency and dissipation of the power is 177 mega watts of the relative protoc of the unit of MAC and 542177 unit of the occupied area inclusive of the delay of the 64 bits transfer for the system oriented processor based performance improvement respectively. Here the complete simulation is done by the help of the VHDL software where the complete coding is made.

V. REFERENCES

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