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EFFICIENT IMPLEMENTATION OF CHANNEL CODING AND INTERSPERSING IN MIMO-OFDM SYSTEMS

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Abstract:- **The standards for high speed data communications in wireless LAN and MAN such as Worldwide Interoperability for Microwave Access (Wi MAX) is mainly used by Orthogonal Frequency Division Multiplexing (OFDM). An analysis of the different channel coding and interleaving schemes is presented in this paper which is used in MIMO-OFDM systems. Based on the bit error rate (BER) performance and hardware implementation issues a comparison of these schemes is presented. An examination is done on the effects of four different types of channel coding and interleaving schemes which are being used. The Wi MAX or IEEE 802.16 is used as a reference for imitation, execution, and analysis. The cross-antenna coding and per-antenna interleaving systems perform better under all signals to noise ratio (SNR) conditions for all modulation schemes which is shown from the above coding and interleaving schemes which are studied. The data rates for IEEE 802.16 are doubled for 2x2 MIMO systems without using the transmit diversity using the proposed schemes.**

Keywords: **MIMO, Bit Error Rate, Wi MAX, Interleaving Schemes, Channel Coding, OFDM.**

I. INTRODUCTION

At the algorithmic and system design levels, the active research is currently being carried out in the field of Multiple-Input Multiple-Output (MIMO)-OFDM systems [1]. Using adaptive modulation and coding rates over a 4x4 MIMO channel an FPGA based MIMO-OFDM transceiver is investigated [2]. In an FPGA implementation of Viterbi decoders for MIMO bit-interleaved coded modulation (BICM) schemes is presented. Using pipelined Fourier Transform (FFTIIFFT) stages an efficient FPGA-based implementation of the MIMO-OFDM physical layer is proposed. Using a high-level design tool the design, validation and FPGA based implementation of an OFDM modulator for IEEE 802.16-2004 is presented [3] and the number of required resources is also reported. By using HDL and AccelDSP tool, two different approaches are used for the implementation of Wi MAX on a Xilinx Vitex-II FPGA [4] comparing the resource usage and performance of both the implementations. The role of the complication coder and intersperse in the system performance is one aspect of the MIMO-OFDM system that is not investigated. In per-antenna complication coding with cross-antenna interleaving is adopted, while in per-antenna complication coding and interleaving is used [5]. In this paper, we analyze the performance and computational complexity of four possible configurations of complication coding and interleaving for the first time. This paper focuses mainly on the FPGA implementation issues and analysis of MIMO-OFDM based communication systems' physical layer [6]. Therefore, channel and interference related issues are out of the scope of this paper.

II. DIFFERENT SCHEMES FOR DOUBLE DATA STREAM MIMO SYSTEMS

The forward error correction (FEC) blocks include difficulty encoding, puncturing, and interspersing. Using punctured codes with constraint length K=7 the input bit stream is first encoded, and then interleaved to leverage frequency diversity. This is followed by gathering mapping which is depending on the Signal-to-Noise Ratio (SNR) at the receiver. The most computationally complex part of the system is the IFFT block which computes a 256-point IFFT of the input symbol. To avoid inter-symbol interference in the case of any delay at the receiver a cyclic prefix is inserted at the start of every symbol. The cyclic prefix is inserted at the end which completes the OFDM symbol and is then transmitted over the channel. In this analysis, we use four different methods of double data stream MIMO systems. These are categorized as follows: Case 1: Cross-antenna (C-A) complication coding with Per-antenna (P-A) interleaving. Case 2: Per-antenna complication coding with per antenna interleaving. Case 3: Cross-antenna complication coding with cross antenna interleaving. Case 4: Per-antenna complication coding with cross antenna interleaving. Using a complication encoder the input data is first encoded followed by puncturing in all these cases.

Using a block intersperse interleaving which is implemented, whose size varies according to the modulation scheme used and the system configuration. The receiver performs these functions in reverse order to retrieve the data.

III. HARDWARE RESOURCE UTILIZATION AND POWER DISSIPATION

The overall resource utilization by the complete system is shown in our paper when Auto or Distributed RAM extraction method is used during synthesis. In order to save distributed RAM resources and improve the operating frequency of the system the block RAMs are instantiated for the higher size intersperses. The slice logic utilization is reduced and the operating frequency of the overall system is improved as it resulted in wastage of RAM resources. This is beneficial when there are enough RAM resources available to be used. There is no wastage of RAM resources but the number of slice logic utilization increases by a small amount and the operating frequency of the overall system are reduced in distributed RAM extraction method. This method is advantageous when we have less RAM resources and the desired speed of the system could be achieved easily. The overall resource utilization of all the four different types of systems is almost the same due to the large number of resource utilization by OFDM modulation. A major difference is in the usage of block RAMs for bigger size of intersperses in Case 3 and Case 4 systems. The power dissipated by each transmitter type being implemented, including two OFDM modulation blocks implemented in parallel on each data stream. We can see that the power dissipation increases with the increase in modulation symbol size from BPSK to 64-QAM as well as going from Case 1 to Case 4 implementation. The clocks and memory are the two main contributors to dynamic power consumption. The power dissipation reduces significantly because of the smaller size of memory used for implementation when using distributed RAM extraction method during synthesis. The power dissipation with distributed RAM shows a significant reduction in power dissipation for Case 3 and Case 4 systems because they use distributed RAM instead of block RAM. Because of the smaller size of intersperses case 1 and case 2 systems use distributed RAM in both the implementations, so the power dissipation is the same in both cases. The power dissipation increases with the increase in operating frequency and size of the memory used for intersperses.

IV. EXPECTED RESULTS

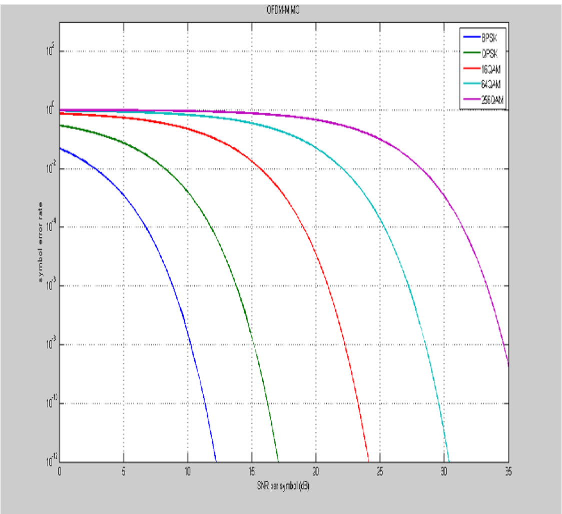

Fig 1: Shows graphical representation

V. CONCLUSION

The Case 1 system wins in all aspects of system performance and power dissipation as discussed above which is followed by Case 2, while the Case 4 system performs worse. Due to the same size of memory required for intersperses where the hardware resource utilization is almost the same for all systems, and the OFDM modulation blocks that requires most of the hardware in the system. Overall, the systems with same type of interleaving scheme follow each other closely in terms of BER performance, resource utilization, and power consumption, among which the P-A interleaved systems perform better. Case 1 system is the best choice as it shows a significant decrease in power dissipation compared to other systems if power indulgence is the most important factor. However, Case 1 system is followed by the Case 3 instead of Case 2 system because of not using a larger block RAM resource for distributed RAM implementation.

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