Power Minimization Of Logical Circuit Through Transistor Stacking

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Abstract- **This paper deals with the reduction of power dissipation in the basic logic circuit like NAND gate and NOR gate by using transistor stacking technique. The logic gates are designed using 130nm technology parameter and are simulated using PSPICE. The input vector combinations are compared with the simulated result on the basis of propagation delay and power consumption. It is found that when the number of low input increases in case of NAND gate the power dissipation decreases but the delay increases and for NOR gate power dissipation decreases with the increase in high input vector combinations.**

Keywords: Low Power, Propagation Delay, Power Dissipation, Sub-threshold current, Stacking effect.

I. INTRODUCTION

With the rapid progress in semiconductor technology, chip density has increased. This scaling of transistor feature sizes has provided a remarkable advancement with the increase in speed and frequency of operation and hence higher performance is achieved but the power dissipation also increases. High power dissipation reduces the battery service life. Therefore, power dissipation has become critical concern in today's VLSI system design [1]

Lowering the supply voltage (V_{DD}) is the most effective way to reduce the power consumption because it quadratically depends on V_{DD} but as V_{DD} reduces circuit delay will increase and thus degrades the performance. At the same time it is possible to maintain the performance by decreasing the threshold voltage (V_{TH}) but then sub-threshold leakage power increases exponentially. Therefore, V_{DD} and V_{TH} have to be optimized to achieve the required performance and lowest power [2]. As the feature size reduces shorter channel length results in sub threshold leakage current through a transistor when it is off. Thinner gate oxides have led to an increase in gate leakage current. Therefore, static power consumption i.e. leakage power dissipation becomes an important portion of total power consumption. In 180 nm and below technologies, leakage accounts for 30-40% of total power.

This paper is summarized as follows: Section II gives brief introduction about sources of power dissipation. Section III discusses stacking technique to reduce the power dissipation. Section IV consists of proposed work and comparison of results.

II. SOURCES OF POWER DISSIPATION

IC power dissipation consists of different components depending on the circuit operating mode [4].

A. Active Component

Dynamic switching power and short circuit power are active component of power dissipation. These occur due to transitions at gate terminals which is caused by charging and discharging of capacitors in the circuit [5].

$$P_{dynamic} = C_L V_{DD}^2 f \quad (1)$$

B. Standby Component

Static biasing power and leakage power are standby component of power dissipation. These occurs in

weak inversion region when gate-to-source voltage is less than threshold voltage.

$$I_{SUB} = Ae^{\frac{q}{nkT}(V_{GS}-V_{THO}-\gamma V_{SB}+\eta V_{DS})}(1-e^{\frac{-qV_{DS}}{kT}}) \quad (2)$$

III. CIRCUIT TECHNIQUES TO REDUCE POWER DISSIPATION

There are various techniques to reduce power dissipation in a circuit. Some of them are: Body Biasing, Source Biasing, Voltage Scaling, Sleep Transistor and Transistor Stacking Technique. In this section we will discuss transistor stacking technique in detail.

A. Transistor Stacking Technique:

Subthreshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off. This effect is known as the "stacking effect" or "self-reverse bias". Leakage currents in NMOS or PMOS transistors depend exponentially on the voltage at the four terminals of transistors. V_G is "0" thus increasing V_S of NMOS transistor reduces subthreshold leakage current exponentially [6].

Let us consider a stack of two NMOS transistors as shown in the Figure.1 below. When both transistor M1 and M2 are turned off, the voltage at the intermediate node (V_M) is positive due to small drain current. Positive potential at the intermediate node has the three following effects:

1) Due to the positive source potential V_M, gate to source voltage (V_{GS1}) of transistor M1 becomes negative; hence, the subthreshold current reduces substantially.
2) Due to $V_M > 0$, body to source potential (V_{BS1}) of transistor M1 becomes negative, which results in an increase in the threshold voltage (larger body effect) of M1, and thus reducing the subthreshold leakage.
3) Due to $V_M > 0$, the drain to source potential (V_{DS1}) of transistor M1 decreases, which results in an increase in the threshold voltage (less DIBL) of M1, and thus reducing the subthreshold leakage.

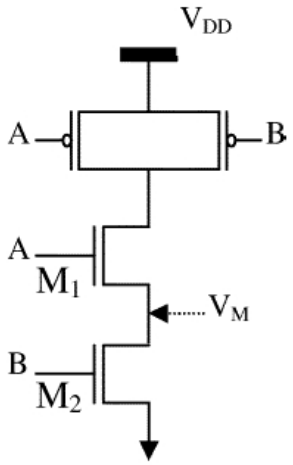

Figure. 1: Effect of transistor stacking on source voltage

If only one NMOS device is off, the voltage at the source node of off transistor would be virtually zero because all other on transistors will act as short circuit. Thus, there is no self reverse biasing effect, and the leakage across the off transistor is large. But if more than one transistor is off, the source voltages of the off transistor, except the one connected to ground by transistors, will be greater than zero, and the leakage will be determined mainly by the most negatively self-reverse biased transistor (because subthreshold leakage is an exponential function of gate-source voltage The reverse bias makes the leakage across the off transistor very small.

1) Input Vector Dependence:

Functional blocks such as NAND, NOR or other complex gates have a stack of transistors. Due to the stacking effect, the subthreshold leakage through a logic gate depends on the applied input vector. By applying proper input vectors in a stack we can increase the number of off transistors and can reduce the standby leakage of a functional block.

2) Source Biasing:

In this technique instead of keeping the source terminal of NMOS transistor at ground it is biased. It is used to reduce the power supply voltage in standby mode. During switching, there would be a voltage

drop across the footer transistor. This reduces the effective V_{DS} for the switch transistor and hence the I_{DS}.

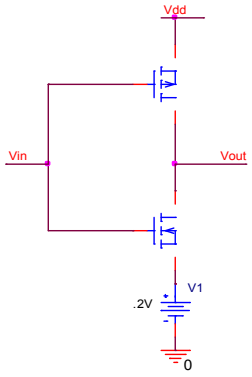

Figure 2: Source Biasing

IV. PROPOSED WORK

Here, we have simulated basic logic gates like inverter, NAND and NOR gate using transistor stacking techniques. By varying the combination of input vectors of the NAND gate and NOR gate the delay and power dissipation have been calculated. All the analysis are done by considering the threshold voltage V_{TO} = 0.39V and by using 130nm technology.

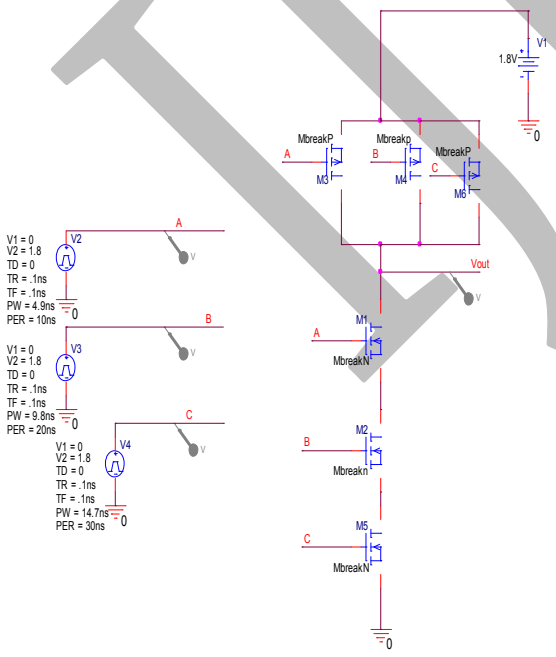

Fig.ure3: Transistor is stacked in NAND Gate

A	B	NAND	Power Dissipation (W)	Delay(ps)
0	0	1	$1.10x10^{-9}$	52.64
0	1	1	$2.27x10^{-9}$	45.38
1	0	1	$2.24x10^{-9}$	40.97
1	1	0	$3.38x10^{-9}$	50.25

Table 1: Estimated power dissipation and delay by varying input vector combination(3-input NAND)

A	B	C	NAND	Power Dissipation(W)	Delay(ps)
0	0	0	1	$7.56x10^{-10}$	10.93
0	0	1	1	$1.10 x10^{-9}$	14.95
0	1	0	1	$1.10x10^{-9}$	9.95
0	1	1	1	$2.27 x10^{-9}$	29.97
1	0	0	1	$1.10x10^{-9}$	4.97
1	0	1	1	$2.24 x10^{-9}$	14.95
1	1	0	1	$2.23 x10^{-9}$	9.97
1	1	1	0	$5.07 x10^{-9}$	0.045

Table 2: Estimated power dissipation and delay by varying input vector combination
(2-input NAND)

- When all the inputs are low (all NMOS transistors are OFF) the power dissipation is minimum and when all the inputs are high (all NMOS transistors are ON) the power dissipation is maximum. As we can see from the above table 4.7, if the number of low input increases, the power dissipation decreases because the sub threshold leakage current that is flowing through a stack of series-connected transistors decreases when more than one transistor in the stack is turned off.

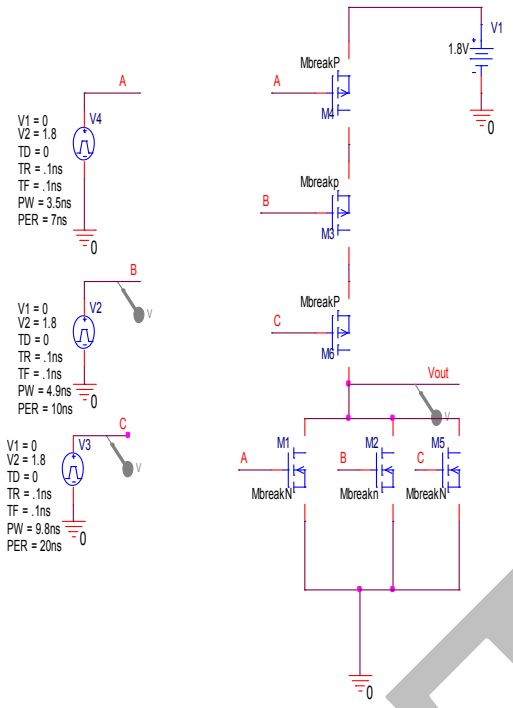

Figure 4: Transistor Stacking in NOR Gate

A	B	C	NOR	Power dissipation (W)	Delay(ps)
0	0	0	1	$6.8x10^{-9}$	58.87
0	0	1	0	$1.69 x10^{-9}$	50.29
0	1	0	0	$1.67x10^{-9}$	50.67
0	1	1	0	$8.22 x10^{-10}$	54.2
1	0	0	0	$1.66x10^{-9}$	52.40
1	0	1	0	$8.22 x10^{-10}$	43.42
1	1	0	0	$8.21 x10^{-10}$	44.48
1	1	1	0	$5.66 x10^{-10}$	48.28

Table 3: Estimated power dissipation and delay by varying input vector combination (3-input NOR)

A	B	NOR	Power Dissipation(W)	Delay(ps)
0	0	1	$4.54x10^{-9}$	47.96
0	1	0	$1.69x10^{-9}$	44.76
1	0	0	$1.67x10^{-9}$	48.87
1	1	0	$8.22x10^{-10}$	46.21

Table 4: Estimated power dissipation and delay by varying input vector combination (2-input NOR)

- When all the inputs are low (all NMOS transistors are OFF) the power dissipation is maximum and when all the inputs are high (all NMOS transistors are ON) the power dissipation is minimum. As we can see from the above table 4.7, if the number of low input increases, the power dissipation increases.

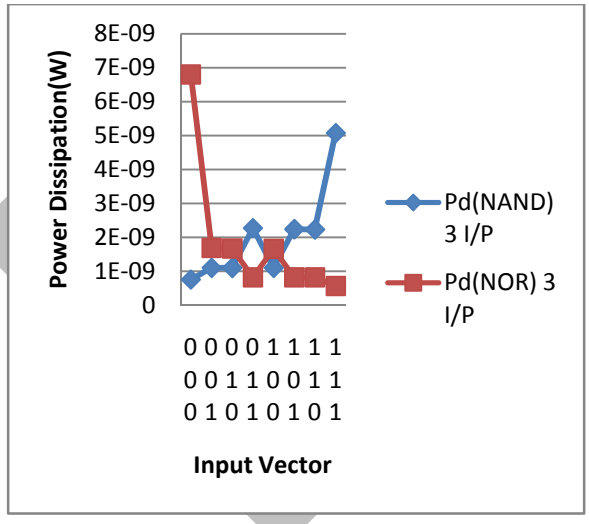

Figure 5: Power Dissipation vs. Input vector (3 input)

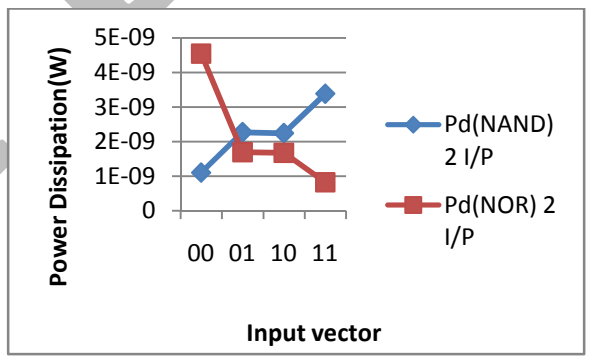

Figure 6: Power Dissipation vs. Input Vector (2 input)

V. CONCLUSION

With the continuous scaling of CMOS devices, leakage current is becoming a major contributor to the total power consumption. We have applied transistor stacking technique to the NAND gate and NOR gate and estimated their delay and power dissipation. From all the simulation and calculation we have come to a conclusion that by varying the input vector combination we can reduce the power dissipation. There is a tradeoff between power and

delay. So, to optimize the circuit we need to have minimum delay and power dissipation without degrading the performance.

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