

Optimal PWM for Three-Level Inverter fed High Speed Drives

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Abstract—Thanks to new field of applications, like high speed/high-pole drives with high rated fundamental frequency or multilevel converters powering medium or high voltage drive systems, optimized PWM techniques became again a hot topic of research interest. The current paper introduces an optimized PWM technique for three-level inverter, which can be applied to supply high speed drives at low pulse ratio. The optimization is done for the lowest loss-factor, which is proportional to the square of rms value of current harmonics. The performance of the optimal PWM technique is demonstrated by simulation and experimental tests by using a NPC type inverter.

I. INTRODUCTION

Nowadays increasing attention has been paid to high speed induction and permanent magnet synchronous machines (PMSMs) [1], [2], [3], [4], [5]. The high rated fundamental frequency f_1 (from few hundred up to thousand Hz) and the limited carrier (switching) frequency f_c ($\leq 15-25$ kHz) result in low $m_f = f_c/f_1$ frequency ratios (usually $m_f < 21$). The low frequency ratios using two-level voltage source inverter (2L-VSI) result in a far more unfavorable stator voltage, flux and current harmonic spectra. Furthermore, the inductance of high speed machine is designed to be small compared to ordinary motors. This can result in high ripple of the current flowing through the motor, which can increase the losses significantly [4].

It should be noted that, the problems mentioned previously with the high speed drives also can occur in high-pole count motors, used for example in hybrid or electric vehicles. The mechanical speed of these motors is a few thousand rpm, but thanks to the high-pole count, the f_1 synchronous frequency should be very high (higher than 1 kHz).

In very high power drive systems, the thermal limitation of semiconductor devices also restricts the switching frequency to a few hundred Hz resulting also a very low m_f frequency ratio even at standard (50–60 Hz) f_1 fundamental frequencies.

A good solution for the problems caused by low frequency ratio is to apply multilevel inverter topology. The most popular multilevel topologies are diode-clamped or neutral-point-clamped (NPC), capacitor-clamped or flying capacitor (FC) and cascaded H-bridge converters (CHB) [6], [7]. In the literature many modulation techniques have been introduced to control multilevel topologies. Most commonly carrier based Pulse Width Modulation (PWM) or Space Vector Modulation (SVM) techniques are used thanks to their high performance,

simplicity, fixed switching frequency and easy digital implementation. Paper [8] introduces a SVM technique which simplifies the detection of the nearest voltage vectors. A simplified PWM technique for three-level NPC inverter is proposed in [9] to balance DC link voltages.

Instead of applying carrier based or SVM techniques, programmed modulation strategies can be used as well to control multilevel VSIs. In this case the overall approach to define the switching times is based on the minimization of a suitable objective function which typically represents system losses [10]. This technique became known as Synchronous Optimal Pulsewidth modulation (SOP), sometimes also referred as Optimized Pulse Pattern [11]. Applying optimal PWM techniques for ac drive systems has been investigated since the seventies of the last century [12], [13], [14]. At the same time, the interest on optimized PWM technique was virtually lost in the last two decades thanks to the evolution of faster power semiconductor devices enabling high switching frequencies [11]. Thanks to the new applications, like high speed/frequency drives or multilevel converters powering medium or high voltage systems, the optimized PWM techniques became again a hot topic of research interest [2], [7], [11], [15], [16], [17], [18], [19]. Paper [11] introduces a novel formulation for the problem of optimizing the modulation pattern of multilevel converters. An optimized PWM technique for three-level NPC inverter to minimize torque ripples of induction machine is introduced in [16]. Paper [17] presents a SOP method with practical implementation issues for modular multilevel converters. A generalized method for optimization for low switching frequency is proposed in [18], where the so-called distortion factor is minimized during the calculation of the switching instants.

Furthermore, the high performance digital devices allows the simpler implementation of optimal methods, which can cause their wider spread in practice. Paper [20] demonstrates the use of a digital card flashmemory to follow a preprogrammed optimal PWM pattern.

The authors presented a loss-optimal PWM for the linear modulation region and for the overmodulation region of a 2L-VSI in [21] and [22], respectively.

The goal of the current paper is to extend the method to three-level voltage source inverter (3L-VSI) for the whole modulation region. In the literature, to calculate optimal

switching angles quarter-wave symmetry is typically assumed and the switching angles are calculated for $0 - \frac{\pi}{2}$ range [2], [3], [7], [11], [16], [17], [19]. In the current paper 60° vector (voltage, current, etc.) symmetry will be assumed and the angles are calculated only for the $0 - \frac{\pi}{6}$ intervallum. It results considerably less computational effort at the same pulse ratio as the number of varying switching angles is less.

The calculation results will be demonstrated by using an NPC type three-level inverter, but it can be easily adopted to any other three-level topology, like CHB or Active NPC. Figure 1 shows the three-level NPC topology with the possible transistor switch states for one phase and the output voltage vectors for the $0 - \frac{\pi}{3}$ intervallum (sector 1).

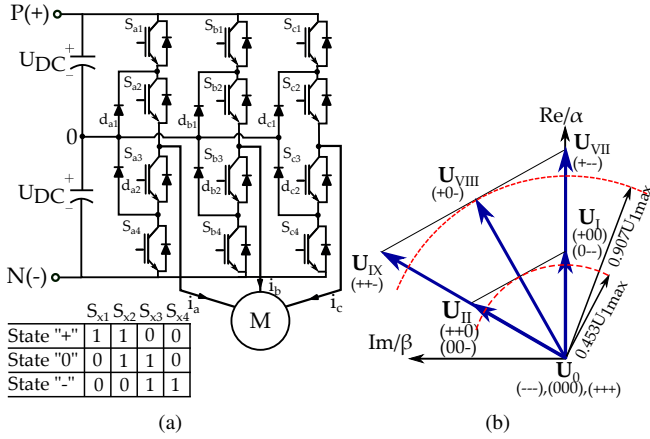


Fig. 1. Topology of NPC with the possible transistor switch state for one phase (a) and the output voltage vectors for the $0 - \frac{\pi}{3}$ intervallum (b)

II. THEORETICAL BACKGROUND

Generally the U_1 peak of the output voltage of a 3L-VSI is expressed with the so-called modulation index $m = U_1/U_{1max}$. U_{1max} is the maximum output phase voltage of a 3L-VSI $U_{1max} = 4U_{DC}/\pi$, where $2U_{DC}$ is the DC-link voltage of the NPC inverter (see Fig.1(a)).

A. Loss-factor

The harmonic losses of an induction machine can be characterized by the loss-factor [14], [22], which can be calculated as follows

$$K'_\Psi = (\sigma L_s)^2 \sum_{\nu>1} i_{s,\nu}^2 = \Psi_s^2 - 1 = \sum_{\nu>1} \frac{U_{s,\nu}^2}{U_{s,1}^2 \nu^2} \quad (1)$$

where $i_{s,\nu}$ and $U_{s,\nu}$ are the stator current and voltage harmonics of the order ν , respectively. σL_s is the stator transient inductance, where $\sigma = 1 - L_m^2/(L_s L_r)$, where L_s , L_r and L_m are the stator, rotor and the mutual inductance, respectively. Ψ_s is the rms value of the stator flux. In (1) all the values are in pu system and it was assumed that the machine operates at its rated stator flux. In opposite case (1) should be multiplied by $\Psi_s^2/\Psi_{s,rated}^2$.

Later on, we will use the relative loss-factor $K_\Psi = K'_\Psi/0.00215$, where $K'_\Psi = 0.00215$ is the loss-factor of the

inverter operating in six-step mode, when $m = 1$ [22]. In practice it is desirable to obtain a K_Ψ loss-factor value lower than 0.1. In this case the effect of the harmonic losses can be neglected and the underrating or additional cooling of the machine is not necessary.

B. Waveform Quality

In the current paper the optimization is elaborated for the lowest loss-factor, which is proportional to the square of rms value of current harmonics (see (1)). In most cases the optimization is done to minimize the THD in line current [10], where I_{THD} is defined as $I_{THD} = \sqrt{\frac{\sum_{\nu>1} i_{s,\nu}^2}{i_{s,1}^2}}$. As I_{THD} depends on machine parameters, another quantity, the weighted THD of the voltage V_{WTHD} is introduced as a performance index of PWM strategies [10], [15]. V_{WTHD} is defined as $V_{WTHD} = \sqrt{\frac{\sum_{\nu>1} U_{s,\nu}^2/\nu^2}{U_{s,1}^2}} = \sqrt{K'_\Psi}$. So V_{WTHD} is the square root of the loss-factor.

In paper [18] the so-called d distortion factor is minimized to obtain optimal pulse pattern. The distortion factor is the square root of the relative loss factor as $d = \sqrt{K_\Psi}$.

Later on, not only the relative loss-factor, but the value of I_{THD} , V_{WTHD} and d are used in some cases as well to indicate the performance of the optimal PWM technique to be able to compare results with those obtained in other papers. Where V_{WTHD} or d are not given directly, they can be calculated easily using the equations above.

III. LOSS OPTIMIZED PWM FOR THREE-LEVEL INVERTER

To goal of the optimization is to find the minimum of the following constrained nonlinear multivariable function

$$F = \frac{\Psi_s^2}{\Psi_{s,1}^2} - 1 + \lambda |\Psi_{s,1}^2 - 1| \quad (2)$$

where $\Psi_{s,1}$ is the value of the fundamental stator flux in per unit, and it was assumed that, the machine operates at its rated stator flux. F depends on θ_i switching (commutation) angles and on λ . The computation starts from a given value of modulation index m , λ and a selected voltage vector sequence as well as initial switching angles. The calculation was done by using numeric methods and by utilizing the `fmincon()` in-built function of MATLAB. All the equations and constraints required to carry out the optimization are given in the Appendix.

Due to the symmetry of vector paths computations should be performed only for $0 \leq \omega_1 t \leq \pi/6$ sector. In this sector only voltage vectors $\mathbf{U}_I = \frac{2}{3}U_{DC}$, $\mathbf{U}_{II} = \mathbf{U}_I e^{j\pi/3}$, $\mathbf{U}_{VII} = \frac{4}{3}U_{DC}$, $\mathbf{U}_{VIII} = \frac{2}{\sqrt{3}}U_{DC}e^{j\pi/6}$, and zero voltage vectors \mathbf{U}_0 can be used for optimal PWM.

In the case of three-level inverters the modulation region can be divided into three regions from calculation point of view. In the first region ($0 < m < 0.453$, see Fig.1(b)) \mathbf{U}_I , \mathbf{U}_{II} and \mathbf{U}_0 voltage vectors can only be used for optimal PWM. Neither \mathbf{U}_{VII} or \mathbf{U}_{VIII} voltage vectors can improve the performance in this region. In the second region ($0.453 <$

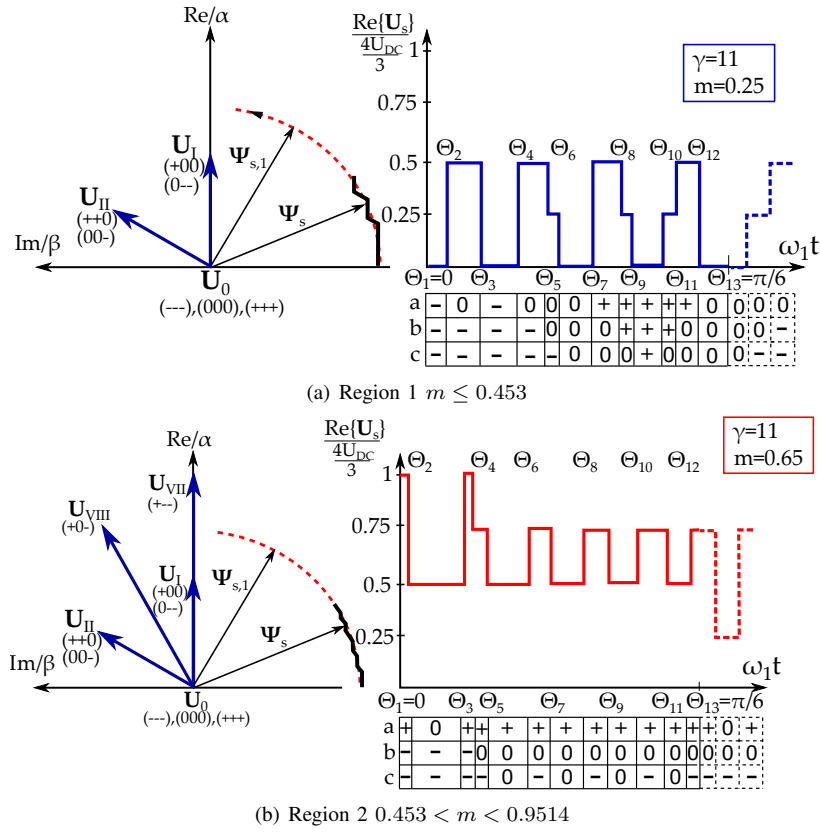


Fig. 2. Voltage vectors, time function of real component of the output voltage and the trajectory of stator flux vector

$m < 0.9514$) the voltage vectors \mathbf{U}_I , \mathbf{U}_{II} , \mathbf{U}_{VII} , \mathbf{U}_{VIII} and \mathbf{U}_0 can be used. However, for optimal operation zero voltage vectors and \mathbf{U}_{II} should be used relatively rarely and only for the lower part of this region. In the third region ($m > 0.9514$) voltage vectors \mathbf{U}_{VII} and \mathbf{U}_{VIII} should be used. Current paper focuses only on region 1 and 2. The third region will be discussed in another paper.

The number of switching per transistor during one fundamental period is denoted by γ . For a given γ the number of applying voltage vectors in $1/12^{th}$ of fundamental period ($0 - \frac{\pi}{6}$ intervallum) is $\kappa = (\gamma + 1)$. The total number of switching angles in $1/12^{th}$ of fundamental period is $(\gamma + 2)$. As $\theta_1 = 0$ and $\theta_{\gamma+2} = \pi/6$, the number of varying switching angles is γ . During the optimization, a minimum duration for each voltage vector, denoted as θ_{min} , is defined to ensure a minimum on time and off time of the power semiconductor switches. Thus, between two consecutive switching angles the following constraint is used: $\theta_{i+1} \geq \theta_i + \theta_{min}$, where $i = 1, 2, \dots, \kappa$.

For demonstration purpose, Fig.2(a) ($m = 0.25$) and 2(b) ($m = 0.65$) present for $\gamma = 11$ the optimal voltage vector sequence, the time function of the real part of the stator voltage ($(\text{Re}\{\mathbf{U}_s\})/(4/3U_{DC})$) and the trajectory of the stator flux by neglecting the stator resistance for the first and the second region, respectively. The switch states of the phases are also denoted. The optimal voltage vector sequence for the $0 - \frac{\pi}{6}$

intervallum at $m = 0.25$ is (see Fig.2(a))

$$\mathbf{U} = [\mathbf{U}_0, \mathbf{U}_I, \mathbf{U}_0, \mathbf{U}_I, \mathbf{U}_{II}, \mathbf{U}_0, \mathbf{U}_I, \mathbf{U}_{II}, \mathbf{U}_0, \mathbf{U}_{II}, \mathbf{U}_I, \mathbf{U}_0].$$

For $m = 0.65$ it is (see Fig.2(b))

$$\mathbf{U} = [\mathbf{U}_{VII}, \mathbf{U}_I, \mathbf{U}_{VII}, \mathbf{U}_{VIII}, \mathbf{U}_I, \mathbf{U}_{VIII}, \mathbf{U}_I, \mathbf{U}_{VIII}, \mathbf{U}_I, \mathbf{U}_{VIII}, \mathbf{U}_I, \mathbf{U}_{VIII}].$$

As it can be seen the number of voltage vectors in the $0 - \frac{\pi}{6}$ region is $\kappa = \gamma + 1 = 12$, the total number of switching angles is $\gamma + 2 = 13$.

As it was mentioned before, due to the symmetry of vector paths, computations were performed only for the $0 - \frac{\pi}{6}$ intervallum and the voltage vectors are always given for this range. However, the voltage vector sequence for the $\frac{\pi}{6} - \frac{\pi}{3}$ intervallum as well as for other sectors can be easily determined from symmetry. For example voltage vector sequence for the $\frac{\pi}{6} - \frac{\pi}{3}$ intervallum for $m = 0.25$ and for $m = 0.65$ ($\gamma = 11$) are $\mathbf{U} = [\mathbf{U}_0, \mathbf{U}_{II}, \mathbf{U}_I, \mathbf{U}_0, \mathbf{U}_I, \mathbf{U}_{II}, \mathbf{U}_0, \mathbf{U}_I, \mathbf{U}_{II}, \mathbf{U}_0, \mathbf{U}_{II}, \mathbf{U}_0]$ and $\mathbf{U} = [\mathbf{U}_{VIII}, \mathbf{U}_{II}, \mathbf{U}_{VIII}, \mathbf{U}_{II}, \mathbf{U}_{VIII}, \mathbf{U}_{II}, \mathbf{U}_{VIII}, \mathbf{U}_{II}, \mathbf{U}_{VIII}, \mathbf{U}_{II}, \mathbf{U}_{VIII}]$, respectively.

For carrier based PWM modulation techniques or SVM, the ratio between the switching frequency f_c and the fundamental frequency f_1 is denoted as $m_f = f_c/f_1$. The equivalent switching frequency of the proposed optimal PWM can be

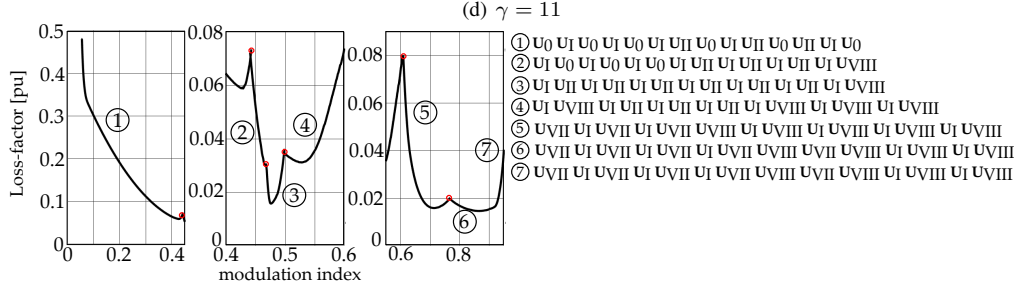
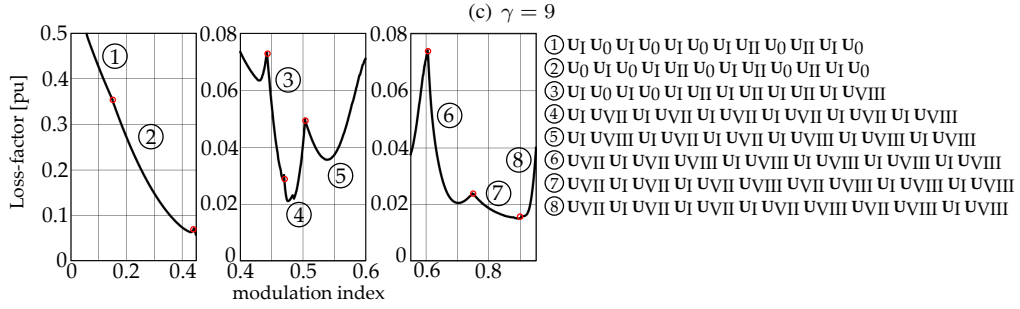
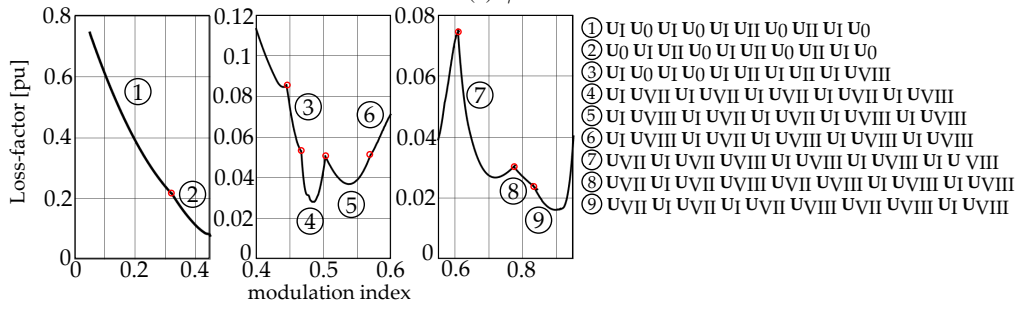
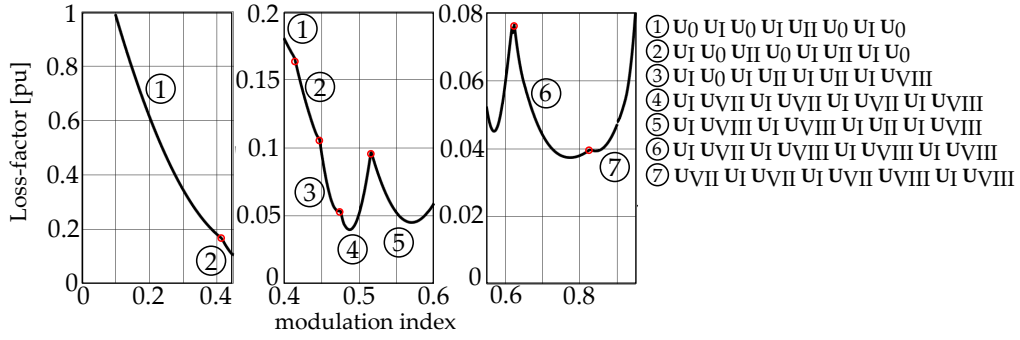
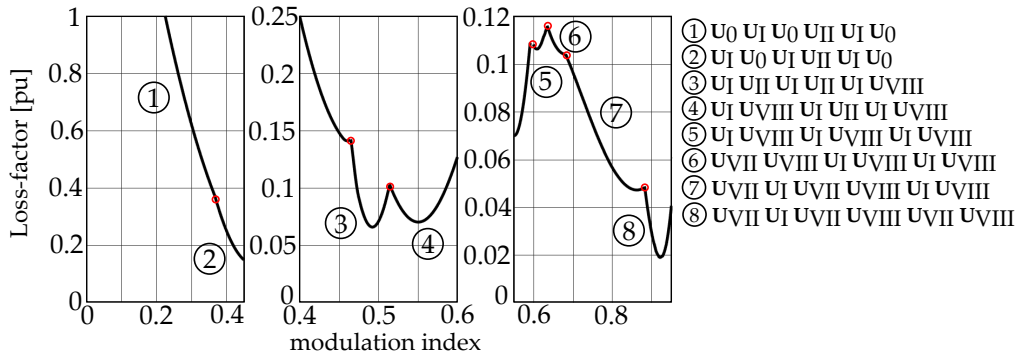


Fig. 3. Loss factor K_Ψ as the function of the modulation index m and the optimal voltage vector sequences in the $0 \leq \omega_1 t \leq \pi/6$ sector

calculated as $(2\gamma + 1)f_1$. Thus, the equivalent frequency or pulse ratio can be given as $2\gamma + 1$.

One of the most crucial part in the optimization is to select the proper voltage vector sequence. As it will be presented in the next section different combination provides the optimal performance at different γ and m values. By using unproper voltage vector sequence the loss-factor can be considerably higher.

IV. CALCULATION RESULTS

The K_Ψ loss-factor as the function of the modulation index for $\gamma = 5, 7, 9, 11$ and 13 are presented in Fig.3, where θ_{min} is selected to be 0.0065 rad, which results a few μs minimum on time even for high fundamental frequencies.

For better representation of the results, the curves are plotted for three different range of m with different vertical axis scale. From the different possible voltage vector sequences, on the basis of reasonable considerations and computations, the one with the lowest loss-factor have been selected. The voltage vector sequences are marked on the figures with circled numbers (1, 2, 3...). The optimal voltage vector sequences are given at the right side of the figures for the $0 \leq \omega_1 t \leq \pi/6$ sector. The borders of different range of voltage vector sequences are denoted by red circles on the figures.

As it can be seen at very low m values the loss factor is very large. It can be even larger than the loss factor belonging to the square wave mode of operation, where $K_\Psi = 1$. In the $m < 0.45$ region by increasing m the loss factor reduces at the same γ . Furthermore, in this part of the modulation range the loss-factor can be drastically reduced by increasing γ .

In the middle part of the modulation range $0.45 < m < 0.6$ a very low loss-factor can be obtained by using optimal voltage vector sequences which utilize voltage vector U_{VIII} . Naturally, by increasing γ the loss-factor is reduced even in this part of the modulation range. However, it can be concluded it is not worth to increase γ in this part of the modulation range, as a good harmonic performance ($K_\Psi < 0.1$) can be obtained even at low γ values.

As it was mentioned previously in the upper part of the modulation range ($m \geq 0.6$) it is not worth to use zero voltage vectors and U_{II} . In this part of the modulation range up to $m \approx 0.9$ the loss-factor decreases by increasing m . Furthermore, the loss factor can be reduced by increasing γ as well. Above $m = 0.9$ the loss factor starts to increase drastically and it cannot be reduced significantly by increasing γ . For $m > 0.95$ only voltage vectors U_{VII} and U_{VIII} should be used.

V. SIMULATION AND EXPERIMENTS

A. Simulation analysis

To verify the calculation results presented previously a complete NPC inverter were built using Matlab/Simulink. The inverter supplied a high speed induction machine with rated speed 18 krpm ($f_1 = 300$ Hz). The main parameters of the machine are: power: $P_N = 3$ kW, $U_{LL,RMS} = 380$ V, $f_{1N} = 300$ Hz, $R_S = 1.125\Omega$, $R_R = 0.85\Omega$, $X_{LS} = 4.71\Omega$

and $X_{LR} = 2.63\Omega$, $X_m = 84.82\Omega$ (all reactance are at rated frequency), number of pole pairs is $p = 1$.

The DC link voltage of the inverter was selected to be $2U_{DC} = 540$ V. The rated frequency of the machine is reached at $m = 0.907$. The voltage of the machine is controlled in open loop by keeping the stator flux constant ($U_1/f_1 = \text{const}$).

The simulated trajectories of the stator flux vector and the stator current vector for optimal PWM are shown in Fig.4(a) ($m = 0.25$, $f_1 = 82.7$ Hz), Fig.4(b) ($m = 0.55$, $f_1 = 182$ Hz) and Fig.4(c) ($m = 0.65$, $f_1 = 215$ Hz) when $\gamma = 11$. For a better comparison, the same results were depicted also for SVM on Fig.4(d), Fig.4(e) and Fig.4(f). The frequency ratio for SVM was $m_f = 2\gamma + 1 = 23$ to obtain the same number of switching over one fundamental period.

The value of the loss-factor K_Ψ , V_{WTHD} , d and the I_{THD} are depicted on the Figures. The simulations were carried out both at no-load and at rated load ($M_{load} = 1.5$ Nm). Generally the no-load I_{THD} is considered as performance index, since this represents the worst case [15] as the value of the no-load current should be substituted for the denominator of the equation.

The simulation results demonstrate that, the simulated value of K_Ψ is the same as the calculated one. As it can be seen for optimal PWM, the stator current and flux vector have a six sided symmetry. It can be concluded the optimal PWM has a better harmonic performance at the same number of switching than the SVM.

The switching loss caused by the optimal PWM technique was also investigated. A detailed loss estimator algorithm of power semiconductor devices, which takes into consideration the temperature dependency as well, was implemented in Matlab/Simulink. During the simulation the parameters of STGF19NC60KD IGBT and MUR1640CT diode were used, as the same devices were available in the laboratory setup.

The distribution of the simulated switching losses in per unit in one phase leg can be seen on Fig.5 for optimal PWM (left column) at rated load at $m = 0.25$, $m = 0.55$ and $m = 0.65$, when $\gamma = 11$. The base value for the per unit is the actual output mechanical power. For the better comparison the results obtained by SVM is also denoted (right column). As it can be seen not only the harmonic loss is smaller for optimal PWM, but the switching losses is also slightly reduced. As it can be seen the loss distribution among the semiconductor devices at low m value (see $m = 0.25$ on Fig.5) is considerably different for optimal PWM and SVM.

B. Experiments

A low power NPC type inverter was built in the laboratory to demonstrate the performance of the optimal PWM techniques. As it was mentioned previously STGF19NC60KD IGBT and MUR1640CT diodes were used to built the inverter.

The optimal PWM technique was implemented on a 32-bit DSP (TMS320F28379D). The duration of the voltage vectors (difference between two consecutive switching angles) divided by 2π is saved in Look-up table (LUT) as the function of m

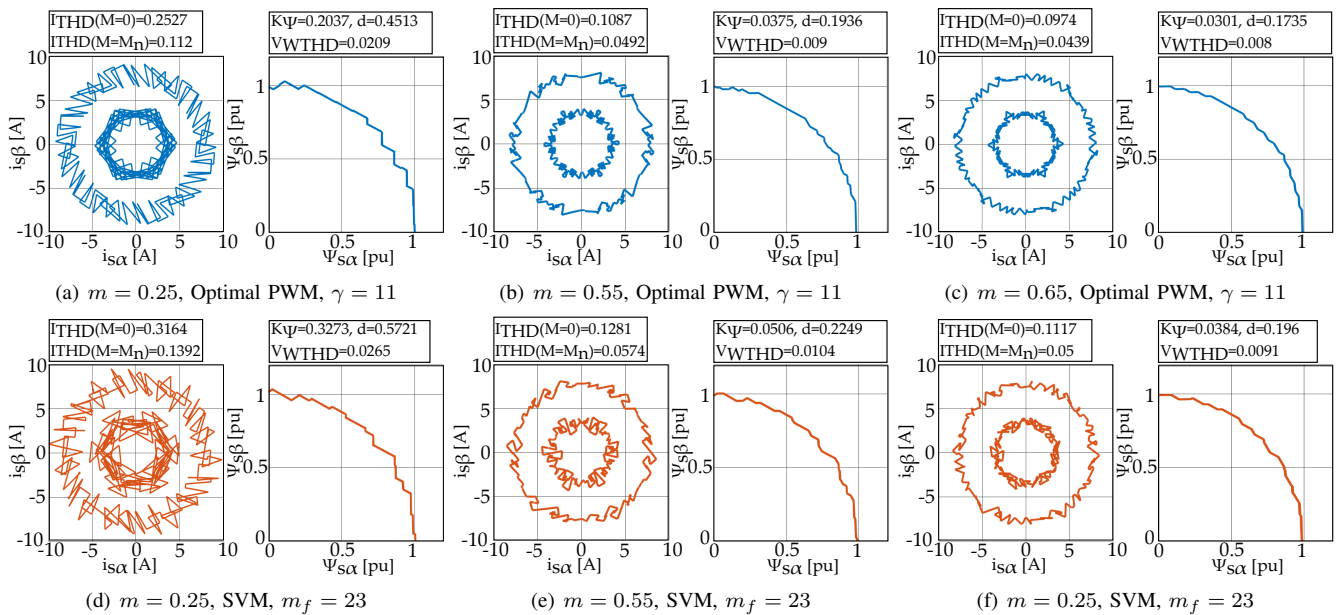


Fig. 4. Simulation result, trajectories of the stator current space vector (at no-load ($M = 0$) and at rated load ($M = M_n$) and the stator flux space vector both for optimal PWM and for SVM

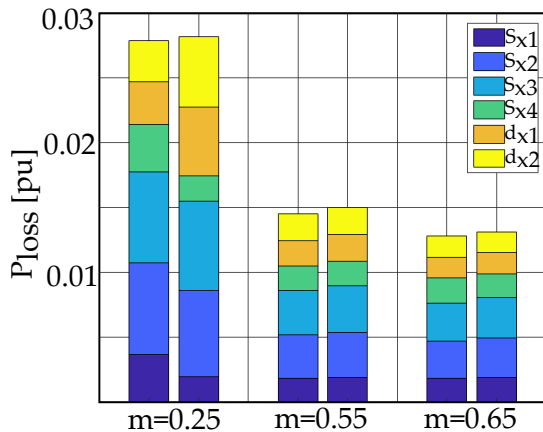


Fig. 5. Simulation result, switching losses in one phase leg. Left column: Optimal PWM, right column: SVM. Numerical values: $m = 0.25$: Optimal: 0.02785, SVM: 0.02812, $m = 0.55$: Optimal 0.0145, SVM: 0.015, $m = 0.65$: Optimal: 0.01279, SVM: 0.0131

and γ . In this way the same array can be used for different f_1 fundamental frequencies.

For simplicity the measurement was carried out using a lower DC bus voltage $2U_{DC} = 120V$ and lower stator frequencies to obtain rated stator flux.

The measured time function of the real and imaginary component of the output voltage space vector, the harmonic spectra of the phase voltage and trajectories of the stator flux vector at $m = 0.25$, $m = 0.55$ and $m = 0.65$ are shown in Fig.6. The value of the measured loss-factor K_Ψ , V_{WTHD} and d are depicted in the captions. The measurements were carried out at no-load.

The experimental results demonstrate that, the measured value of K_Ψ , V_{WTHD} and d is practically the same as the

calculated and simulated one. As it can be seen, the stator flux vector has a six sided symmetry and it is very similar to the simulated one presented previously. The harmonic spectra of the phase voltage shows that, the optimal PWM technique has a good harmonic performance.

The authors intend to carry out further laboratory measurements at higher frequencies, which will be presented in another paper.

VI. CONCLUSIONS

An optimal PWM technique for three-level inverter was introduced in the paper, which can be applied to supply high speed drives at low pulse ratio. The optimization is done to obtain the lowest loss-factor. The optimization was carried for the whole modulation region for $\gamma = 5, 7, 9, 11$ and 13 . The value of the loss-factor as well as the optimal voltage vector sequences as the function of γ and the modulation index m were presented in the paper. The results of computations were checked by simulation and experimental tests.

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APPENDIX

The value of the fundamental stator flux can be calculated as

$$\Psi_{s,1} = \frac{2}{m} \sum_{i=1}^{\kappa} \left[\sin(\theta_{i+1} - \beta_i) - \sin(\theta_i - \beta_i) \right] |SV|_i \quad (3)$$

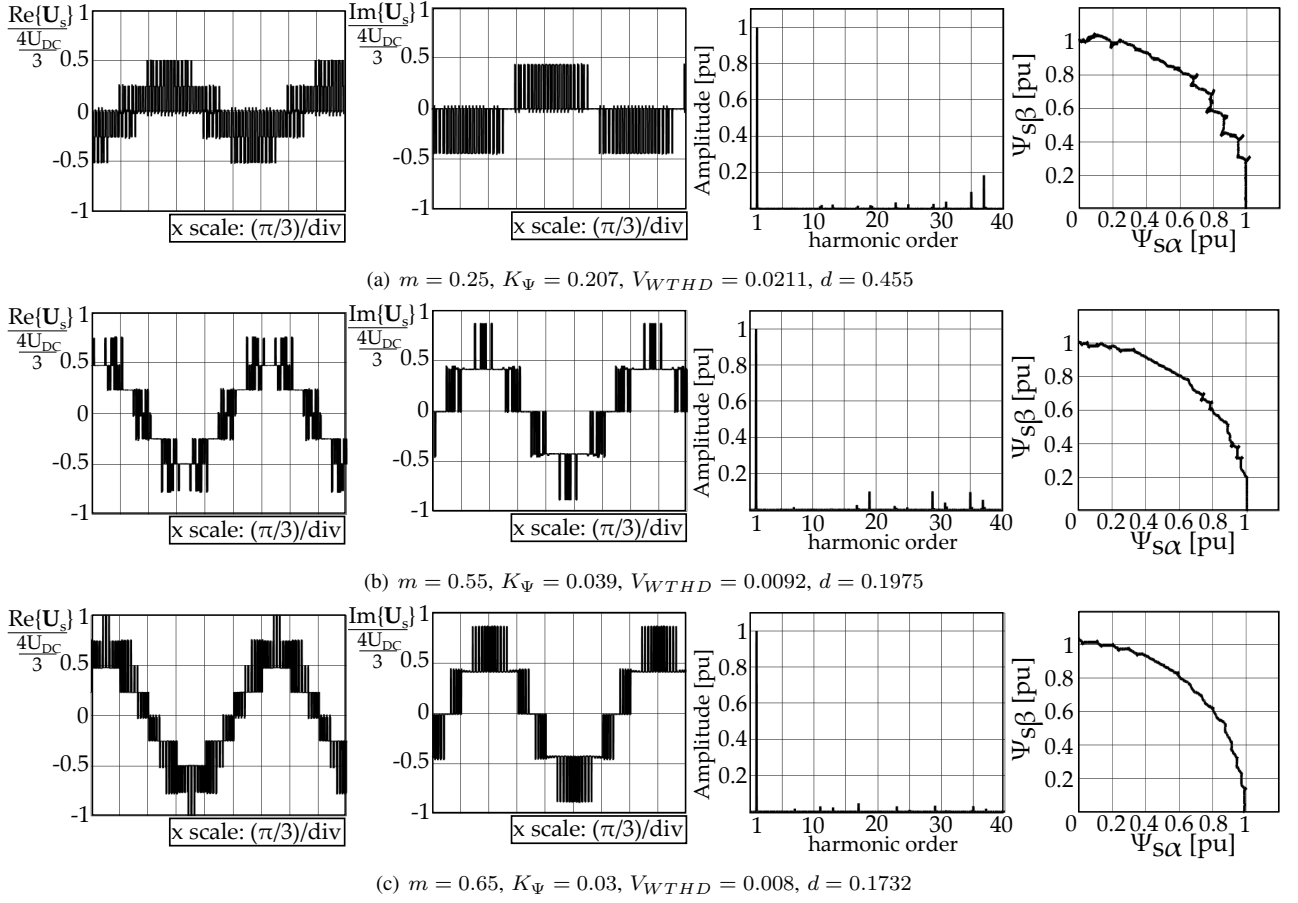


Fig. 6. Experimental results, time function of the real and imaginary component of the output voltage space vector, harmonic spectra of the phase voltage and trajectory of the stator flux vector at $\gamma = 11$

where $m = U_1/U_{1,max}$ is the modulation index, $\kappa = (\gamma + 1)$ and where

$$\beta_i = \begin{cases} \pi/3, & \text{if } i^{th} \text{ voltage vector is } U_{II}. \\ \pi/6, & \text{if } i^{th} \text{ voltage vector is } U_{VIII}. \\ 0, & \text{otherwise.} \end{cases}$$

$$SV_i = \begin{cases} 1, & \text{if } i^{th} \text{ voltage vector is } U_{VII}. \\ \sqrt{3}/2, & \text{if } i^{th} \text{ voltage vector is } U_{VIII}. \\ 0.5, & \text{if } i^{th} \text{ voltage vector is } U_I \text{ or } U_{II}. \\ 0, & \text{for zero voltage vectors.} \end{cases}$$

The square of the stator flux can be calculated as

$$\Psi_s^2 = \frac{6}{\pi} \int_0^{\frac{\pi}{6}} (\Psi_{s\alpha}^2 + \Psi_{s\beta}^2) d\omega_1 t \quad (4)$$

where $\Psi_{s\alpha}$ and $\Psi_{s\beta}$ are the real and imaginary components of the stator flux vector, respectively (see Fig.2). Ψ^2 can be derived by using partial integration as

$$\Psi_s^2 = \left(\frac{\pi}{3m} \right)^2 \left[F_0^2 + \sum_{i=1}^{\kappa} \frac{2}{\pi} \left(\theta_{i+1}^3 - \theta_i^3 \right) |SV_i|^2 - A \frac{6}{\pi} \theta_{i+1}^2 C_i + B_0 \frac{6}{\pi} \theta_i^2 C_i \right] \quad (5)$$

$$A = -U_{\beta,i}(B_1 - \Psi_{s\alpha,i}) + U_{\alpha,i}\Psi_{s\beta,i}$$

$$B_0 = -U_{\beta,i}(B_1 - B_2) + U_{\alpha,i}B_3$$

$$C_i = \begin{cases} 1 & \text{if } i^{th} \text{ voltage vector is active.} \\ 0, & \text{for zero voltage vectors.} \end{cases}$$

$$U_{\alpha,i} = \frac{Re\{\mathbf{U}\}}{4U_{DC}/3} = \begin{cases} 1, & \text{if } i^{th} \text{ voltage vector is } U_{VII} \\ 0.75, & \text{if } i^{th} \text{ voltage vector is } U_{VIII} \\ 0.5, & \text{if } i^{th} \text{ voltage vector is } U_I \\ 0.25, & \text{if } i^{th} \text{ voltage vector is } U_{II} \\ 0, & \text{for zero voltage vectors.} \end{cases}$$

$$U_{\beta,i} = \frac{Im\{\mathbf{U}\}}{4U_{DC}/3} = \begin{cases} \sqrt{3}/4, & \text{if } i^{th} \text{ voltage vector is } U_{II} \text{ or } U_{VIII} \\ 0, & \text{otherwise.} \end{cases}$$

$$\Psi_{s\alpha,i} = \sum_{j=1}^i U_{\alpha,j}(\theta_{j+1} - \theta_j)$$

$$\Psi_{s\beta,i} = \sum_{j=1}^i U_{\beta,j}(\theta_{j+1} - \theta_j)$$

$$F_0 = 2\Psi_{s\alpha,\kappa}$$

$$B_1 = \Psi_{s\alpha,\kappa} + \Psi_{s\beta,\kappa}\sqrt{3};$$

$$B_2 = \begin{cases} 0, & \text{if } i = 1 \\ \Psi_{s\alpha, i-1}, & \text{if } 1 < i \leq \kappa \end{cases}$$

$$B_3 = \begin{cases} 0, & \text{if } i = 1 \\ \Psi_{s\beta, i-1}, & \text{if } 1 < i \leq \kappa \end{cases}$$

$\Psi_{s\alpha, i}$ and $\Psi_{s\beta, i}$ is the value of the real and imaginary components of the stator flux vector at the end of applying i^{th} voltage vector (see Fig.2). $U_{\alpha, i}$ and $U_{\beta, i}$ are the real and imaginary components of the i^{th} voltage vector. It should be noted, the equations can be adopted to multilevel inverters with higher number of voltage levels by defining the possible value of $U_{\alpha, i}$, $U_{\beta, i}$ and $|SV|_i$ output voltage vector components.

Constraints: To minimize an objective function applying numeric methods inequality or equality constraints should defined. In the paper the following constraints are used for the switching angles

$$\begin{aligned} \theta_1 &= 0 \\ \theta_{i+1} &> \theta_i + \theta_{min} \quad i = 1, 2, \dots, \kappa \\ \theta_\kappa &= \pi/6 \end{aligned}$$

where θ_{min} is a constant value to define a minimum duration of the i^{th} voltage vector, thus ensure a minimum on time and off time of the power semiconductor switches.

REFERENCES

- [1] A. Tenconi, S. Vaschetto, and A. Vigliani, "Electrical machines for high-speed applications: Design considerations and tradeoffs," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp. 3022–3029, June 2014.
- [2] F. Mink, K. Peter, H. Kasten, and S. Beineke, "Feedback control of high-speed pmsm with synchronous optimal pwm," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–10.
- [3] K. Peter, S. Hanke, F. Mink, and J. Bcker, "Inverter loss management for an electrical high-speed drive system," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–10.
- [4] A. Tumurbaatar, S. Mochidate, K. Yamaguchi, T. Matsuda, and Y. Sato, "Harmonic loss reduction in high speed motor drive systems by flying capacitor multilevel inverter," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, May 2018, pp. 1972–1976.
- [5] H. Jrvialo, J. Korhonen, J. Honkanen, and P. Silventoinen, "Considerations for a high-speed pmsm drive featuring a gan-anpc inverter," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Sep. 2017, pp. P.1–P.6.
- [6] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multi-level voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930–2945, Dec 2007.
- [7] A. Edpuganti and A. K. Rathore, "A survey of low-switching frequency modulation techniques for medium-voltage multilevel converters," in *2014 IEEE Industry Application Society Annual Meeting*, Oct 2014, pp. 1–8.
- [8] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1873–1886, March 2016.
- [9] Z. Ye, Y. Xu, X. Wu, G. Tan, X. Deng, and Z. Wang, "A simplified pwm strategy for a neutral-point-clamped (npc) three-level converter with unbalanced dc links," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3227–3238, April 2016.
- [10] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003, vol. 18.
- [11] J. Lago and M. L. Heldwein, "Generalized synchronous optimal pulse width modulation for multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6297–6307, Aug 2017.
- [12] S. Halasz, "Optimal control of voltage source inverters supplying asynchronous motors," in *Proceedings of International Conference on Electrical Machines ICEM, Brussels*, 1978, pp. 3–5.
- [13] F. C. Zach, R. Martinez, S. Keplinger, and A. Seiser, "Dynamically optimal switching patterns for pwm inverter drives (for minimization of the torque and speed ripples)," *IEEE Transactions on Industry Applications*, vol. IA-21, no. 4, pp. 975–986, July 1985.
- [14] S. Halasz, A. A. M. Hassan, and B. T. Huu, "Optimal control of three-level pwm inverters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 1, pp. 96–106, Feb 1997.
- [15] A. Tripathi and G. Narayanan, "Investigations on optimal pulse width modulation to minimize total harmonic distortion in the line current," *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 212–221, Jan 2017.
- [16] A. Tripathi and G. Narayanan, "Torque ripple minimization in neutral-point-clamped three-level inverter fed induction motor drives operated at low-switching-frequency," *IEEE Transactions on Industry Applications*, vol. 54, no. 3, pp. 2370–2380, May 2018.
- [17] A. Edpuganti and A. K. Rathore, "Optimal pulsewidth modulation of medium-voltage modular multilevel converter," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3435–3442, July 2016.
- [18] A. K. Rathore, J. Holtz, and T. Boller, "Generalized optimal pulsewidth modulation of multilevel inverters for low-switching-frequency control of medium-voltage high-power industrial ac drives," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4215–4224, Oct 2013.
- [19] N. Oikonomou, C. Gutscher, P. Karamanakos, F. D. Kieferndorf, and T. Geyer, "Model predictive pulse pattern control for the five-level active neutral-point-clamped inverter," *IEEE Transactions on Industry Applications*, vol. 49, no. 6, pp. 2583–2592, Nov 2013.
- [20] D. O. Neacu, J. C. Kim, and B. Lehman, "A three-phase multi-optimal pwm implemented on 2-gbit flash memory integrated circuits," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5813–5826, July 2017.
- [21] P. Stumpf and S. Halasz, "Optimal pwm for two-level inverter fed high speed induction machines," in *2018 IEEE 18th International Power Electronics and Motion Control Conference (PEMC)*, Aug 2018, pp. 1012–1018.
- [22] P. Stumpf and S. Halasz, "Optimization of pwm for the overmodulation region of two-level inverters," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3393–3404, July 2018.