Dissertation

submitted to the

Combined Faculties for the Natural Sciences and for Mathematics

of the Ruperto-Carola University of Heidelberg, Germany

for the degree of

Doctor of Natural Sciences

Put forward by

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Born in: Bremen, Germany

Oral examination: 23.7.2019

Charge Carrier Transport in Solution-Processed Organic Semiconductor Thin Films

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Ladungstransport in lösungsmittel-prozessierten dünnen Filmen organischer Halbleiter

Verständnis und Kontrolle über den Fluss elektrischer Ladungsträger sind eine der Grundvoraussetzung der heutigen Gesellschaft, da sie das Fundament für den Betrieb elektronischer Bauteile bilden. Im Rahmen dieser Arbeit wurde der Ladungstransport innerhalb dünner Filme lösungsmittel-prozessierter organischer Halbleiter untersucht. Beginnend mit detaillierten Untersuchungen an Metall-Isolator-Halbleiterkondensatoren wurden zunächst grundlegende Studien zum Ladungstransport in solchen Filmen durchgeführt. Im Anschluss wird eine neuartige Methode zur Messung der Ladungsträgermobilität in Halbleitern präsentiert, die - bei minimalem Einfluss der häufig vorkommenden Injektionsbarrieren - einen robusten Zugang zu diesem wichtigen Transportparameter ermöglicht. Außerdem wurden Untersuchungen bezüglich der lokalen elektrischen Eigenschaften eines Transistors unter Betriebsbedingungen durchgeführt. Im zweiten Teil dieser Dissertation wurden zwei Materialklassen mit potentiellem Anwendungsbezug im Bereich der organischen Elektronik im Detail untersucht. Zunächst konnte gezeigt werden, dass das prototypische halbleitende Polymer Poly(*para*-phenylene) auch in unsubstituierter Form halbleitende Eigenschaften besitzt. Die Kristallinität dieses Materials konnte außerdem durch eine verbesserte Vorläuferroute gesteigert werden. Des Weiteren konnten erfolgreich Zimtsäure-Derivate durch Elektronenstrahlen quervernetzt werden. Dieses neuartige Konzept zur Quervernetzung funktioneller Materialien wurde daraufhin in einem halbleitenden Polymer angewendet, in dem die halbleitenden Eigenschaften auch nach der Strukturierung durch Elektronenstrahlen erhalten blieb.

Charge Carrier Transport in Solution Processed Organic Semiconductor Thin Films

Understanding and controlling the flow of charge carriers lies at the heart of today's society as it is the basis for the successful operation of electronic devices. Here, the charge transport properties of organic semiconductor thin films will be investigated. The first part of this work focusses on the fundamentals of charge transport in such films starting with investigations into metal-insulator semiconductor capacitors. A robust and widely applicable approach to measure the charge carrier mobility in semiconductors will be presented next, enabling a novel way to measure this important transport parameter with minimal influence of the commonly occurring injection barriers. Further investigations into the local electrical properties of a transistor under operation condition are carried out. The second part of this thesis is focused on detailed studies into two material classes bearing potential applications in the field of organic electronics. It is shown that the prototypical organic semiconductor Poly(*para*-phenylene) indeed possesses semiconducting properties in its unsubstituted form. The materials crystallinity was further improved through careful precursor design. Cinnamic acid derivatives are further shown to cross-link under electron radiation. This finding is applied in a semiconducting polymer which preserves its semiconducting properties even after electron beam patterning.

Contents

1 Introduction

Today's society is characterised by the omnipresent use of electronic devices for recreational or professional use. With the advent of the long-awaited (or feared) Internet of Things (IoT) the penetration of electronic devices in all aspects of life is going to increase even further. IoT applications are believed to have the most impact in the healthcare and manufacturing sector where small scale electronic devices can help in identification, sensing and communication tasks. [1] At the heart of all electronic devices lies the controlled transport of charge carriers and it's central element, the transistor. While transistors and its related components are still commonly fabricated from inorganic materials such as silicon or germanium, the field of organic electronics has gained traction in which electronic materials are mainly carbon-based. The main advantages of organic electronic is their comparably low cost since they can be processed from solution (e.g. through printing). They can be further produced on flexible substrates which makes them an ideal candidate for applications in the IoT sector (e.g. as healthcare diagnostic devices or smart labels) where their main disadvantage of a lower efficiency and lifetime does not limit their application perspective. [2, 3] The vast toolbox of organic chemistry further allows the field of organic electronics to develop materials tailor-made for their specific need. Academically, this field is of great interest as their materials are of molecular nature, meaning that their external properties (e.g. colour, conductivity) are closely connected to the properties of their constituting molecules. This molecular nature further leads to an electronic transport governed by intermolecular interactions. [3]

Since understanding and engineering of charge transport behaviour takes such a critical role for the operation of all electronic devices, this thesis is dedicated to fundamental and experimental studies on the charge transport properties of organic semiconductors. More precisely this thesis will focus solely on solution-processed organic semiconductor thin films, closely matching their envisioned application. Charge carrier transport in semiconductors is often classified along its most important figure of merit: the charge carrier mobility μ. A semiconductors mobility reflects its ability to conduct charge carriers where a higher mobility can be translated into a transistor featuring a lower power consumption and a higher switching speed. [3] Thus, high mobilities are generally desired. The mobilities of organic semiconductors are exceeding $10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, a value above the mobility of amorphous silicon but still below crystalline inorganic materials. [2, 4, 5] Measurements of the charge carrier mobility are an integral part of the characterization of novel materials for potential applications in the field of organic electronics. This task is complicated by the fact that these investigations are usually influenced by a large number of factors such as measurement method, device layout, utilized materials and many more. As a result, several different strategies have

been proposed to measure the charge carrier mobility, all with different advantages and disadvantages. [6–11] As such, contrasting techniques for mobility measurements will be presented and developed throughout this work. Another focus of this study are investigations into the (local) energetic landscape of organic semiconductor thin films. Such films are either of multicristalline nature or fully amorphous. [12] Their charge transport is thus characterized by a high amount of positional disorder where carriers are forced hope from one state to the other instead of the desired band-like transport occurring in inorganic semiconductors. [3] As such, investigations into the density of states (DOS) of these films are of big importance to identify and ameliorate possible bottle-necks of charge transport. Although investigations into the shape of DOS and their relationship to charge transport in concrete examples have been carried out in the past, we are still far from a complete picture. [13]

After a short introduction and an excursion into materials and methods, chapter 4 is dedicated to investigations into one of the simplest organic devices, the metal-insulator-semiconductor (MIS) capacitor. A capacitor based technique for mobility measurements will be first validated after which it is applied to calculate the DOS width σ. This important parameter will be accessed through a complimentary approach for comparison reasons, relying on a static device model based on a Poisson ansatz in combination with experimentally recorded capacitance voltage curves. After this method assessment study, chapter 5 presents a novel method to measure the lateral charge carrier transport behaviour in modest mobility semiconductors through Kelvin-probe measurements of externally induced surface potential oscillations. Injection barriers are a common occurrence in the field of organic electronics which can severely influence the charge transport properties of real devices. [14, 15] They are further notoriously hard to quantify which bears the potential of over- or underestimation of the extracted mobilities. The presented approach is especially insensitive to injection barriers and can be applied to all classes of semiconductors making it a worthwhile addition in the toolbox of mobility measurement methods. Chapter 6 will terminate the first part of this thesis by taking a look at the local electrical properties of organic semiconductors. The occurence of a significant injection barrier in transistors is usually inferred indirectly from its electrical characterisation. Here such an injection barrier will be directly visualized using scanning Kelvin-probe microscopy depicting a transistors channel potential under operation conditions.

After these more principal studies, two novel classes of materials will be investigated in more detail in the context of organic functional materials. The aim of these studies is explicitly not placed on achieving outstanding transistor mobility but rather on learning fundamental characteristics of these materials. First, chapter 7 will examine the long sought after prototypical conjugated polymer Poly(*para*-phenylene) in its unsubstituted form to which access was gained just recently. [16] The semiconducting properties of this material, as well as a number of related compounds, will be investigated, all accessed through a conversion from an insulating precursor. This conversion process will be studied in detail through a broad collaboration consisting of several research groups widening the available expertise. These studies give valuable lessons about the interplay between chemical structure and the resulting charge transport properties.

The advanced technique of electron beam lithography (EBL) allows the fabrication of nanostructures with unprecedented resolution. [17, 18] There are very few examples of functional materials processable through EBL which could enable – in principle – novel research approaches and device layouts. [19–22] Chapter 8 investigates the cross-linking behaviour of cinnamic acid derivatives upon electron irradiation in a second collaboration which could open a novel route towards EBL processable functional materials of different kinds. The first proof of concept study showing successful cross-linking of such molecules through electron beams will be presented. Then, a semiconducting material derivatized with cinnamic acids will be investigated in transistors proving the applicability of the proposed approach.

The work presented here is set in a way that readers suffering from colour-deficiencies of any kind can clearly understand the graphs shown. This especially prohibits the use of red/green colour contrasts since red-green colour deficiency exhibits the highest prevalence. [23]

2 Fundamental Concepts

Here a brief overview over the most important concepts used over the course of this work will be given. After an introduction into the basics of organic semiconductors with particular reference into charge transport in those materials the contact formation and doping of this material-class will be discussed. This chapter finishes with a short introduction into the two organic electronic devices investigated in this thesis: metal insulator semiconductor (MIS) capacitors and the organic-field effect transistor (OFET).

2.1 Organic Semiconductors

Organic semiconductors are – in opposition to their inorganic counterpartrs – materials consisting of molecules or polymers in which carbon is the main structural element. Charge transport in these materials is based on conjugated π systems and was first discovered by Chiang et al in doped polyacetylene. [24] Due to the vast possibility of organic chemistry and the strong correlation between chemical structure and physical properties these materials can be tailor made according to a specific need. [7] As such, organic semiconductors have been established in the past as an alternative materials for the fabrication of classical semiconducting devices. While organic light emitting diodes (OLEDS) have reached a high market penetration, organic photovoltaics (OPVs) and organic field effect transistors (OFETs) lack behind. Other organic devices[1] such as sensors and memristors are further topics of ongoing research. [25]

The class of organic semiconductors is divided into the two subgroups of small molecules and polymers, each with their own advantages and disadvantages. Small molecules are generally easier to purify and allow high-vacuum based processing, enabling the fabrication of defined multilayer devices of high performance. High vacuum fabrication of electronic devices on the other hand is slow and costly and offers limited scalability towards bigger substrates. Polymeric semiconductors are solution processable wich makes them compatible with numerous printing techniques for fast and cost effective fabrication on large substrates. This advantage comes for the price of a more difficult purification and a more complex fabrication of multilayer devices as underlying layers can be dissolved by the processing of the top layer.

[1] Here an organic device is in its broadest sense an electric device in which at least one component of the active layers is an organic semiconductor

2.1.1 Electronic Structure and Charge Transport

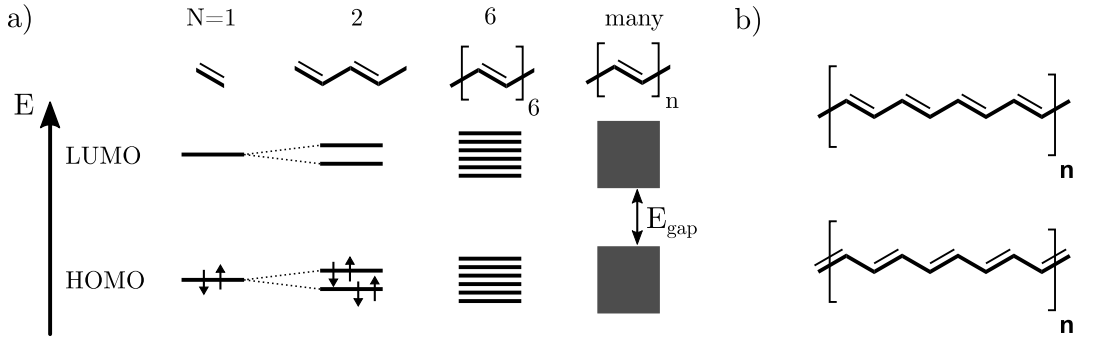

Figure 2.1: Evolution of the HOMO/LUMO molecular orbitals of different length π-systems (a) and equivalent Lewis-structures of polyacetylene (b). a) Each additional double bond introduces an additional energy level splitting until a homogeneous band is formed for many repeating units (a polymer). After [26].

The basic principle underlying charge transport in organic semiconductors is the concept of charge carrier de-localization through conjugated π-orbitals. [26] A very simple example of a π-orbital can be found in ethylene (see figure 2.1a). In this molecule the two sp2-hybridized carbon atoms join their highest energy p_z-orbitals to form a common bonding π-orbital binding orbital in which two electrons are located and an empty antibonding $\pi*$-orbital. These orbitals are thus also named highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), respectively. Once two π-systems are located on one molecular they interact leading to an energy level splitting reducing the HOMO-LUMO distance also called the energy gap E_{gap}. This trend continues the larger the π-system until it eventually saturates (e.g.for polymeric materials). Another important feature of extended π-system is that their common π-electrons are delocalized over the whole system. Figure 2.1b depicts the two equivalent Lewis structures of polyacetylene (PA). In reality the system has to be imaged in an intermediate resonance between these two structures where the π-electrons are delocalized over the whole system further stabilizing this molecule.

Organic semiconductors are molecular solids where the constituting molecules are only weekly bound by Van-der-Waals forces. Thus, the electronic interaction between its individual units is generally low so that the electronic structure of the individual constituents dictates the solids electronic structure. As such, the HOMO and LUMO of their constituents is often used to discuss the behaviour of the solid itself.[2] While charge carriers in inorganic semiconductors can often be seen as delocalized, charge carriers in organic semiconductors on the other hand are generally rather localized on distinct sites (e.g. single molecules in the case of small molecules or small coherent chain segments in the case of polymers). [2, 4, 27, 28] Apart from a few notable examples in highly

[2] Due to the experimental inexcessibility of the HOMO and the LUMO levels, the corresponding properties of the solid, the innonization potential (IP) and electron affinity (EA) are usually discussed.

crystallinity materials, charge carrier hopping is generally regarded as the general conduction mechanism in organic semiconductors. [29, 30] Before discussing the theory of charge transport in organic semiconductors a short detour into the most important figure of merit for charge transport will be taken.

The Charge Carrier Mobility

The charge carrier mobility is an important property of semiconductors and metals alike as it gives insight into the charge carrier transport of these material. The mobility μ relates the drift velocity of free carriers (here electrons are assumed) to the driving force of an applied electic field F

$$v = \mu \cdot F. \tag{2.1}$$

The current density as result of this carrier movement can be calculated as

$$j = qnv = \underbrace{qn\mu}_{\sigma} F \tag{2.2}$$

with n the charge carrier density and q the elemental charge and σ the conductivity. The charge carrier mobility is often measured as a figure of merit describing a semiconductors ability to conduct charges which is of vital importance for efficient device operation. In both OLEDs and OPVs for example device efficiency can be hindered by imbalanced mobilities of electrons and holes in their respective n and p-type layers. [8, 31] In transistors the mobility determines parameters such as the maximum current through the device (at a given voltage) and the maximum achievable switching speed. [3, 4, 12] There are in principle two methods to determine this important parameter. Either the charge carrier velocity can be measured for a known at a given applied field (e.g. in a transit time experiment) or the current at known field and charge carrier density is recorded (e.g. in a transistor). See Section 2.1.2 for more details of mobility measurements.

Theory of Charge Transport

Apart from a few notable examples, the high disorder prevailing in organic semiconductors causes charge carrier transport to be mediated through hopping of electrons from one localized state to the other.[3] [3] As such, the energetic distribution and spatial location of these hopping sites is of great influence on charge transport. Due to the

[3] Hopping transport is thermally activated resulting in a higher mobility for higher temperature. The inverse case is very rarely found and the transport is assumed to be band-like e.g. Sakanoue et al. [29]

vast amount of material systems in the field of organic electronics different descriptions of the spatial and energetic positions of these hopping sites and the hopping mechanism involved were published. The resulting predictions of the temperature and charge carrier density dependence of the mobility μ often contradict each other and/or only predict experimental findings in a their respective domain. [30]. Thus, a very simple and informative model for charge transport shall be discussed here, which has lost some of its experimental relevance through more advanced approaches. Marcus proposed in 1956 a model desribing the charge transfer between two chromophores. [32, 33] Following Schmidt-Mende and Weickert [34] in their description the Marcus transfer rate of electrons k_M reads:

$$k_M = \frac{2\pi}{\hbar} |J_{AB}|^2 \frac{1}{\sqrt{4\pi\lambda k_\mathrm{B} T}} \exp\left(-\frac{(\lambda + \Delta G_0)^2}{4\lambda k_\mathrm{B} T}\right) \tag{2.3}$$

with J_{AB} electronic coupling between initial chromophore A and final chromophore B, λ the reorganization energy and ΔG_0 the difference in total Gibbs free energy between initial and final chromphore (reading zero for identical species), $k_\mathrm{B}T$ the product of Boltzmann-constant and temperature and $\hbar$ the reduced Planck constant. The electronic coupling (also named transfer integral) is influenced by the orbtial overlap between initial and final states and is to be maximized for efficient transport. The reorganization energy on the other hand stands for the necessary reorganization upon charge transfer of the system (e.g. nuclear coordinates or other charges) and should be minimal. These two quantities can be used for example in the context of high throughput computational chemistry to find materials suitable as organic semiconductors. [35]

In disordered semiconducting materials both J_{AB} and λ are not constants but depend on the local surroundings. Thus a much simpler approach for the transfer rate between neighbouring sites i, j is commonly used in the form of a Miller-Abrahms ansatz:

$$k_{i,j} = k_0 \exp\left(-2\gamma r_{i,j}\right) \begin{cases} \exp\left(\frac{\epsilon_i - \epsilon_j}{k_\mathrm{B} T}\right) & \epsilon_i > \epsilon_j \\ 1 & \epsilon_i \leq \epsilon_j \end{cases} \tag{2.4}$$

with k_0 the attempt to escape frequency, γ the inverse localization radius (influenced by the electronic wave function overlap), ϵ_i, ϵ_j the site energies and $r_{i,j}$ their distance. The Miller-Abrahms model describes the situation of a low electron-phonon coupling regime where polaronic effects can be disregarded. A charge transfer to a lower energy site shows probability of 1 while a higher energy is calculated with Boltzmann-term. Often the site energies are assumed to be independent from each other. The distribution of site energies $g(\epsilon)$ – also named density of states (DOS) – can then be further assumed to take a gaussian shap (thus named gaussian disorder model or GDM) with width σ:

$$g(\epsilon) \propto \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{\epsilon^2}{2\sigma^2}\right) \tag{2.5}$$

Other DOS models assume correlated gaussian distributed states (CDOS) or a purly exponential distribution. By setting a combination of charge transfer model and DOS function the charge carrier mobility of a system can be calculated. One of the earliest and still widely used description of the hopping mobility in disordered organic semiconductors comes from Bässler. [36] He chose a Miller-Abraham ansatz in combination with a gaussian DOS. As this combination posseses no analytical solution monte carlo simulations were used to calculate the field and temperature dependence of the system [37]:

$$\mu(\hat{\sigma}, F) = \mu_0 \exp\left[-\left(\frac{2}{3}\hat{\sigma}^2\right)\right] \begin{cases} \exp\left\{C\left(\hat{\sigma}^2 - \Sigma^2\right)\sqrt{F}\right\} & \Sigma \geq 1.5 \\ \exp\left\{C\left(\hat{\sigma}^2 - 2.25\right)\sqrt{F}\right\} & \Sigma < 1.5 \end{cases} \tag{2.6}$$

with μ_0 a field and temperature independent prefactor, $\hat{\sigma} = \frac{\sigma}{k_B T}$ the disorder parameter, C a numerical constant influenced by the lattice used in the monte carlo simulation, Σ a positional disorder parameter and F the electric field. It is apparent that the Bässler model shows a Pool-Frenkel like behaviour ($\ln \mu \propto \sqrt{F}$) of the mobility often observed in the disordered organic semiconductors. [34, 37]. The temperature dependence of the mobility is given by $ln(\mu) \propto T^{-2}$. Due to the nature of organic semiconductors the temperature window where experimental measurements of the charge carrier mobility can be achieved is small so that often both an Arrhenious type $ln(\mu) \propto T^{-1}$ and the here described dependence $ln(\mu) \propto T^{-2}$ are accurate descriptions of the observed data. [37]

Charge transport in thin films

Based on the Bässler model discussed in the previous section it is already apparent that a small disorder parameter leads generally to a better charge transport. A simple way to decrease the disorder inside a semiconducting thin film is to achieve a high order of the constituting molecules, a crystal. To achieve this goal a common approach focuses on the chemical structure of the constituting molecule. Side-chain engineering for example can have a big impact on the crystallinity and ultimately the charge transport properties of the material under investigation. [38] The small molecule pentacene for example crystallizes in a herringbone structure not optimal for charge transport due to a low transfer-integral between neighbouring molecules. The introduction of solubility offering Triisopropylsilyl side-chains towards 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-

PEN) [4]also changed the packing motife towards a more favorable brick-wall packing motif.[3]

Due to the fact that charge transport in organic thin films is so strongly governed by the thin film morphology the fabrication of these films has a great influence on the resulting charge carrier transport properties. [12, 39, 40] Investigations in the local electrical properties of transistors exhibiting only a single grain boundary for example showed that this single grain boundary was governing charge transport in the whole device. [41, 42] The strong correlation between morphology and transport properties of thin films renders statements about the general charge carrier properties of a material complicated. Consequently, significant effort is put into the optimization and development of fabrication techniques for organic thin films to achieve optimal charge transport. [25, 43–47]

2.1.2 Mobility Measurements in Organic Semiconductors

Since the charge carrier mobility of organic semiconductors plays such an important role for device operation, a vast amount of techniques exist to measure this quantity. To achieve this goal organic devices such as diodes or transistors are often fabricated for pure measurement purposes without any applicational relevance.

Hall mobility measurements are used exctensively in the context of inorganic high mobility semiconductors and has seen some emergencee in the field of organic electronics aswell. [48]. The lateral charge carrier mobility of lower mobility organic semiconductors is typically charaterized by thin-film transistors. [6, 7, 9, 49] Via the shockley equation (see 2.2.2) the charge carrier mobility can be directly calculated from a measured current voltage characteristic. [50] Furthermore, the lateral mobility in OFETs can be measured with dark injection techniques where a charge carrier package is injected in one contact and the time is measured until the package has reached the extracting contact. [51, 52]

In comparison to transistor measurements time of flight (TOF) measurements are usually carried out on diodes, giving access to the vertical charge carrier mobility. Here a charge carrier package is usually excited via a laser close to a transparent electrode, immediately extracting one charge carrier species. The drift of the complimentary charge carrier species to the other electrode can be measured via an external circuit. The resulting transit time gives then acces to the charge carrier mobility. [8]

Varying the semiconductor thickness in a set of otherwise identical space-charge limited current (SCLC) diodes gives access to the charge carrier mobility. [9] Other methods for the vertical charge carrier mobility are charge extraction by linearly increased voltage (CELIV) [4] or dark current injection transients. [11, 53] MIS capacitors can be also used to measure the vertical charge carrier mobility (see section 2.2.1). [10]

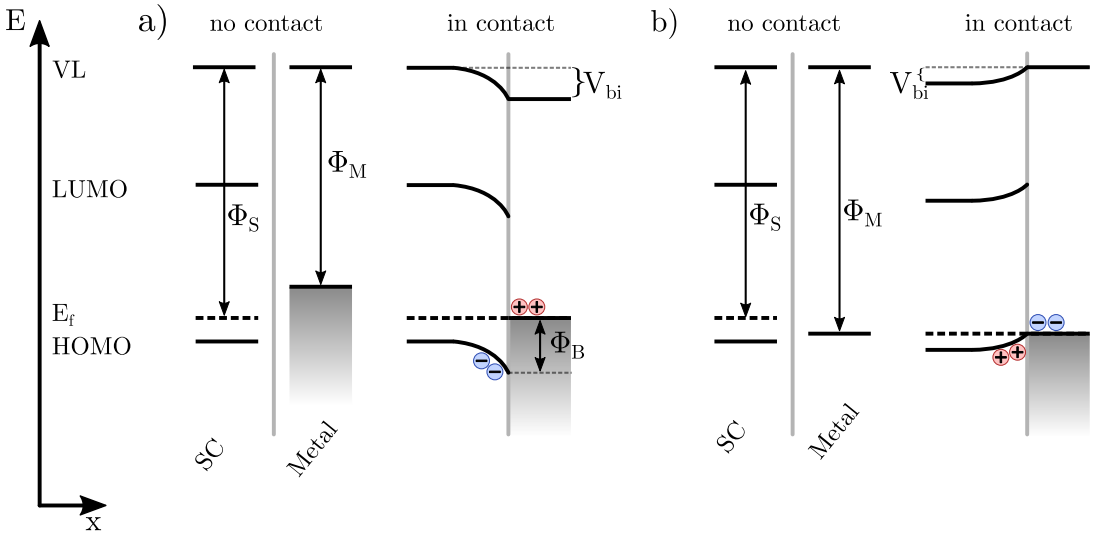

Figure 2.2: Formation of a semiconductor metal junction according to the Mott-Schottky-picture. a) Formation of a metal semiconductor junction where the metals work function Φ_M is lower than the p-types semiconductors work function Φ_S, leading to the formation of a depletion layer to establish a barrier Φ_B. b) Depicts the inverse case of $\Phi_M > \Phi_S$ where an ohmic contact is formed. VL: vacuum level; SC: semiconductor; V_{bi}: built in potential

2.1.3 Contact Formation

Due to their multilayer nature, the performance of nearly all devices in the field of organic electronics are highly influenced by processes at interfaces. The most common interface in electronic devices is that between a semiconductor and a metal electrode. Here the widely studied interface between an inorganic material and a metal shall be discussed first. Figure 2.2 thus exemplary shows the contact formation of a p-type semiconductor with a metal of high/low work function according to the MOTT-SCHOTTKY-rule. Contacting two materials of different work functions generally leads to a flow of charge carriers between the two materials until a flat chemical potential has been achieved. [5] In figure 2.2a the semiconductor possesses a higher work function Φ_S than the metal Φ_M. Thus, holes travel from the semiconductor into the metal forming a depletion layer in the contact near region of the semiconductor. The amount of resulting band bending is directly related to the charge carrier density of the material so that no bending can be assumed for the common metals while the bending of the semiconductor can be directly controlled through processes influence the charge carrier density (e.g. doping see section 2.1.4). Holes travelling from the metal into the semiconductor thus have to overcome a SCHOTTKY-Barrier Φ_B, impeding the charge transport. In the inverse case (figure 2.2b) when the metals work function is higher then the semicon-

[4] See section 3.1.2 for more information about this material

[5] Here the chemical potential will be used instead of the FERMI-level as it is common practice in the community

ductors work function, an ohmic contact is formed where the contact acts as a charge carrier reservoir. Regardless of this reservoir charge carriers travelling over the interface have to overcome an injection barrier. If this barrier is impeding charge transport upon application of a voltage depends whether the re-population (from the metal) or de-population (through a readout of the charge carriers) of the interfaces reservoir is the dominating process. V_{bi} marcks a build-in potential formed through the chemical potential alignment. For an n-type semiconductor the inverse situation prevails where an ohmic contact is formed for $\Phi_M < \Phi_S$ and an blocking contact for $\Phi_M > \Phi_S$.

The injection barriers predicted by the MOTT-SCHOTTKY-rule often greatly differ from experimental values already in the field of inorganic electronics. The main reason for this deviation is the fact that surface states are not taken into account. These states can either come from the broken periodicity of the semiconductor or can be induced by the presence of the metal (metal induced gap states, MIGS). [27, 48]

In the field of organic electronics the situation is even more complex as interface chemistry (e.g. dipoles) and deposition effects (e.g. MIGS) can strongly influence the contact behaviour in addition to the fact that the position of the chemical potential is generally unknown. [54] Advanced concepts such as the charge neutrality level (CNL) and induced densities of interface states (IDIS) again borrowed from the field of inorganic semiconductors were applied to their organic counterparts as well. [55–57] Nevertheless, accurate a-priori predictions of the contact interface energetics between different organic materials are very challenging as elucidated by the amount of research dedicated to this field. [58, 59] Thus, the energy level alignement on paper is usually done at their vacuum levels and the injection barrier is estimated from the difference of the metals work function to the electron affinity or the ionization potential of the semiconductor.[6] There exist several different strategies to tune and improve the contact between metals and organic semiconductors among which are different contact materials, buffer layers (e.g. poly(3,4-ethylenedioxythiophene) polystyrene sulfonate PEDOT:PSS) the use of dipolar self-assembled monolayers or interfacial doping (see section 2.1.4). [15, 60]

2.1.4 Doping

Doping is a widely used technique to alter the electronic properties of organic and inorganic semiconductors alike. In the field of organic electronics dopants can be either other organic molecules or inorganic materials such as elemental alkali metals or molybdenum oxide (MoO_3). [60, 61] Doping in organic devices is commonly done in two different approaches: Interfacial doping through the introduction of a small interlayer between two materials can alter their contact formation or passivate trap states. Volume doping on the other hand intermixes dopant and semiconducting material to change the electrical properties of the bulk, changing the semiconductors charge transport properties (e.g. chemical potential, charge carrier density).

From a theory perspective molecular and non-molecular doping achieve the doping of the semiconductor via the same process described in figure 2.3. A transfer of an electron

[6] As a rule of thumb a difference of less than 0.2 eV is expected to result in an ohmic contact.

from a higher lying orbital of the dopant into the semiconductor is responsible for n-doping, while p-doping is achieved via an electron transfer from the semiconductor into a free state in the dopant molecule. This results in either free electrons or holes in the semiconductor, respectively while the dopant is ionized with the complementary charge. An alternative theory used exclusively for molecular dopign assumes the formation of a joint charge transfer complex of semiconductor and dopant. [60]

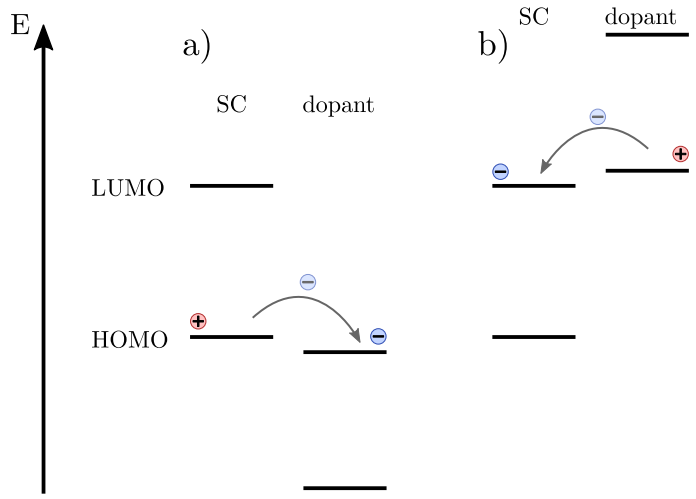

Figure 2.3: Sketch of p-type (a) and n-type (b) doping. P-type doping is achieved through electron transfer from the SC (semiconductor) into the dopant while n-type dopant is caused by an electron transfer from the dopant into the semiconductor.

It is noteworthy that molecular doping as well as doping with the common dopant MoO_3 are known for their low doping efficiencies, requiring a high amount of dopants to achive significant charge transfer between the dopant and the semiconductor. [61–63] This low doping efficiency can be caused by a number of reasons. Phase separation between dopant and semiconductor in volume doping can for example not only reduced the amount of ionized dopant but further act as scattering centers for charge transport.

2.2 Organic Electronic Devices

2.2.1 Organic Metal Insulator Semiconductor Capacitors

Organic metal insulator semiconductor (MIS) capacitors are a simple devices allowing investigations into the charge transport in semiconducting layer. The devices consist of a double layer of semiconductor and insulator sandwiched between two electrodes (see figure 2.4a for details). Due to the insulating layer, a significant flow of DC current through the device is not possible, offering certain advantages and disadvantages. Let us first look at the exemplary case of a p-type semiconductor with an ohmic contact towards the source electrode which is grounded. In such a capacitors the application of

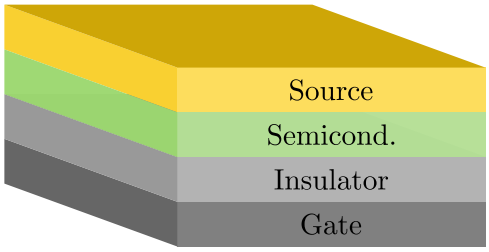

Figure 2.4: Layer sketch of a MIS capacitor. The sketch shows a bottom gate capacitor while the inverse stack is called a top-gate capacitor.

a negative voltage at the gate electrode leads to an accumulation of holes at the semiconductor insulator interface through the field-effect. In the inverse case of a positive voltage electrons cannot be injected very efficiently into the semiconductor (high injection barrier). It was shown that some amount of electrons can be injected nevertheless into the semiconductor which can accumulate at the semiconductor/insulator interface (see chapter 6).[7] Thus, a complete depletion of the semiconductor is impossible to reach for pure DC operation. Due to the assumed discrepancy of injection barriers for electrons and holes it can be assumed that no electrons can be injection under AC operation. Here MIS capacitors will be investigated via impedance spectroscopy where both a DC and an AC bias are applied. The DC bias sets the operation point of the device (hole accumulation or depletion) which is probed with a small perturbing AC bias (of variable frequency). Depending on the location of the hole centre of charge (COC), the system either shows a low ($C_{Depl.}$ for $V > 0$) or a high ($C_{Acc.}$ for $V < 0$) capacitance due to the changing distance towards the countering gate electrode (see figure 2.5a). These capacitances can be estimated using the well known formulas for plate capacitors. The electron operation condition cannot be probed as no electrons can be injected by the AC perturbation. In combination with numerical simulations these experimental measurements of the capacitance C vs. the applied voltage V can be used to extract the DOS width σ of the semiconducting material (see chapter 4 and [64]).

Furthermore, measurements of the frequency dependent capacitance C(f) can be used to measure charge carrier mobility normal to the device surface. First a strong constant potential is applied driving the device in strong accumulation. Then the device is probed with a small perturbing electric field of frequency f. Due to the limited carrier mobility of charge carriers a finite transit time τ is needed until charges injected at the contact can migrate through the thickness of the semiconductor d_s towards the semconductor/insulator interface. According to Stallinga et al [10] this transit time reads:

[7] In the case of an n-type material it is vice versa, while an ambipolar material shows a fast charge carrier accumulation at the semiconductor/insulator interface for both electrons and holes at $V > 0$ and $V < 0$, respectively.

$$\tau = \frac{d_s^2}{D_h} = \frac{q}{k_B T}\frac{d_s^2}{\mu_h} \tag{2.7}$$

with D_h the diffusion coefficient and q the elementary charge. This defines a cut-off frequency of

$$f_c = \frac{1}{2\pi\tau} = \frac{\mu_h k_B T}{2\pi q d_s^2} \tag{2.8}$$

Probing the device with a perturbation of a higher frequency then (or in the order of) f_c gives the holes not enough time to fully accumulate at the semiconductor/insulator interface resulting in a reduced capacitance (see figure 2.5b). Experimentally measuring the cut-off frequency thus gives access to the horizontal charge carrier mobility. Here the f_c is defined is a the maximum in $\frac{\partial C}{\partial f}$ while other definitions are also possible. [10] Here MIS capacitors will be mainly used in chapter 4 for lateral charge carrier transport investigations complimenting the investigations into the horizontal transport carried out in the majority of the other chapters.

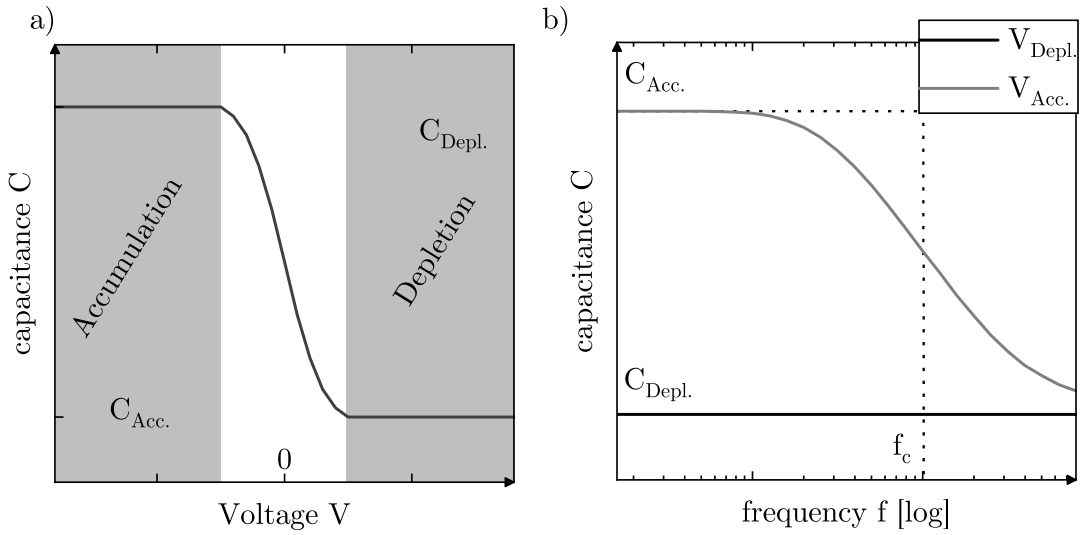

Figure 2.5: Sketch of an exemplary capacitance voltage (a) and capacitance frequency (b)characteristic of a MIS-capacitor. a) Capacitance voltage C(V) characteristic of the MIS capacitor from figure 2.4 exhibiting for negative voltages ($V_{ACC.}$) a high capacitance ($C_{ACC.}$) and for positive voltages ($V_{Dep.}$) a low capacitance ($C_{Dep.}$). The capacitance frequency C(f) plot of the same device (b) indicates at $V_{ACC.}$ for low measurement frequencies $C_{ACC.}$ and a decrease of capacitance with increasing frequency. At $V_{Dep.}$ the capacitance is frequency independent. f_c marks the critical frequency (see text for calculation).

2.2.2 Organic Field Effect Transistors

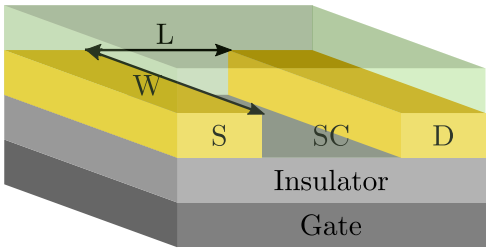

Figure 2.6: Layer sketch of an organic field-effect transistor (OFET). S/D stands for the source/drain contacts, W and L for the channels width and length, respectively and SC for the semiconducting layer. The here shown OFET is a bottom contact bottom gate device, one of several possible field-effect transistor layouts.

The simplest analogon for an organic field-effect transistors (OFET) is an electrical switch operated via an external voltage. In parallel to anorganic devices there exist severall different architecture for the construction of field-effect transistors all operating via the same principle. Figure 2.6 shows the layer sketch of a bottom-gate bottom contact device which shall be used to explain an OFETs working principle. The source and drain electrode are the main current carrying electrodes between which a third gate electrode can modulate the current. The active material connecting source and drain is a semiconducting layer insulated against the gate electrode via an insulator (also called dielectric). Following their names the drain electrode is usually grounded while the gate voltage (V_g) is applied at the gate and the drain voltage (V_d) at the drain contact.

Pristine organic semiconductors are nearly completely devoid of movable charge carriers so applying a voltage between source and drain leads to no or only a very small current. The transistor is thus in its off state showing only the off current I_{off}. Depending of the nature of the semiconductor (p- or n-type) and the contact behaviour for electrons and holes, applying a potential at the gate electrode leads to the accumulation of charge carriers at the semiconductor/insulator interface in the same manner as in an MIS capacitor (see section 2.2.1 for more details). The accumulated charge carriers are forming a conductive channel which can carry the current between the source and drain electrodes. The amount of accumulated charges is influenced by the magnitude of the applied gate voltage V_g, the insulators thickness d_i and its dielectric constant $\epsilon_{r,i}$. The areal capacitance of the gate/insulator/semiconductor system reads $C_i = \frac{\epsilon_{r,i}\epsilon_0}{d_i}$

The response of a transistor is commonly described using the Shockley-Model for transistors originally developed for their anorganic counterparts. [2–4]. It describes the drain current I_d as a function of drain V_d and gate voltage V_g for the linear and saturation regimes:

$$I_{d,lin} = \frac{W\mu C_i}{L}\left[(V_g - V_{th})\,V_d - \frac{1}{2}V_d^2\right] \quad \text{for} \quad |V_g - V_{th}| > |V_d| \tag{2.9}$$

$$I_{d,sat} = \frac{W\mu C_i}{2L}(V_g - V_{th})^2 \quad \text{for} \quad |V_g - V_{th}| < |V_d| \tag{2.10}$$

with W/L the transistors width and length, μ the charge carrier mobility and V_{th} the threshold voltage of conduction. $(V_g - V_{th}) | > |V_d|$ is called linear regime as the drain current increases linearly with drain voltage. $|(V_g - V_{th}) | < |V_d|$ is called saturation regime as the drain current is independent of the drain voltage. Reformulation of equation (2.10) allows the calculation of the charge carrier mobility in the saturation regima via:

$$\mu_{sat} = \frac{2L}{C_i W}\left(\frac{\partial\sqrt{I_d}}{\partial V_g}\right)^2 \quad \text{for} \quad |V_g - V_{th}| < |V_d| \tag{2.11}$$

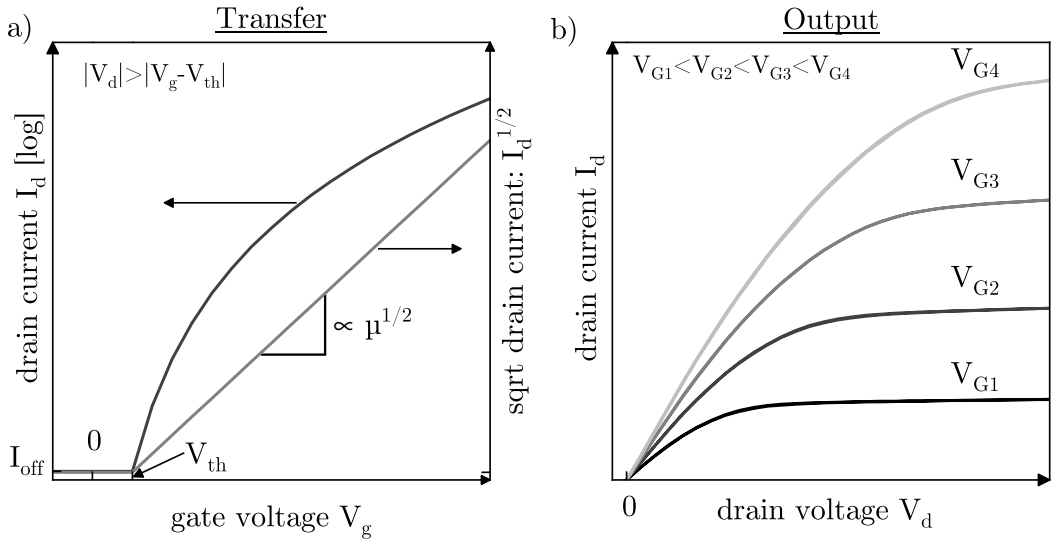

Figure 2.7: Sketch of an exemplary transfer (a) and output characteristic (b) of an organic field-effect transistor. a) At gate voltages V_g below the threshold voltage V_th the drain current I_d reads I_{off} while it exhibits a linear dependence in the $I_d^{1/2}$ plot used to calculate the mobility μ from its slope. b) An ideal output curve exhibits a linear drain voltage V_d form for voltages around zero while it saturates at higher voltages. The branching point between linear an saturation regime shifts for increasing gate voltage towards higher drain voltages.

Figure 2.7 shows a sketch of a typical OFET charateristic according to the SHOCKLEY-Model. The transfer plot $I_d(V_g)$ on the left is typically used to calculate the charge carrier mobility via equation (2.11). A calculation of the mobility in the linear regime is less common as this regime is stronger influenced by contact phenomena. Apart from the mobility calculation the transfer plot is used to calculate the threshold voltage of conduction V_{th} and the off current I_{off}. Furthermore, the turn-on voltage V_{on}, defined as the voltage at which the transistors shows a current higher then the off current can

also be determined from the transfer plot.[8] The output plot shown in figure 2.7 gives additional information about charge transport. An ideal output curve shows a linear dependance in V_d for low voltages (linear regime) and saturates for higher voltages in the saturation regime. Significant injection barriers are often found to lead to an s-shape in the output curve (see chapter 6 for a detailed study of this phenomenon).

[8] In the here shown example V_{on} and V_{th} are identical but in some experimental situation the calculation of on or the other is more practical.

3 Materials and Methods

In the following chapter a brief overview of the most important materials and methods used in this thesis will be given. A particular focus will lie on macroscopic and microscopic Kelvin-probe methods as they are the basis of the investigations carried out in chapters 5 and 6, respectively. This chapter ends with a short introduction into finite element methods which were applied in chapter 5.

3.1 Materials

The investigations presented in the first part of this work (chapters 4 to 6) focus on the fundamental aspects of charge carrier transport. As such these studies were carried out with two well known reference materials which will be presented first. Next, the insulating material Parylene-C is introduced which is used here as a dielectric and encapsulation material.

3.1.1 P3HT

Poly(3-hexylthiophen-2,5-diyl) (P3HT, see figure 3.1a) in one of the most used organic semiconducting polymers. Its ease of processing in combination with its good performance in both OFETs as well as OPVs make this p-type polymer one of the best understood material in the field of organic electronics, making it one of the most often used reference materials in the field. P3HT is known for its strong doping through oxygen exposure. [65] This doping can be reversed for example through the use of vacuum, driving out the oxygen. Spincoated films of P3HT show a nanocrystalline structure where the size and orientation can be tuned through the processing and post-processing parameters (e.g. solvent, thermal annealing etc.) Furthermore, the degree of regioregularity and the molecular weight are know to influence device performance. [66, 67] Here a regioregular P3HT from Sigma-Aldrich with a number average molar mass M_n = 15000-45000 was used as delivered (see figure 3.1a for chemical structure). Although properly processed P3HT is able to achieve very high mobilities (up to $0.1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) its poor stability severely limits its perspective for industry applications.

3.1.2 TIPS-PEN

Another important p-type reference material is the small molecule 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-PEN, see figure 3.1a). TIPS-PEN utilizes a pentacene

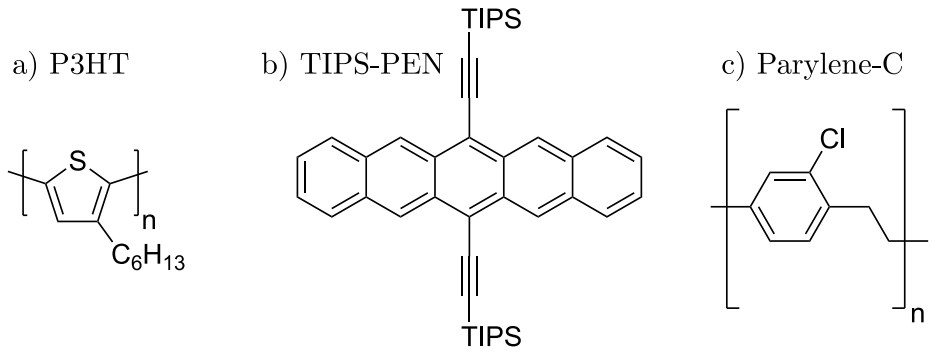

Figure 3.1: Chemical structure of P3HT (a), TIPS-PEN (b) and Parylene-C (c). P3HT and TIPS-PEN are polymeric or small-molecular semiconducting p-type reference materials used in the field of organic electronics. Parylene-C is used here extensively as an insulating material due to its non-trapping nature.

core modified by TIPS side-chains, making the previously insoluble pentacene core available for solvent processing. Furthermore these side-chains improve the packing-motif of pentacene towards a more favourable brick-wall motif. (see section 2.1.1). Depending on the deposition technique very large crystals of TIPS-PEN can be achieved offering high mobilities (in the order of $1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) [29, 47, 68]. Substituting carbon atoms in the central pentacene for nitrogen atoms can invert the polarity of the molecule to n-type where equally high mobilities can be achieved. [69] But it is also this high cristallinity which makes the material challenging for industry applications.

Parylene-C

Parylene-C is a versatile insulating material used for for numerous applications. It can be used as an encapsulation layer due to its transparency and low oxygen and water permeability. It can be further used as a dielectric in various applications. [70, 71] Here Parylene-C is used for both applications. Parylene-C is known to be slightly cristalline upon deposition. [70] This crystallinity can be further increased through thermal treatments. In comparison to the commonly used metal oxides SiO_2 and Al_2O_3 Parylene exhibits a much weaker tendency to trap charges making this material a good choice as where charge trapping (most commonly occuring at the semiconductor/insulator interface) can negatively influence device operation. [70] On the other hand the lowe dielectric constant ($\epsilon_r = 3.15$) and resistance of Parylene-C is much lower requiring thicker films in OFETs for good device performance. Combining SiO_2 and Parylene-C into a double layer dielectric can further improve device performance. [49] Nevertheless, the not negligible permeability of Parylene-C for charge carrier anyway lead to a gate bias stress effect for repeated device operation where charge are trapped at the SiO_2 /Parylene-C interface.

Parylene-C was deposited via chemical vapour deposition in a coater by Specialty Coating Systems (SCS) oparting in a three step process to form the Parylene. First, the parylene dimer is vaporized (T=135 °C) in mild vacuum. Then the Parylene vapours pass through a furnace (T=690 °C) where the parlyne dimers are pyrolised into monomers. Finally, the monomers cool in the deposition chamber to room temperature polymerizing in the process to form the final insoluble film. The thickness of the film is set by the initial amount of dimer used.

3.2 Sample Fabrication

Fabrication of samples (e.g. for spectroscopy) and devices (MIS capacitors, OFETs) always started with the preparation of their respective substrates. Substrates were either prepared manually by cutting a glass or silicon wafer into the appropriate size or taken as is in the case of pre-cut substrates. Then the substrates were cleaner via sonication in acetone and isopropanol for a minimum of 10 min and subsequently dried using a nitrogn gun. Unless noted otherwise all further device preparation steps were carried out in a nitrogen filled glovebox with an oxygen/water concentration below 5 ppm/3 ppm, respectively. For process control film thickness measurements were carried out by default with a Bruker DektakXT tactile surface profilometer in air. Devices were fabricated in a number of architectures which will be discussed in their respective chapters. Thus, here only a brief overview over the general procedures will be given.

Semiconductor deposition: Semiconductors were deposited using spincoating from various concentrations to vary the thickness of the semiconductor and its morphology. Unless noted otherwise toluene solutions with a semiconductor concentration of $10\,\mathrm{mg\,ml^{-1}}$ was spin cast at 1000 rpm for 50 s. To improve the film morphology and drive out remaining solvent the films were annealed at 60 °C for 5 min.

Electrodes: The electrodes (Ag and Au) and MoO_3 were deposited using a thermal evaporator inside a glovebox operation at pressures below 2×10^{-6} mbar with a rates in the order of $0.1\,\mathrm{Å\,s^{-1}}$ to $1\,\mathrm{Å\,s^{-1}}$ for Ag and Au and $0.1\,\mathrm{Å\,s^{-1}}$ to $0.2\,\mathrm{Å\,s^{-1}}$ for MoO_3 . Patterning of the the evaporated films was done via shadow masks. To improve the adhesion of Gold layers evaporated directly on Si or glass substrates a small interlayer of 3 nm of either Cr or MoO_3 was used. Evaporation materials were used as bought.

Pre-Fabricated Substrates: Pre-patterned substrates fabricated by the Fraunhofer-Institut für Photonische Mikrosysteme (IPMS) were used when noted. The $225\,\mathrm{mm^2}$ substrates consist of 16 individual transistors (W=10 mm, L=20/10/5/2.5 µm) in a bottom gate bottom contact structure where the semiconducting layer can be deposited on top. The injecting contacts are made of Gold (30 nm) deposited via photolithografie on highly doped Si wafer with an 90 nm or 230 nm thermally grown SiO_2 layer serving as a gate dielectric. Substrates were thoroughly rinsed with acetone prior to the normal cleaning steps to remove the top dicing resist layers.

3.3 Electrical Characterization

Unless noted otherwise, electrical measurements were carried out in a nitrogen filled glovebox with an oxygen/water concentration below 3 ppm/2 ppm, respectively. In the case of mutiple devices on the same substrates the individual devices were separated from each other with great care. This was achieved via a removal of material in the area between the individual devices (semiconductors and/or gold/silver/ITO contacts)

Current voltage measurements were carried out in the dark using a homemade probe station with a Keithley 4200-SCS parameter analyzer. Prestructured substrates were contacted with a special contact card.

Impedance spectroscopy was done with a ModuLab impedance spectrometer by Solartron analytical. Measurements were carried out in the four point probe mode with junctions as close as possible to the device. In room temperature measurements this was done by connecting two probes of a probe station directly on the respective contacts. Temperature dependent measurements were carried out in a specially designed holder where the two probes were connected on its outside. The amplitude of the perturbing oscillation was set to 200 mV.

3.4 Kelvin Probe Methods

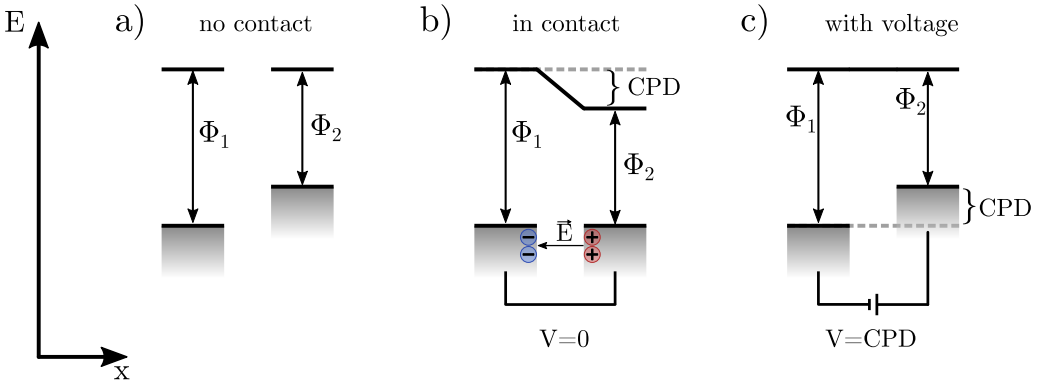

Figure 3.2: Sketch of the energy levels in a Kelvin-Probe experiment. a) Two metals with different work functions Φ_1 and Φ_2 in close proximity. b) Connecting them via an external circuit leads to current flow until an electric field E between the two materials is established. c) This field can be compensated via a voltage matching the contact potential difference (CPD).

More then 100 years ago Lord Kelvin showed that a potential is generated between two different conductors once they are contacted via an external circuit. [72] This effect is schematically depicted in figure 3.2. Once two materials of different work function Φ_1 and Φ_2 are brought to close proximity and are contacted via an external circuit the chemical potentials equilibrate via a charge transport through the circuit (figure 3.2b).

This leads to the formation of an electric field E between the two materials. If vice versa a voltage of the contact potential difference (CPD) of $V_{CPD} = q(\Phi_1 - \Phi_2)$ is applied no field prevails between the two materials (figure 3.2c). Experimentally, Kelvin-probe methods are used to measure the surface potentials of a variety of samples. If a reference electrode with known work function Φ_{ref} is used, measurements of V_{CPD} can be used to calculate the surface potential of the sample via $\Phi_s = \Phi_{ref} - V_{CPD}/q$. Determining V_{CPD} is usually achieved by measuring the electric field interaction between the reference electrode and the sample and setting the interaction to zero via the applied voltage.

3.4.1 Macroscopic Kelvin Probe Measurements

Chapter 5 utilizes a macroscopic Kelvin-probe set up in which the electrical interaction between sample and reference electrode is studied by oscillating the reference electrode with frequency ω_k (see figure 3.3a). In the case of a non-zero electric field between sample and reference the varying distance d between the two electrodes form a plate capacitors with osciallting distance and thus oscillating capacitance. This results in an osciallting electric current I_{ext} through the external circuit (figure 3.3b). An appropriate feedback-loop can be set up to minimize this current by adjusting the voltage V. At zero current flow the voltage reads $V = V_{CPD}$.

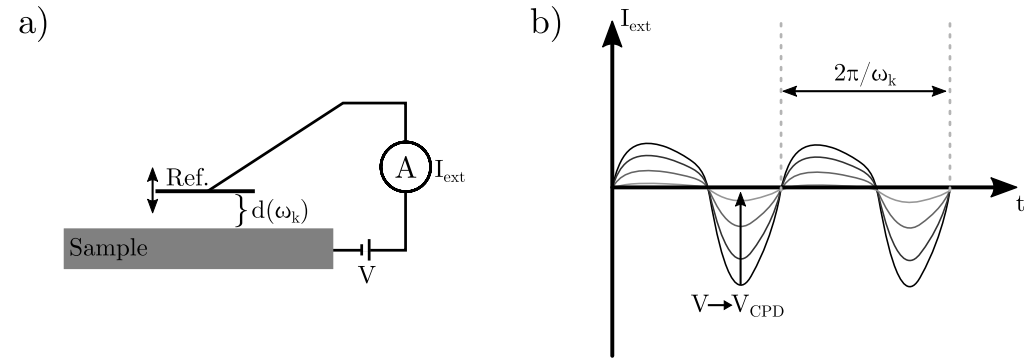

Figure 3.3: Setup of a macroscopic Kelvin-Probe experiment. a) Experimental setup in which the reference electrode is oscillated with frequency ω_k changing sample distance $d(\omega_k)$ accordingly. b) Resulting external current I_{ext} for voltages V closing in to V_{CPD}.

One has to note that the surface potential difference is not exactly the difference of work functions as either surface dipoles or additional electric fields can alter this property. Surface dipoles are often deliberatly introduced (e.g. through self-assembled monolayers) but can also come from the environment such as water from the ambient atmosphere. [15, 73] As both of these effects can alter the measured surface potentials in the order of several 100 meV great experimental care has to be taken. The experimental measurements in chapter 5 were carried out on a home-made probe station

with a xy-translation stage based on a Besocke Kelvin-probe S in ambient conditions. The probe itself consists of an Au coated metal grid with a diameter of $\approx 3\,\mathrm{mm}$. The response speed of the Kelvin-setup was measured as $0.4\,\mathrm{s}$ by applying a step voltage to a conductive surface and tracing the Kelvin-probes response.

3.4.2 Scanning Kelvin Probe Microscopy

In order to measure the local surface potential distribution with sub micrometer resolution the method of scanning Kelvin-probe microscopy (SKPM) was developed. [74] In SKPM, the surface potentials are probed in an atomic force microscop (AFM) with a conductive tip. A measurement of V_{CPD} through a nullification of an external current is not feasible in this context due to the nanometre dimensions of the tip, resulting in very small currents. Therefore the interaction between tip and sample is detected via a change in the oscillating properties of the AFMs tip. To achieve this goal, a constant potential V_{DC} and a perturbing bias V_{AC} of frequency ω_k are applied to the tip. The force between tip and sample is given by the following formula:

$$F = -\frac{1}{2}\Delta V^2 \frac{dC}{dz} \tag{3.1}$$

with the change in tip/sample capacitance $\frac{dC}{dz}$ and the voltage difference between tip and sample ΔV as

$$\Delta V = V_{tip} - V_{CPD} = V_{DC} + V_{AC}\sin(\omega_k t) - V_{CPD} \tag{3.2}$$

Expanding equation (3.1) with this expression for ΔV leads to

$$F = \underbrace{-\frac{dC}{dz}\left[\frac{1}{2}(V_{DC} - V_{CPD})^2\right]}_{F_{DC}} \underbrace{-\frac{dC}{dz}(V_{DC} - V_{CPD})V_{AC}\sin(\omega_k t)}_{F_{\omega}} \underbrace{+\frac{1}{4}\frac{dC}{dz}V_{AC}^2\left[\sin(2\omega_k t) - 1\right]}_{F_{2\omega}} \tag{3.3}$$

In the case of small perturbing voltage V_{AC} the second order term $F_{2\omega}$ can be neglected. In the case of a non-zero force between sample and tip mechanical oscillations of frequency ω_k are introduced in the cantilever and can be tracked via the AFMs photo-detector. Measuring the surface potential in this way can either be done simultaneously to measurements of the surface topography (single pass) or first a topography measurement can be recorded, followed by a measurement of the surface potential (dual

pass mode).[1] Depending on the choice of frequency and equipement used the two common measurement modes amplitude modulated (AM) and frequency modulated (FM) SKPM are distinguished. [75]

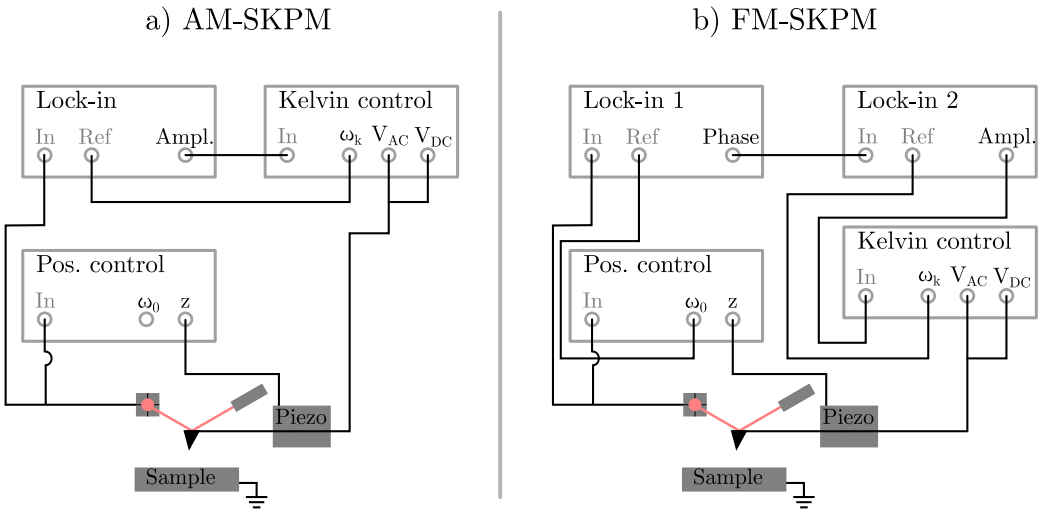

Figure 3.4: Sketch of two typical SKPM setups. Both setups consist of a positional control unit adjusting the spatial position of the AFM tip in all three dimensions and keeping a constant sample tip distance (z) through a piezo actuator. Furthermore, in both setups a DC voltage (V_{DC}) and a small perturbing AC disturbance (V_{AC}) of frequency ω_k are applied to the tip. a) In a AM-SKPM setup the cantilevers oscillations at ω_k are directly used in a feedback-loop to null the tip-sample interaction via adjusting V_{DC}. b) In the FM-KPFM mode, the change of the mechanical resonance frequency $\Delta\omega$ is detected through two lock-in amplifiers and used to null the tip-sample interaction by adjusting V_{DC}. The here shown configuration is employed in Bruker FM-SKPMs used within this work.

Figure 3.4a shows a sketch of a typical AM-SKPM setup. The figure shows a setup where the sample is grounded and the tip is biased. The inverse scenario of biased sample may also be used.The topography of the sample is measured by driving the cantilever at its resonance frequency ω_0, the height and position of the tip is maintained by the position control unit. The frequency used for Kelvin measurement can in principle be chosen arbitrarily. In practice ω_k is chosen to be in resonance with the cantilever maximising the cantilevers amplitude. In single pass mode ω_k is set on a second or higher order resonance to avoid crosstalk between the Kelvin-probe and the topography measurements as the first resonance is used for the topography measurements. In dual pass the machanical osciallтion of the cantilever can be stopped and $\omega_k = \omega_0$ my be used. A lock-in amplifier is used to detected the oscillations of the cantilever at the

[1] A dual pass experiment is usually done line-by-line where first the topography is recorded and then the tip is traced again over the line with a set distance to the surface to avoid electrical interference between tip and sample

frequency ω_k and a feedback-loop in the Kelvin control unit adjusts V_{DC} so that its amplitude is minimal and the value is stored.

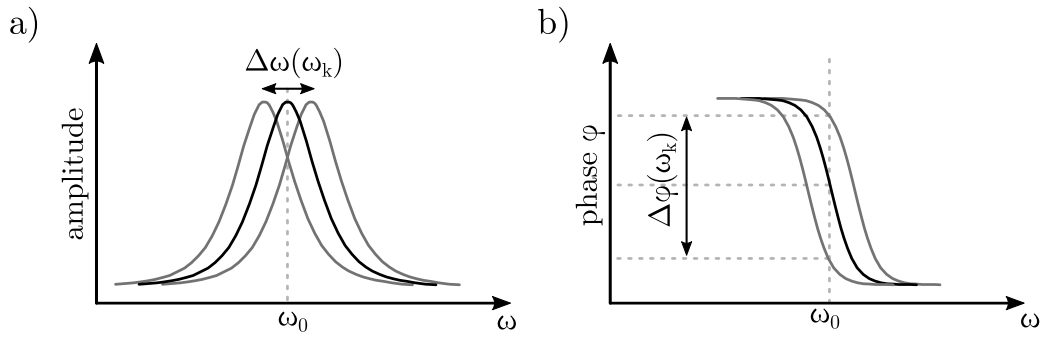

Figure 3.5: Shift of the resonance amplitude (a) and phase (b) of an AFM cantilever through an oscillating electrical field. Application of an oscillating electric field of frequency ω_k between tip and sample leads to a periodic shift of resonance frequency $\Delta\omega(\omega_k)$ (a) and phase $\Delta\varphi(\omega_k)$ (b). This shift of frequency/phase is the basis for FM-SKPM.

In an FM-SKPM setup (see figure 3.4b) the change in the cantilevers main resonance frequency ω_0 is detected. The electrical force gradient acting on the tip changes the cantilevers resonance frequency to higher/lower values for repulsive/attractive forces. [75] This change in resonance frequency $\Delta\omega$ is proportional to the derivative of the electric field. In line with the change in resonance frequency comes a shift in phase φ regarding to the applied stimulus. Experimentally the AFMs cantilever is driven at its resonance frequency ω_0 and a constant potential V_{DC} is applied. Then a small electric oscillation of much smaller frequency ω_k is applied to the tip. This results in an oscillation of the resonance frequency $\Delta\omega$ and phase $\Delta\varphi$ with frequency ω_k alike (see figure 3.5). The change in frequency/phase can then be used as an input parameter for a feedback loop, adjusting it to zero, finding $V_{DC} = V_{CPD}$ where the force gradient (as E=0) is zero.

There exist severall different setups under the name of frequency modulated SKPM to either find $\Delta\omega$ or $\Delta\varphi$. The setup used in this work was fabricated by Bruker and uses a combination of 2 lock-in amplifiers (see figure 3.4b). The first lock in amplifier detects the phase shift between stimulus and response at ω_0. The second outputs the change of phase at the much lower frequency of electrical perturbation ω_k. The Kelvin-control unit then adjusts V_{DC} to null this signal. A competing design which can be found in [74] utilizes a frequency demodulator to obtain the frequency spectrum of the cantilevers oscillation in combination with a lock-in amplifier.

In general does not only the electrical interaction between tip and sample influence surface potential measurements but also the electrical field between sample and the much bigger cantilever. This effect is less pronounced in the FM-mode resulting in better spatial resolution. On contrary, the setup of the AM mode generally leads to a

better signal-to-noise leading to an energy resolutions of up to 5 meV (FM: 10-20 meV). [74]

3.5 Further Thin Film Characterization

Ultraviolet photon emission spectroscopy (UPS) was carried out by Silke Koser on a Phi VersaProbe II spectrometer with an Omicron HIS 13 helium dis-charge lamp (HeI: $h\nu = 21.22\,\mathrm{eV}$).

Atomic force microscopy (AFM) measurements were carried out on a Bruker Nanoscope MultiMode VIII in the ScanAsyst PeakForce mode. The resulting images were treated with the software Gwyddion for row alignment and scar correction.

Electron beam lithography (EBL) was done on a EO 1530 Secondary electron microscope (Zeiss) with a Raith Elphy Plus pattern generator system together with Christian Huck.

3.6 Finite Element Techniques

Many physical problems are expressed through partial differential equations (PDEs) to which only in the most simple cases analytical solutions can be found. Thus, sophisticated tools to analyse those problems were developed among which Finite-Element-Methods (FEM) have seen a wide range of applications. Here only a brief overview of this subject shall be given following the books by Bronstein et al. and Koutromanos while a more in-depth view can be found in many textbooks of applied numerical methods. [76, 77] Consider for example the following one-dimensional Poisson-equation defined in a specific domain of length L:[2]

$$\frac{d^2u(x)}{dx^2} = f(u(x)) \quad \text{for} \quad 0 < x < L \tag{3.4}$$

featuring a known function $f(u(x))$ while the solution of $u(x)$ is desired over the whole domain. Furthermore, at the edges of the domain, $u(x)$ is known in the form of boundary conditions reading for example u(0)=u(L)=0. In FEMs an approximate solution to this problem is found in three steps. First, the problem is re-formulated in its weak form – also called the variational form – through the use of N sufficiently smooth test functions $v_j(x)$ $(j = 1, ..., N)$ which are vanishing on the edge of the domain. Then, the problem is integrated over the whole domain, giving in this example:

[2] This is the poisson equation for electrostatics for $u(x) = \varphi(x)$ the electrical potential and $f = -\rho(\varphi(x))/\epsilon$ the charge density divided by the permittivity of the medium.

$$\int_0^L \frac{d^2u(x)}{dx^2} v_j(x)dx = \int_0^L f v_j(x)dx \quad \text{for} \quad j = 1, ..., N. \tag{3.5}$$

This weak formulation transformed the problem of finding a matching (functional) solution for the given problem towards an expression in which numbers are compared so it can be treated with a computer. Secondly, the domain is discretized into small subdomains and the finite element approximation is introduced. Often the discretization is done through triangulation where triangles are closer together at points of particular interest (e.g. edges of contacts). Here the interval can, for example, be divided into N-nodes (x_i to x_N) equally spaced apart by $\Delta x = N/L$. In the GALERKIN-method, this suggests an expression of all functional behaviour (u(x),v(x) and f(u(x)) within one subdomain to be described by a common set of basis functions. Often, linear LAGRANGE-basis functions (also called "hat functions") φ are chosen through which these functions can be described as:

$$\tilde{u}(x) \approx \sum_i^N u_i \varphi_i(x). \tag{3.6}$$

Directly on the nodes i, this approximation exactly reproduces $u(x)$ while the value between nodes are interpolated. $f(u(x))$ is treated in the same way to obtain

$$\tilde{f}(x) \approx \sum_i^N f_i \varphi_i(x), \tag{3.7}$$

while v_j is set as φ_j. Then the problem adopts the following form:

$$\sum_i^N u_i \int_0^L \frac{d^2\varphi_i(x)}{dx^2} \varphi_j(x)dx = \sum_i^N f_i \int_0^L \varphi_i \varphi_j dx \quad \text{for} \quad j = 1, ..., N. \tag{3.8}$$

This expression is a set of N equations giving access to the N unknown u_i. These equations can be solved in the third step through a computer program to obtain the approximative values for $u(x)$ at all the N nodes, the final solution. The accuracy of FEMs is dependent on a number of factors among which are the discretization strategy and the types of test and basis functions used. This opens room for a wide variety of FEM approaches to solve the many different types of PEDs. Often only a part of the problem at hand (e.g. the spatial dependence) is solved through FEM approaches while the rest of the problem (e.g. its temporal evolution) is solved through a finite difference ansatz. [77] There a number of different commercial or open-source software

available to carry out FEM simulations of different problems. Here the commercial software COMSOL Multiphysics© is used to model the electrical response of MIS capacitors. The software was thus supplied with the geometrical layout of the device, the boundary conditions and the equations describing the physical response of the system e.g. transport (drift, diffusion and continuity terms), injection and recombination. The internal finite-element routines were used to solve this problem and extract the desired data.

4 Probing Charge Carrier Transport via MIS-Capacitors

Understanding and engineering charge carrier transport in thin films is an important prerequisite for the efficient operation of organic electronic devices. While OLEDs and OPVs are highly dependent on charge carrier transport along the layer normal, OFETs are influenced by both horizontal and vertical charge carrier transport.[1] Here the validity of experiments using metal insulator semiconductor (MIS) capacitors for charge carrier transport investigations will be tested. While the use of capacitors for charge carrier transport investigations may seem questionable at first as they do not carry a DC current, this absence of significant DC current allows capacitor based techniques different access to transport parameters such as the charge carrier mobility μ and the density of states (DOS) width σ. First, a technique based on experimental measurements of the capacitance frequency (Cf) spectra of such capacitors for mobility measurements will be presented, applied and further validated. This technique was then utilized to measure the semiconductors DOS width σ through temperature dependent measurements. This Cf approach towards σ is compared to a second technique utilizing capacitance voltage (CV) measurements in combination with numerical simulations. Due to the fundamental nature of these comparisons only the two reference materials P3HT and TIPS-PEN will be employed here, giving access to sufficient literature values when needed.

4.1 The Model System

To enable the envisioned comparative studies, first a robust and reproducible MIS capacitor device has to be established. As both fabrication technique and device layout can have a strong influence on device operation the considerations for the here chosen system will be briefly discussed. Vertical organic MIS capacitors can in principle be fabricated in two different ways. In a bottom gate device the semiconducting material is deposited on the insulator and the charges are injected from the top while in a top gate device the charge carriers are vice versa injected from the bottom. The here presented system is the result of an optimization process over the course of which different MIS capacitor layouts have been investigated (e.g. dielectrics, layer-stacks and semiconductor processing parameters). In analogy to OFETs MIS capacitors are greatly influenced by the interplay between semiconductor and insulating material. After initial experiments with Si/SiO_2 substrates, Parylene-C was chosen as an insulating material. While Parylene-C exhibits a lower leak resistance in comparison to the often used

[1] Depending on the film thickness, one or the other may be more important.

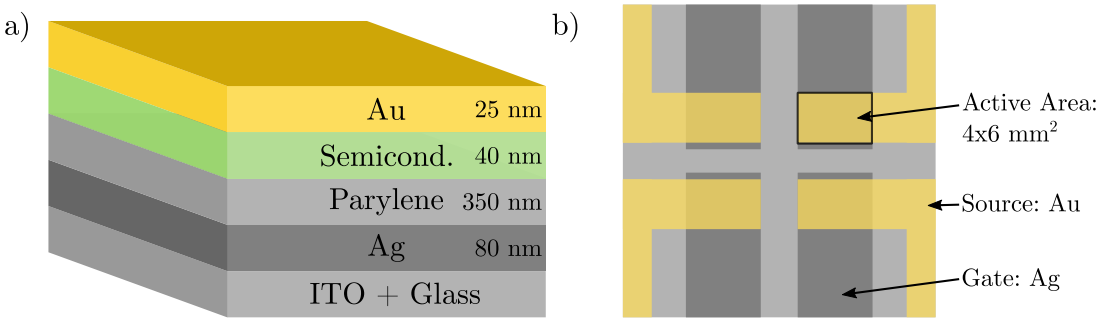

Figure 4.1: Layout of the MIS capacitor model system. a) Layer-sketch of the capacitors fabricated. P3HT or TIPS-PEN were used as semiconductors. b) Top view of the capacitors. On a substrate of size 25 mm × 25 mm four capacitors are fabricated.

metal oxides (e.g. SiO_2 or Al_2O_3) it is known for a much lower tendency to trap charge carriers at the semiconductor/insulator interface. [70, 71] This behaviour is to be preferred as trap state population/depopulation can lead to a dispersive transport along the layer normal, possibly influencing the envisioned Cf measurements. [78, 79] Here a bottom gate layout was chosen where the semiconductor is processed on the insulator to further eliminate adverse effects of the insulator on semiconductor deposition. Another reason for the bottom gate architecture comes from the growth process of Parylene-C. Different surfaces are known to result in different Parylene thicknesses due to a different growth behaviour for the first few nanometre. Thus, reference devices without the semiconducting layer are best suited when fabricated on identical surfaces (here the Ag gates). The two semiconducting materials P3HT and TIPS-PEN were deposited via spin-coating followed by an annealing step at 60 °C for 5 min. Due to the position of P3HTs HOMO level, gold was used as electrode material, commonly known to result in ohmic contacts for holes. [14, 66, 67] For TIPS-PEN a slight injection barrier is to be expected. [80] As P3HT is easily doped by ambient oxygen, the P3HT layer can be assumed to be at least lightly doped as the devices are fabricated in one glovebox but have to be transported through ambient conditions to a second glovebox for electrical characterization.[2] Figure 4.1a shows the layout of the capacitors fabricated in this chapter. Contacting the gate electrode is facilitated by using glass substrates coated with patterned indium doped tin oxide (ITO) on which the silver is evaporated. On each 25 mm × 25 mm substrate four identical condensators with an area of 4 mm × 6 mm are processed (see figure 4.1b). Devices were analyzed via impedance spectroscopy. A constant DC voltage was applied between the Au source contact and the Ag/ITO electrode superimposed by a small AC perturbation (200 mV) of variable frequency. The response of the system was recorded and the capacitance as a function of DC voltage and perturbing frequency was calculated (see section 3.3 for more experimental details).

[2] This assumption is supported by the later fabricated identical transistors which exhibit signs of a slight doping.

4.2 Room Temperature Operation

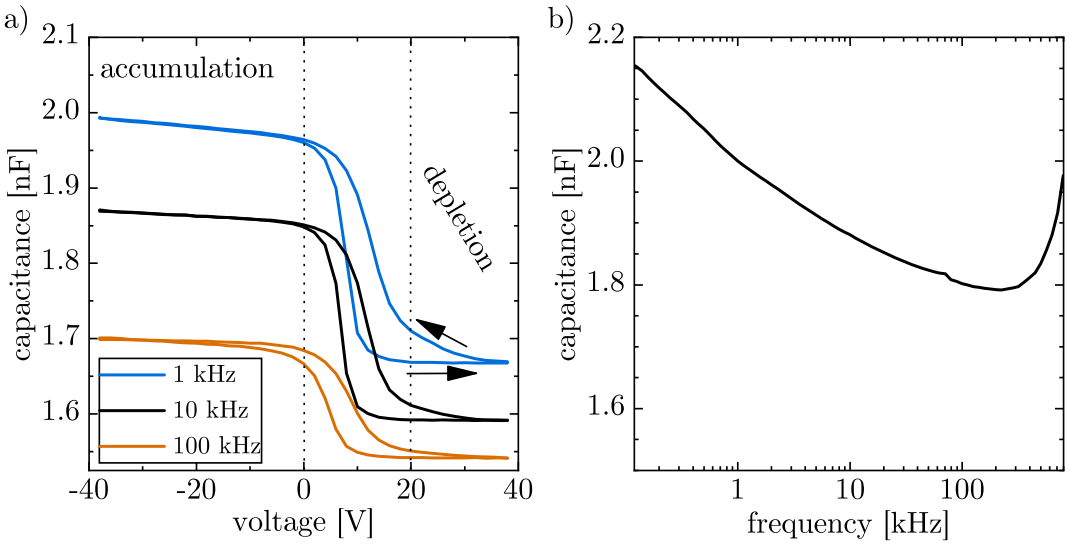

Figure 4.2: Capacitance voltage measurement of a P3HT MIS capacitor (a) and capacitance frequency plot (b) of a reference capacitor. a) The measurement exhibits a high capacitance in accumulation and a low capacitance in depletion. b) In the Cf plot of a reference device an increase of capacitance for frequencies below 300 kHz indicate a frequency dependent dielectric constant of the insulating Parylene-C layer used. See figure 4.1 for device layout.

Figure 4.2a depicts an exemplary CV plot of a P3HT capacitor using the above presented layout (see section 2.2.1 for more details of MIS capacitor operation in general). For negative voltages ($V < 0\,\mathrm{V}$) the capacitor depicts a high capacitance ($C_{Acc.}$) while high voltages ($V > 20\,\mathrm{V}$) result in a low capacitance ($C_{Depl.}$). At intermediate voltages, a hysteretic shift between these two values can be observed. Both $C_{Acc.}$ and $C_{Depl.}$ increase for decreasing frequency of the perturbing AC amplitude. The shift between $C_{Acc.}$ and $C_{Depl.}$ can be explained through the accumulation and depletion of holes in the semiconducting layer. Negative voltages lead to the injection of holes into the P3HT which accumulate at the semiconductor/insulator interface. These accumulated charge carriers can be probed through the AC amplitude resulting in the high capacitance. In depletion ($V > 20\,\mathrm{V}$) the semiconductor is devoid of holes as the polarity of the voltage renders charge carrier injection improbable. This increases the distance of charge carriers in the whole capacitor (gate electrode vs. source electrode) while decreasing the observed capacitance. Through the asymmetric injection barriers for electrons (high barrier) and holes (low barrier) the (possible) accumulation of electrons during hole depletion cannot be probed (see chapter 6 where electron accumulation will be shown in TIPS-PEN). The position of the shift between accumulation and depletion capacitance is caused by a built-in potential influenced through the choice of electrodes and further dipole moments. The hysteresis of the CV measurements can be caused for example by

those dielectric dipole moments and/or trap states in the semiconductor or insulator much like in organic transistors. [81]

The decrease in accumulation and depletion capacitance observed in Figure 4.2a can be rationalized with a frequency dependent dielectric constant of the used insulator. Figure 4.2b depicts a Cf measurement of a reference device without the semiconducting layer. The gradual increase in capacitance for frequencies below 300 kHz is attributed to a frequency dependent dielectric constant of Parylene-C, likewise increasing the accumulation and depletion capacitance in devices with semiconductor. The strong rise above 300 kHz is connected to an increasing contributions of the cables used. The measurement is independent of the DC voltage (not shown).

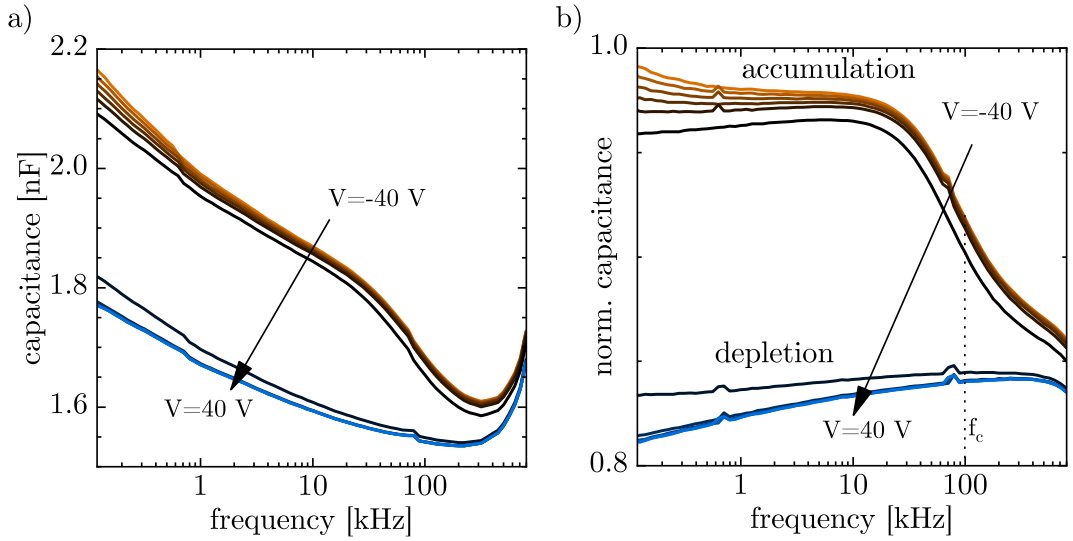

Figure 4.3: Capacitance frequency (a) and normalized capacitance frequency (b) of a P3HT MIS-Capacitor. a) Cf characteristic of a P3HT capacitor for different voltages. b) Normalized Cf curve of the same device. Normalization was carried out by deviding (a) through a measurement of a capacitor without semiconductor (e.g. figure 4.2b) For low voltages (e.g. $V = -40\,\mathrm{V}$) a frequency dependent accumulation capacitance is obeserved. In depletion ($V = 40\,\mathrm{V}$) the capacitance is ideally frequency independent at a lower value. f_c is the cut-off frequency. The CV of this device can be found in figure 4.2a

Figure 4.3a shows the Cf characteristic of the P3HT device from Figure 4.2a. All curves exhibit three measurement artefacts: two small inhomogeneities 80 kHz and 0.8 kHz as well as a the capacitance increase at frequencies higher than 300 kHz. While the former are the results of an internal switching in the measurement equipment the latter can be explained again by the increasing influence of the cables impedance at higher frequencies. The increase in depletion and accumulation capacitance for decreasing frequency can be explained likewise via the insulators frequency dependent dielectric constant. The frequency dependence of the accumulation capacitance changes for frequencies higher than 10 kHz. Above this threshold, the frequency of perturbing voltage is too high so that the charge carriers cannot traverse the whole thickness of the semi-

conductor during half a period length. Since the centre of charge thus cannot fully reach the semiconductor/insulator interface the measured capacitance decreases. Under hole depletion conditions (e.g. $V = 40\,\mathrm{V}$) this effect is not observed since holes and electrons cannot be injected by the AC voltage.[3] To make the analysis of such Cf curves more convenient and to eliminate the insulators frequency dependence a normalization can be carried out. Figure 4.3b shows the same Cf curve divided by a measurement carried out on a reference capacitor (e.g. Figure 4.2b without semiconductor, normalizing the accumulation capacitance to one. A small discrepancy from the ideal behaviour can be explained by a potential small slight deviation in capacitor area between sample and reference.

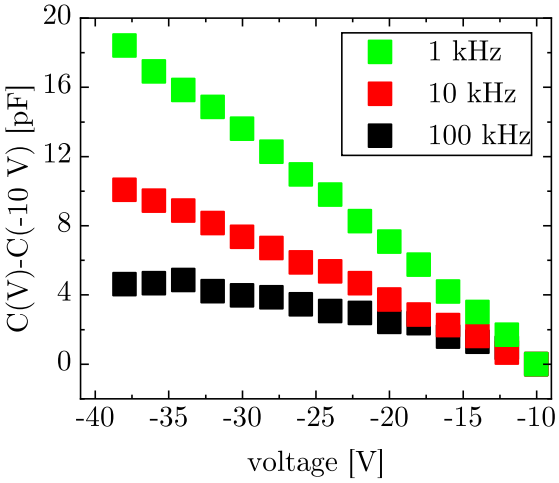

Figure 4.4: Slow decrease the accumulation capacitance for increasing voltage in P3HT MIS capacitor. To better elucidate this trend the capacitance at $-10\,\mathrm{V}$ was substracted from the measured data. Cf and CV curves of this device can be found in figure 4.2a and figure 4.3, respectively.

The CV charateristic from figure 4.2a shows another interesting behaviour which was not discussed yet. The accumulation capacitance exhibits a steady increase for decreasing voltage. Normalizing the capacitance to the value at V=$-10\,\mathrm{V}$ results in figure 4.4. An increase of accumulation capacitance with decreasing voltage can be seen. A decreasing frequency furthermore increases the slope of this dependency. An explanation of this behaviour is based on the geometric layout of the capacitors. Due to the extended gate contacts in combination with the unpatterned insulator and semiconductor layers, charge carriers can drift from under the source contact outwards along the gate contact, accumulating at the much bigger gated semiconductor/insulator interface. This accumulation induced parasitic capacitance (AIPC) increases the measured capacitance. This effect is more pronounced for higher applied voltages as it increases the related electric field for drift outside of the capacitors active area. Furthermore, a decreas-

[3] The polarity of the voltage prevents hole injection while AC electron injection is prevented by their high injection barrier

ing frequency increases this effect by increasing the maximum time the charge carriers may spread horizontally, increasing the area broadening. The hole's drift distance is ultimately governed by their vertical charge carrier mobility making the effect less pronounced for low mobility materials. How this effect can be used to measure the charge carrier mobility of organic semiconductor will be explored in detail in chapter 5.

4.3 Mobility measurements

Stallinga et al. have presented an approach to measure the vertical charge carrier mobility in MIS capacitors through Cf measurements (see 2.1.2 for a more detailed discussion of mobilty measurement techniques). [10] Their approach offers several advantages over other techniques for mobility measurements along a layers normal. The use of an insulating layer, for example, prevents significant DC current facilitating the analysis in comparison to other techniques using admittance spectroscopy. This method can be further easily applied for ambipolar materials and it requires little experimental input (in contrast to for example SCLC techniques). [10] As such, this technique could be a valuable addition to the various other mobility measurement techniques. Here, this – in its current state – rarely applied technique will be further validated and later applied to temperature dependent measurements.[4] In a MIS capacitors Cf spectra, the cut-off frequency f_c discriminates between frequencies at which full accumulation can or cannot be reached (for more details see section 2.2.1). Stallinga et al. give this frequency as: [10]

$$f_c = \frac{\mu_h k_\mathrm{B} T}{2\pi q d_s^2} \tag{4.1}$$

with μ_h the hole mobility, $k_\mathrm{B}T$ the product of Boltzmann-constant and temperature, q the elementary charge and d_s the thickness of the semiconductor. This technique effectively measures the charge carriers transit time through the whole thickness of the semiconductor film in the frequency domain (see section 2.1.2). As such, different approaches to the extraction of f_c from experimental Cf curves are viable. The calculation of the cut-off frequency is done here from the inflection point of the normalized CV curves (see figure 4.3b). In the original publication, the maximum of the dielectric loss defined as $L = G/2\pi f$ with G the electrical conductance was used. It was found that both the derivative of the CV plot and the maximum in loss gives identical results.

A first test of this method to obtain the hole mobility was carried out using the above discussed MIS-capacitor model system (section 4.1) with P3HT as a semiconductor (an exemplary Cf characteristic is given in figure 4.3). The cut-off frequency of a set of devices was measured as $f_c = (1.1 \pm 0.1) \times 10^5\,\mathrm{Hz}$ from which an average vertical

[4] The original publication does not compare the obtained mobilities to those measured via a different approach.

hole mobility of $\mu_{h,Cap.} = (4.5 \pm 0.5) \times 10^{-4}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ can be calculated using equation (4.1). This μ_h value was verified by building a set of transistors with identical layer-stack in which the hole mobility was calculated through transfer measurements. Figure 4.5 depicts the results of an exemplary transfer and output measurement of an Ag/Parylene-C/P3HT/Au transistor. Here the average field effect mobility was determined as $\mu_{h,OFET} = (7 \pm 2) \times 10^{-4}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Thus, the horizontal field-effect mobility (measured in OFETs) and the vertical mobility (measured in MIS capacitors) differ only very slightly. P3HT is known to exhibit an increase in mobility for higher charge carrier densities. [82] As both transfer and output characteristics of the OFETs do not indicate charge transport impeded by contact phenomena the obtained transistor mobilities can be seen as a purely field-effect property, measured at high charge carrier densities. The capacitor measurement, on the other hand, requires the holes to traverse a low carrier density semiconductor as the charge carriers are accumulated only at the semiconductor/insulator interface. Thus, the here obtained mobilities fit remarkably well.

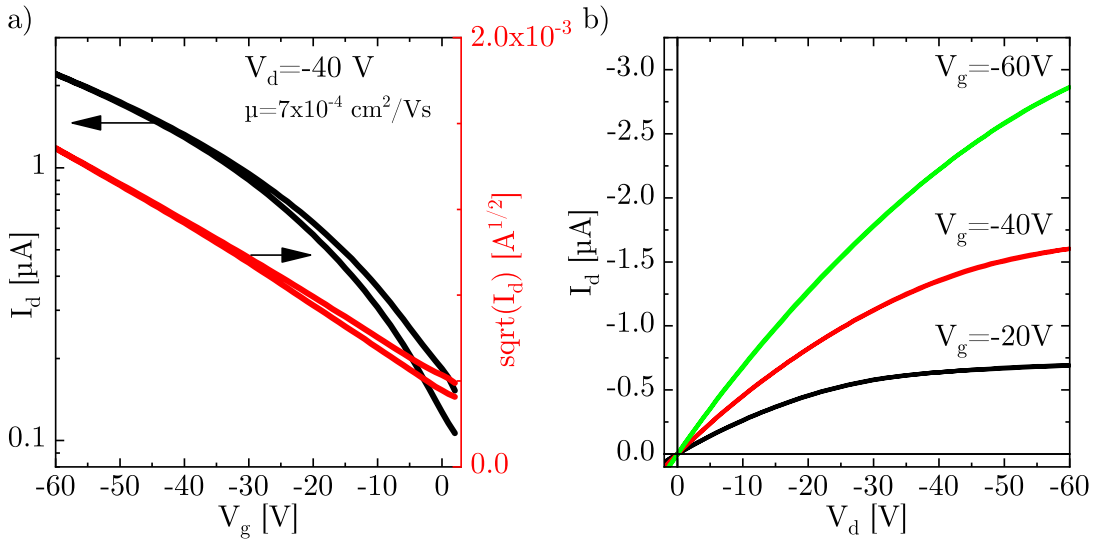

Figure 4.5: Transistors measurement of P3HT transistor. a) Transfer characteristic. As the transistor is not depleted yet within the measurement range it can be assumed that the transistors was doped (most likely by ambient oxygen) b) Output charateristic. The transistor employs an identical layer-stack and thicknesses as the MIS capacitor model system (Ag/Parylene-C/P3HT/Au transistor, see figure 4.1).

To further validate the geometric dependence of method of mobility calculations, a set of capacitors with increasing semiconductor thickness was fabricated. Here, the same model system was used this time employing TIPS-PEN as a semiconductor, spin-coated from solutions with doubling concentrations resulting in thicknesses of d=40 nm to 160 nm. TIPS-PEN instead of P3HT was used due to the higher solubility of TIPS-PEN, allowing the fabrication of thicker layers. The Cf curves obtained very closely resemble the ones from figure 4.3. Figure 4.6 depicts the extracted cut-off frequencies

as a function of semiconductor thickness. The fit of the measured cut-off frequencies closely matches the proposed d_s^{-2} behaviour further underlining the validity of method to measure the charge carrier mobility.

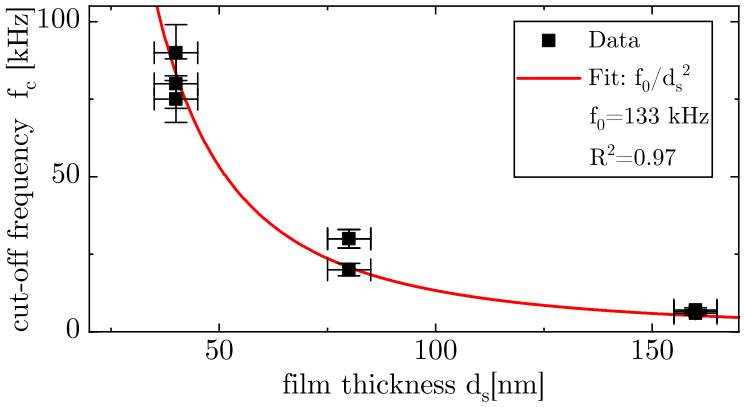

Figure 4.6: Cut-off frequency as a function of semiconductor film thickness in TIPS-PEN model system MIS capacitors. f_c was measured in a set of MIS capacitors utlizing 40 nm to 160 nm thick TIPS-PEN films as semiconductor (see figure 4.1 for the device layout).

After the validity of capacitor based mobility extractions in the here utilized model system was proven this method will be further applied for temperature dependent measurements.

4.4 Temperature Dependent Measurement

Temperature-dependent mobility measurements of organic semiconductors can give valuable insight not only into the charge transport processes but also on the width of the underlying energy level. Here, the temperature dependent vertical charge carrier mobility was measured via the previously employed method through cut-off frequency determinations in MIS capacitors. Samples were cooled using a stream of cool gaseous nitrogen reaching temperatures down to 176 K. Devices utilizing the above presented MIS-capacitor model system (section 4.1) were used with P3HT as the semiconductor. Temperature-dependent reference capacitor measurements were carried out for normalization purposes (see appendix for data). As it proved experimentally challenging to measure the reference capacitor with the exact temperatures as the MIS capacitors, the capacitance at a given temperature was interpolated from the recorded data.[5] The obtained temperature dependent normalized Cf curves under accumulation conditions can be seen in figure 4.7. Based on the strong shift of high/low capacitance switching point towards lower frequencies, it is already obvious that the transport of the here investigated system is strongly thermally activated.

[5] The temperature was set through the flow-rate of the gaseous cold nitrogen by hand. An increased temperature stability could for example be reach through the use of an appropriate feedback loop.

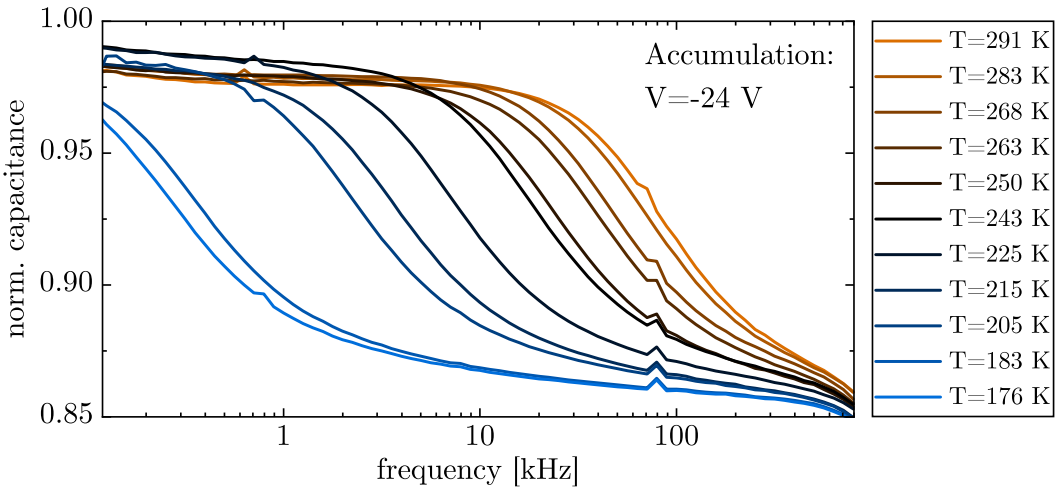

Figure 4.7: Temperature dependent capacitance frequency plot of a P3HT-MIS capacitor. A shift of the switching point between high (around 1) and low (≈ 0.86) norm. capacitance towards lower frequencies for decreasing temperature can be seen.

Figure 4.7 allows the calculation of the charge carrier mobility through the cut-off frequency, again defined as the inflection point of the normalized CV curve. There are – as discussed in section 2.1.1 – many different descriptions in literature for the charge carrier mobility as a function of temperature. Figure 4.8 assumes am $ln(\mu) \propto T^{-1}$ dependency while in figure 4.9 an $ln(\mu) \propto T^{-2}$ dependency is used. The first plot assumes an Arrhenius type behaviour. Fitting an Arrhenius function to the experimentally measured mobility results in an activation energy of $E_A = (204 \pm 5)\,\mathrm{meV}$. The activation energy can be interpreted as a trap level above the HOMO level from which the charge carriers have to be excited in order to contribute to conduction. This value of around 200 meV is a factor 2-3 higher than values reported previously in literature calculated through temperature dependent OFET measurements. [83] The reason for this big difference remain unclear. A possible explanation may involve the vastly different charge carrier densities through which the charge carriers have to travel (high in OFETS, low in MIS capacitors) or a significantly higher disorder in comparison to the literature value.

The $ln(\mu) \propto T^{-2}$ assumption in figure 4.9 comes from the Bässler-model (see section 2.1.1 for a more detailed explanation) which has seen some criticism over the years but still remains a widely used model. [30] The Bässler-model assumes a gaussian DOS described solely through its width σ. Here, the transport of charge carriers is driven by the AC perturbation of 200 mV which is much smaller then the DC voltage needed to

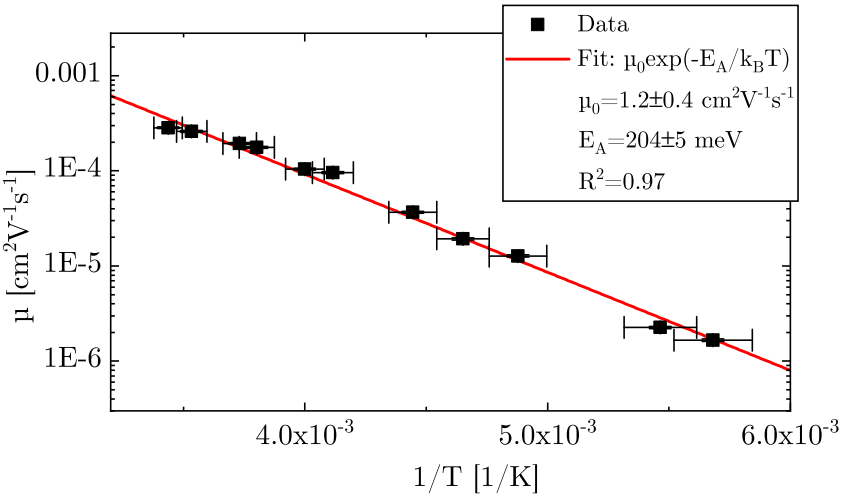

Figure 4.8: P3HT MIS capacitor mobility as a function of inverse Temperature (symbols). A fit of an ARRHENIUS model (line) closely reproduces the observed trend where the activation energy was found as $E_A = (204 \pm 5)\,\mathrm{meV}$.

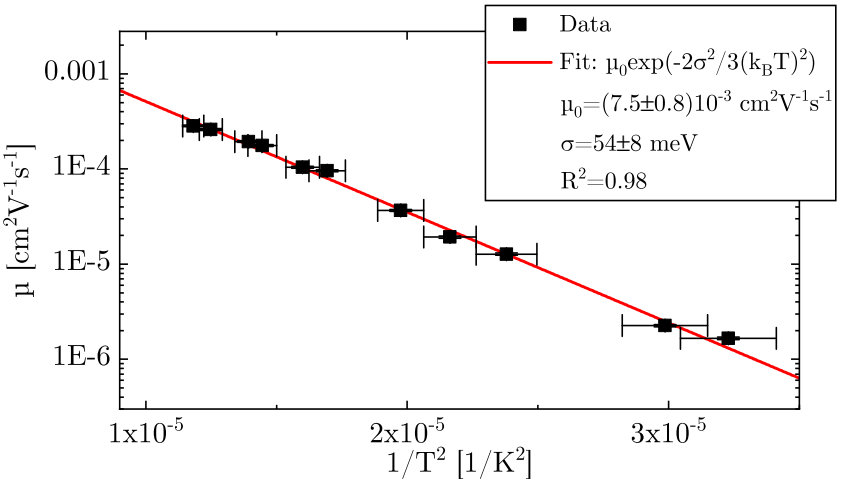

Figure 4.9: P3HT MIS capacitor mobility as a function of squared inverse temperature (symbols). A fit of an BÄSSLER model (line) closely reproduces the observed trend with a DOS width of $\sigma = (54 \pm 8)\,\mathrm{meV}$.

drive the capacitor in accumulation (-24 V). Thus, neglecting the field dependent term of this model gives:[6]

[6] Setting the used constants in the field dependent term according to [37] as C=2.9 × 10^{-4} $\sqrt{\mathrm{cm/V}}$ and calculating the electric field as $F = 200\,\mathrm{mV}/340\,\mathrm{nm}$ gives an additional term of $\approx 0.02\hat{\sigma}^2$ in the exponent of equation (4.2) which can be clearly neglected.

$$\mu(\hat{\sigma}^2) = \mu_0 \exp\left[-\left(\frac{2}{3}\hat{\sigma}^2\right)\right] \tag{4.2}$$

The disorder parameter $\hat{\sigma} = \frac{\sigma}{k_B T}$ allows the calculation of the DOC width, reading here $\sigma = (54 \pm 8)\,\mathrm{meV}$. In the past Torricelli et al. (with data from Tanase et al.) investigated the temperature dependent mobility in P3HT diodes and OFETs. [82, 84] It was shown that the energetic landscape in P3HT can accurately be described through a single gaussian DOS of width $\sigma_{lit.} = 98\,\mathrm{meV}$. Although this study did use a different approach for charge carrier transport (Bässler uses a Miller-Abrahams ansatz while Torricelli et al. a variable range hopping model) their results should be – in principle – comparable to the here used approach. The lower σ value found here suggests a P3HT film with a much lower disorder.

Both the Arrhenius and the Bässler model offer very close fits to the experimental data (nearly identical R values). In order to decide which of these two models describes the real devices better experimental data spanning a wider range of temperatures would need to be collected. This is experimentally not viable as the here measured lowest cut-off frequency of 251 Hz is already close to the lower limit of the used approach. Analysing both models for their behaviour at $T \to \infty$ reveals a clear difference between the two models. [36] While the Arrhenius-model with $\mu_0 = (1.7 \pm 0.5)\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ most likely overestimates the mobility, the Bässler-model offers a much more resonable value of $\mu_0 = (7 \pm 1) \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ in line with the experimental values obtained from room temperature operation of the transistors and capacitors of $\mu_{h,OFET} = (7 \pm 2) \times 10^{-4}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $\mu_{h,Cap.} = (4.5 \pm 0.5) \times 10^{-4}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, respectively.

Both models fare in their comparison to literature very differently. While an Arrhenius approach overestimates the activation energy a Bässler model underestimates σ. There are several possible explanations for this behaviour. Stallinga's approach to vertical mobility measurements could become inaccurate at low temperature. Thus, the method of cut-off frequency calculation from the Cf curves was varied. The cut-off frequency was re-calculated as the intersection of a line describing the accumulation capacitance and a second line describing for the decay of capacitance in the switching area (see appendix). This changed procedure to cut-off frequency calculation only slightly changed E_A or σ. Thus the exact nature of the cut-off calculation seems to have no impact on the temperature-dependence of the obtained mobilities. Further validation thus need charge carrier investigations in a similar geometry at similar charge carrier densities (e.g. temperature-dependent time of flight) which are experimentally very challenging. Both the Arrhenius and the Bässler model are known to be only a rough description of the temperature dependence of the hole mobility. Thus a more sophisticated model could alleviate this issue (e.g. the extended gaussian disorder model). [30] It is well known that organic devices fabricated at different labs generally show some variance so some degree of discrepancy is to be expected. [9] As E_A or σ investigations in MIS capacitors are not available a potentially erroneous comparison to other device layouts featuring e.g. different charge carrier densities had to be made.

In conclusion, the room temperature mobility measurements of this Cf approach seem to be a reasonable estimate while assertions about the accuracy of the E_A or σ values are more complex. Thus a different capacitor based technique was investigated in P3HT model system capacitors giving access to σ from room temperature CV measurements.

4.5 Simulating Capacitance Voltage Curves

Maddalena et al. published in 2015 a research article describing a simple Poisson approach which gives access to the DOS width σ via a fit of experimental to simulated CV curves. [64] A quick and easy access to σ could enable further studies on the relationship between σ and μ for different fabrication techniques and organic semiconductors, giving a deeper insight into the charge transport of organic semiconductors. In this section, Maddalena's approach will be presented briefly and is then applied experimental data of P3HT capacitors.

4.5.1 The Algorithm

Maddalena's algorithm starts with a purely one-dimensional p-type capacitor under steady-state conditions with a DC voltage applied. As no current will flow, the Fermi level position can be set independently from z as $E_f = 0$. Furthermore, the reference level for the electrical potential $\varphi(z)$ shall be chosen in such a way that $\varphi(z) = \frac{E_{HOMO}(z)}{q}$ with q the elemental charge and $E_{HOMO}(z)$ the (energetic) centre of the HOMO level as a function of position. Assuming a semiconductor/insulator thickness of d_{sc} and d_{ins} the Poisson equation for such a system reads:

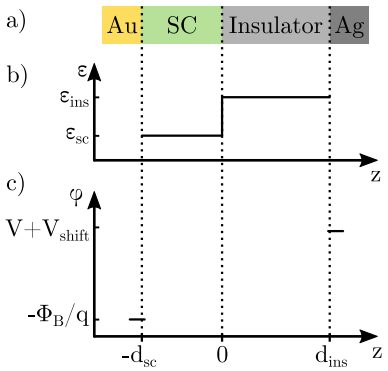

Figure 4.10: Sketch of the simulations layout. a) Sketch of the layers forming the MIS capacitor. b) Evolution of the dielectric constant. c) Boundary conditions for the potential $\varphi(z)$ at the semiconductor/source and insulator/gate interface. The text gives an explanation for the used notation.

$$-\frac{d}{dz}\left(\epsilon(z)\frac{d\varphi(z)}{dz}\right) = qp(\varphi(z)) \tag{4.3}$$

$$\varphi(-d_{sc}) = \frac{-\Phi_B}{q}; \quad \varphi(d_{ins}) = V + V_{shift} \tag{4.4}$$

with $p(\varphi(z))$ the density of holes and $\epsilon(z)$ the piecewise defined dielectric constant (see figure 4.10 for a sketch of the simulation):

$$\epsilon(z) = \begin{cases} \epsilon_{sc} & z \leq 0 \\ \epsilon_{ins} & z > 0 \end{cases} \tag{4.5}$$

The two boundary conditions at $z = -d_{sc}$ and $z = d_{ins}$ assume an injection barrier of height Φ_B at the semiconductor/source interface and an applied bias of V at the insulator/gate interface. V_{shift} accounts for the built-in potential and additional dipole moments, shifting the applied bias by a constant value. Let $\bar{\varphi}(z)$ be the solution to equation (4.3), then an additional voltage perturbation δV results in a perturbation of the potential in the form $\varphi(z) = \bar{\varphi}(z) + \delta\varphi(z)$. Neglecting second order terms, the differential equation for the potential perturbation $\delta\varphi$ reads:

$$-\frac{d}{dz}\left(\epsilon(z)\frac{d\delta\varphi(z)}{dz}\right) = q\left.\frac{dp}{d\varphi}\right|_{\varphi=\bar{\varphi}}\delta\varphi \tag{4.6}$$

$$\delta\varphi(-d_{sc}) = 0; \quad \delta\varphi(d_{ins}) = \delta V \tag{4.7}$$

$$\tag{4.8}$$

In the unperturbed case, the charge per unit area residing at the insulator/metal contact reads:

$$\bar{Q} = -\epsilon(z)\left.\frac{d\bar{\varphi}(z)}{dz}\right|_{z=d_{ins}} \tag{4.9}$$

This motivates the following expression for the perturbed case:

$$\bar{Q} + \delta Q = -\epsilon(z)\left.\frac{d\bar{\varphi}(z) + \delta\varphi(z)}{dz}\right|_{z=d_{ins}} \tag{4.10}$$

Solving equation (4.10) with equation (4.9) gives access to the additionally stored charge density δQ:

$$\delta Q = -\epsilon(z) \left. \frac{d\delta\varphi(z)}{dz} \right|_{z=d_{ins}} \tag{4.11}$$

The differential capacitance C is now simply the product of the capacitors active are A and δQ divided by the additional applied voltage δV:

$$C = A\frac{\delta Q}{\delta V}. \tag{4.12}$$

δV can be set to any value without loss of generality as long as it remains a small perturbation but will be set here to $\delta V = 1\,\mathrm{V}$ for convenience reasons. [64] The algorithm further requires an assumption about the functional dependence of the density of states in order to calculate $p(\varphi(z))$. In principle, different DOS forms can be used. To maintain comparison to the previously carried out investigations (BÄSSLER-model) a simple gaussian DOS of the following form is assumed:

$$g(E) = \frac{N_0}{\sigma\sqrt{2\pi}} \exp\left(-\frac{E^2}{2\sigma^2}\right) \tag{4.13}$$

where N_0 denotes the number of total states per unit volume. Then, the hole density is the integral of the fermi distributed occupation probability $f(E)$ times the density of states $g(E)$, reading:

$$p = \int_{-\infty}^{\infty} g(E + E_{HOMO}) f(E) dE \tag{4.14}$$

using the integration variable $\alpha = \frac{E+E_{HOMO}}{\sigma\sqrt{2}}$ this integral reads:

$$p(\varphi(z)) = \int_{-\infty}^{\infty} \frac{\frac{N_0}{\sqrt{\pi}} \exp(-\alpha^2)}{1 + \exp\left(\frac{\sqrt{2}\sigma\alpha - q\varphi(z)}{k_\mathrm{B}T}\right)} d\alpha \tag{4.15}$$

This integral and its derivative $\frac{dp}{d\varphi}$ can be calculated numerically as required in equation (4.3) and equation (4.6). Thus the approach of the algorithm is the following: First, the unperturbed potential distribution and hole density for a given applied bias V is calculated. Then, the unperturbed solution $\bar{\varphi}$ is used to calculated the potential perturbation $\delta\varphi$, followed by the calculation of the differential capacitance. Repeating these three steps for a number of different voltages gives a CV curve. In order to better fit experimental CV curves to the simulated ones an additional parallel voltage

Table 4.1: Standard parameters of the simulation.

Name	Value	Unit	Comment
σ	100	meV	DOS width
d_{sc}	40	nm	Semiconductor thickness
d_{ins}	350	nm	Insulator thickness
V_{shift}	0	V	Voltage shift
C_{fix}	0	pF	Parasitic capacitance
ϵ_{sc}	3.0	-	semicondcutor diel. const.
ϵ_{ins}	3.4	-	insulator diel. const.
A	2.4^{-5}	m^2	Capacitor area
Φ_B	0.1	eV	Injection barrier
N_0	1	nm^{-3}	volume density of states
T	293	K	Absolute temperature

independent capacitance C_{fix} was introduced, modelling various parasitic effects such as the capacitance of the used cables.

This approach and the transition from the depletion to the accumulation capacitance it describes can be best explained by looking at the centre of charge (COC) for holes. In strong accumulation it resides at the semiconductor/insulator interface while strong deplection leads to a capacitor devoid of charge carriers and the COC is located the metal/semiconductor interface. Depending on the location of the COC a different capacitance is measured. The closer the COC is to the insulator/semiconductor interface the higher is the measured capacitance. The variation of V_g and the resulting variation of $\varphi(z)$ can be understood to scan the density of states. At depletion voltages no charge carriers are injected as the HOMO level has not yet reached the Fermi energy. [7] Once the edge of the gaussian broadened HOMO level has reach the Fermi energy a limited number of charge carriers can be injected which accumulate at the semiconductor/insulator interface. In this state, the COC resides neither at the semiconductor/insulator nor at the metal/semiconductor interface but rather in the middle of the semiconducting layer. A strongly increasing DOS (low σ) thus leads to a fast transition in the CV plot and vice versa.

The standard parameters used in the simulation can be found in table 4.1. The parameters used are chosen to closely match the values used in the previous experiments. The dielectric constants for example were calculated using the well known formulas for plate capacitors and measurements of the layers thicknesses and the capacitor area. An injection barrier of Φ_B=0.1 eV was chosen to describe the ohmic behaviour seen in

[7] A quick reminder: E_f was set to zero and $\varphi(z) = E_{HOMO}/q$

the transistors. N_0 was set to $1\,\mathrm{nm}^{-3}$ under the assumption that the polymer P3HT exhibits roughly one state per nm^{-3}.

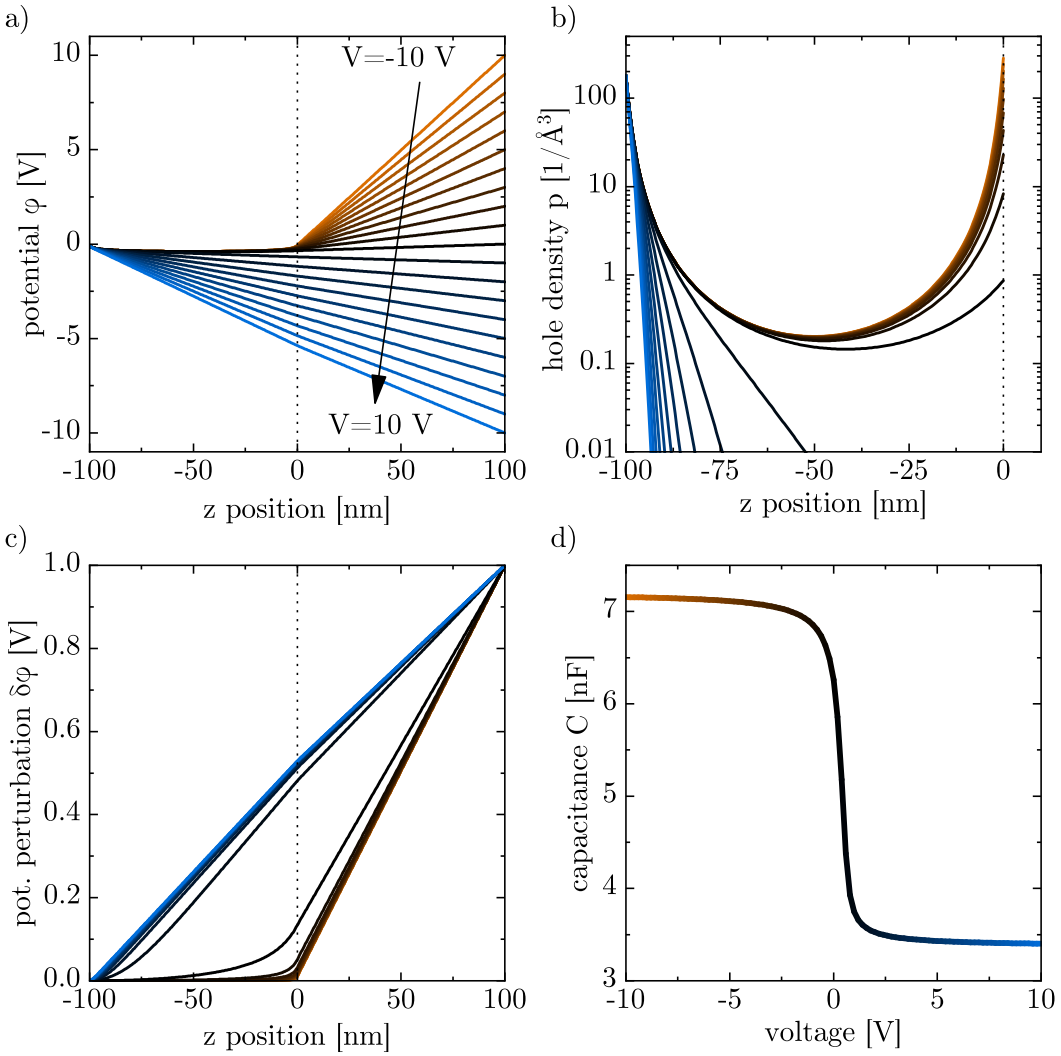

Figure 4.11: Results of an examplary CV simulation. a) Potential; b) hole density; c) potential perturbation and d) capacitance voltage curve of an exemplary simulation. The standard parameters from table 4.1 with the exception of identical semiconductor and insulator thicknesses of $d_{ins} = d_{sc} = 100\,\mathrm{nm}$ were used.

Simulations are carried out by computer code written in Matlab 2018b. Differential equations were solved using the built in solvers for boundary value problems `bvp5c` for which the second-order one dimensional equation was reduced to a two-dimensional first order problem. `bvp5c` is a finite-difference solver with dynamic step sizes. Fitting of results to experimental data was done using the function `fminsearch` designed for finding local minima in unconstrained multi-variable functions.

An exemplary output of the algorithm can be found in figure 4.11 in which the standard parameters with the exception of identical semiconductor and insulator thickness of $d_{sc} = d_{ins} = 100\,\mathrm{nm}$ were used for clarity reasons. At $V = -10\,\mathrm{V}$ the capacitor is operated in accumulation. The potential (figure 4.11a) in the semiconductor ($z \leq 0\,\mathrm{nm}$) is flat and increases linearly in the insulator layer ($z > 0\,\mathrm{nm}$). The hole density (b) is highest at the semiconductor/insulator interface at $z = 0$. Increasing the voltage towards zero decreases the amount of charge carriers accumulated at the interface. At $V = 0\,\mathrm{V}$ the situation abruptly changes and the semiconductor becomes depleted. Above $V = 0\,\mathrm{V}$ the hole density in the device strongly decreases and only a limited amount of charges at the source/semiconductor interface remain. Thus, the entirety of the potential drops linearly in both the semiconductor and insulator. The slightly different slopes are caused by the difference in dielectric constant in both layers. In accumulation the potential perturbation reads zero in the semiconducting layer while it increases linear (again with different slopes) in depletion. Calculating via $C(V) = A\frac{\delta Q(V)}{\delta V}$ results in the CV curve shown in figure 4.11d). In the accumulation regime a high capacitance can be seen while the it adopts much lower values in depletion.

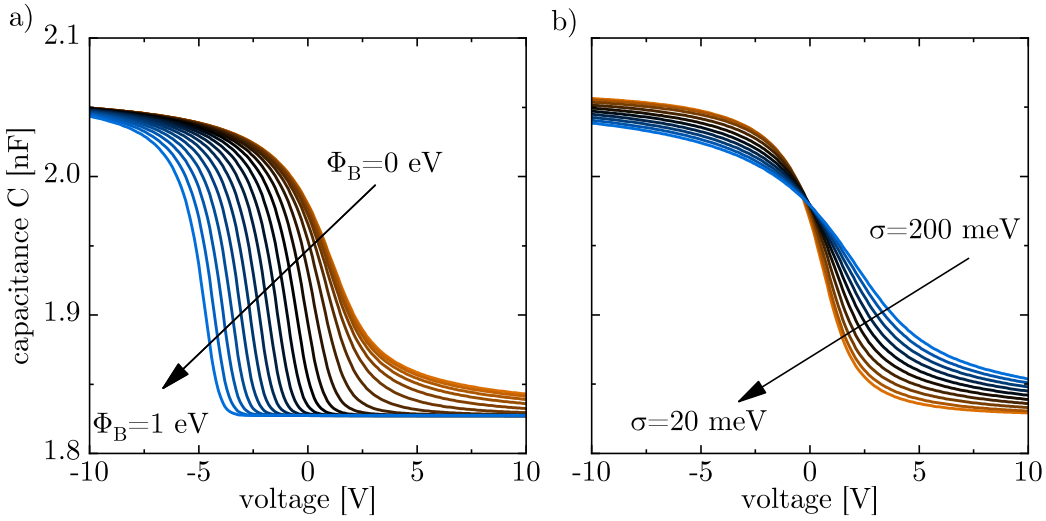

Figure 4.12: Influence of injection barrier (a) and DOS width (b) on the simulated CV curves. a) Small injection barriers ($0\,\mathrm{eV} \leq \Phi_B \leq 0.2\,\mathrm{eV}$) only weakly influence the shape of the CV curve. For intermediate barriers the steepness of the CV curve rapidly while higher barriers ($\Phi_B > 0.6\,\mathrm{eV}$) only lead to static shift of the CV curve. b) A decrease of σ on the other hand continuously sharpens the shape of the CV curve. With the exception of a variation in Φ_B and σ the standard parameters from table 4.1 were used.

Both Φ_B and σ critically influence the shape and steepness of a CV curve as can be seen from figure 4.12. Going from low to high injection barriers three regimes are discernible. Small injection barriers $0\,\mathrm{eV} \leq \Phi_B \leq 0.2\,\mathrm{eV}$ do not significantly influence the shape of the CV curve. Intermediate injection barriers ($0.2\,\mathrm{eV} < \Phi_B \leq 0.6\,\mathrm{eV}$) strongly increase the steepness of the CV curve altering its overall shape. High injection barriers of

$\Phi_B > 0.6\,\mathrm{eV}$ again do not alter the CV curves shape but induce a steady shift towards lower voltages which can be understood as a change in built-in potential. Decreasing σ on the other hand continuously changes the shape of the CV curve towards a sharper drop. For accurate extractions of σ from experimental CV curves it is thus important to investigate devices regime where the injection barrier does not alter the shape of the CV curve. Thus, devices with either no injection barrier or a very high injection barrier are best suited for this approach.

The influence of the combination of dielectric constant and film thickness of the semiconductor and insulator layer on the shape of the CV curves were investigated. To do this, the accumulation and depletion capacitance were kept constant, meaning that an increase of d_{ins}/d_{sc} was compensated by a decreasing $\epsilon_{ins}/\epsilon_{sc}$. It was found that the choice of dielectric constant and film thickness does not alter the shape of the CV curve significantly. [8]

The integrity and validity of the written code was validated twofold. First, the depletion and accumulation capacitance can be calculated through the formulas for plate capacitors. The accumulation capacitance is given by the insulators thickness, dielectric constant and area while the depletion capacitance can be calculated as the two capacitors in series. The analytically calculated values deviate by less then 1 % from the simulated values presented in figure 4.11. Additionally, the data presented by Maddalena et al. in his publication were treated with the here presented algorithm resulting in nearly identical values. Having understood the parameters influencing the shape of the CV curve and beeing able to predict experimental curves, measurements of real devices shall be treated with the algorithm next.

4.5.2 Fitting Experimental CV Curves

The here used fitting parameters are the insulators/semiconductor thickness d_{sc} and d_{ins}, the parasitic capacitance C_{fix}, a voltage shift V_{shift} and the DOS width σ. A two staged approach was chosen here to render the fit more robust and to exploit the unique traits for the used approach. First, the accumulation and depletion capacitance of the CV curve far away from the switching point were fitted to the experimental data. This was done by varying d_{sc}, d_{ins} and C_{fix} accordingly. Then the derivative of the CV curve $\frac{dC}{dV}$ – which is mostly independent to the three previously used parameters – was fitted to the experimental data over the whole range with V_{shift} and σ as free parameters. While V_{shift} shifts the whole curve along the voltage axis, preserving its shape, σ influences the steepness of the curve. This fitting cycle was repeated multiple times until sufficient overlap was achieved.

In a first step, the CV curve of a P3HT model system capacitor (see section 4.1 and figure 4.2 for CV curve) given the number **1** was analyzed. The CV curve recorded at 1 kHz well below the cut-off frequency of around 100 kHz was used where the accumulation capacitance fully reaches its maximum value. The fit of the algorithm to

[8] In the limit of very small film thicknesses the spacing of the mesh points has to be increased for accurate numerical calculations.

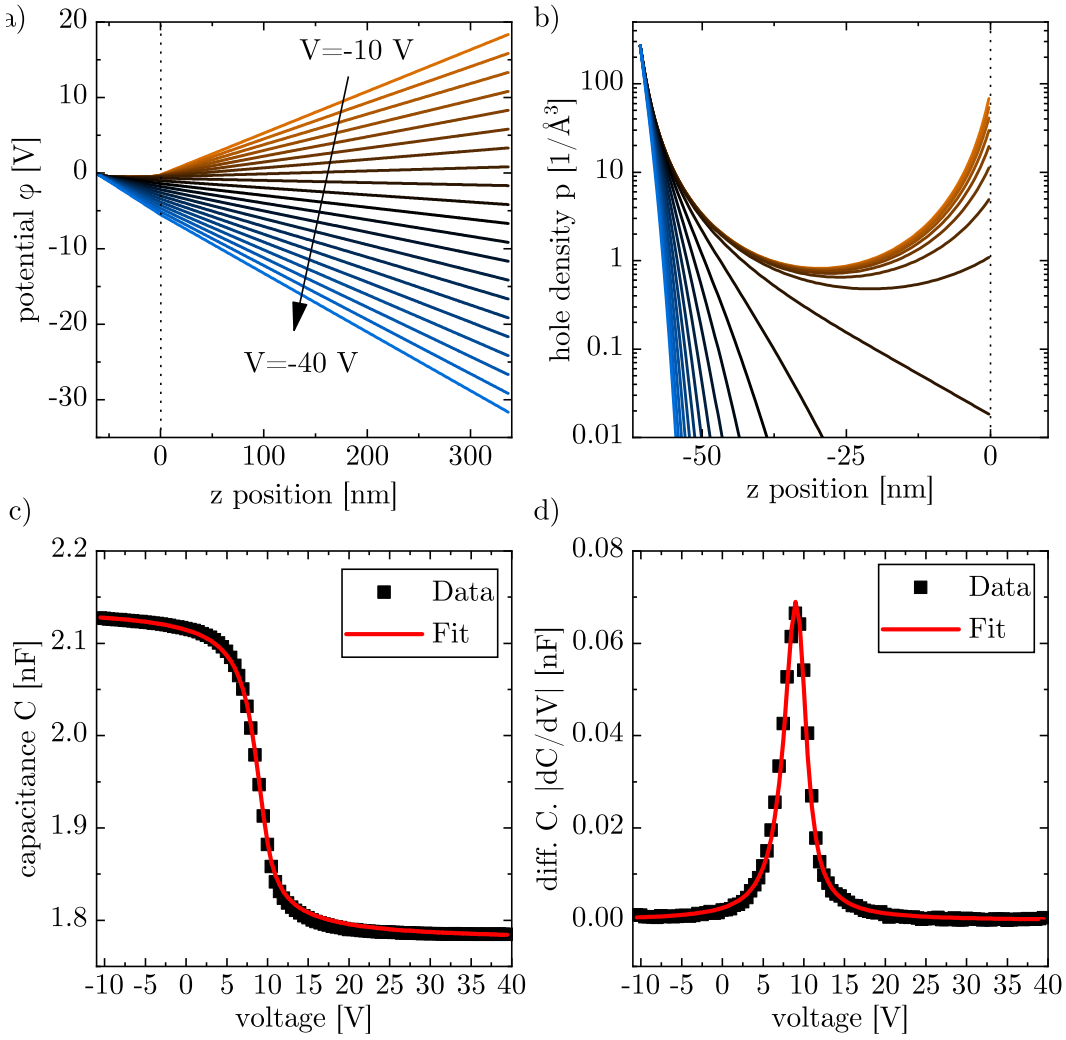

Figure 4.13: Fit of the simulation to experimental the CV curve of sample 1 at 1 kHz. a) Simulated potential distribution; b) hole density as a function of voltage. c) and d) show a comparison of the experimental CV and $\frac{dC}{dV}$ data and corresponding fit of the simulation. The standard input parameters were used. The resulting fit parameters can be found in table 4.2.

sample **1**'s recorded CV spectra can be found in figure 4.13. The algorithm is able to reproduce the experimentally measured data very well. The resulting fit parameters can be found in the second column of table 4.2. The film thicknesses of $d_{sc} = 59\,\text{nm}$ and $d_{ins} = 337\,\text{nm}$ are close to the experimentally measured values of 40 nm and 350 nm, respectively. The deviation can be explained by a slightly incorrect choice of dielectric constant and/or by experimental errors of the film thickness measurements. The obtained value for $\sigma_{CV} = 157\,\text{meV}$ on the other hand seems to be too large. The temperature dependent Cf measurements indicated $\sigma_{Cf} = (54 \pm 8)\,\text{meV}$ and Literature $\sigma_{lit.} = 98\,\text{meV}$ well below the here extracted value. This overestimation of σ might

Table 4.2: Fit results of different capacitor samples. The active area of the samples used are **1**: A = 24 mm^2; **2**: A = 7 mm^2; **3**: A = 4 mm^2. The number in brackets denotes the expected film thickness values. Sample **1** was fabricated from the layout shown in figure 4.1 whil **2** and **3** utilized the layout from figure 4.14.

Sample	**1**		**2**		**3**	
Freq. [kHz]	10	1	10	1	10	1
σ [meV]	106	157	156	243	236	298
d_{sc} [nm]	59 (40)	61 (40)	85 (80)	92 (80)	82 (80)	75 (80)
d_{ins} [nm]	337 (350)	337 (350)	247 (250)	242 (250)	235 (250)	230 (250)
V_{shift}[V]	-7.2	-7.8	-1.8	-2.3	-3.6	-3.7
C_{fix} [pF]	20	17	27	5	27	2

be the product of the used capacitor geometry. As already noted, the here used capacitor layout (see figure 4.1) allows the charge carriers to drift outside of the active area introducing an accumulation induced parasitic capacitance (AIPC). This effect is stronger for increasing negative bias and decreasing frequency (figure 4.4). Maddalena et al. commented on this effect and postulated in their publication that only devices with a significantly flat Cf curve in accumulation can be used. [64] They employed a sophisticated patterning approach to achieve devices with a flat Cf curve. The here presented unpatterned devices already show Cf curves similar to the characteristics of patterned devices depicted in their publication so patterning seemed to be unnecessary (the flat Cf curve is most likely the result of the comparably much bigger active area).

To further investigate the overestimated σ the simulation was fitted to data of the same capacitor recorded at 10 kHz where the device can still barely reach full accumulation but AIPC is expected to be reduced. To account for the lower dielectric constant at this higher frequency, ϵ_{ins} was reduced to 3.2. Again the fit matches the experimental measurement very well (see table 4.2). All fit parameter remain nearly unchained with the exception with a reduction of σ to 106 meV. This reduced σ indicates an influence of AIPC on the extracted values but further influences of dynamic effects of the σ cannot be excluded at frequencies close to f_c

If AIPC is indeed a factor which co-determines the extracted σ values, investigations into the device layout can further support this hypothesis. As the here presented capacitors are fabricated via shadow masks it is impossible to achieve full alignment of the two electrodes. Thus, the possibility of charge carrier drift outside of the active area is always given. As the charge carrier drift is an effect happening at the edges of the active area, we expect substrates with an increased area to perimeter ratio to be less impeded by this effect. This hypothesis was studied by fabricating capacitors with a different device layout (see figure 4.14). Sample **2** and **3** are two capacitors fabricated on the same substrate with active areas of 7 mm^2 and 4 mm^2, respectively. Although different thicknesses of the P3HT and Parylene-C layers were used, we expect these

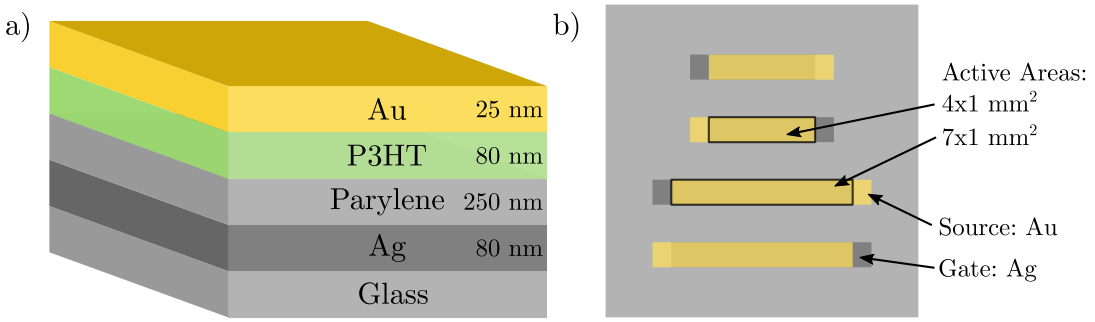

Figure 4.14: Layout used for capacitors featuring a reduced device area. a) Sketch of the layers tacks used in sample **2** and **3**. b) Top view of these capacitors. While the thickness of the respective layers was changed (in comparison to sample **1**) their materials stayed the same. The change in film thickness is not expected to change the fundamental charge carrier transport properties in any way.

devices to be comparable to the previously reported sample **1**.[9] Both devices exhibit device characteristics similar to the ones reported for samples **1**. The CV curves of these samples at 1 and 10 kHz were treated with the algorithm and the results can be found in table 4.2. Two clear trends are visible when comparing the DOS width σ. Significantly higher values are obtained for smaller active areas and frequencies. Both of these findings are another prove that AIPC is responsible for the changing σ.

The simplest model to account for AIPC is to simply assume that this charge carrier drift is increasing the active area of capacitor regardless of the voltage applied. This assumption is easy to implement and test as the capacitors active area is an input parameter of the simulation. Thus, the CV spectrum of **1** at 1 kHz was used as input data and the device area was varied. The results of such a simulation can be found in the appendix. While a change of the device area by up to $\pm 20\,\%$ is directly translated to a variation of the same magnitude of t_{sc}, t_{ins} and C_{fix}, σ and V_{shift} remain nearly unvaried. This behaviour is not surprising since t_{sc}, t_{ins} and C_{fix} ultimately change the position of the CV curve while σ and V_{shift} determine the shape of the CV curve and are fitted using the $\frac{dC}{dV_g}$ curve. Thus, a more sophisticated model has to be developed which will be done in the next chapter.

The here presented algorithm bears the promise of fast and easy access to σ from room temperature CV measurements. After detailed investigations into this approach these conclusions can be drawn: First, the extracted σ seems to be influenced by drift of charge carriers outside the active area (called here the AIPC effect). As a result largely different σ values are obtained for capacitors with different areas. This renders quantitative extractions of σ for samples with an unstructured semiconductor layer challenging. Structuring of solution processed organic semiconductors is a currently highly researched topic, generally requiring specially designed materials (see chapter 8) influencing their electrical properties. [85] As such, it would be desirable to gain access

[9] Of course the value of the accumulation and depletion capacitances (smaller area) and the cut-off frequency (thicker layers) changes change towards lower values.

to σ for unstructured semiconductor thin films as well. Thus, further description of the AIPC are needed so that unstructured samples can be treated with this algorithm. Another addition could introduce dynamic effects into the currently totally steady state simulation. This could enable the analysis of CV curves at 10 kHz where the charge carriers just barely reach the semiconductor/insulator interface and AIPC has a lower influence. Maddalena and coworkers have addressed another issue of their technique in a recent publication. [86] An uncertainty in the injection barrier introduces an uncertainty in σ in the present algorithm for intermediate injection barriers.[10] Their improved approach reduces this uncertainty and gives simultaneous access to the charge carrier mobility, injection barrier and density of states width but requires CV and Cf spectra of (still structured) capacitors in combination with OFET transfer measurements. [86]

4.6 Conclusion

This chapter evaluated different techniques for charge carrier transport measurements in organic MIS capacitors. First, a model system for all further investigations was established and charaterized in its room temperature operation. A mobility measurement technique for those devices put forward by Stallinga et al. based on cut-off frequency (f_c) measurement in Cf spectra was successfully validated two fold. Then, this technique was applied to measure the temperature dependent hole mobility in P3HT MIS capacitors. A description of these measurements through a Bässler-model gave access to the density states width as $\sigma_{Cf} = (54 \pm 8)\,\mathrm{meV}$. This same property was extracted from experimental CV curves through a sophisticated numerical algorithm as $\sigma_{CV} = 157\,\mathrm{meV}$. In comparison to the literature value of $\sigma_{lit.} = 98\,\mathrm{meV}$ (measured in OFETs and diodes) the temperature dependent Cf approach is found to slightly underestimate σ while the CV approach is found to overestimate σ. [87] It was found that the stronger the here employed capacitors are operated in accumulation the higher their measured capacitance is (see figure 4.4). This accumulation induced parasitic capacitance (AIPC) is caused by a drift of charge carriers outside of the capacitors active area. AIPC is attributed to be the underlying cause for overestimation of σ in the CV approach. Although both of the techniques used here still have room for improvement it was clearly shown that MIS-capacitor measurements can be a valuable addition for the characterisation of charge carrier transport in organic semiconductors. The here detrimental AIPC will be used in the next chapter in a constructive way to measure the charge carrier mobility in a novel and unimpeded fashion.

[10] Here devices are assumed to operate under no or only very little injection barrier where its influence on σ is small. Intermediate injection barriers on the other hand can strongly alter the apparent σ (see figure 4.12).

5 A Kelvin Probe Technique for Mobility Measurements

Several different techniques for charge carrier mobility measurements have been proposed all with different advantages and disadvantages (see section 2.1.2). Lateral charge carrier mobilities are commonly calculated through experimental transistor measurements in combination with their theoretical description in the form of the Shockley equation (see section 2.2.2) [3, 49, 88]. A disadvantage of transistor measurements is that the device operation can be hampered by injection barriers which are notoriously hard to quantify. Last chapters investigations into the density of states width σ were complicated through an extended drift of charge carriers outside of the capacitors active area. Here, this previously undesired effect will be used to measure the charge carriers mobility in a regime where injection barriers are less influential. The presented AC Kelvin-probe (ACKP) method utilizes a Kelvin-probe experiment to measure externally induced surface potential oscillations in MIS capacitors operated in accumulation. The propagation of these surface potential oscillations are described by a simple analytical model which shall be presented first. Then, the model will be applied to calculate the charge carrier mobilities in real devices. Finally, the ACKP method will be reviewed by finite element simulations to test for its applicability and accuracy. An additional modification of the proposed model is introduced to further increase the robustness of the presented approach.

This chapter is the result of a collaboration of several members of the research group Melzer. The presented model was established together with Christian Melzer. Its experimental verification was mainly carried out by Valeria Milotti in a co-supervised Master thesis where experimental guidance was provided. [89] This project was published in two peer-reviewed publications. [90, 91]

5.1 Modelling Externally Induced Surface Potential Oscillations

The low intrinsic charge carrier density makes organic semiconductors in their natural state bad conductors. The field-effect is responsible for the good charge transport in OFETs through the establishment of a low resistance accumulation zone at the semiconductor/insulator interface. Charge carriers injected at the source contact accumulate via the capacitive coupling to the gate electrode at this interface. The dynamics of channel formation can be investigated for example by Kelvin-probe, giving valuable insights

into the charge carrier transport properties of the semiconductors. [92] The channel formation was modelled on the basis of telegraphers equation by Burns in 1969. [93] This model can be used for lateral dark-injection transient measurements where a step voltage is applied to the source contact. Measuring the drift of the induced charge carrier package can give access to the charge carrier mobility. [51, 52] The arrival of the charge carrier package at a given position can either be detected directly via a read-out electrode or indirectly via a change in surface potential. An indirect measurement of the charge carriers can be carried out by a Kelvin-probe setup not interfering into the charge carrier transport (as opposed to a redout over a contact where an injection barrier can influence the measurement). A method put forward by Bürgi et al. [94] utilizes such a Kelvin-Probe setup where the lateral charge carrier mobility in OFETs can be measured independently of potential injection barriers. The proposed technique requires both a microscopic potential profile as well as a macroscopic current-voltage measurement rendering the method fairly complex.

5.1.1 Theoretical Description

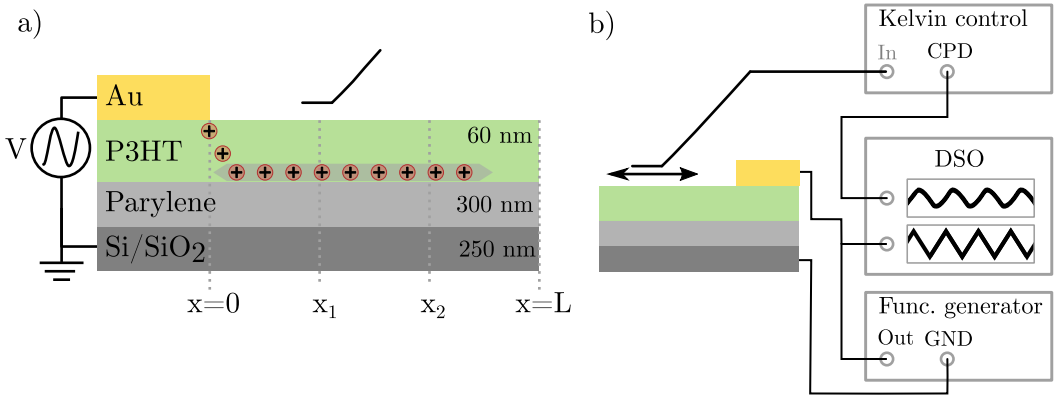

Figure 5.1: Sample layout (a) and experimental setup (b) of the proposed ACKP technique. a) The sample is in its essence a simple bottom gate MIS capacitor where only a small part of the semiconductor (P3HT) is covered by the top electrode. A perturbing bias induces charge carrier density oscillations propagating from the contact into the device. The resulting oscillating surface potential is measured at different positions using a Kelvin-probe. b) Sketch of the measurement setup consisting of a Kelvin-probe with control unit, a digital storage oscilloscope (DSO) and a function generator.

Here a novel method to measure the charge carrier transport properties relying on the application of a oscillating bias is presented. Consider an MIS-capacitor with exposed channel as presented in figure 5.1a. Application of a gate voltage leads to an accumulation of charge carriers at the semiconductor/insulator interface. In the limit of long times and no gate leakage the charge carrier will evenly accumulate over the hole semiconductor/insulator interface. The application of a small oscillating bias at the source contact leads to a periodic perturbation of the accumulated charge carrier density which

can be detected with a Kelvin-probe at different distances from the injecting contact. The amplitude of this charge carrier oscillation is damped for increasing distances from the injecting contact. The magnitude of this damping depends on the charge carriers transit time, ultimately determined by their mobility. Thus, the ACKP method is a transit time measurement where the movement of charge carriers are indirectly measured through Kelvin-probe.

Assume the limit of a purely one dimensional p-type semiconductor with a homogeneous doping density per unit length P_x placed on a insulator/gate stack with a capacitance per unit length of C_x. The semiconductor is in contact at $x = 0$ with a source electrode (see figure 5.1a). With the space and time dependent surface potential $\varphi(x,t)$ the charge per unit length is given by $\rho_x = C_x\varphi + qP_x$. The current equation in a drift-diffusion ansatz in the gradual channel approximation reads then: [93]

$$I = -\mu \underbrace{(C_x\varphi + qP_x)}_{\rho_x} \frac{\partial\varphi}{\partial x} - C_x D \frac{\partial\varphi}{\partial x}. \tag{5.1}$$

Here, I is the electrical current, μ_h the hole mobility and D the diffusion coefficient for holes. Based on the continuity of holes the following equation can be derived:

$$-\frac{\partial I}{\partial x} I = C_x \frac{\partial\varphi}{\partial t}. \tag{5.2}$$

Utilizing equation (5.1) and equation (5.2) a differential equation for the surface potential can be derived:

$$\frac{\partial\varphi}{\partial t} = \frac{\mu}{2}\frac{\partial^2}{\partial x^2}\left[\varphi\left(\varphi + \frac{2qP_x}{C_x} + \frac{2D}{\mu}\right)\right] \tag{5.3}$$

Assuming the Einstein relation $\frac{D}{\mu} = \frac{k_B T}{q}$ this equation can be reformulated to:

$$\frac{\partial\varphi}{\partial t} = \frac{\mu}{2}\frac{\partial^2}{\partial x^2}\left[\varphi\left(\varphi + \frac{2qP_x}{C_x} + \frac{2k_B T}{q}\right)\right] \tag{5.4}$$

with k_B the Boltzmann constant and T the absolute temperature. Up to this point no applied bias was assumed. Now a constant bias of magnitude V_0 with a small perturbation of $\nu(t)$ shall be applied between source and gate. V_0 shall be chosen in such a way that the device is operated under accumulation conditions. The externally applied bias of the form $V_0 + \nu(t)$ suggests a factorisation of the surface potential in the same form: $\varphi(x,t) = \Phi_0(x) + \Phi(x,t)$ with $\Phi_0(x)$ a time-independent part and $\Phi(x,t)$ a

time-dependent small perturbation. $\Phi(x,t)$ can be regarded as a small perturbation as long as the following equation is satisfied:

$$2\left(\Phi_0(x) + \frac{2qP_x}{C_x} + \frac{2k_Bt}{q}\right) \gg \Phi(x,t). \tag{5.5}$$

This equation states that either a strong bias has to be applied ($\Phi(x,t)$ dominates) or strong doping ($\frac{2qP_x}{C_x}\frac{2k_Bt}{q}$ dominates) has to prevail. Using this formula, equation (5.4) can be linearised to the following boundary value problem of $\Phi_0(x,t)$:

$$0 = \frac{\partial^2}{\partial x^2}\left(\Phi_0^2(x) + 2\Phi_0(x)V_{th}\right) \tag{5.6}$$

$$\Phi_0(0) = V_0; \quad \left.\frac{\partial\Phi_0}{\partial x}\right|_{x=L} = 0 \tag{5.7}$$

where a threshold voltage of conduction $V_{th} = -2qP_x/C_x - k_BT/q$ is introduced which accounts for the influence of doping and the diffusion potential. At $x = 0$ a DIRICHLET boundary condition with the applied bias of V_0 is assumed. It is further assumed that no carriers can exit the device at its end ($x = L$). As any gradient in potential would result in a current a NEUMANN boundary condition is assumed at $x = L$. The solution to equation (5.6) simply reads $\Phi_0(x) = V_0$ causing the DC current in the capacitor to read zero. The expression for $\Phi(x,t)$ from the linearized equation (5.4) reads

$$\frac{\partial\Phi(x,t)}{\partial t} = \frac{\mu}{2}\frac{\partial^2}{\partial x^2}\left[2\Phi(x,t)\left(\Phi_0(x) - V_{th}\right)\right]. \tag{5.8}$$

Using the constant DC solution of $\Phi_0(x) = V_0$ the equation can be transformed in Fourier space resulting in

$$-i\omega\tau\Phi(\hat{x},\omega) = \frac{\partial^2\Phi(\hat{x},\omega)}{\partial\hat{x}^2}. \tag{5.9}$$

Where the x-coordinate was normalized to $\hat{x} = x/L$ and the following definition of the transit time τ with the threshold voltage V_{th} was used:

$$\tau := \frac{L^2}{\mu\left(V_0 - V_{th}\right)} \tag{5.10}$$

Assuming boundary conditions which are similar to the time independent part

$$\Phi(0,\omega) = \nu(\omega); \qquad \left.\frac{\partial\Phi(\hat{x},\omega)}{\partial\hat{x}}\right|_{\hat{x}=1} = 0, \tag{5.11}$$

the solution of equation (5.9) is given by:

$$\Phi(\hat{x},\omega) = \nu(\omega)\underbrace{\frac{\cos\left(\sqrt{i\omega\tau}\,(1-\hat{x})\right)}{\cos\left(\sqrt{i\omega\tau}\right)}}_{R(\hat{x},\omega)}. \tag{5.12}$$

Thus, the frequency evolution of the surface potential is given by the Fourier transform of the perturbing bias $\nu(w)$ and a response function $R(\hat{x},\omega)$ which is independent of the nature of the applied bias. The time dependent surface potential can be calculated through a simple Fourier back-transformation of equation (5.12). The response function $R(\hat{x},\omega)$ is responsible for both the damping of the perturbations amplitude introduces a phase shift with respect to the applied bias. The evolution of the amplitude and phase shift for different $\hat{x}$ and $\omega\tau$ can be found in figure 5.2.

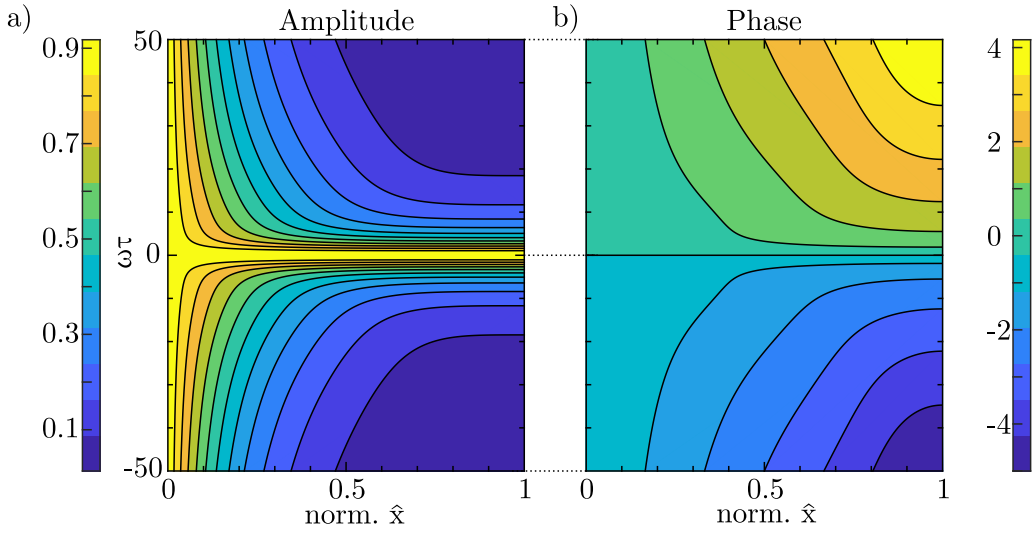

Figure 5.2: Amplitude (a) and phase (b) of the response function (see equation (5.12)**) as a function of normalized distance and** $\omega\tau$**.** For increasing distance from the injecting contact ($\hat{x} \to 1$) a decrease of the amplitude and an increase of phase is visible more pronounced for increasing $\omega\tau$.

For increasing $\hat{x}$ the amplitude decreases while the phase shift increases. For small $\omega\tau$ no or only a very small damping can be seen. Under the assumption of an harmonic perturbation of frequency ω, $\nu(\omega)$ takes a very simple form (see appendix) and large

$\omega\tau$ lead to an exponential decrease of the amplitude for increasing $\hat{x}$. The response function can in this case be approximated as

$$R(\hat{x},\omega) \approx \exp\left(\frac{i-1}{\sqrt{2}}\sqrt{\omega\tau}\hat{x}\right), \tag{5.13}$$

meaning that oscillations are exponentially damped in space with a characteristic length of $\sqrt{2/\omega\tau}$, expressing the length until which the the surface potential oscillations can propagate. Likewise, the phase shift is given by $\sqrt{\omega\tau/2}\hat{x}$, increasing with distance from the injecting contact and $\omega\tau$.

Due to the nature of the assumptions made, the model works best for devices either operated under strong accumulation or for strongly doped semiconductors. As the presented model is purely one dimensional it is best applied to devices with high aspect ratios. The charge carrier mobility can then be measured via a fit of the ACKP model to experimentally measured surface potential profiles. The definition of the transit time (equation (5.10)) gives access to the mobility and threshold voltage if a set of measurements with different V_0 are carried out.

5.1.2 Experimental Considerations

The ACKP method predicts the evolution of surface potentials via equation (5.12) for arbitrary applied biases. Externally induced surface potential oscillations are envisioned to be experimentally detected via a Kelvin-probe. An exemplary experimental setup can be found in figure 5.1b while further information Kelvin-probe techniques and additional experimental details can be found in section 3.4.1. As such, the shape and size of the Kelvin-probes tip can potentially influence the measured surface potentials. The here used Kelvin-probe setup utilizes a macroscopic circular tip of about 3 mm diameter operated under open circuit conditions (no current over the external circuit) assumed to be only weakly interacting with the MIS capacitor itself. [95, 96] Nevertheless, the rather large extension of the tip measures the surface potential in an extended area. The external Kelvin-current $I_{ext.}$ – adjusted to zero through the Kelvin-potential of the tip φ_K – can be expressed through an integral over the whole tip area A as

$$I_{ext.} = \frac{dC_K}{dt}\int_A \left(\varphi(t,x) - \varphi_K(t,x)\right) dA \stackrel{!}{=} 0. \tag{5.14}$$

Here $\frac{dC_K}{dt}$ is the time derivative of the tip-sample capacitance caused through the oscillation of the tip and $\varphi(t,x)$ the time and space dependent surface potential of the sample. Following the previously made assumption of $\varphi(x,t) = \Phi_0(x) + \Phi(x,t)$ and utilizing the solution of equation (5.6) ($\Phi_0(x) = V_0$) the Kelvin-potential satisfying equation (5.14) is

$$\varphi_K(t,x) = V_0 + \frac{1}{A}\int_A \Phi(t,x)dA. \tag{5.15}$$

Converting this equation into Fourier space and utilizing equation (5.12) the integration over a circular tip of radius r can be executed, resulting in the following Kelvin-potential:

$$\varphi_K(\omega,\hat{x}) = \sqrt{2\pi}V_0\delta(\omega) + \Phi(\omega,\hat{x})\sum_{k=0}^{\infty}\frac{1}{\Gamma(k+2)}\frac{z^k}{k!} \tag{5.16}$$

with $\hat{x}$ the normalized position of the tips center, $\hat{r}$ the normalized tip radius, δ the delta function, Γ the gamma function and $z = -1/4i\hat{r}^2\omega\tau$. Again, the time-domain behaviour is accessible through an inverse Fourier transform. Thus, the measured Kelvin-potential strongly deviates from the actual surface potential if the surface potential strongly varies within the extension of the tip. In this fashion a smaller tip leads to a smaller error, in the case of $\hat{r} = 0$ the sum in equation (5.16) reads one and the surface potential is accurately measured. Experimentally, higher currents $I_{ext.}$ caused through a higher area tip increases a setups energetic resolution and robustness rendering very small area tips experimentally not viable. Form figure 5.2 it becomes apparent that low frequencies lead to small surface potential curvatures. Furthermore, the finite response time of Kelvin-Probe setups (here 0.4 s) makes high frequency measurements impossible. Thus, experimental measurements will be carried out at small frequencies, decreasing the error caused through the non-zero tip area. Based on the experimental parameters chosen below the maximum deviation of the surface potential introduced through the non-zero area tip is calculated as 0.6 % and can thus be neglected.

The application window of the ACKP method is governed by a combination of different experimental factors and the characteristic time scale of charge carrier transport (the transit time) $\tau = \frac{L^2}{\mu(V_0 - V_{th})}$. Measurable surface potential variations across the length of the MIS-capacitor are a prerequisite for the ACKP method. Assuming an harmonic bias, the charateristic length of surface potential oscillation damping is $\sqrt{2/\omega\tau}$ (see equation (5.13)). In order to gain a set amount of damping (e.g. 50 %) over the whole length of the device high mobility semiconductors would either need high frequencies or long device (and vice versa for low mobilities). Both very long and very short channels pose experimental challenges due to the finite leake resistance of the available dielectrics and the finit-size of the tip, respectively. Furthermore, the use of a high frequency bias is prohibited through the limited response-speed of the Kelvin-Probe setup. Thus, the ACKP method is best applied for modest mobility semiconductors where $\omega\tau$ is within the experimental accessible region. Having proposed a novel method to measure the charge carrier mobility via surface potential measurements, this approach was experimentally verified next.

5.2 Experimental Verification

For the experimental verification devices optimized for the ACKP method were built whose layout can be found in figure 5.1a. A double layer dielectric consisting of a 250 nm SiO_2 and a 300 nm thick layer of Parylene was used to decrease the gate leakage and prevent trap states common at the SiO_2 interface. A 60 nm thick layer of P3HT was used as semiconductor, annealed at 110 °C. Gold and Silver were used as electrode materials. Three MIS structure were fabricated per substrates and were confined to an area of 5 mm width and 15 mm length. The devices were encapsulated by an additional layer of Parylene-C (310 nm) to prevent over doping of the P3HT layer through ambient oxygen. Due to the insulating properties of Parylene-C this additional layer is completely transparent for the Kelvin-probe measurements which were done a home-made setup (see section 3.4.1 for more details). V_{AC} and V_{DC} were applied via a HM8150 programmable function generator, while the output of the Kelvin setup was recorded using a DSO1012A digital oscilloscope. The homogeneity of the fabricated devices were tested with optical microscopy and Kelvin-probe measurements. It was found that the application of a constant DC bias (8 V) between source and gate commonly led to a loss of less then 0.2 V in surface potential along the entire length of the device.[1] Due to the fact that Kelvin-probe measurements may be impeded by work function differences the CPD was arbitrarily set to zero for no applied bias to eliminate influences for subsequent surface potential investigations. A total of 18 samples were investigated fabricated in three batches. The four best devices were used for in-depth data analysis. A triangular applied bias was chosen as it posses a relatively simple Fourier transform (see appendix) and is rich in sharp edges, optimal to visualize the occurring change in surface potential shape. The model describing the surface potential oscillations at different spatial coordinates can then by described by three variables: the magnitude of the applied DC and AC bias as well as the transit time of the charge carriers.[2]

[1] In the case of only a constant DC bias a constant surface potential is to be expected. The loss in surface potential can be attributed to a gate leakage.

[2] The period length of oscillation is another parameter which was here set to be identical to period length of the applied bias.

5.2.1 Mobility Extraction

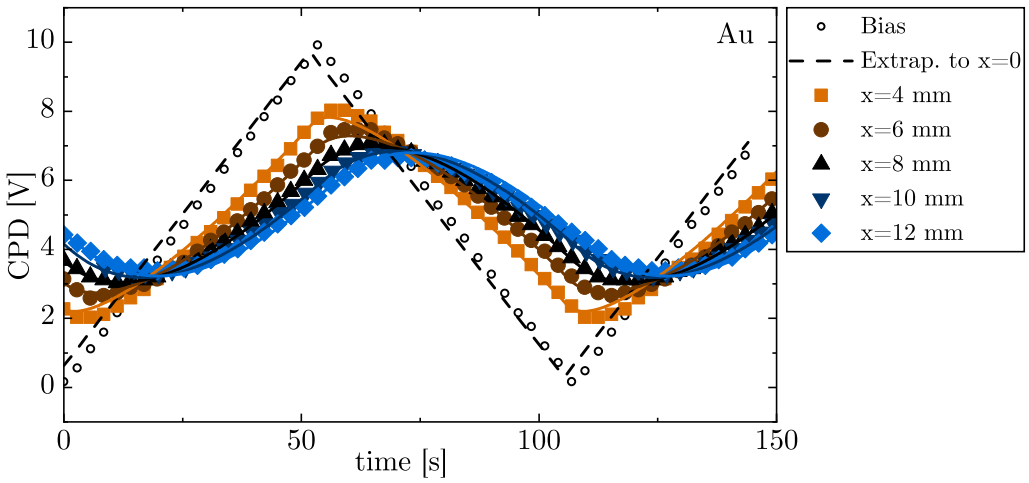

Figure 5.3: Measured surface potential oscillations and fit of ACKP model: Gold contacts. Measured surface potentials (symbols) and fit of the ACKP model at different distances from the injecting contact (solid lines). The fit has been carried out for all distances simultaneously. An extrapolation of the model towards $x = 0$ (dashed line) reproduces the applied bias hinting towards ohmic contact behaviour.

First investigations were carried out using samples with an injecting contact made out of gold. Identical DC and AC bias of $V_0 = V_{AC} = 5\,\mathrm{V}$ were applied to the injecting contact. Due to the strong background doping of P3HT the small signal condition of the AC voltage is still met. [65, 97] As the measurement range of the used Kelvin-probe setup is limited to 10 V higher voltages could not be chosen. The given response speed is much smaller then the chosen period length of $P = 107\,\mathrm{s}$. An example of a typical ACKP measurement is shown in figure 5.3. For increasing distances from the edge of the injecting contact two clear trends are visible. First the amplitude of the surface potential oscillations decrease and secondly, the signal is stronger phase shifted with respect to the applied bias. The form of the oscillations changes for distances further away from the contact. The solid lines represent a simultaneous fit of the proposed model to the measurements taken at the different x. The model parametrized by only the DC/AC bias and the transit time describes the experimental data very well. The DC and AC biases take values very close to their experimental inputs with $(5.0 \pm 0.2)\,\mathrm{V}$ and $(4.7 \pm 0.1)\,\mathrm{V}$, respectively. The errors are a propagation of the fitting errors and measurement uncertainties. The transit time $\tau = (77 \pm 1)\,\mathrm{s}$ is a measure of the charge transport properties of the semiconductor.

Through the definition of $\tau = \frac{L^2}{\mu(V_0 - V_{th})}$ the charge carrier mobility can be calculated if τ is measured for different V_0. The results of such a measurement can be found in figure 5.4 for a single device. A carrier mobility of $(1.6 \pm 0.4) \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and a threshold voltage of $(16 \pm 4)\,\mathrm{V}$ was extracted. On average over more devices, the mobility is $\mu = (2.3 \pm 0.2) \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ with a threshold voltage of $V_{th} = (15.7 \pm 0.3)\,\mathrm{V}$.

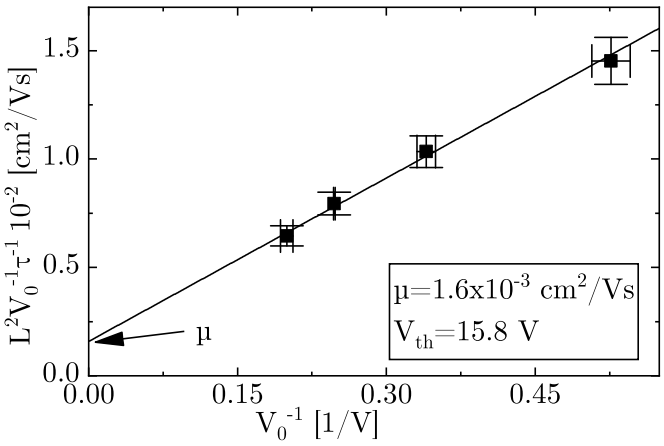

Figure 5.4: Mobility and threshold voltage calculation through multiple ACKP measurements. Plot of $L^2/(\tau V_0)$ against V_0^{-1} for different V_0. A fit to hese data points with the definition of the transit time $\tau = L^2/(\mu(V_0 - V_{th}))$ (soldi line) allows the calculation of $\mu = (2.3 \pm 0.2) \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $V_{th} = (15.7 \pm 0.3)\,\mathrm{V}$. V_0 and τ were extracted from fits of the ACKP model to experimental data (Au contacts, see e.g. figure 5.3).

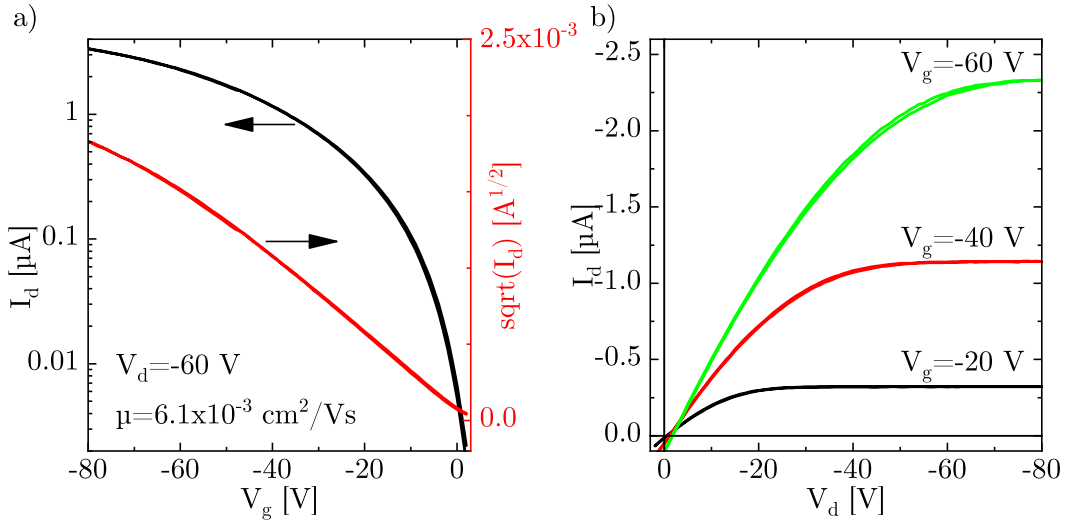

Figure 5.5: Transfer (a) and output charateristic (b) of an exemplary P3HT transistor. An identical layerstack as the MIS capacitors (see figure 5.1) for the ACKP measurements was used.

For comparison reasons the charge carrier mobility was measured using OFETs as a complementary method. This approach is viable as the transport limiting length scales in spin-coated films of P3HT are in the nanometer domain (or below) due to their tendency to form amorphous or nanocristalline domains. [98] Thus the shorter channel of transistors can be compared to the long channel ACKP measurements. Transistors

with identical layerstack (W/L=6 mm/200 µm) to the previous fabricated ACKP devices were fabricated. The additional encapsulation layer was omitted as the transistors were measured inside a nitrogen fillged glovebox. The transfer and output charateristic of such a transistors can be found in figure 5.5. The average field effect mobilities measured over 15 devices are $(6.1 \pm 0.2) \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ with threshold voltages of $(3 \pm 2)\,\mathrm{V}$. The here measured transistor mobilities are slightly higher then the ACKP mobilities. P3HT is known to exhibit an increased hole mobility for increasing hole density. [82] As OFETs and MIS capacitors are operated at different hole densities the higher charge carrier density in transistors is most likely originating from this effect. The threshold voltages extracted by ACKP are in the contrary much higher in comparison to the transistor data. This effect can be explained by a difference in doping. While the ACKP devices show clear signs of strong doping the measured transistors indicate only weak doping. [99, 100] The difference in doping can be attributed to a suboptimal encapsulation of the devices via the additional encapsulation layer. Nevertheless the here presented ACKP method is very well applicable to estimate the charge transport properties in low mobility semiconductors.

5.2.2 Influence of Contact Material

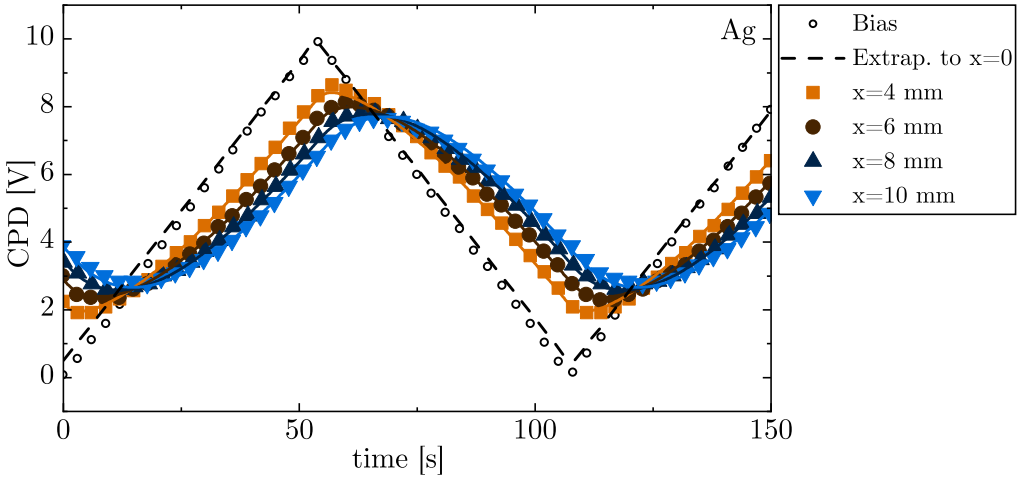

Figure 5.6: Measured surface potential oscillations and fit of the model: Silver contacts. Experimentally measured surface potentials (symbols) and fit of the ACKP model at different distances from the injecting contact (solid lines). An extrapolation of the model towards $x = 0$ (dashed line) reproduces the applied bias indicating a low influence of possible contact phenomena.

Extrapolating the model shown in figure 5.3 to $x = 0$ gives access to the surface potential directly under the contact, otherwise not experimentally accessible. This extrapolation closely matches the applied bias suggesting that no significant injection barrier reduces the applied potential, seeming plausible by the interface energetics between Gold and P3HT. [101] Devices with a silver electrode exhibit the same behaviour as the previously measured gold devices in ACKP measurements as can bee seen from figure 5.6. This

behaviour is somewhat counter-intuitive as the different work function of silver and gold suggest a different contact formation. The contact between silver and P3HT was reported both to be ohmic or to be subjected to a significant injection barrier. [101, 102] Here the low frequency chosen results in low current and thus a low influence of the injection barrier no matter weather it is indeed ohmic or injection limited which are common occurences in devices such as OFETs or diodes. The current per width flowing in the ACKP experiment is given by

$$I_c = \frac{C_A L}{\tau} \frac{\partial \Phi(\omega, \hat{x})}{\partial \hat{x}} \tag{5.17}$$

with C_A the areal capacitance of the insulator. In the limit of an harmonic oscillation with large $\omega\tau$ the current amplitude at the contact reads $C_A L \nu_0 \sqrt{\omega/\tau}$. For the here used triangular bias in combination with a period length of 107 s a current amplitude of $10 \times 10^{-7}\,\mathrm{A\,m^{-1}}$ can be estimated, a value substantially lower then what is found in transistors at the same charging with $10 \times 10^{-5}\,\mathrm{A\,m^{-1}}$. The much lower currents flowing over the contacts explain why the bias is reproduced irrespective of the contact material used. Thus, the here presented ACKP method can be used to probe the charge carrier transport at biases usually used for transistor operation but seems to be much more insensitive to contact effects due to the lower currents. We will see later that the method can be applied to extract μ fully independent of he injection barrier. To further investigate the validity of the ACKP method finite-element simulations were carried out allowing investigations into areas with complicated or no experimental access.

5.3 Simulations

Further validation of the ACKP method was done through two-dimensional time-dependent drift-diffusion simulations using the software COMSOL Multiphysics©. A two-dimensional semiconducting layer of 50 nm height and 6 µm length with bipolar transport was studied. A reduced device length was simulated to decrease the otherwise very high aspect ratio of the thin-film, slowing down the stabilization of the simulation. The hole and electron mobilities were decreased likewise to values of $\mu_h = 6.5 \times 10^{-10}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $\mu_e = 3.5 \times 10^{-10}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to keep the transit time close to the experimentally observed values. A substantially larger hole mobility was chosen in order to express the dominating hole transport. Lengevin recombination between electron and holes was included into the simulation. The organic semiconductor is further modeled by its HOMO, LUMO and effective density of states given by 5 eV, 3 eV and $1\,\mathrm{nm^{-3}}$, respectively. The transport of charges was described using time dependent drift-diffusion of electron and holes, complemented by the respective time-dependent continuity equations. The interaction to the gate electrode was modelled by placing the semiconductor on a metal/insulator stack consisting of a 4.9 eV work function metal followed by a 210 nm thick insulating layer with dielectric constant of $\epsilon_{ins} = 3.9$. A 1 µm wide contact was placed at the edge of the semiconductor to allow

Table 5.1: Standard parameters of the ACKP simulations. The parameters were chosen to closely match the experimental parameters.

Name	Value	Unit	Comment
L	6	µm	Length of device
L_c	1	µm	Length of contact
d_{sc}	50	nm	Semiconductor thickness
d_{ins}	210	nm	Insulator thickness
$HOMO$	5	eV	HOMO semiconductor
$LUMO$	3	eV	LUMO semiconductor
W_s	4.9	eV	Source workfunction
W_g	4.9	eV	Gate workfunction
μ_h	6.5×10^{-10}	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$	Hole mobility
μ_e	3.5×10^{-13}	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$	Electron mobility
ϵ_{sc}	3	-	Semiconductor diel. constant
ϵ_{ins}	3.9	-	Insulator diel. constant
V_0	15	V	DC bias
V_{AC}	2	V	AC bias
P	25	s	Period length
T	293	K	Absolute temperature

charge carrier injection. The contacts work function was set to 4.9 eV, favouring hole injection into the close lying HOMO level of the semiconductor. Identical work functions of the gate and source contacts were chosen to prevent the formation of a built-in potential. Electron and hole injection was modelled via thermionic emission, assuming an effective Richardson constant of $120\,\mathrm{A\,K^{-2}\,cm^{-2}}$ describing injection into vacuum. The device boundaries were set to be free of electric fields. A further overview of the standard parameters used can be found in table 5.1.

The simulations carried out were set to closely match the experimental procedures. As the experiments were carried out in highly doped devices the effective applied DC bias was not the applied bias of $V = 5\,\mathrm{V}$ but instead $V_{eff} = 5\,\mathrm{V} + V_{th} \approx 20\,\mathrm{V}$. As the simulation assumes no threshold voltages a triangular bias with $V_0 = 15\,\mathrm{V}$ and $V_{AC} = 2\,\mathrm{V}$ was applied, which results in an expected transit time of $\tau_i = L^2/\mu V_0 = 25.64\,\mathrm{s}$. The period of oscillation was chosen to be $P = 25\,\mathrm{s}$. First, an initial steady-state solution of the lowest applied bias of $V_0 - V_{AC}$ was calculated, used in the second step as a initial values for the time-dependent simulations. The time-dependent simulations were calculated until a quasi-steady-state has been reached. Only swung in surface potential

oscillations have been used for analysis purposes. The internal electrical potential are used to calculate the surface potential $\Phi(x,t)$ at increasing distances ($\hat{x} = x/L$=0.26; 0.4; 0.53; 0.67 and 0.8) from the injecting contacts. The proposed ACKP model is then fitted simultaneously for all values of x to these simulated surface potential oscillations. The fit parameters used are – as before – the transit time τ, the DC/AC part of the applied voltage Φ_0/Φ_{AC} in combination with a newly intruded phase shift Δt, describing a contact induced phase shift between external stimulus and the response of the system. The value of the used fit parameters can then be compared to the simulations input values of τ_i, V_0 and V_{AC} to evaluate the models validity for a range of simulated conditions.

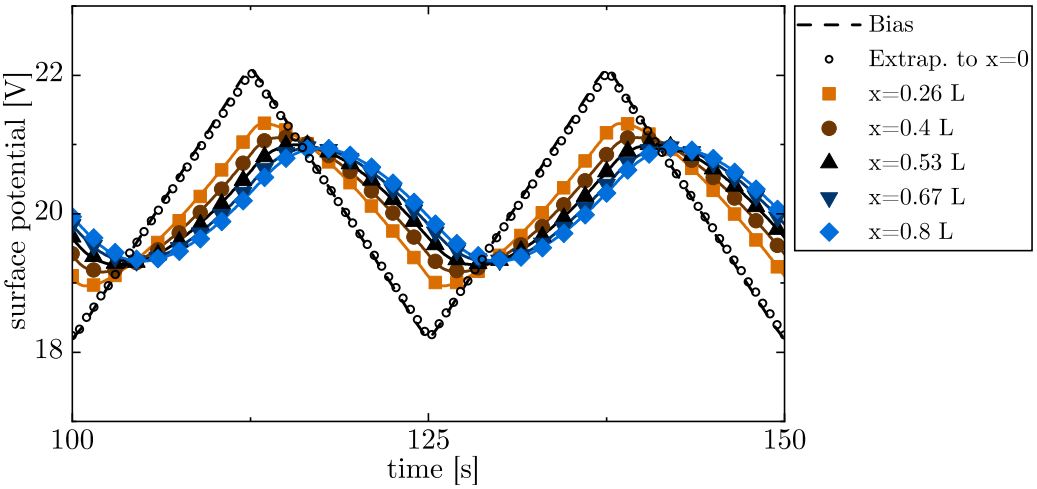

Figure 5.7: Simulated surface potential oscillations and fit of the ACKP model. The simulated surface potentials (symbols) closely matches the ACKP model (solid lines) simultaneously fitted for all x to the simulated data. Extrapolating towards $x = 0$ (dashed line) results in the applied bias. The standard parameters of table 5.1 were used.

Figure 5.7 shows the results of an exemplary simulation carried out using the standard parameters shown in table 5.1. No traps or doping was introduced and the energetic landscape at the injecting contact results in ohmic injection behaviour for holes. The good fit of the ACKP model to the simulated surface potential oscillations indicates the proposed model to be a good description of the simulated results. The models assumptions such as the gradual channel approximation are thus supported by the presented data. Charge carrier diffusion or the transport of electrons seem to have no relevance for the description of the underlying process. The extracted fit parameters thus very closely match the simulations input parameters with $\Phi_0 = 15.04\,\mathrm{V}$, $\Phi_{AC} = 1.93\,\mathrm{V}$ and $\tau = 25.88\,\mathrm{s}$. The extracted phase shift is $\Delta t = -0.06\,\mathrm{s}$, also close to the expected value of 0 s. Extrapolating the model with these obtained parameters to $x = 0$ perfectly reproduces the applied bias indicating no injection barriers. This behaviour was already expected based on the parameters used in the simulation.

To further test the rigidity of the proposed model various input parameters of the simulation were tested via a subsequent fit of the ACKP model to the generated results. Here the discussion of the results is limited to the transit time as it possess the highest experimental weight by granting access to the charge carrier mobility. The three remaining fit parameters generally follow very closely their expected values. Deviations from this behaviour will be noted on an individual basis and the full datasets can be found in the appendix.

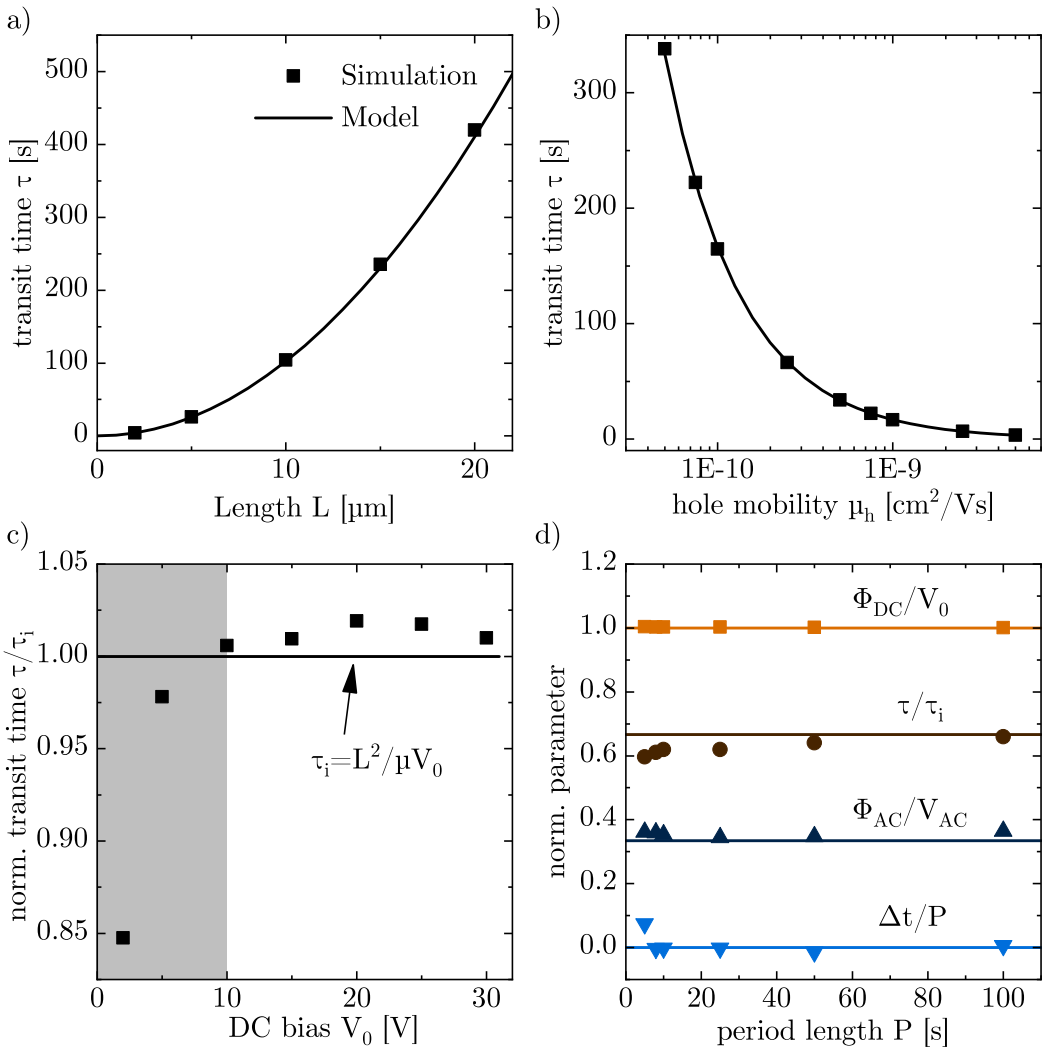

Figure 5.8: Results of the simulation for a variation of various input parameters. The ACKP model accuretly precits the behaviour of transit time for increasing device length (a) and hole mobility (b). A low DC bias (V_0<10 V) violates the models assumptions and leads to deviations between the extracted transit time and its expected value (c). A variation of the period length (d) has no only a very small influence. Lines/symbols shifted for clarity reasons in (d). The standard parameters of table 5.1 were used.

First, the influences of the experimental setup such as device layout and applied voltages are tested (see appendix for full data). The ACKP model predicts a quadratic relationship between transit time and device length which can be perfectly reproduced through simulations (see figure 5.8a). The definition of the transit time further predicts a charge carrier mobility dependence of $\tau \propto \mu_h^{-1}$, clearly reproduced by the simulation as can be seen from figure 5.8b. By contrast, the electron mobility has no influence on the simulation. Reducing the aspect ratio on the other hand through an increase in semiconductor thickness ($d_{sc}/L \gg 0.1\,\mu m/5\,\mu m$) increases the contact resistance to such an extend that the proposed model fails. Likewise, if the applied AC voltages is not a small perturbation in comparison to V_0 the model fails as well. Figure 5.8c shows the normalized transit time τ/τ_i for increasing DC bias. For low DC biases, $V_0 \approx V_{AC}$ the model fails and the expected transit time clearly deviates from the obtained values. The opposite approach of increasing the AC part until $V_0 \approx V_{AC}$ yields the same result. Figure 5.8d finally shows investigations into the period length P. Low period lengths result in a small deviation from the expected values while longer values lead to accurate results. Having tested these simple dependencies the influence of trap states is investigated next.

5.3.1 Trap States

The occurance of charge carrier traps in organic semiconductors is very common, mainly influencing the charge carrier properties in negative ways. [79, 103, 104] As such, the very common form of charge carrier trapping at the semiconductor/insulator interface will be invesitgated in detail here. [105] Trapping is introduced through additional mono-energetic trap states at energy E_{trap} above the HOMO level inside the band gap, equally distributed along the semiconductor interface with varying density. Depending on the distance of the trap level both shallow (E_{trap}=0.05 eV) and deep traps (E_{trap}=0.3 eV) are investigated. Figure 5.9 shows the results of simulations for both trap depths. All simulation parameters apart of the shown transit time remained constant. For increasing trap density the transit time strongly increases, where a higher density of lower energy traps can be better tolerated. At very high trap densities the model fails to predict the shape of the surface potential oscillation and thus cannot be applied any further.

The influence of traps on device characteristics is most commonly described through the introduction of a threshold Voltage V_{th} as it was already done above. Here it is most convenient to express the threshold voltage in the following way:

$$V_{th} = \frac{-q\bar{p_t}}{C_A} \tag{5.18}$$

where C_A stands for the areal capacitance of the metal/insulator/semiconductor system and $\bar{p_t}$ the areal density of trapped charges. [106] The transit time then takes the following form

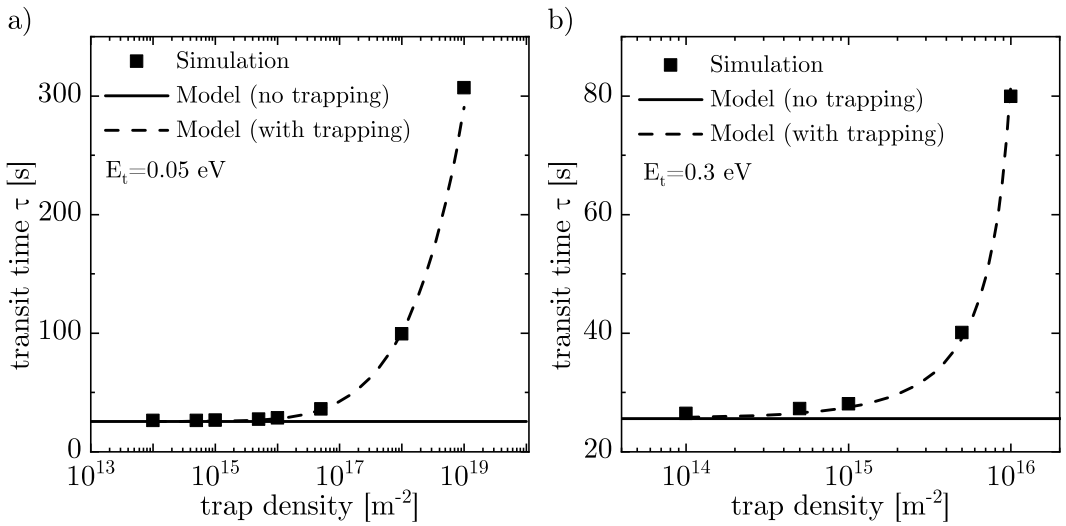

Figure 5.9: Extracted (symbols) and predicted transit times (lines) as a function of trap density for shallow (a) and deep traps (b). High trap densities lead to strong deviations of the simulated transit times from the models predictions (solid line). Accurate predictions can be recovered by introducing trapping into the model (dashed line, see equation (5.19)). Deeper traps lead to a faster increase in transit time as opposed to more shallow traps. The standard parameters of table 5.1 with the exception of a longer period length of P=107 s were used.

$$\tau = \frac{L^2}{\mu\left(\Phi_0 + \frac{-q\bar{p}_t}{C_A}\right)} \tag{5.19}$$

The density of trap states g_t can be assumed to adopt the following form:

$$g_t = \bar{N}_t \delta(E - E_t)\delta(z). \tag{5.20}$$

with N_t the density of areal traps, δ the dirac delta function, E_t the trap energy and z the spatial coordinate along the layer normal. Then the density of trapped holes is given by:

$$p_t(z) = \int_{-\infty}^{\infty} \bar{N}_t \delta(E - E_t)\delta(z)(1 - f(E)dE. \tag{5.21}$$

Executing this integral leads to:

$$p_t(z) = \bar{N_t}\left[1 + \exp\left(\frac{E_f(z) + E_t}{k_B T}\right)\right]^{-1} \delta(z) \tag{5.22}$$

with E_F the Fermi energy, k_B the Boltzmann constant and T the temperature. The free charge carrier density is given by $p = N_V \exp(-E_F/k_B T)$ giving rise to the following formulation for $p_t(z)$

$$p_t(z) = \bar{N_t}\left[1 + \frac{N_V}{p(z)} \exp\left(-\frac{E_t}{k_B T}\right)\right]^{-1} \delta(z) \tag{5.23}$$

where N_V stands for semiconductors effective density of states. An integration over the whole thickness of the semiconductor yield the areal trap density

$$\bar{p_t} = \bar{N_t}\left[1 + \frac{N_V}{p(0)} \exp\left(-\frac{E_t}{k_B T}\right)\right]^{-1} \tag{5.24}$$

in which the volume density of free holes at the semiconductor/insulator interface p(0) is expressed through the areal density of free carriers $\bar{p}$ as

$$p(0) = \frac{q^2 \bar{p}}{2 k_B T \epsilon_0 \epsilon_{sc}} \tag{5.25}$$

with ϵ_0 the permittivity of vacuum and ϵ_{sc} the semiconductors dielectric constant. [106] The total areal charge density under steady state conditions $q(\bar{p} + \bar{p_t}) = C_A \Phi_0$ is determined by the dielectrics capacitance and the applied voltage. [106] Using this equation the areal density of trapped charges can be determined via equation (5.24) needed for the calculation of the desired threshold voltage from equation (5.18). The transit time is increased for larger trap densities as fewer carriers are effectively free for transport. Through an increase in trap depth the thermal release of charge carriers is hindered rendering the charge carrier trapping more efficient. Modifying the model via the above described description of trapping fully describes the simulated data as can be seen from figure 5.9.

5.3.2 Doping

Charge transfer doping is another common occurrence in the field of organic electronics where dopants are either deliberatly introduced or result from external factors (e.g. ambient conditions). [60, 107] In the experimental investigations for example doping through ambient oxygen was assumed to explain the strongly positive threshold voltage

observed in the MIS devices but not the OFETs (see figure 5.4). Spatial homogeneous volume doping results in additional free charge carriers but leave the other charge transfer properties such as the mobility unchanged.

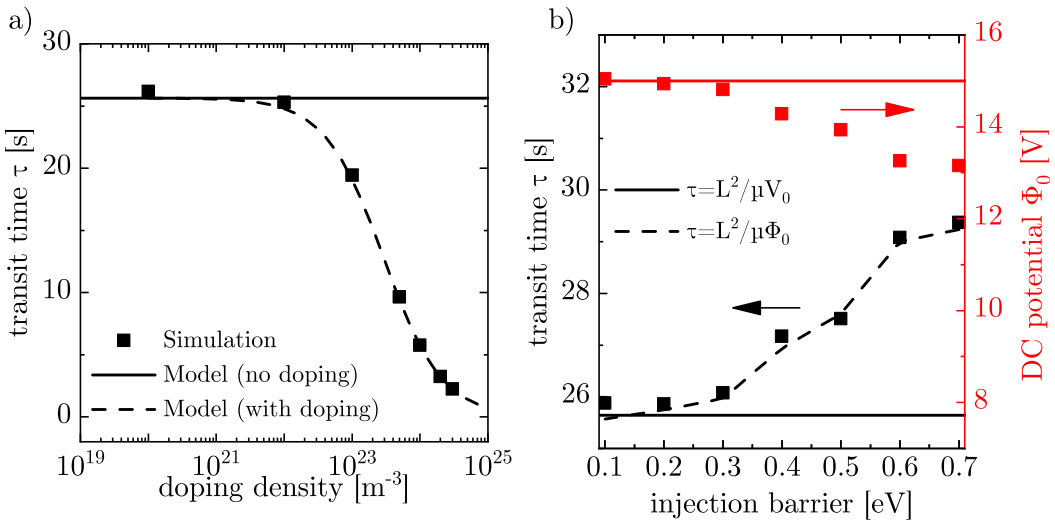

Figure 5.10: Extracted (symbols) and predicted parameters (lines) for simulations introducing doping (a) and injection barriers (b). Extending the model (solid line) to include doping recovers accurate predictions of the transit time for changing doping density (dashed line, see equation (5.26)). Changing the injection barrier (b) above a level of 0.3 eV leads to deviations of the simulation's results from the model's predictions (solid lines). Recalculating the transit time via $\tau = L^2/\mu\Phi_0$ (dashed line) recovers a good agreement between model and simulation.

Here, the total ionization of dopants is assumed, resulting in an increase of charge carrier density proportional to dopant density. The results of such a simulation can be found in figure 5.10a. The decrease in transit time with increasing dopant density is a result of the decreasing channel conductivity through the additional charge carriers. Doping can be introduced through a threshold voltage taking the following form: [108]

$$V_{th} = -\frac{qd_sN_A}{C_A}. \tag{5.26}$$

Where N_A is the volume density of acceptor states, d_s the semiconductors thickness, C_A the areal capacitance of the insulator. This expression of the threshold voltage closely reproduces the simulations results. Furthermore, strong doping extends the application window of the proposed model through additional charge carriers, effectively widening the window in which the device is operated in accumulation and the ACKP method can be applied. Strong trapping on the other hand can distort the shape of the surface potential oscillation through asymmetric rates since trapping and detrapping are fast ad slow processes, respectively. In addition, strong charge carrier trapping induces a threshold shift in the negative direction, further limiting the application window of the proposed model.

5.3.3 Injection Barriers

Finally, simulations with a changing injection barrier were carried out whos results can be found in figure 5.10b. This was done by lowering the work function of the injecting contact while the HOMO level of the organic semiconductor was kept constant at 5 eV. The work function of the gate contact was decreased in the same manner to prevent the formation of built-in potential between source and gate. The proposed model accurately predicts the simulations results for injection barriers up to 0.3 eV (corresponding to work function of 4.7 eV). Higher injection barriers lead to a decrease in Φ_0 and an increase in τ when compared to the ACKP predictions. This finding is caused by the asymmetric injection/ejection behaviour of the barrier limited contact, effectively reducing the applied bias. Predicting the transit anew with this reduced DC bias Φ_0 as $\tau_r = L^2/(\mu\Phi_0)$ recovers a high accordance with the simulated results (dashed line in figure 5.10b). Using both the extracted transit time τ and DC potential Φ_0, the mobility can be calculated which closely matched the simulations input parameter.

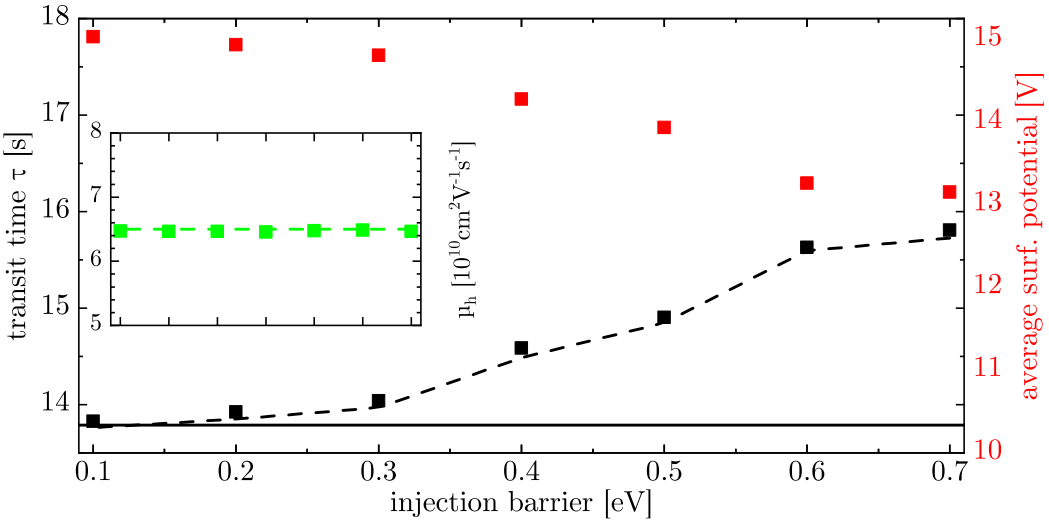

Figure 5.11: Fit of the F-ACKP model to the simulations results (symbols) for increasing injection barriers. The simple ACKP model (solid line) can not accurately describe the increasing transit time (black). The F-ACKP model (dashed line) on the other hand closely predicts the transit time increase. Using τ and the average surface potential (red) vice versa to calculate the mobility gives values to their input (inset). Note the changing absolute value of the transit time due to the renormalization of $L' = (1 - x_1) = 0.73L$.

Due to the unique formulation of the ACKP method in Fourier space a more general analysis method – called here Fourier ACKP (F-ACKP) – in full independence of the contact properties can be chosen Equation (5.12) describes the evolution of the surface potential oscillations in frequency space as the product of the Fourier transform of the applied bias $\nu(\omega)$ and the response function $R(\hat{x}, \omega)$. In the above presented situation of increasing injection barriers, the applied bias before and after the contact can differ greatly. This leads to inaccurate predictions of Φ_0 and τ as the effectively applied bias

$\nu(\omega)$ is changed in an unknown way. Despite this fact, the propagation of the charge carriers inside the device is still solely described by the semiconductors transport properties modelled by the response function $R(\hat{x}, \omega)$. Setting the first measurement point x_1 as the virtual injection point of charge carriers can overcomes this issue. $\nu(\omega)$ can then be calculated as the numeric Fourier transform of the measured surface potential at x_1 as:

$$\nu(\omega) = (F\Phi(x_1, t))(\omega) \tag{5.27}$$

Next, $\hat{x}$ is renormalized to the reduced device length. Then, equation (5.12) can be solved via the (numerical) back transform into time space resulting in a predicted $\Phi(\hat{x}, t)$ behaviour. The only free parameter used in this approach is the transit time which can be used to fit the model to the experimental data. Calculations of the mobility via the transit time $\tau = L^2/(\mu\Phi_0)$ still require a DC potential which can be easily calculated as the time average of the surface potential. This approach was tested on the data set of increasing injection barriers found in figure 5.11. The new F-ACKP approach accurately predicts the charge carrer mobility for all injection barriers resulting in errors below 1 %. The F-ACKP approach offers furthermore the added benefit of only requiring one fit parameter to accurately describe any applied bias even if the bias is altered via contact phenomena in an unknown way. This addition to the ACKP model renders this already injection barrier insensitive method (see section 5.2.2) more tolerant towards this phenomenon.

5.3.4 Revisiting Capacitance Voltage Simulations

Having developed a sophisticated model to describe the drift of charge carriers in extended MIS-Capacitors gives us the opportunity to revisit and possibly improve the approach used in the previous chapter 4 where it was attempted to extract the density of states width σ via a fit of simulated CV curves to experimental ones. It was found that this approach most likely overestimates the obtained σ which was attributed an accumulation induced parasitive capacitance caused by a drift of charge carriers outside the capacitors active area (due to an unstructured semiconductor). A capacitance voltage measurement is in its base the same experiment for which the ACKP method was used. The difference lies in the smaller extend of the open channel and the fact that the applied bias is of much greated frequency. As the applied bias is of sinusoidal form the calculation of the drift length is easy giving us access to the amount of charges which have left the active area (see appendix for more details). The thusly obtained additional parasitic capacitance ΔC can be described by

$$\Delta C = C_A W \sqrt{\frac{\mu(V_{th} - V_{DC})}{f_0 \pi}}. \tag{5.28}$$

Here C_A is the areal capacitance of the insulator, W the width of the contact from which the carriers can diffuse, μ the charge carrier mobility V_{DC} the applied DC voltage, V_{th} the threshold voltage of conduction and f_0 the frequency of the perturbing bias. The $\sqrt{V_{DC}}$ behaviour of the additional capacitance closely results the experimentally observed behaviour for capacitors under strong accumulation (see figure 4.4). Thus, this description seems to predict the capacitance drift for strong accumulation fairly well. V_{th} is the threshold voltage of field-effect conduction not necessarily an easily accessible parameter in capacitors. Setting $V_{th} = V_{shift}$ and μ to the value measured through transistors, this description can be included in the simulation as an additional capacitances for voltages higher than V_{th}.

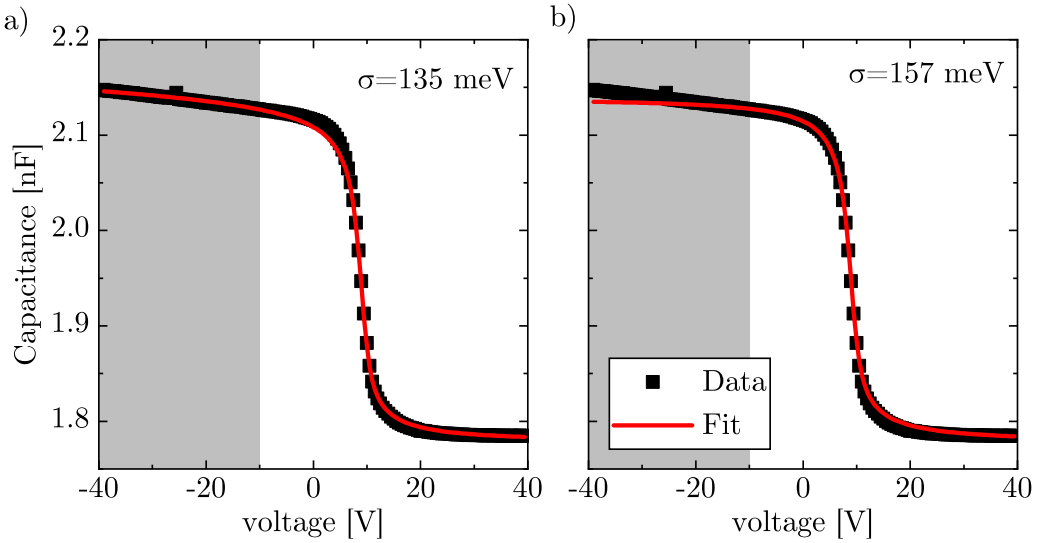

Figure 5.12: Experimental (symbols) and simulated (line) capacitance voltage spectra of a P3HT MIS capacitors form chapter 4. a) Includes in the simulation a description of the accumulation induced parasitic capacitance described in equation (5.28) while b) does not. While both simulations closely match the experimental data within the fit area (−10 V to 40 V) outside of the fit range (marked in grey) the addition to the algorithm clearly results in a better fit of experimental data and simulation. Furthermore the obtained fit parameter σ is reduced. See chapter 4 for more details (**1**, 1 kHz).

A comparison of the simulation results with/without the inclusion of ΔC can be found in figure 5.12. The same data set was used as a fitting target (**1**, 1 kHz). The fit area was chosen identically to before (−10 V to 40 V) For strong accumulation the proposed addition clearly reproduces the experimental much better although fitting was done between −10 V to 40 V. Within the fit interval both approaches yield very good approximation to the experimental curve. The value of the fit parameters remain constant[3] with the expection of σ which is significantly reduced from 157 meV to 135 meV. This value is still higher then the value reported in literature $\sigma_{lit.} = 98$ meV. [82, 84] At smaller active areas the parasitic capacitance plays a more important role and the

[3] $d_{sc} = 57/61$ nm; $d_{ins} = 340/337$ nm; $V_{shift} = -8.0/-7.8$ V; $C_{fix} = 17/17$ pF

obtained σ values remain much higher. Here the limitations of the ACKP model become apparent. It was developed for devices in full accumulation and is a worthwhile addition for unstructured capacitors in accumulation. In the switching point between accumulation and depletion the situation is much more complex. Following the explanation given in the previous chapter a capacitor at this operation point is described in the following way: due to the applied gate voltage the gaussian broadened HOMO level is position at the edges of Fermi-level so that some amount of charge carriers can populate the semiconductor while not enough states are addressable to inject all the charges necessary to fully shield the potential. It becomes readily apparent that this operation state is not fully described by the ACKP model. Thus, the σ extraction from large unstructured samples may benefit from equation (5.28) rendering the obtained σ values plausible.

5.4 Conclusion

Here a novel method to calculate the charge carrier mobility of semiconductors via Kelvin-probe surface potential measurements is reported. The ACKP method describes the propagation of a surface potential perturbation in MIS capacitors with extended channels under accumulation conditions. A surface potential perturbation coupled into the semiconductor via an injecting contact was found to be damped and phase shifted according to the proposed response function. Via a fit of the ACKP model to experimentally measured surface potential oscillations, the charge carrier mobility of the employed semiconductor can be calculated. A comparison to OFETs with identical layer stack proved the validity of this approach. The method was further tested and refined via two-dimensional finite element simulations. It was shown that the ACKP model provides robust predictions for a variety of experimental conditions and additional effects such as doping or trapping can be included. The model was further improve through the use of numeric Fourier transformations (then named F-ACKP) to completely eliminate any potential influence of contact effects on the mobility extraction while reducing the necessary fit parameters to one. In conclusion, the ACKP model offers very robust measurements for modest charge carrier mobility semiconductors, not only limited to their organic representative but can be applied to other material classes such as metal oxides or compound semiconductors. The ACKP model was further applied to the MIS capacitor based technique to extract σ from capacitance voltage curves which was presentend in chapter 4. There, it successfully described the accumulation induced parasitic capacitance observed in unstructured capacitors.

6 Local Electrical Property Investigations

Investigations into the macroscopic density of states (DOS) were done in chapter 4 while the previous chapter employed a macroscopic Kelvin-probe technique to measure the mobility in organic semiconductors. Here a closer look into the local electrical properties of OFETs is taken via the microscopic Kelvin-probe technique of Scanning Kelvin-probe microscopy (SKPM). This technique is used here to elucidate the potential landscape of TIPS-PEN transistors under operation conditions. TIPS-PEN transistors are often found to exhibit an s-shape in their output characteristic ascribed to the occurence of injection barriers which will be directly visualized in this chapter. Furthermore, clear evidence of electron accumulation during hole depletion will be shown, which was previously only assumed in chapter 4. After a brief description of the design process to obtain the necessary specialized SKPM holder, first investigations on a reference sample will be presented, elucidating the advantages and disadvantages of the two fundamental SKPM modes. Then, the desired transistors measurements were carried out. Finally, an SKPM based technique to measure the DOS will be presented and its requirements tested.

The measurements in this chapter were done in cooperation with Katelyn Goetz from the research group of Prof. Jana Zaumseil[1] who generously provided access to their SKPM.

6.1 Experimental Details

SKPM is a versatile tool to obtain insights into the potential landscape of electronic devices under operation conditions through surface potential measurements with resolutions of up to 10 nm (see section 3.4.2 for a more detailed description of the SKPM technique in general). Thus, SKPM was used in the field of organic electronic for example to study dopant drift or investigate the role of trapped charge carriers in transistors. [6, 109, 110] Initially an SKPM setup from DME was used.[2] Over the course of several different test experiments the machine proved to be too unstable for the envisioned measurements and the setup was switched. Thus, all of the here reported measurements

[1] Physikalisch-Chemisches Institut, Universität Heidelberg

[2] The setup was located at the innovationLab research center in Heidelberg to which access was generously provided by Dr. Robert Lovrincic. Measurements were carried out in cooperation with Dr. Sebastian Hietzschold to whom I want to extend my gratitude.

were done with a Bruker Dimension Icon Atomic Force microscope for which a special holder was constructed.

6.1.1 Design of the SKPM Sample Holder

Experimental surface potential measurements of electronic devices under operation conditionas require – apart from the SKPM setup itself – usually a specialized sample holder, device layout in combination with an adequate contacting solution. Since the aim of this chapter are measurements on transistors, a specialized sample contacting solution for OFETs is needed, ideally satisfying all of these requirements:

- **Interference-free Measurement**: The sample setup should not interfere with the SKPM measurement itself. This encompasses both mechanical interference (e.g. vibrations) and electric stray fields (e.g. through electrostatic potentials).
- **Reusability**: The holder should ideally be reusable to save time and resources.
- **Flexibility**: The ideal solution should be flexible when it comes to the layout, number and positions of transistors it can contact. Contacting multiple transistors at once offers increased reliability in case a device failure occurs.
- **Accesability**: The holder has to offer access of the SKPMs AFM tip to the transistors channel. This requires flat contacting solutions and/or special transistor layouts.
- **Shielding**: Due to the typical small currents of the investigated devices, cables should be shielded to decrease the noise level.

After one design iteration the simple sample holder shown in figure 6.1 was constructed. The holder consist of a rigid PVC body which can be fixed with 3 screws to the baseplate of the AFM to ensure a rigid connection and eliminate vibrations. The substrate holder offers 6 independently usable contacts as well as an additional grounding cable to ensure good connections to the AFMs conductive baseplate. The sample holder is attached to a shielded cable leading all connections to the outside into a switchbox where a connection to the respective pins can be made. Transistor containing substrates (with a total area of up to 9 cm) can be glued on a flat protrusion of holder where their gate contacts can either be contacted through the backside of the substrate through a small slit or by the top pins 1 and 6. Pins 2 to 5 can be used to connect the source and drain electrodes. All contact pins are made of gold. Contact between the pins and respective contacts on the substrate were made using a conventional wire bonding machine (Al wires). Bonding was carried out as flat as possible in order to preserve the necessary horizontal space for the AFMs tip.

In conclusion, the sample holder can support substrates with different sizes on which up to two transistors can be contacted. Reference measurements of the same samples with and without the constructed holder showed that the holder does neither influence the SKPM measurement itself nor does it influence the topography measurement through additional vibrational noise. Furthermore, measurements of the same transistors on the

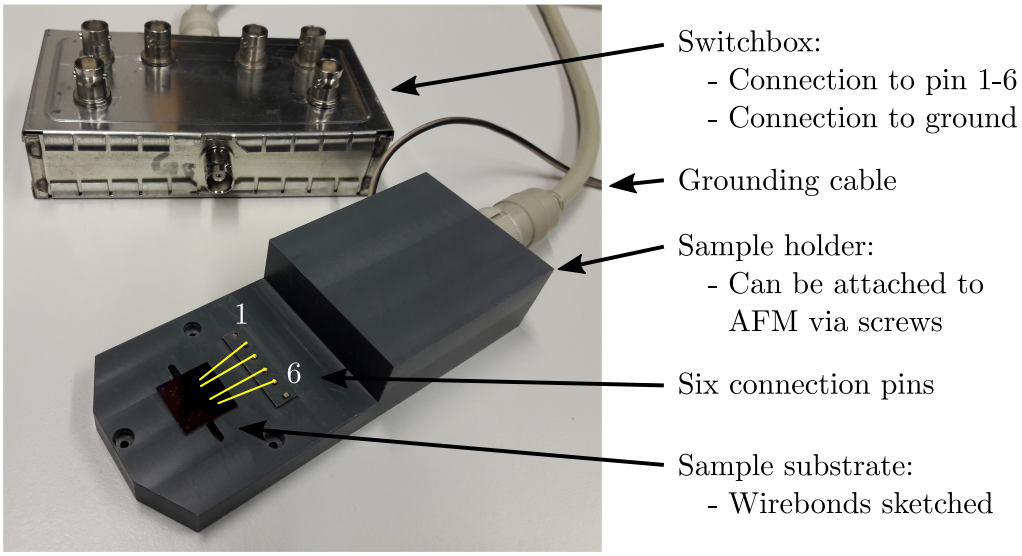

Figure 6.1: Picture of the sample Holder used for SKPM measurements of transistors. Up to six different electrodes on top of the substrates can be contacted via wire bonding on the respective pins on the sample holder (sketched by yellow lines).

sample holder or on the conventionally used probe station yield identical results. Thus, the sample holder satisfies all of the necessary requirements for successful measurements of OFETs in this SKPM setup.

6.1.2 Experimental Parameters

The SKPM was operated in either the AM- or FM-mode where the AM mode used a dual pass approach while the FM mode utilized a single pass mode for potential and topography measurements. Platinum-Iridium coated tips were used (SCM-PIT-V2). AM Measurements were carried out in tip-bias mode where the sample is grounded while both V_{DC} and V_{AC} are applied to the tip. FM measurements were done with the software variable *Drive2routing* set to sample. Here it is assumed that the bias is applied to the sample while V_{AC} is applied to the tip (inverting the sign of CPD changes in comparison to the AM mode). The maximum measurable voltage with this setup was 10 V. To prevent damage to the SKPM the maximum operation voltage was thus set to 10 V as well. All measurements were carried out under ambient conditions. Application of voltages to the transistors was done using a Keithley 2614B SMU. As the used setup does not allow measurements of single points or time.dependent measurements of single lines alternative approaches were used to make such measurements possible. Time.dependent measurements were achieved by choosing a very high aspect ratio scan (e.g. 20 µmx100 nm) where the long axis gives the spatial resolution and the short axis gives the time dependence. This approach is feasible in light of the low spatial resolution of the SKPM which we expect here to be at least 100 nm. The time dependence then can

be calculated by multiplying the line number by the scan rate (given in lines/second), which was set between 0.25 Hz and 0.2 Hz. Measurements of only a single point were done by further decreasing the scan area (e.g. 200 nmx20 nm).[3]

6.2 The Reference Substrate

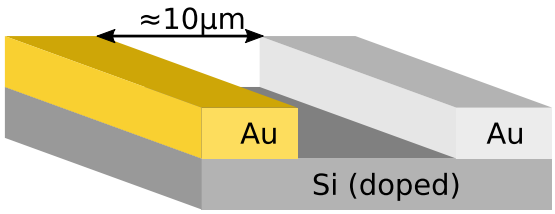

Figure 6.2: Layout of the SKPM reference sample. The sample consists of gold and aluminum layer deposited ≈ 10 µm apart on a doped silicon wafer.

To achieve a first understanding of the SKPM setup a reference sample with known work functions and geometries was used. The sample consists of three materials with different work functions in that gold and aluminium were deposited unto a doped silicon wafer. The layers of aluminium and gold are separated from each other by a ≈10 µm large gap through which the doped silicon can be measured (see figure 6.2).

After initial measurements, carried out to find suitable parameters for the lock-in amplifiers and feedback loops, the reference sample was used to compare the AM- and FM-mode regarding their energetic and spatial resolution. Such a comparison can be found in figure 6.3. While the topography measurements of both modes yielded comparable results (not shown), the FM mode shows in the potential measurements a fare better resolution as exemplified by the much sharper behaviour at the Si/Au edge. The AM-mode is expected to show in contrast a higher energetic resolution in the form of a smaller signal to noise ratio. Furthermore, the AM-mode depicts a general linear increase of CPD from left to right. This increase is most likely the result of the lower influence of the tip on the measured surface potential. In the AM mode the cantilever (and not only the AFMs tip) couples much more strongly to the substrate so that the measured CPD can be understood to be an average of much higher areas. Both modes fail to show a strong difference in CPD between the Si and the Al areas which would be expected from their work function. [75] As repeated measurements of this sample resulted in identical results we attributed this effect to an oxidation/contamination of the Al surface. Additionally, it was found that the resolution of both measurement

[3] The here used approach is non-ideal since a prolonged measurement time of only a small sample surface might lead to degradation of the sample surface due to the prolonged tapping of the tip on the surface.

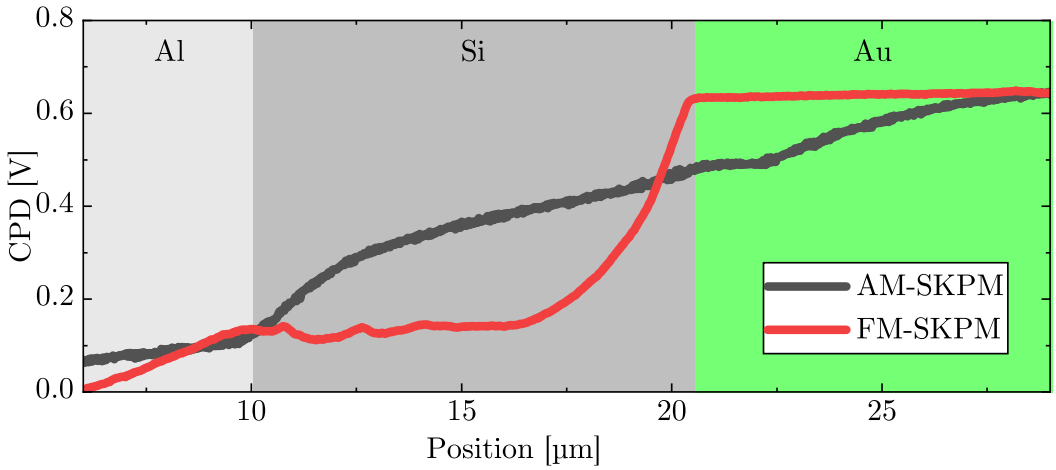

Figure 6.3: Comparison of AM and FM SKPM measurements of the reference substrate. While the FM-SKPM mode shows – as expected from theory – sharper transitions at the edges of two materials the AM mode exhibits a lower amount of noise within the spectra. Average of 20 lines of potential measurement. Measurements were shifted for clarity reasons.

modes is very dependent on a careful choice of lock-in amplifier parameters. A non-ideal lock-in configuration can furthermore lead to strong crosstalk between potential and topography measurement. Due to the fact that the AM mode utilizes only one lock-in amplifier it offers a more reliable handling. Additionally, the AM mode is operated in dual-pass mode to minimize electrical interaction between sample and tip while the CPD is measured. Having investigated both modes future measurements will be carried out in either the AM mode (low noise and spatial resolution) or FM mode (high noise spatial resolution) depending which mode is better suited for the experimental task at hand.

6.3 TIPS-PEN Transistors

During preliminary studies in chapter 4, a number of different capacitor and transistor designs were investigated utilizing both P3HT and TIPS-PEN as semiconductors. TIPS-PEN Transistors, utilizing gold as the electrode material, were frequently found to exhibit signs of injection barriers such as an s-shape in the output curve. The deep-lying HOMO of TIPS-PEN at 5.1 eV makes the occurrence of injection barriers into gold plausible. [80] To study this effect TIPS-PEN devices compatible with the SKPM measurements were fabricated exhibiting the same characteristic of a non-zero threshold voltage in combination with an s-shape in the output plot (see figure 6.4). Due to the nature of the used SKPM setup, the devices had to operate at voltages smaller than ±10 V and provide an exposed transistor channel for surface potential measure-

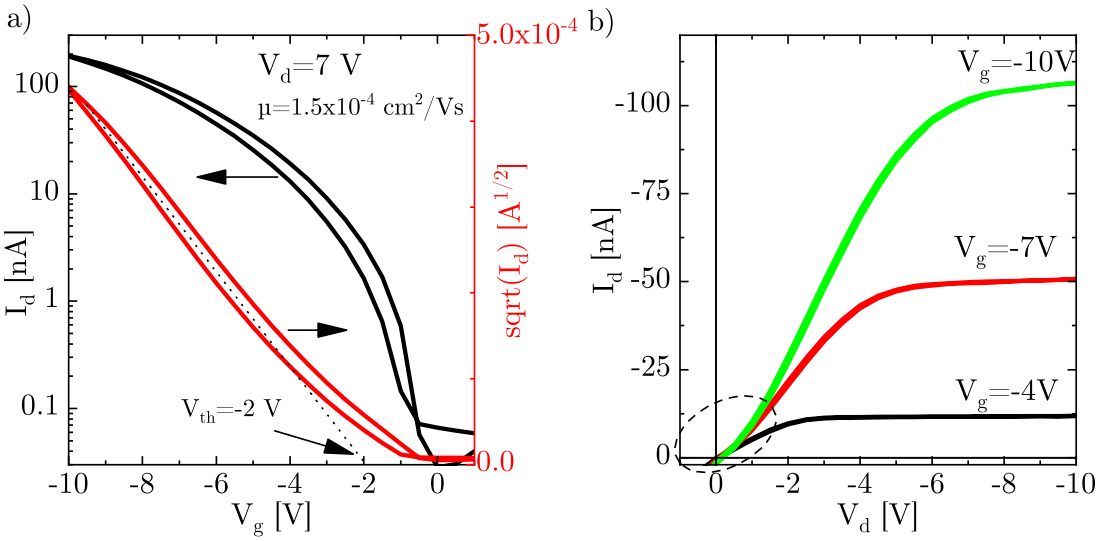

Figure 6.4: Transfer (a) and output charateristic (b) of an exemplary TIPS-PEN transistor. a) The line in the $\sqrt{I_d}$ plot indicates a threshold voltage of $V_th = 2\,\mathrm{V}$. b) The dashed region in the output curves highlight the region of the observed s-shape. Both the threshold voltage and the s-shape indicate the occurence of an injection barrier ($L = 10\,\mu\mathrm{m}$).

ments. As such only bottom-gate architectures with very thin dielectric layers could be chosen. Thus, devices were fabricated from pre-patterned bottom-contact bottom-gate substrates with gold contacts (W=10 µm, L=2.5; 5; 10; 20 µm) utilizing a 90 nm thick SiO_2 layer as dielectric followed by a strongly p-doped Si wafer. TIPS-PEN was spin coated on top of the substrates from a $10\,\mathrm{mg\,ml^{-1}}$ toluene solution at 1000 rpm forming a 40 nm thick micro-crystalline film. Figure 6.5 shows a top and side sketch of the device layout and an optical microscopy image of an exemplary transistor.

To ensure successful device operation, transistors were measured prior to SKPM measurements showing characteristics similar to the ones shown in figure 6.4. SKPM measurements were always carried out on freshly made devices to exclude degradation effects. The threshold voltages for the used devices ranged between 2 and 4 V.

6.3.1 Measurements Without Gate Voltage

Before a deeper look into the s-shape behaviour of these TIPS-PEN transistors could be taken, investigations using ungated transistors (V_g grounded) were carried out using both the AM and the FM mode. Variations in the drain voltage V_d should be – in principle – directly visible as a change in CPD of the contacts by the same amount. As the here used transistors are bottom-contact devices the semiconducting layer on top of the source/drain contacts can distort the measured CPD leading to small variations in the measured values. Figure 6.6 depicts an AM-SKPM measurement of a transistor for increasing drain voltage V_d =0;-1;-2;−3 V while source and gate contacts are grounded.

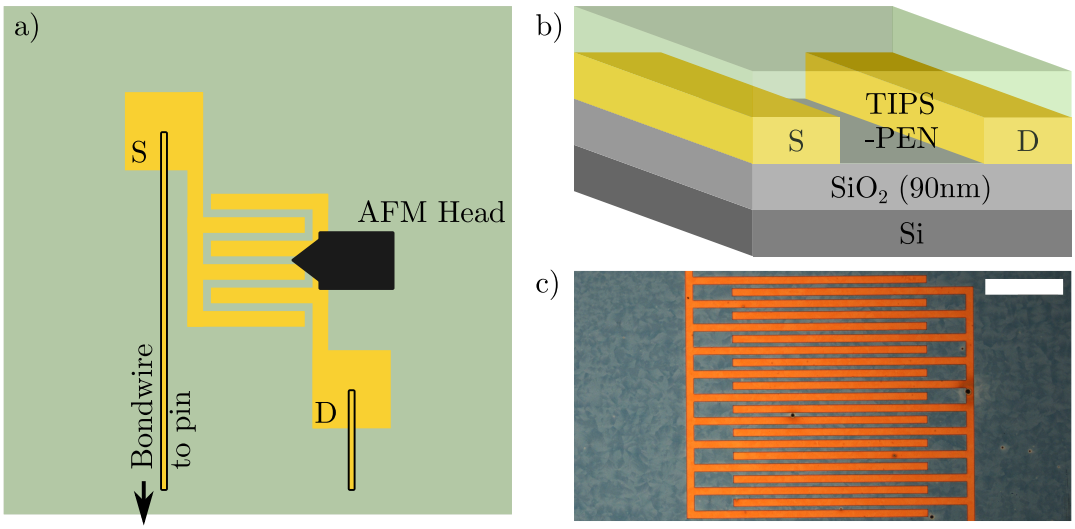

Figure 6.5: Layout of the TIPS-PEN transistors used throughout this chapter. a) Sketch of the top view of a transistor under the SKPM setup. Contact to the source (S) and drain (D) contacts is established through wire-bonding to their respective pins (see figure 6.1). The gate is contacted through the back of the substrate. b) Schematic side view of the transistors. c) Optical micrograph of an exemplary transistor (the white scale-bar are 200 µm).

After a quick glance at the topography profile of the investigated channel, a step in height becomes apparent. This $\approx 30\,\text{nm}$ high step happens simultaneously to a switch of the drain voltage from $V_d = -2\,\text{V}$ to $-3\,\text{V}$ as can be seen from the CPD profile as well as the x-integration in the inset. Measurements with voltages applied to the source side and/or a repetition of the same measurement on different samples yielded identical results. Thus the here observed behaviour has to be explained on by changing oscillating properties of the AFMs tip.

An explanation for this effect starts at the base of the here employed AM mode which operates in the following way: first a line topography measurement is recorded. Then the tip retraces the topography measurement at a given horizontal distance (here 100 nm). While carrying out the initial topography measurement the feedback loop used to regulate the electrical interaction between sample and tip is disabled. In the second pass, this feedback-loop is activated again to measure the CPD. Due to the change in topography upon application of an increased voltage ($\geq -3\,\text{V}$) an increase in electrical interaction between tip and sample for the first pass has to be assumed. This attraction/repulsion of the tip results in faulty topography measurements on contacts with applied bias. Thus, the second pass of the tip does not maintain a constant distance between tip and sample. It remains unclear why this effect happens so abruptly for voltages above $-3\,\text{V}$ and not in a more continuous manner. As changes in tip sample distance can potentially alter the CPD measured the AM mode cannot be used to measure small changes in CPD.

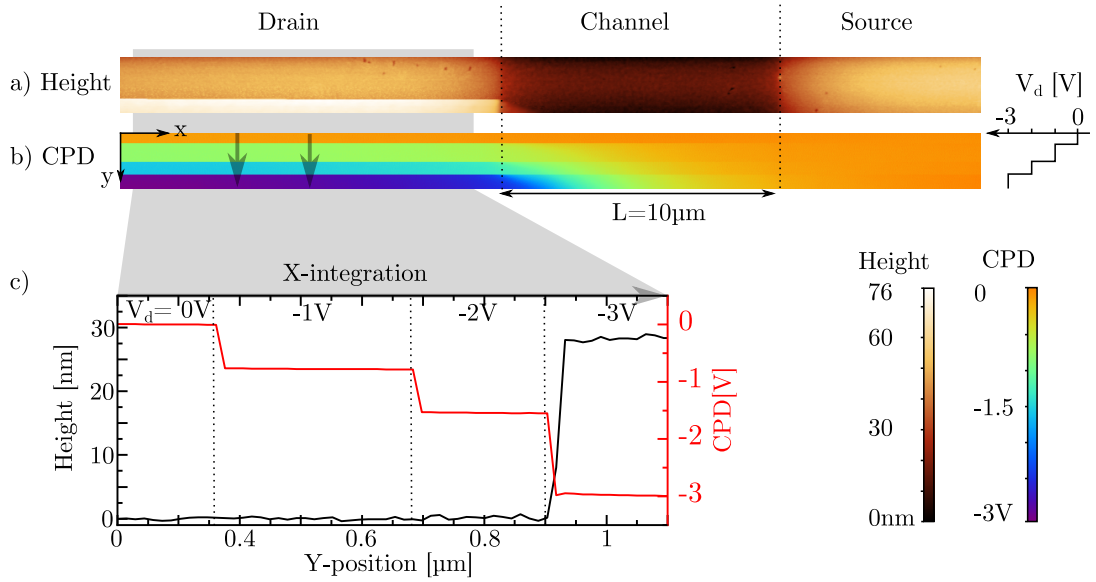

Figure 6.6: Height (b), CPD (b) and their integration along the x-axis (c) of a TIPS-PEN transistor under increasing source-drain voltage. The transistors channel is measured from the top downwards. At set y-positions V_d is increased. The switch from $V_d = -2\,\mathrm{V}$ to $-3\,\mathrm{V}$ induces a step in the height profile (a). The increasing drain voltage can be clearly seen in the CPD measurement (b). The undesired steip in height can potentially influence the CPD measurement as well (V_g =V_s =0 V). Measurement done in AM mode.

In conclusion, the AM mode can be used to measure qualitative changes in surface potential upon applications of medium voltages. Quantitative investigations on the other hand are might be influenced by the topography crosstalk. As such the same experiment was repeated using the FM mode where no potential topography crosstalk could be found. Thus, the next step of investigations in TIPS-PEN transistors under accumulation conditions will be carried out using the FM mode.

6.3.2 Accumulation Regime

In order to find out if the observed s-shape in the output characteristic and the non-zero threshold voltage are indeed the result of injection problems (see figure 6.4), TIPS-PEN OFETs utilizing the above-described structure (see figure 6.5) were investigated in their accumulation behaviour with FM-SKPM. The outputs s-shape at low drain voltages ($V_d = 0\,\mathrm{V}$ to $-1\,\mathrm{V}$) suggests a drain voltage-dependent device resistance (sum of channel, injection and ejection resistance) not covered by the SHOCKLEY-model (see section 2.2.2). For more negative drain voltages ($V_d < V_g - V_{th}$) the current eventually saturates. Under saturation conditions, the high drain voltage has depleted the channel of charge carriers in the vicinity of the ejecting source contact in an effect called channel pinching (or pinch-off). Thus the majority of the source-drain potential drops

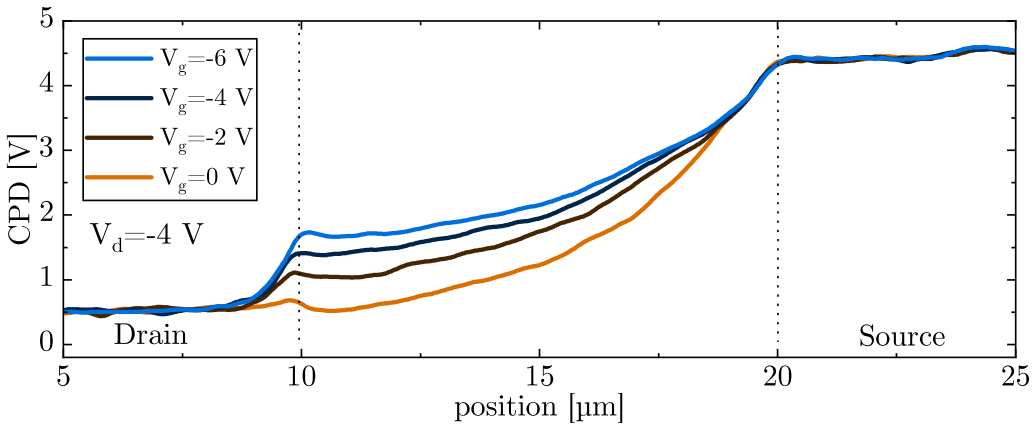

Figure 6.7: CPD profiles of a transistor channel in accumulation under increasing gate voltage. Increasing the gate voltage in a TIPS-PEN transistor at constant source-drain voltage ($V_d = -4\,\mathrm{V}$) changes the surface potentials shape. The increasing gate voltage induces a significant potential drop at the drain contact, a clear sign of a contact resistance. Measurement done in FM mode.

inside this depleted region. The extend and width of the pinch-off region can be modulated through the gate voltage which sets the amount of charge carriers accumulated in the channel. Here, spectra of the channel potential for a fixed source-drain voltage (V_d=$-4\,\mathrm{V}$) and varying gate voltage were investigated. As the source-drain potential is fixed the magnitude of the potential drop across the channel is fixed as well. An increase in channel conduction through an increase in V_g thus only changes the shape of the channel potential through a change of the relative contributions of the different effects mediating the potential drop (e.g. pinch-off resistance, channel resistance or contact resistance).

The results of an FM surface potential measurement of a transistor at constant drain voltage ($V_d = -4\,\mathrm{V}$) and varying gate voltage can be found in figure 6.7. Increasing the gate voltage from $0\,\mathrm{V}$ to $6\,\mathrm{V}$ introduces a significant drop of potential at the drain/channel interface located at $\approx 10\,\mu\mathrm{m}$. Furthermore, the majority of the potential drops in the second half of the channel regardless (pos. $15\,\mu\mathrm{m}$ to $20\,\mu\mathrm{m}$). This behaviour is not surprising since the increasing gate voltage switches the device from a point where it is completely operated in saturation ($V_g \geq -4\,\mathrm{V}$, see figure 6.4) to a point where linear regime operation starts to begin ($V_g = -6\,\mathrm{V}$). The decreasing strength of pinch-off results in the formation of a potential drop at the drain-contact (e.g. as opposed to a more continuous dependence at the contact). This behaviour is a prove of charge carrier transport impeded by contact resistances which was already hinted by its transfer and output charateristic in figure 6.4.

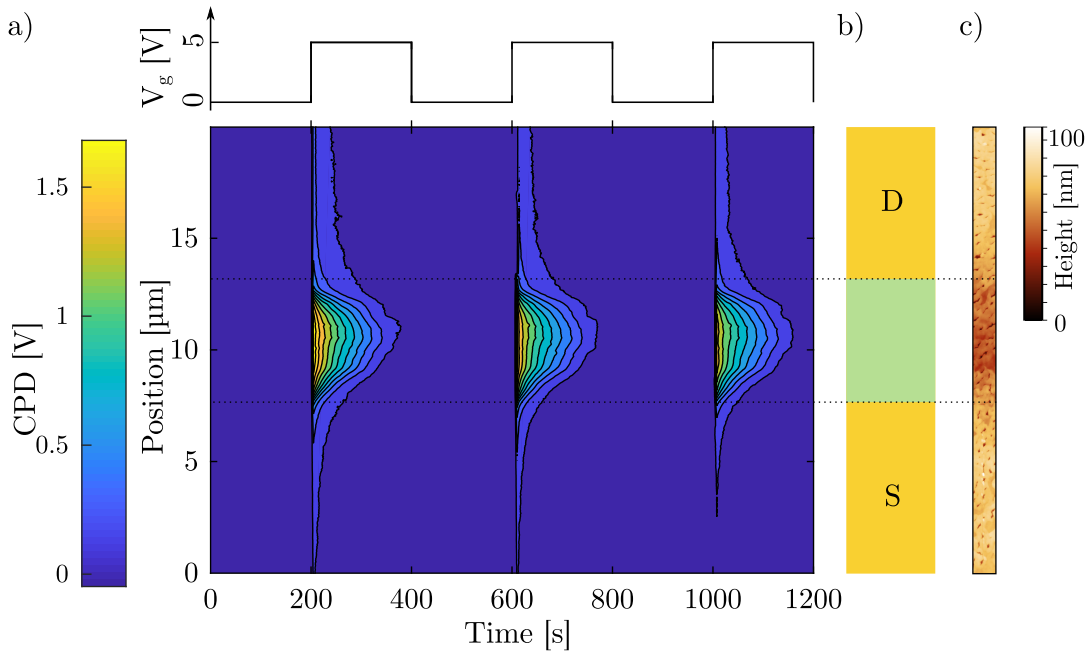

Figure 6.8: Measurements on a TIPS-PEN transistor repeatedly driven in depletion. a) CPD of a transistor channel for gate voltages switching between V_g =0 V and 5 V. Switching the gate voltage from 0 V to 5 V leads to a strong increase in CPD decaying over the next 200 s towards zero. A switch back to V_g =0 V does not influence the CPD. b) Sketch of the source drain position and c) surface topography measurement of the channel. (V_d =V_s 0 V). Measurement done in AM mode.

6.3.3 Depletion Regime

Having shown that charge carrier transport in TIPS-PEN transistors is indeed impeded by contact resistances further investigations which focus on their behaviour in depletion were carried out using the AM-SKPM mode.[4] The here used devices show only a very small current in depletion (V_g >0 V) suggesting the absence of charge carriers in this regime. Such a unipolar behaviour of transistors is very common and can be caused by a number of reasons. First and foremost do certain semiconductors only conduct either electrons or holes. Secondly, can the unipolar behaviour be caused by the chosen device architecture, as contacts or gate dielectrics can hamper charge transport for one carrier species. [105, 111] It was shown in pentacene devices in the past by Melzer and co-workers that p-type devices driven into depletion are not in the sense of the word depleted but show a slow accumulation of electrons in the channel. [6, 92, 112] A similar behaviour was already suggested in the discussion of the p-type MIS-Capacitors in chapter 4. These electrons can be injected over very high injection barriers but since this injection is a very slow process the semiconductor is rapidly depleted once a channel potential is applied and no/only a small continuous current can be observed if a channel

[4] The AM mode is used since a high spatial resolution is not required.

potential is applied (determined by the slow injection of charge carriers).[5] Figure 6.8 shows a measurement of a transistor (L=5 µm) repeatedly driven into depletion by applying an alternating gate voltage of V_g =0 V and V_g =5 V. The transistor channel located between x=7 µm and x=13 µm exhibits for no applied gate voltage surface potentials nearly identical to those over the contacts (CPD(t = 0...200s) ≈ 0). The application of a gate voltage of 5 V at t = 200 s leads to a strong increase in CPD. This rise in CPD is caused by the accumulation of holes at the gate/insulator interface not compensated by complementary charge carriers in the semiconductor. Over the next 200 s the CPD slowly decays towards zero. This decay is caused by a slow drift of electrons into the semiconductor, compensating the potential and decreasing the measured CPD. The alternative explanation of injection of electrons through the AFMs tip is unlikely due to the shape of the CPD decay in that the surface potential close to the contacts is compensated faster in comparison to the centre of the channel.[6] As repeated cycles give identical results and no undershoot in the CPD at V_g =0 V is visible we conclude that either electrons very quickly exit the transistors channel once the gate voltage is switched off or holes very quickly compensate the electrons after the switch. SiO_2 surfaces are well known for their electron trapping ability. [111] As such, rapid compensation through holes is the more likely alternative. A definite proof of this hypothesis could be done through measurements of a transistors threshold voltage hysteresis after longer electron accumulation as the presence of long-lived electrons shifts the threshold voltage towards more positive voltages. Thus we have conclusively shown that, although TIPS-PEN transistors do not exhibit significant current in its off state, electrons can be accumulated in its off state (at no applied channel potential). Next, the possibility of gaining density of states (DOS) information from SKPM measurements will be explored.

6.4 Density of States Measurements via SKPM

6.4.1 Theory

A technique to measure the DOS in transistors via SKPM was first introduced by Tal et al. in 2005. [113] Figure 6.9 shows an exemplary SKPM setup used for a DOS measurement in transistors. A bottom-gate transistor with an exposed channel is placed under an SKPM and both source and drain contacts are grounded. The grounded source and drain contacts are fixing the absolute position of the Fermi level in the transistors channel. In the case of a zero threshold voltage, varying the applied gate voltage V_g by ΔV_g leads to the accumulation of charge carriers inside the semiconducting layer through the field effect, screening the charge carriers residing on the gate electrode. This is done via a shift in HOMO level with respect to the Fermi level of the semiconductor so that a sufficient amount of states can be populated to accommodate the required charges.

[5] Furthermore, the electron mobility can be several orders lower in comparison to holes so they do not form a sufficiently large current for detection any way.

[6] We further repeated the same measurement at positions very far away from the injecting contacts where most of the potential remained uncompensated (measuremnets of up to 7 min).

This shift in HOMO level is anti-proportional to the DOS size at this energy and can be directly related to a shift in the channel potential φ_c. A small density leads to a strong shift in the channel potential while a big DOS induces a small shift. This channel potential can be directly measured through SKPM. Thus, a measurement of $\varphi_c(V_g)$ can give insights into the DOS around the HOMO level.

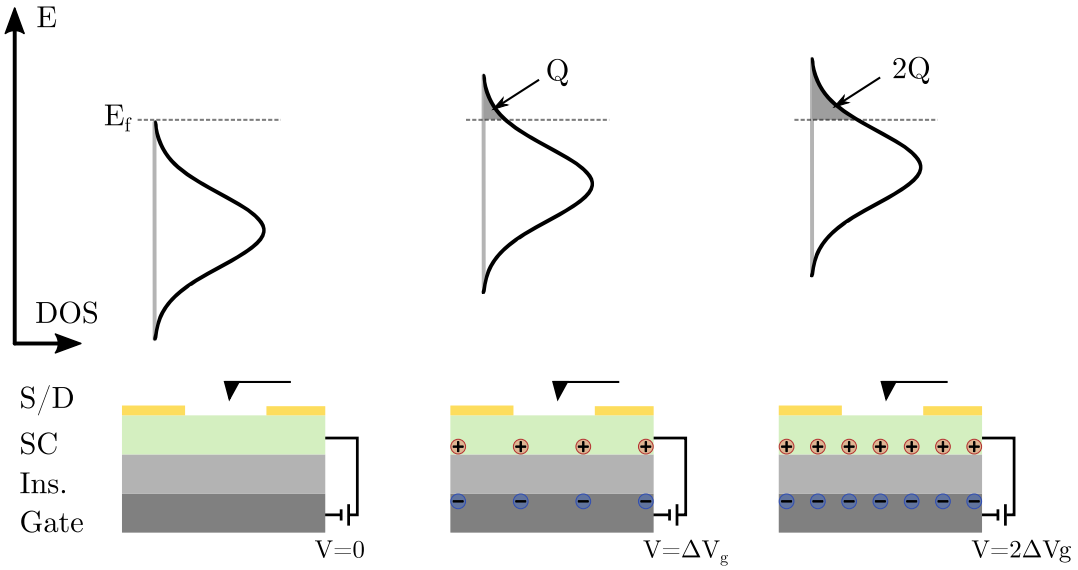

Figure 6.9: Evolution of HOMO-level position with respect to the Fermi level and charge accumulation in an SKPM experiment for DOS measurements. The top row shows how the HOMO level position inside the organic semiconductor (SC) upon application of a gate voltage (bottom). If the DOS is small at a given energy the change of HOMO induced through ΔV_g is big. At high higher DOS values the change in HOMO level decreases. The source and drain contacts (S/D) are grounded fixing the absolute HOMO position.

In their original publication, Tal et al. give the following formula for the calculation of the density of states $g(q\varphi_s)$

$$g(q\varphi_s) = \frac{C_g}{q^2 d_s}\left[\left(\frac{dV_s}{dV_g}\right)^{-1} - 1\right] \tag{6.1}$$

with q the elementary charge, $\varphi_s(V_g)$ the surface potential over the transistors channel as a function of applied gate voltage V_g, C_g the areal capacitance of the gate dielectric and d_s the thickness of the semiconducting layer. The most serious assumption leading to this formula for g is the postulation of a constant channel potential which is clearly violated for thicker films. The gate bias rather leads to an accumulation of charge carriers at the semiconductor/insulator interface distorting the channel potential and screening the surface potential φ_s. Although a self-consistent approach of correcting the surface potential via a Poisson equation or further theoretical additions have been put

forward, thin films are of big importance for the accuracy of this measurement. [114–116] Furthermore, trap states can distort the measurement for small voltages (where the film thickness is less important). As the energetic resolution of SKPM lies (depending on the measurement mode) at around 10 meV, this technique can only investigate the tail end of the DOS as changes in surface potential in the centre of the DOS are below the noise limit. Furthermore, SKPM suffers from the same challenges as all Kelvin-probe technique in that it is highly sensitive to surface effects (e.g. water adhesion). To circumvent environmental effects these measurements are usually carried out under ultra-high vacuum conditions or inside a nitrogen filled glovebox. [109]

A big benefit of this technique is that it can be used to probe the DOS with high spatial resolution. In combination with topography measurements, this allows the identification and characterisation of charge transport bottlenecks in thin films. Thus, the technique is best used to investigate stable devices consisting of very thin films of organic semiconductor with a diverse morphology. Here the possibility for such measurements in the previously used TIPS-PEN transistors will be investigated using solely the FM mode.[7]

6.4.2 FM Stability Measurements

In order to carry out experimental DOS measurements in transistor with the FM mode, the stability of FM measurements needed to be validated first. Thus, a TIPS-PEN transistor with fully grounded contacts ($V_g = V_s = V_d = 0\,\mathrm{V}$) was measured for extended periods. These measurements were carried out on a single spot[8] inside the transistors channel analogously to the envisioned DOS measurements. The results of such a measurement can be found in figure 6.10. A strong drift in the CPD in the range of 150 mV over 15 min is clearly visible. Measurements with an applied gate voltage show similar drift behaviour.

Based on the findings from figure 6.10 we conclude that the FM measurement mode does neither offer sufficient measurement stability for DOS investigations nor a sufficient CPD resolution, to begin with. A possible explanation for this slow drift can be the adsorption and desorption of water molecules from the ambient conditions. It has become apparent by other users of the same setup that the humidity level has a big influence on the measurement accuracy even when measuring simpler samples such as flat films on conductive substrates. Furthermore, the repeated tapping of the AFMs tip on the sample's surface may also alter its electronic properties via the deposition of charge carriers and/or morphological changes. One the one hand the slow drift in CPD disallows measurements in the order of 100 s to obtain the necessary high energetic resolution. The charge carrier dynamics in transistors, on the other hand, forbid significantly faster measurements as it takes the charge carriers some time until they have established a stable operation regime. Thus DOS measurements, requiring resolutions below 20 meV are neither in the FM nor in the AM mode possible with the

[7] The accuracy of the AM mode is hard to quantify since the possibility of a topography to potential crosstalk cannot be excluded.

[8] Or rather a very small area of size 200 nmx20 nm.

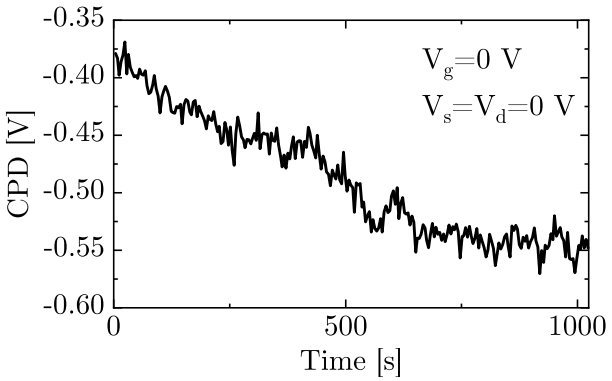

Figure 6.10: CPD as a function of time in the middle of the channel in an unbiased TIPS-PEN transistor. A clear decrease as a function of time can be seen. Measurement done in AM mode.

given setup. Additional work into sufficient environmental protection (e.g. a glovebox for the setup) may enable these investigations in the future.

6.5 Conclusion

In conclusion, SKPM was successfully used to investigate TIPS-PEN transistors under operation conditions. It was proven first that these transistors suffer indeed from high contact resistances as speculated from their current-voltage characteristic. Furthermore, investigations in depleted transistors revealed that they are in fact not devoid of charge carriers but vice versa exhibit a slow accumulation of electrons in their channel. Detailed investigations into the setup used revealed insufficient accuracy for further investigations into the DOS of the employed semiconductor. Having established a number of different analysis techniques for charge carrier transport in organic semiconductors, the following two chapters will investigate two classes of functional materials in greater detail.

7 Poly(*para*-phenylene)s for Organic Electronics

Poly(*para*-phenylene) (PPP) is a prototypical organic semiconducting polymer with high chemical and thermal stability. [117, 118] Despite its simple chemical structure of only linearly connected phenyl rings, synthetic access to high purity unsubstituted PPPs has proven challenging. [119–122] Alkyl or alkoxyl substituted PPP were highly investigated as active materials in light emitting diodes where their large band-gap was used to emit blue light. [123] Recently a new precursor route towards unsubstituted PPP was presented, giving for the first time access to true polymeric PPP with sufficient purity to warrant investigations into the semiconducting properties of the bare PPP backbone. [16] Here the conversion of a precursor polymer to the final PPP will be investigated in great detail. It will be shown by transistor measurements and doping experiments that the thusly obtained PPP indeed possesses semiconducting properties. Various types of PPP – obtained through thermal annealing of different precursor materials – are analysed to improve and understand the physics and chemistry of the underlying conversion process and to ultimately improve the semiconducting properties of the final product. The notation in this chapter is done to distinguish between the different kinds of Poly(*para*-phenylene) obtained. $\mathbf{PPP_1}$ indicates Poly(*para*-phenylene) obtained through precursor $\mathbf{P_1}$, while PPP represents the general molecule (for example in simulations).

This work is a product of a close cooperation of several research groups. Material synthesis was carried out by Ali Abdulkarim from the group of Prof Klaus Müllen while X-ray scattering was done by Tomasz Marszalek from the group of Prof Wojciech Pisula.[1] Infrared (IR) spectroscopy and VIS ellipsometry was done by Sebastian Beck, Rainer Bäuerle and Jakob Bernhardt from the group of Prof. Annemarie Pucci.[2] Ultraviolet photon-emission spectroscopy (UPS) was done by Silke Koser form the group of Prof Uwe Bunz.[3] The work is being published in two publications [124], [125].

[1] All Max Planck Institute for Polymer Research, Mainz
[2] Kirchhoff-Institut für Physik, Universität Heidelberg
[3] Organisch-Chemisches Institut, Universität Heidelberg

7.1 First Generation Precursors: Syn-Polymers

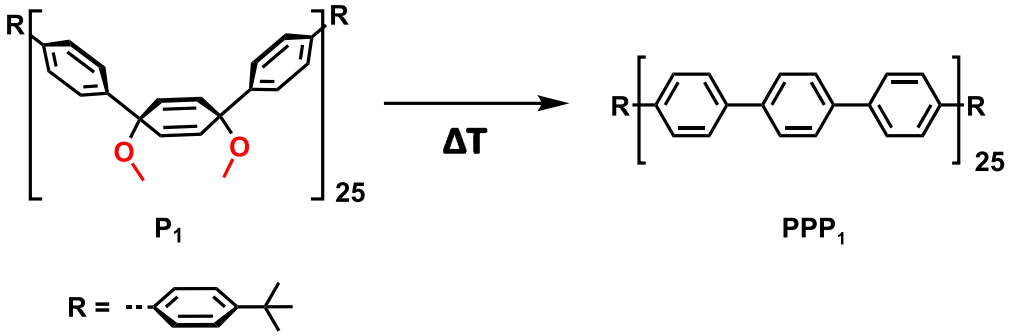

Figure 7.1: Chemical structure of the first generation PPP precursor P_1. Thermal annealing of P_1 leads to a cleavage of the two methoxy groups shown in red, rendering the previously soluble material insoluble and inducing a strong conformational change.

Figure 7.1 shows a sketch of the conversion process of the first generation precursor molecule $\mathbf{P_1}$ to $\mathbf{PPP_1}$. [16] The central two methoxy groups (shown in red) mediate the precursors good solubility while breaking the conjugated system of π-electrons which would otherwise include the central phenyl ring. These two groups are necessary for synthetic reasons and to allow solution processing of this material. Thermal treatment of $\mathbf{P_1}$ thin films lead to aromatization of the molecule via a cleavage of methoxy groups, resulting in totally insoluble films with high fluorescence. [16] It was already shown that this conversion leads to a strong shift of absorption towards smaller energies indicating a reduced band gap. Furthermore, IR spectroscopy measurements have revealed that thermal annealing at 300 °C for 2 h lead to a complete conversion of $\mathbf{P_1}$ to the final $\mathbf{PPP_1}$. Further details of the conversion process as well as the electrical properties of the resulting thin film remained open and will be investigated here. The precursor was processed via spincoating (900 rpm) from a 3.5 mg mL^{-1} chloroform solution. Thermal annealing was done on a standard laboratory hotplate. Unless noted otherwise, conversion was done at 300 °C for 2 h. To begin with, electrical and optical properties of a fully converted thin-film were carried out using UPS and absorption measurements on a highly doped silicon or quartz substrate, respectively.[4] A short summary of the measurement's results can be found in table 7.1 while the full spectrum is located in the appendix.

Table 7.1 shows that the conversion of $\mathbf{P_1}$ into $\mathbf{PPP_1}$ leads to a strong decrease of the optical gap from 3.95 eV to 2.9 eV as calculated from a Tauc plot. The UPS spectra of pristine films showed signs of sample charging prohibited further analysis. Thus, the large band-gap and the charging in the UPS suggest insulating properties of the precursor. The ionization potential (IP) of a converted film is measured as 5.8 eV in line with the previously reported IPs for substituted PPPs (typical 5.8 eV to 6 eV). [123] In combination with the large band gap, the electron affinity (EA) of this material is

[4] UPS measurements were dony by Silke Koser.

Table 7.1: Optical and electrical parameters of P_1 and its resulting PPP_1. $\lambda_{max}$is the maximum of the optical absorption, IP was measured through UPS while E_{gap} was calculated with a Tauc plot.

	P_1	PPP_1
λ_{max} [nm]	268	350
E_{gap} [eV]	3.95	2.90
IP [eV]	-	5.80

calculated as 2.9 eV. $\mathbf{PPP_1}$ shows potential as a hole transporting material, although a significant injection barrier to the commonly used contact materials (Au, Ag, Pt) is to be expected. Electron injection and transport in this material seems to be very unlikely for two reasons. First, an EA of 2.9 eV suggest the ubiquitously occurring trap states located at 3.6 eV to severely limited charge transport. [126] Secondly, efficient charge injection into the LUMO level would require very low work function electrodes (e.g. Ca, Na), known to be very unstable and detrimental to reproducible device fabrication. Thus, PPP will be here investigated primarily as a p-type semiconducting material to further understand and improve the conversion process.

7.1.1 Pristine Transistors

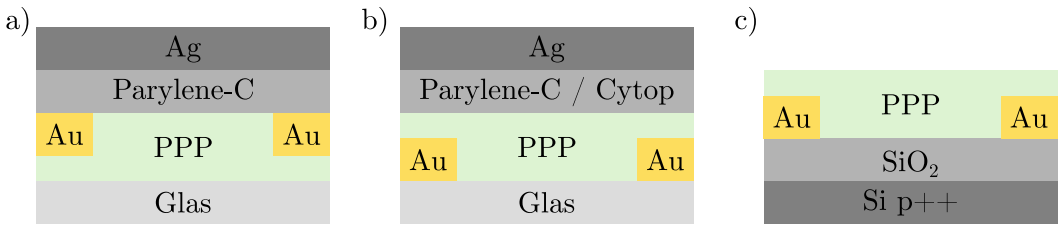

Figure 7.2: Sketch of the three different device layouts tested for PPP_1 transistors. Both the here shown top contact, top gate (a) and bottom contact, top gate (b) layouts did not result in functional devices with PPP as a semiconductor. A bottom gate, bottom contact layout (c) was successful.

Due to the fact that efficient device operation is always influenced by transistor layout and dielectrics used, several different transistor architectures were tested (see figure 7.2). All structures employed gold as a contact material due to its low lying work function. Due to the elevated temperatures needed for conversion of $\mathbf{P_1}$, the number of materials which can be deposited before tempering are very limited. Thus, a top gate bottom contact layout employing either parylene-C or the commercially available dielectric Cytop was tested first since a top gate architecture permits the dielectric layer to be deposited on cured films. All devices failed through a gate/source short occuring at

elevated gate voltages before any measurable transistor current could be registered. A top contact top gate layout with parylene-C as the dielectric layer suffered the same fate. We attribute this behaviour to the expected high injection barrier, requiring high gate voltages until a conductive channel is formed. In conclusion, both Parylene-C and Cytop did not offer a sufficiently large break resistance for this application. Thus a simple bottom gate layout as shown in figure 7.2c utilizing the very robust and leak resistant SiO_2 gate dielectric was investigated next. The prefabricated substrates consisting of interdigitating gold contacts ($W = 10\,\text{mm}$, $L = 20/10/5/2.5\,\mu\text{m}$) on top of a Si/SiO_2 (SiO_2 thickness: 230 nm). layer showed successful device operation.

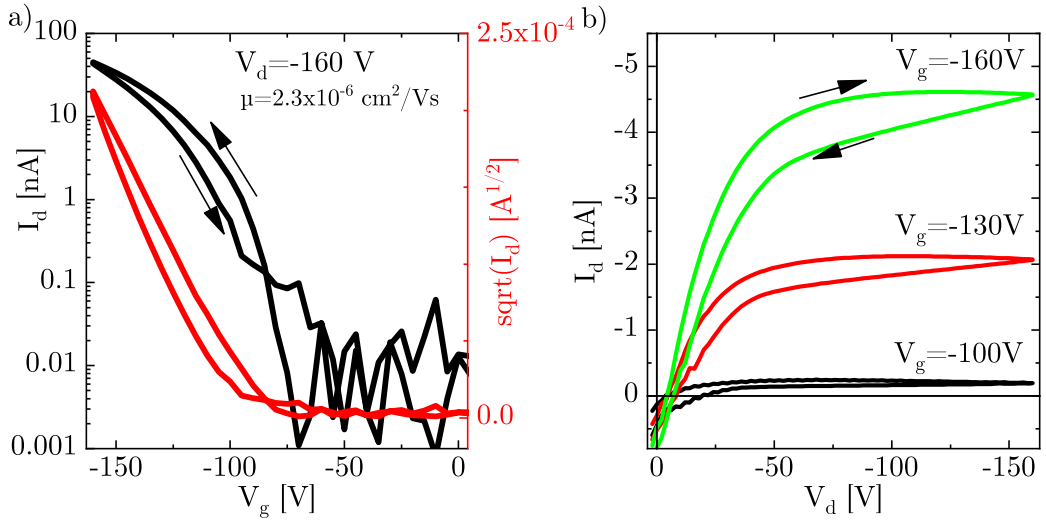

Figure 7.3: Third measured transfer (a) and output (b) characteristic of an exemplary PPP_1 transistor. a) The transfer charateristic depicts a high turn-on voltage ($V_{on} \approx -70\,\text{V}$). $\mathbf{P_1}$ was fully converted by annealing at 300 °C for 2 h ($L = 20\,\mu\text{m}$).

The transfer and output characteristic of an exemplary device with a SiO_2 gate dielectric can be found in figure 7.3 in which curing of the $\mathbf{P_1}$ layer was done at 300 °C for 2 h. The very high turn-on voltage of around −70 V indicates charge carrier transport impeded by traps and/or injection barriers. The occurrence of an injection barrier seems plausible due to $\mathbf{PPP_1}$s very low lying IP. Additionally, SiO_2 dielectrics are known to trap charge carriers at the semiconductor/insulator. [105]. This holds especially true for electrons prohibiting the use of SiO_2 as a dielectric layer in n-type semiconductors [111]. Here, hole trapping is assumed, rationalized by the repeated transfer and output measurements depicted in figure 7.4 which exhibit a strong shift in threshold voltage towards more negative values for repeated measurements. Repeated transfer measurements show an initial strong decrease of the threshold voltage (a) until a stable operation regime (c) is reached. The hysteresis in the output curve observed can also be explained by the strong trapping behaviour of the SiO_2 interface. The filled trap states are slowly depopulated over the course of one day leading to measurements very close to pristine devices. Thus the here fabricated transistors most likely suffer from both trap

states and a high injection barrier. Trap states are often passivated via self-assembled monolayers or through thin buffer layers, two approaches not feasible here due to the high conversion temperatures necessary. [49, 127] Due to the strong charge trapping of the semiconductor/insulator interface future discussions will be focused on the third measured transfer characteristic where the observed threshold voltage shift within one measurement is already significantly reduced.

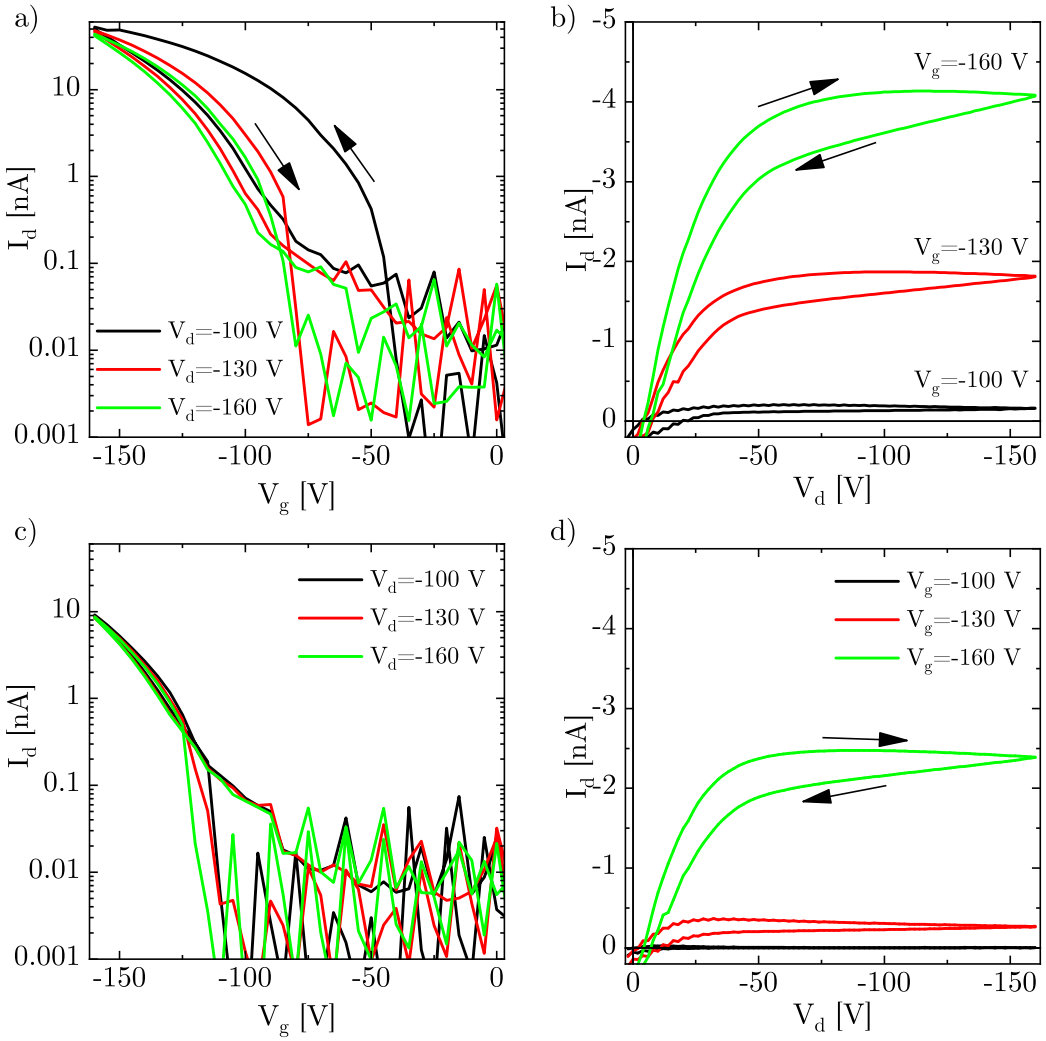

Figure 7.4: Repeated transfer and output measurements of a PPP_1 transistor. First, a set of three transfer measurements (a) was recorded, directly followed by three output measurements (b). This process was repeated again (c and d) until a negligible shift in threshold voltage was found in the transfer curves ($L = 20\,\mu m$).

Having demonstrated the semiconducting properties of $\mathbf{PPP_1}$, the dependence of the semiconducting properties on annealing time shall be investigated next. It was found

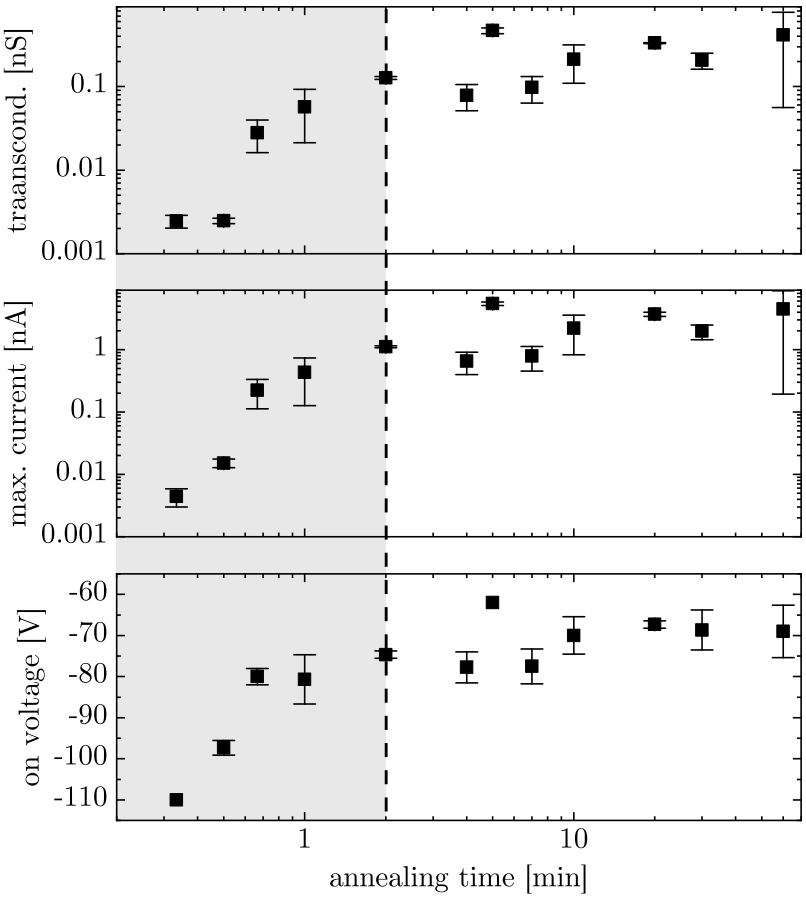

Figure 7.5: Transconductance, maximum current and turn on voltage of PPP_1 transistors for increasing annealing time. A rapid increase in all three parameters can be found for annealing times between 20 s and 2 min (grey area) followed by a pleateau where further annealing only lightly improves device operation ($L = 5\,\mu m$).

that the previously rather thin films of 30 nm[5] lead to a non-optimal reproducibility in transistor operation and thin film forming properties. Thus the film thickness was increased to 45 nm to partly alleviate this issue. Furthermore, the very high operation voltages of up to 160 V will be limited if possible to 110 V in order to prevent inadvertent destruction of transistors. 49 devices ($L = 5\,\mu m$) with varying annealing times at 300 °C were fabricated and measured. The resulting values for transconductance defined as

$$g = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d=const.}, \tag{7.1}$$

[5]Thickness is given prior to conversion as measured by Dektak.

maximum current and turn-on voltage can be seen in figure 7.5. At very short annealing times (20 s and 30 s) the transistors show no or only small signs of charge carrier transport.[6]. Then the intensity of charge carrier transport rapidly increases (up to 2 min). The transconductance and maximum current increase by two to three order of magnitude while the turn-on voltage is reduced by around 30 V. Above the threshold of 2 min annealing time all three parameters are nearly unvaried hinting towards a completed conversion process. Annealing beyond this point results in stable device operation. The strongly changing error bars are a result of the suboptimal batch-to-batch reproducibility where annealing times only investigated in one batch carry a small error bar and annealing times investigated in multiple batches have a larger error (error calculated as the standard deviation). Annealing times up to 2 h were investigated with unchanged device parameters.

Transistors can give valuable insights into the charge transport properties of semiconductors but do not give information about the chemical composition of the thin films. To assess the real degree of conversion further analytical tools were needed. The temperature and time dependence of the conversion process was thus studied via IR Spectroscopy and ellipsometry (in the visible range) offering additional insights into the molecular landscape of the PPP films. An overview over these investigations gives figure 7.6.[7] DFT calculated precursor and PPP spectra match closely their experimental counterparts (figure 7.6a) of measurements in thin films of $\mathbf{P_1}$ and $\mathbf{P_1}$ films annealed for 40 min at 300 °C. This indicates complete conversion of $\mathbf{P_1}$ into $\mathbf{PPP_1}$ for these parameters. Next, a dielectric model for the IR response of pristine and fully converted thin films was developed. [124] These two models can then be used to fit the spectra of intermediate annealing times quantifying the fraction of PPP obtained. Figure 7.6b depicts the results of such an analysis for different annealing times, temperatures and film thicknesses. The film thickness was varied via an increasing precursor concentration (6 mg mL^{-1} to 24 mg mL^{-1}) in the solution and/or an increased spin-coating speed (900 rpm to 4000 rpm). It was found that higher temperatures and thicker layers exhibit a faster conversion. VIS-Ellipsometry studies (see figure 7.6c) indicated a loss of film thickness normalized to its starting value of around 20 % (δd_{norm}) for fully converted films. Likewise the refractive index increases by about 10 % (δn_{norm}). This finding can be rationalized through the loss in material caused the demethoxylation (see figure 7.1) leading to thinner and denser films.

While a faster conversion for higher temperatures is to be expected for a thermally activated process a faster conversion for thicker films is somewhat surprising. Thus, AFM images of precursor films as a function of film thickness were recorded. The results depicted in figure 7.7 indicate a higher tendency to form holes. Furthermore the refractive index of the precursor films monotonously decreased with film thickness from 1.78 to 1.62. This indicates that thicker films are less densely packed (lower refractive index, more holes) and are converted faster towards $\mathbf{PPP_1}$. A possible explanation for this finding starts at the chemical structure of the precursor molecule. Films of $\mathbf{P_1}$ are expected to adopt a conformation rich in coils and kinks while the final PPP ideally

[6] The noise level of transconductance is ≈ 0.03 nSv and for currents ≈ 0.01 nA

[7] Measurements/simulations were carried out by Sebastian Beck

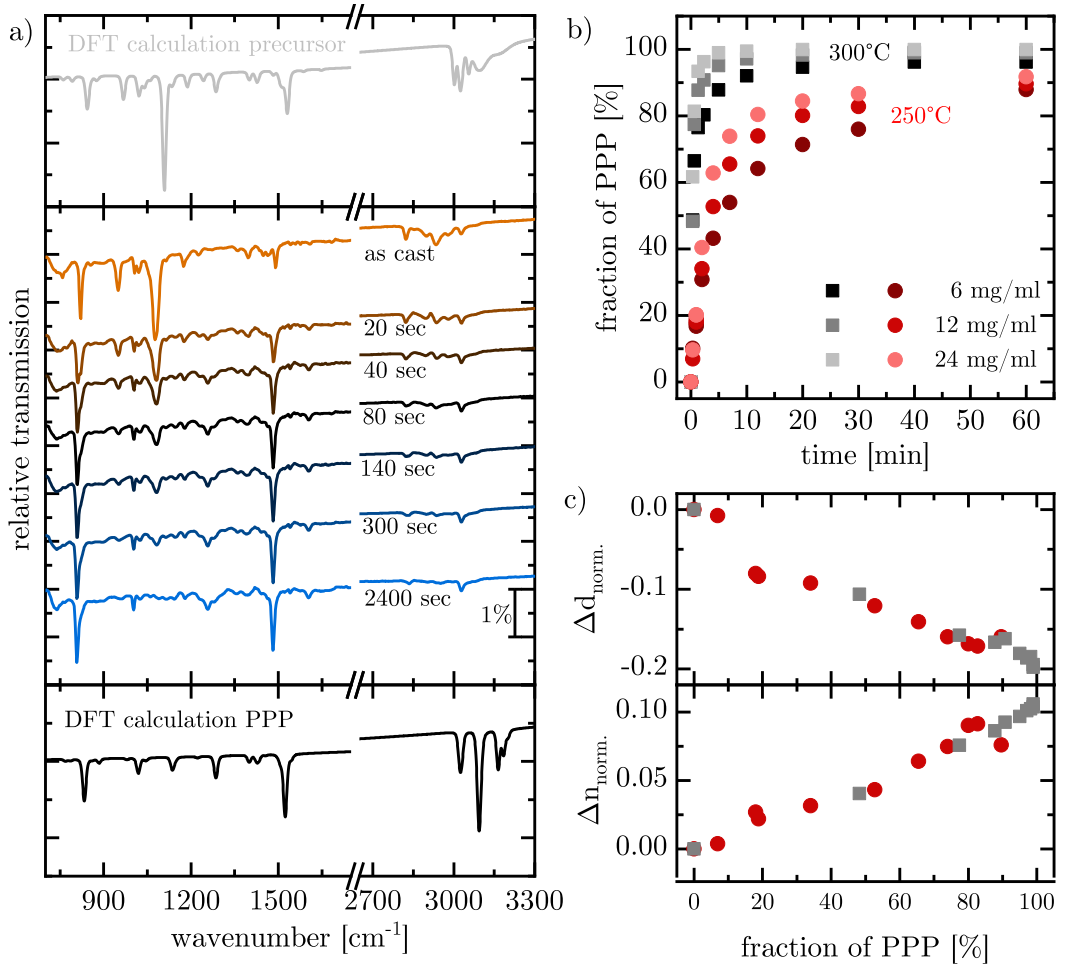

Figure 7.6: IR and VIS ellipsometry measurements of P_1 and its conversion to PPP_1. a) DFT calculated precursor and PPP IR spectra in comparison with experimental measurements for increasing annealing times at 300 °C. b) Calculated PPP fraction for different conversion times, annealing temperatures and precursor concentrations (see text for explication of procedure). c) Rrelative change in film thickness Δd and refractive index Δn as a function of PPP fraction (normalized to their pristine value). [124]

adopts the form of straight rods with minimal bending. This strong conformational change upon annealing seems to be facilitated in thicker, less dense films, indicating a high activation volume needed for the conversion process.

Angular dependent IR measurements did not indicate a preferred orientation neither in the precursor nor in the final PPP. 1D x-ray diffraction (XRD) measurements likewise did not find any evidence of thin film order (see appendix). Thus, the here obtained precursor and PPP films can be regarded as fully amorphous. Combining this knowledge of the composition of the investigated films with their observed charge carrier transport properties enables us to draw a clearer picture of the charge transport in $\mathbf{PPP_1}$.

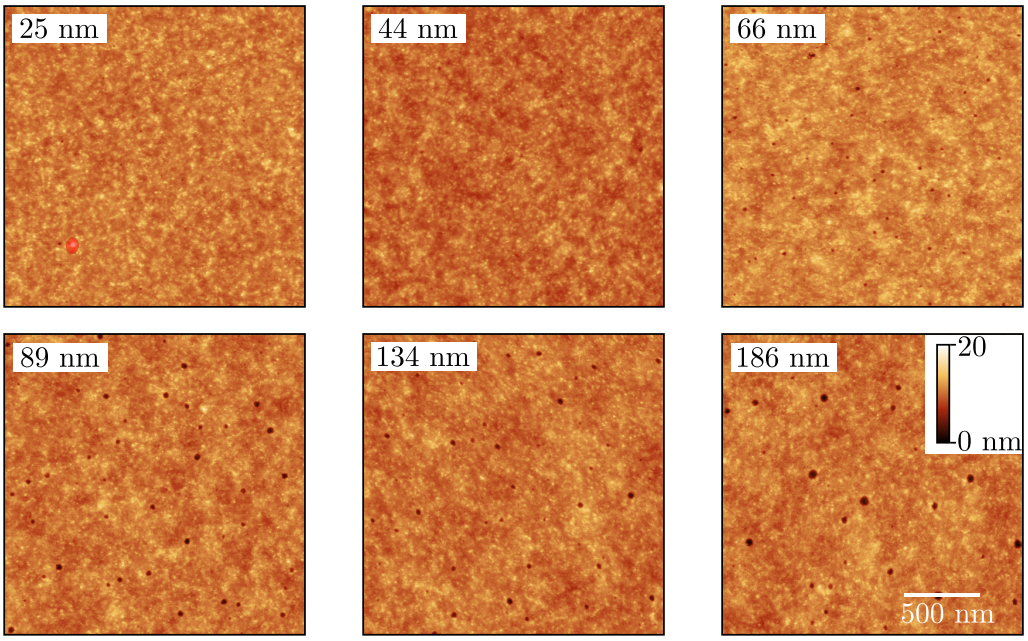

Figure 7.7: AFM images of P_1 films for different film thicknesses. These images show an increasing tendency to form holes for thicker films.

The saturation of the charge carrier properties at 2 min where $\approx 80\,\%$ conversion is reached (as indicated from figure 7.6b) indicates that further conversion of previously unconverted material only weakly improves charge carrier transport. It remains unclear whether a partly converted PPP film is formed through PPP chains which are in their entirety only partly aromatized or through a combination of fully converted strains existing side by side with partly or completly un-converted chains. While the former suggests a homogeneous phase the latter allows some extend of phase-separation. We will later see that some degree of molecular motion is possible during conversion (see below and figure 7.8) which could enable phase separation. Nevertheless, we assume a homogeneous phase during the whole transition in which all polymer strands are aromatized in more or less the same speed. [8] The low lying IP of the precursor suggests a situation where un- or partly aromatized PPP strands act as insulator and not as charge carrier traps. The inclusion of insulating materials into semiconductors can sometimes improve device operation either through an improved domain purity or a reduction of trap states. [50, 128]

The overall modest transistor performance with mobilities ranging in the order of $1 \times 10^{-7}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $1 \times 10^{-6}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ can be rationalized by a number of findings. Apart from a few notable exceptions efficient charge carrier transport requires some degree of crystallinity. [2, 129] The here investigated films on the other were

[8] The high length of $\mathbf{P_1}$ with ≈ 75 phenyl units introduces a high variation within each chain, supporting this assumption.

found to be completely amorphous (through AFM, 1D-XRD and IR). This lack of cristallinity can be attributed to the precursors shape and its conformational change during the conversion process. Several different ways were investigated to obtain at least some degree of long range order in thin-films of $\mathbf{P_1}$ prior to conversion but they all failed (e.g. off-center spin coating or tilted substrate drop-casting). Ultimately, the conversion of $\mathbf{P_1}$ to $\mathbf{PPP_1}$ is connected to a strong conformational change from a coiled to a highly linear conformation. This change is expected to severely influence all previously obtained order and strongly strain or even break the molecule, inducing additional disorder and trap states, further hampering charge transport. Furthermore, the IP of 5.8 eV is expected to induce an injection barrier at the gold contacts. A direct comparison to devices reported in literature is not possible since access to unsubstituted PPP was discovered just recently. Mobility measurements of substituted PPP could also not be found. Unsubstituted *para*-paraphenylens ($n = 4 - 6$) were reported in literature were mobilities between $1 \times 10^{-2}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $1 \times 10^{-1}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ were reported. [130] These materials were processed via vacuum sublimation which results in highly ordered films in which a higher charge carrier mobility has to be expected.

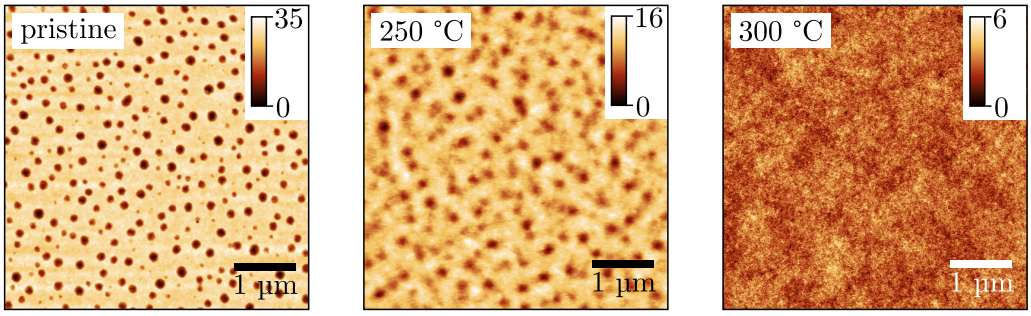

Figure 7.8: AFM images of $\mathbf{P_1}$ for different annealing temperatures. An initially highly porous $\mathbf{P_1}$ film equilibrates through thermal annealing at different temperatures for 10 min indication some form of reorganization during the conversion process.

The atomic force microscopy images of a highly $\mathbf{P_1}$ film with increasing annealing temperatures can be found in figure 7.8.[9] When comparing these three images it becomes immediately apparent that some sort of material transport is occurring resulting in the disappearance of the holes. This behaviour is unexpected as thermogravimetric anaylsis and differential scanning calorimetry(TGA/DSC) do not indicate a melting point or phase transition. [16] In light of this result at least some degree of reorganization might be possible while converting the precursor to $\mathbf{PPP_1}$.

7.1.2 Doping

To further elucidate the electrical properties of $\mathbf{PPP_1}$ its ability to be doped will be investigated next. Doping is an important concept of semiconductor physics allow-

[9] This films is spin coated from $3.5\,\mathrm{mg\,mL^{-1}}$ solution which sometimes resulted in such films.

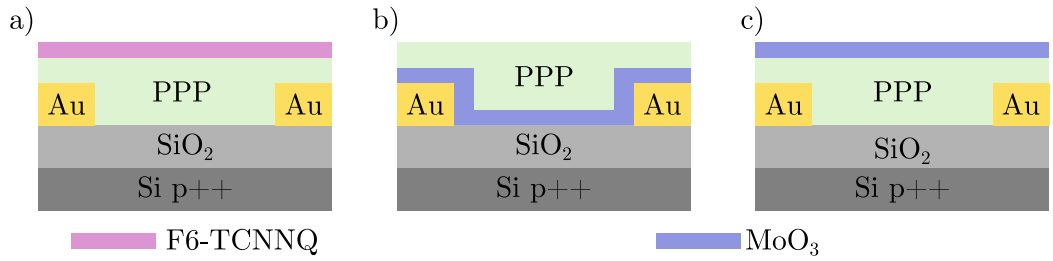

Figure 7.9: Sketch of the tested doping methods. a) Top layer doping with F6-TCNNQ; b) bottom layer doping with MoO_3 ; c) top layer doping with MoO_3 . F6-TCNNQ was deposited via spincoating while the 4 nm MoO_3 layer was deposited through thermal evaporation.

ing the controlled modifications of charge carrier transport properties. In transistors doping can shift the threshold voltage to higher or lower values for p or n-doping, respectively. Furthermore, doping influences the off-current in transistors through a modifications of the semiconductors background conductivity. [7] Here, interfacial doping was investigated in the previously presented bottom gate bottom contact architecture. Doping was done through the organic molecule hexafluorotetracyanonaphthoquinodimethane (F6-TCNNQ), a close relative to the common 7,7,8,8-tetracyano-2,3,5,6-tetrafluoroquinodimethane (F4-TCNQ), [60, 131] and the metal oxide MoO_3 .[10] With a F6TCNNQ's LUMO energy of 5.4 eV doping of $\mathbf{PPP_1}$ can prove challenging due to its IP of 5.8 eV so that rather F6-TCNNQ is expected to act as a trap state. [131] MoO_3 on the other hand is expected to successfully dope $\mathbf{PPP_1}$ due to its lower lying workfunction of 6.7 eV. [61–63]. Doping was done through the addition of an interlayer at either the semiconductor/insulator or semiconductor/air interface (see figure 7.9). MoO_3 was deposited via vacuum sublimation with a thickness of 4 nm. F6-TCNNQ is weakly soluable in organic solvents and can thus only be processed on top of processed devices which was done via spincoating from a saturated chloroform solution. Samples were tempered for 2 h at 300 °C before/after the deposition of the dopant to ensure complete conversion. To increase the chance of successful doping at the semiconductor/insulator interface the semiconductor thickness was reduced ($c = 3.5\,\mathrm{mg\,mL^{-1}}$) resulting in ≈ 30 nm thick films.[11]

The use of F6-TCNNQ resulted in strongly reduced currents which is likely caused through the inappropriate energy level of this material causing it to act as a charge carrier trap instead of a dopant. Doping at the semicondutor/insulator interface with MoO_3 resulted in over-doped devices where the source drain current is strongly increased but can be only weakly modulated through the gate voltage (nearly ohmic IV curve). A remedy for this behaviour would be a much smaller dopant thickness. It remains unclear how much of the dopant stays of the surface after deposition of the precursor through spin coating. Parts of the remaining dopant layer is expected to diffuse/dissolve into the semiconducting layer through the prolonged high temperature

[10] The F6-TCNNQ was generously provided by Ali Abdulkarim.
[11] Prior to conversion.

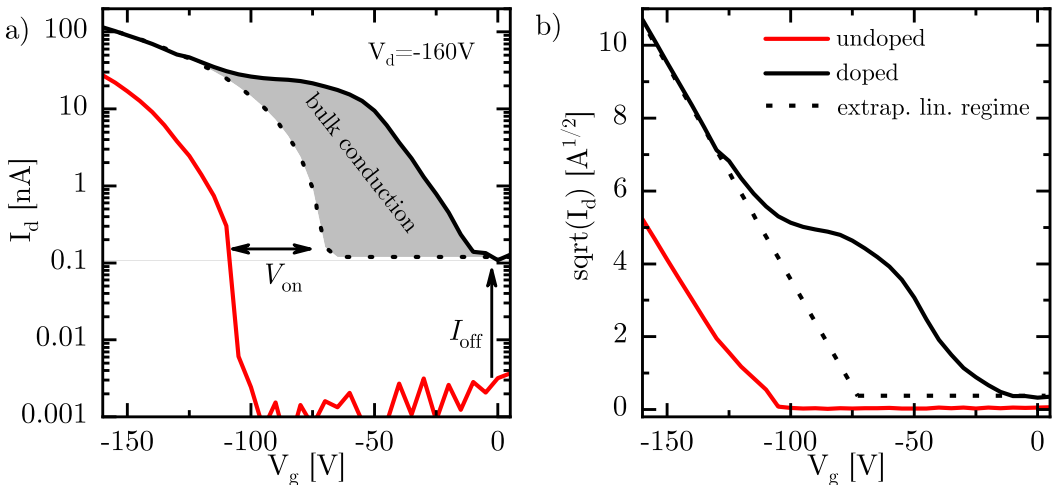

Figure 7.10: Transfer curves of a doped and undoped PPP_1 device. a) Log plot of the transfer curve of a doped (black solid line) and undoped device (red line). Doping induces a shift in turn-on voltage, and increase in off-current and introduces an additional bulk conduction channel (shaded area). The dashed line indicates the transistors behaviour without the bulk conduction channel. b)$\sqrt{I_d}$ plot of the same device showing a clear deviation from the linear behaviour in doped devices for intermediate voltages ($L = 10\,\mu m$). See also figure 7.11.

annealing resulting in the overdoped transistor. Doping via a top dopant layer with MoO_3 resulted in successfully doped devices as can be seen from figure 7.10. Parts of the dopant layer are here assumed to diffuse into the bulk of the semiconducting layer during deposition where the sucseffull doping was probed through the IV measurements (see figure 7.12). Doping resulted in a strong shift of turn-on voltage and further increased the off current by nearly two orders of magnitude. Doping further decreased the hysteresis for repeated transistors measurements while the calculated saturation regime mobilities remained constant. Thus the interfacial doping with MoO_3 lessened the influence of charge carrier trapping at the semiconductor/insulator interface through an increased charge carrier density. Devices with only a MoO_3 layer for comparison reasons showed no signs of charge transport. [12] The clear deviations from the Shockley model for doped devices can be explained through an additional bulk conduction channel as proposed by Meijer et al. in 2003. [65]

Figure 7.11 shows the exemplary situation of a very strongly p-doped accumulation mode OFET experimentally observed in figure 7.10. In strong accumulation the current between the source and drain electrodes is carried through two conductive pathways ($V_g = -160\,V to -70\,V$ in figure 7.10). First, the well know field-effect channel at the semiconductor/insulator interface. Second, strong doping establishes a bulk conduction channel able to transport additional charges. At voltages below the turn-on voltage of field-effect conduction V_{FET} (reading $-70\,V$ in figure 7.10), the bulk conduction channel can remain open to carry a non-zero source drain current. A further increase in gate

[12] Tempering and/or spin-coating of pure chloroform resulted in the same results

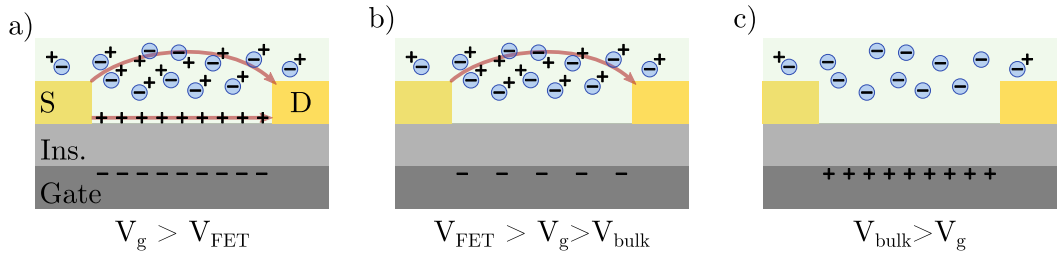

Figure 7.11: Sketch of the formation of a bulk conduction channel in highly doped transistors. a) At high accumulation voltages charge carriers can flow between source and gate both through the conductive channel at the semiconductor/insulator interface aswell as through the highly doped bulk. b) At voltages lower than the channels threshold voltage V_{FET} charge can only flow through the bulk. c) in fully depleted devices no/very little current is observable. Adapted from Meijer et al. [65] In figure 7.10 V_{FET} is $-70\,\mathrm{V}$ and $V_{bulk} = -10\,\mathrm{V}$.

voltage can deplete this second conduction channel until it is completely depleted at V_{bulk} (V_{bulk}−10 V in figure 7.10). This model very accurately describes the here observed transistor behaviour. One has to note that the employed interfacial doping method does not result in homogenous doping but rather a dopant gradient in vertical direction of the semiconductor film has to be assumed formed through the diffusion of dopants from the top pure MoO_3 layer. This effect could be reduced through a more evenly form of doping (e.g. adding MoO_3 in the spin-coating solution). Nevertheless, PPP was shown to be successfully doped through MoO_3 , proving its semiconducting properties once again.

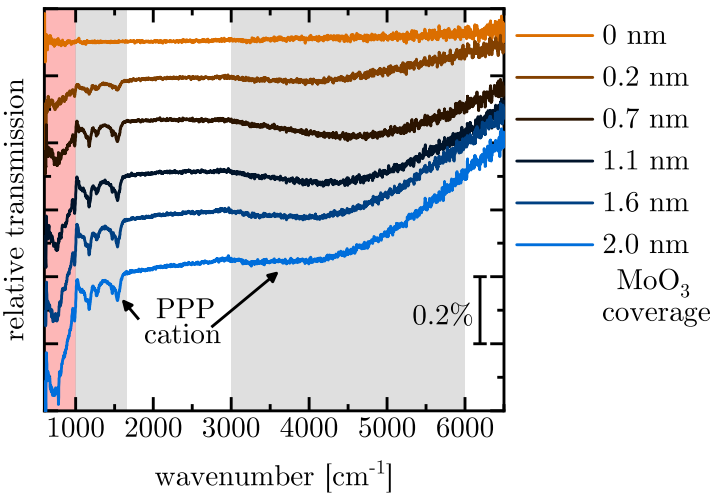

Figure 7.12: Relative IR spectra of a PPP_1 film with increasing MoO_3 coverage. An increase in MoO_3 coverage induces signs of PPP cations indicating doping of the PPP polymer chains through MoO_3 . A pristine PPP spectra was used as a reference. [124]

The validity of the here observed interfacial doping method was further investigated via IR spectroscopy.[13] Figure 7.12 shows the relative transmission spectra for increasing MoO_3 coverage of a completely converted 53 nm PPP film. For increasing MoO_3 coverage clear signs of charge transfer between the dopant and the PPP are visible in the form of a polaronic absorption (broad band around 4500 cm^{-1}) and IR activated vibrational modes between 1000 and 1600 cm^{-1}.[63, 132, 133] These modes saturate at around 1.6 nm meaning that further deposition of material is not entering the semiconductor but is rather forming a capping layer on the surface of the **PPP$_1$**. The IR measurements prove that a true charge transfer is happening between the MoO_3 dopant and **PPP$_1$** instead of a simple incorporation of the material into the thin film.

In conclusion the PPP films resulting from conversion of **P$_1$** show semiconducting properties but suffer from several bottlenecks of charge transport among which the most important factors seem to be the total amorphous nature of these films. The true semiconducting nature of **PPP$_1$** was further proven through doping experiment. The strong conformational change required in the conversion process ultimately leads to films of significant disorder featuring suboptimal transport properties. In conclusion, we learned that optimization of the charge transport properties have to start at the chemical structure of the precursor itself. Thus a precursor molecule with a conformation in close proximity to the desired PPP was suggested. Additionally a decrease in conversion temperature could enable different device layouts eliminating at metal oxide/semiconductor interface could further improve charge carrier transport.

[13] Measurements done by Sebastian Beck

7.2 Second Generation Precursors: Anti-Polymers

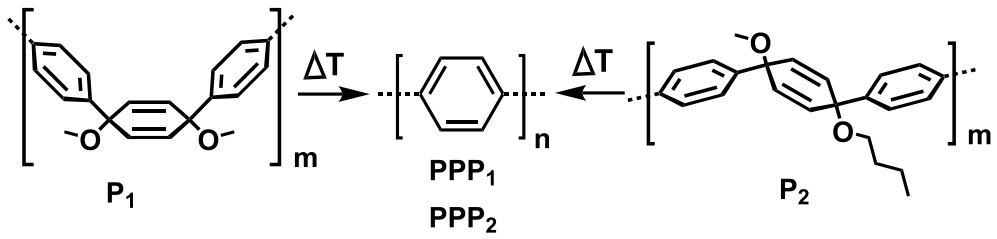

Figure 7.13: Chemical structure of the two precursor polymers P_1 and P_2.

Having learned a valuable lesson about the interplay between precursor structure and properties of the resulting PPP films, a new generation of anti-connected precursor polymers was synthesized by Ali Abdulkarim (see figure 7.13). While the syn-connection of $\mathbf{P_1}$ is expected to lead to a conformation rich in kinks and coils in thin films the anti precursor $\mathbf{P_2}$ is expected to adopt a much more linear conformation closer to the completely linear conformation of PPP. To obtain sufficient solubility and to decrease the conversion temperature one of the methoxy groups was further exchanged by a butoxy group. Processing of the material remained identical with the exception that a slightly decreased concentration for spincoating was chosen in order to keep the film thickness comparable to $\mathbf{P_1}$.[14] First, an IR spectroscopy study on the conversion kinetics of $\mathbf{P_2}$ was carried out by Rainer Bäuerle. [125, 134] Via a fit of model IR spectra consisting of unconverted/converted samples to experimental thin film spectra the fraction of PPP for different annealing times and temperatures was found (see figure 7.14). $\mathbf{P_2}$ converts faster to PPP then the first generation precursor $\mathbf{P_1}$, much so at 300 °C. With a resolution of the used approach of around ±5 %, $\mathbf{P_2}$ reaches full conversion after less then 5 min while $\mathbf{P_1}$ requires 20 min. No thickness dependence of the conversion speed was found for $\mathbf{P_2}$. Furthermore, a preferred orientation molecular orientation of $\mathbf{P_2}$ and the resulting $\mathbf{PPP_2}$ was measured, giving a first indication of a potential increase in order.

Thin films of $\mathbf{P_2}$ annealed at different temperatures for 10 min were investigated next via AFM to gain further indications for the suspected higher film order (see figure 7.15). While pristine films and those annealed at 200 °C show identical morphology, clear nanometre sized features can be observed for films annealed at 250 °C (≈ 50 % conversion) and 300 °C (100 % conversion). This further hints towards an increasing thin film order for converted films. The definitive proof of thin film order was done trough Grazing-Incidence Wide-Angle X-ray Scattering (GIWAXS) indicating a week degree of molecular order in thin films (see Appendix). [15] While pristine films did not indicate any signs of molecular order weak reflexes could be observed for fully converted films (2 h at either 250 °C or 300 °C). In conclusion the change in precursor layout resulted in an slight increase in molecular order for the final PPP, while – at the same time – lowering the necessary conversion temperature.

[14] concentrations were reduced by 20 % from 6 mg mL^{-1} to 5 mg mL^{-1}.
[15] Measurements were done by Thomasz Marszalek

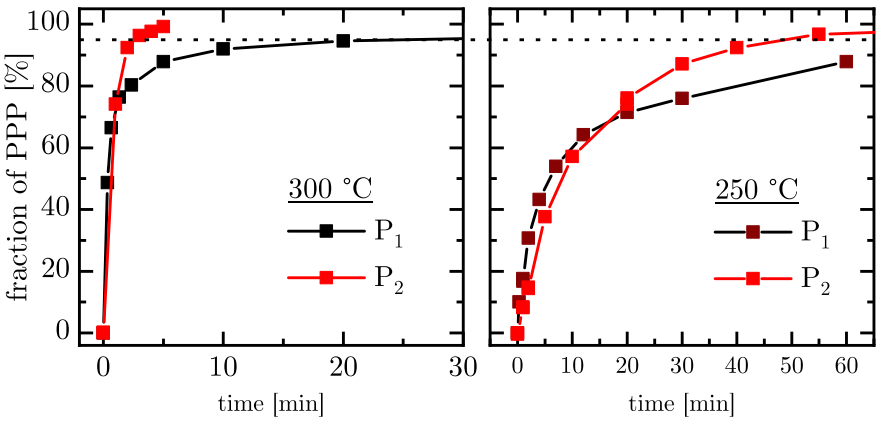

Figure 7.14: PPP fraction as a function of annealing time and temperature for P_1 and P_2. The PPP fraction was calculated from IR spectra at the respective conversion times (see text for a detailed explanation). P_2 shows a faster conversion in comparison to P_1 both a 300 °C and 250 °C. The dashed horizontal line marks complete conversion (95 % is considered full conversion as the error is ≈5 %).

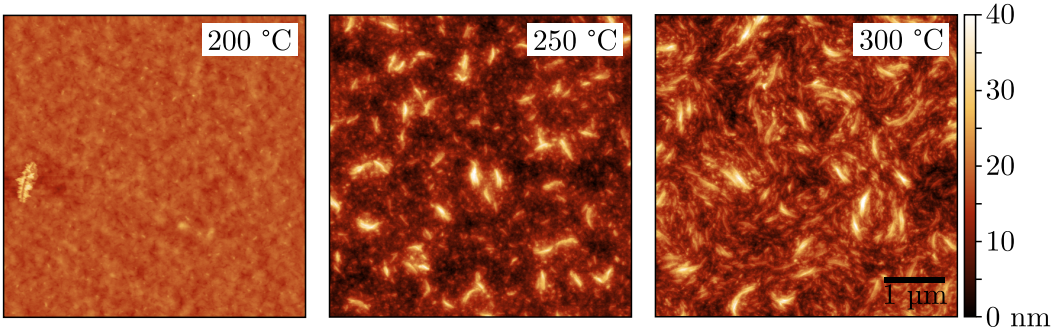

Figure 7.15: Atomic force microscopy images of P_1 layers annealer at different temperatures for 10 min**.** The emergence of structures through higher temperature annealing suggest molecular order in the thin films.

The PPP films obtained through annealing of precursor $\mathbf{P_2}$ were assessed next regarding their behaviour in organic transistors. For comparison reasons an identical device layout to the previously investigated devices was chosen. The transfer curves for two transistors annealed at 300 °C and 250 °C for 10 min can be found in figure 7.16. Surprisingly the observed semiconductor response of $\mathbf{PPP_2}$ was slightly inferior to the previously investigated $\mathbf{PPP_1}$. A possible reason for the inferior charge carrier transport properties might be the more bulky butoxy substituent, more likely to remain in the film disrupting intermolecular interaction and hampering charge carrier transport. Although the GIWAXS measurement indicate some sort of molecular order the degree

of order is rather weak thus a strong increase in charge carrier transport cannot be expected.

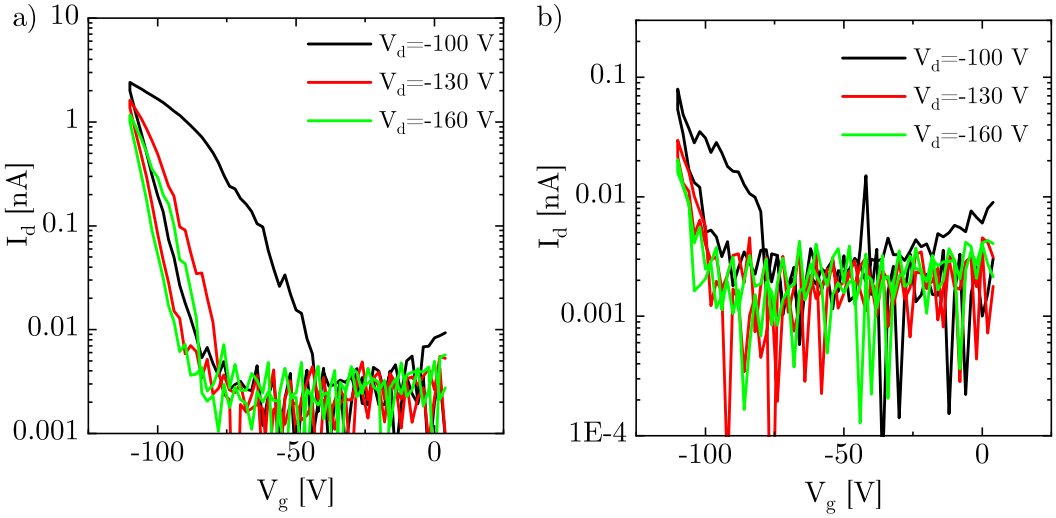

Figure 7.16: Transfer characteristics of transistors using PPP_2 as semiconducting layer. Annealing was done for 10 min at 300 °C(a) and 250 °C (b).

In conclusion the second generation precursors achieved the goal of reducing the conversion temperature while introducing a small degree of crystallinity. This increased order could not be translated into increasing charge carrier transport properties which might be a result of the novel side-chain used. Not giving up on the idea of the possibility that an increased order is beneficial for the mobility in the resulting PPPs, a third generation of precursor molecules in the form of oligomers was synthesized.

7.3 Third Generation Precursors: Oligomers

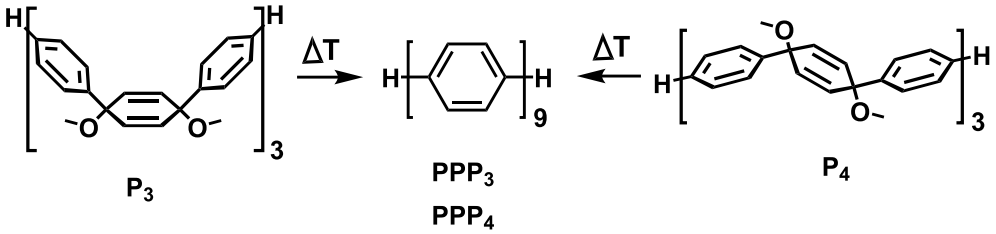

Figure 7.17: Chemical structure of the third generation oligomeric precursors P_3 and P_4. The reduced size of oligomers is expected to facilitate molecular rearrangement during conversion, resulting in higher order films.

As both syn- and anti-connected precursor polymers resulted in only modest charge transport properties caused by a no or low thin film order a third generation of precursor materials in the form of syn and anti oligomers was synthesized (see figure 7.17) to achieve a higher thin film order. To keep the novel materials comparable to $\mathbf{P_1}$ only methoxy groups were employed. Due to their smaller size oligomeric materials generally exhibit a stronger tendency for aggregation resulting in higher crystallinity. Furthermore both of the previously investigated precursor molecules already exhibited some sort of mass transport during the conversion process (apparent for example by the AFM images in figure 7.15 and figure 7.8). The reduced size of oligomers is expected to further improve this effects. This higher drive for aggregation comes at the expense of lower melting points and stronger dewetting behaviour in solution processing, two properties which can prove detrimental for device fabrication. As such $\mathbf{P_3}$ and $\mathbf{P_4}$ are promising candidates to further investigate the charge transport in PPPs.

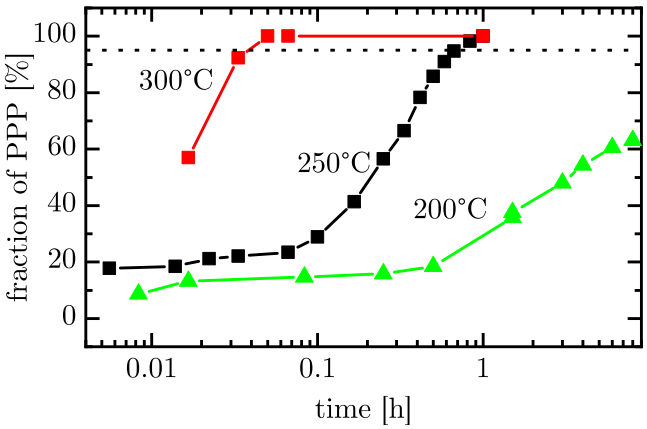

Figure 7.18: Fraction of converted P_4 as a function of time for different annealing temperatures. Full conversion (95 % due to an error of ≈5 %) is reached after 3 min at 300 °C or after 50 min at 250 °C. At 200 °C ≈ 65 % conversion is reached after 8 h. PPP fraction calculated from IR spectra. [134]

$\mathbf{P_3}$ was discarded after initial thin film heating experiments as it exhibits strong dewetting for temperatures surpassing 140 °C prohibiting the use of this precursor in devices. Thus, the conversion kinetics of $\mathbf{P_4}$ were investigated analogously to the previous two cases by Rainer Bäuerle via IR spectroscopy. The fraction of obtained $\mathbf{PPP_4}$ for different annealing times and temperatures can be found in figure 7.18. [134] For both 250 °C and 300 °C total conversion can be reached after annealing after 50 min and 3 min, respectively. This conversion speed is comparably to the ones obtained in $\mathbf{P_2}$. Conversion at 200 °C for 8 h on the other hand leads leads to $\mathbf{PPP_4}$ fraction of around 65 %. These conversion parameters will be utilized for a transistor study as a lower conversion temperature gives the molecules more time for aggregation improving the films crystallinity. Furthermore, incomplete aromatization was previously already found to not severely limit charge carrier transport (as long as sufficienty percolation paths

exist, see figure 7.5 and figure 7.6b). Figure 7.19 shows the transistor characteristics of a $\mathbf{P_4}$ device annealed for 8 h at 200 °C in the same device structure as used before. The device shows similar operation to the ones obtained from $\mathbf{P_1}$ with an average mobility of μ=2.8 × 10^{-7} $cm^2\,V^{-1}\,s^{-1}$ (4 Transistors). Severall effects might impede the charge transport here. While highly cristalline aggregates can improve the charge transport the connectivity between highly crystalline domains is crucial as well. Furthermore, incomplete conversion may have an impact on $\mathbf{PPP_1}$ as the here obtained $\mathbf{PPP_1}$ fraction is still below the value found in $\mathbf{PPP_1}$ of 80 %. This hypothesis is disproven by devices annealed for the same time at 220 °C which show similar device operation while they are expected to be further converted. Oligomers usually have an increased band-gap which could further lead to these low mobilities.[16] This was further supported through IR doping studies revealing a much lower doping efficiency of $\mathbf{PPP_4}$ in comparison to $\mathbf{PPP_1}$ attributed to a decrease in HOMO level through the shorter chain. [134]

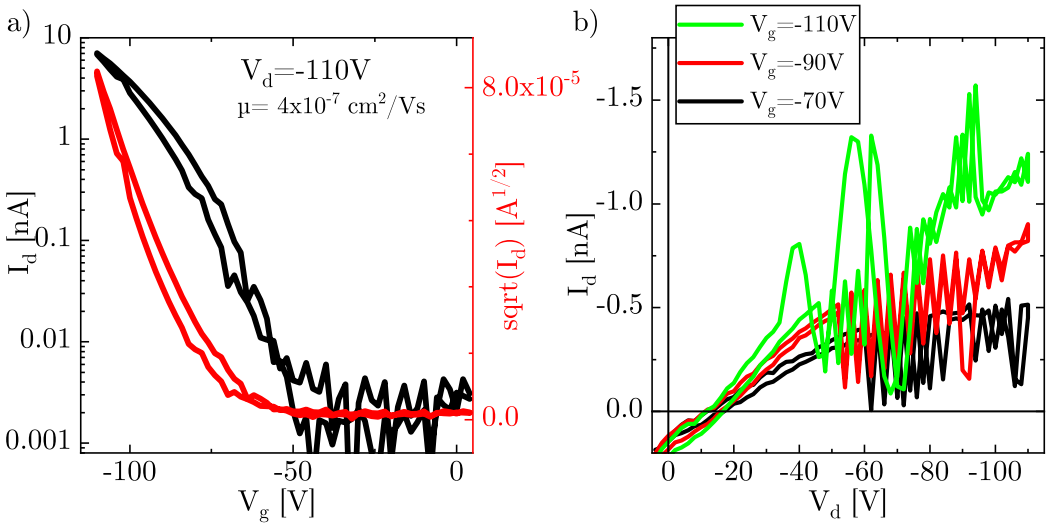

Figure 7.19: Transfer (a) and output (b) characteristic of a PPP_{40} transistor. The precursor was annealed for 8 h at 200 °C. At low currents the output measurements are frequently disturbed for unknown reasons.

To investigate the cristallinity of $\mathbf{PPP_4}$ thin films and explain their transistor performance AFM investigations of differently annealed films were carried out (see figure 7.20) Annealing of $\mathbf{P_3}$ leads to the previously mentioned dewetting. Annealing of $\mathbf{P_4}$ for 8 h at 200 °C leads to the formation of aggregates exhibiting a tightly packed structure of terraces. At 300 °C (1 h) high islands spaced several micrometers apart are formed. The structure obtained at 200 °C directly explains their transistor performance. The lacking connectivity of these structures through very thin amorphous regions leads to a charge carrier transport within the film impeded by the these amorphous region. The morphology at 300 °C on the other hand seems not suitable for good charge transport as these islands are spaced to far apart.

[16] UV-VIS or UPS spectra could elucidate this point.

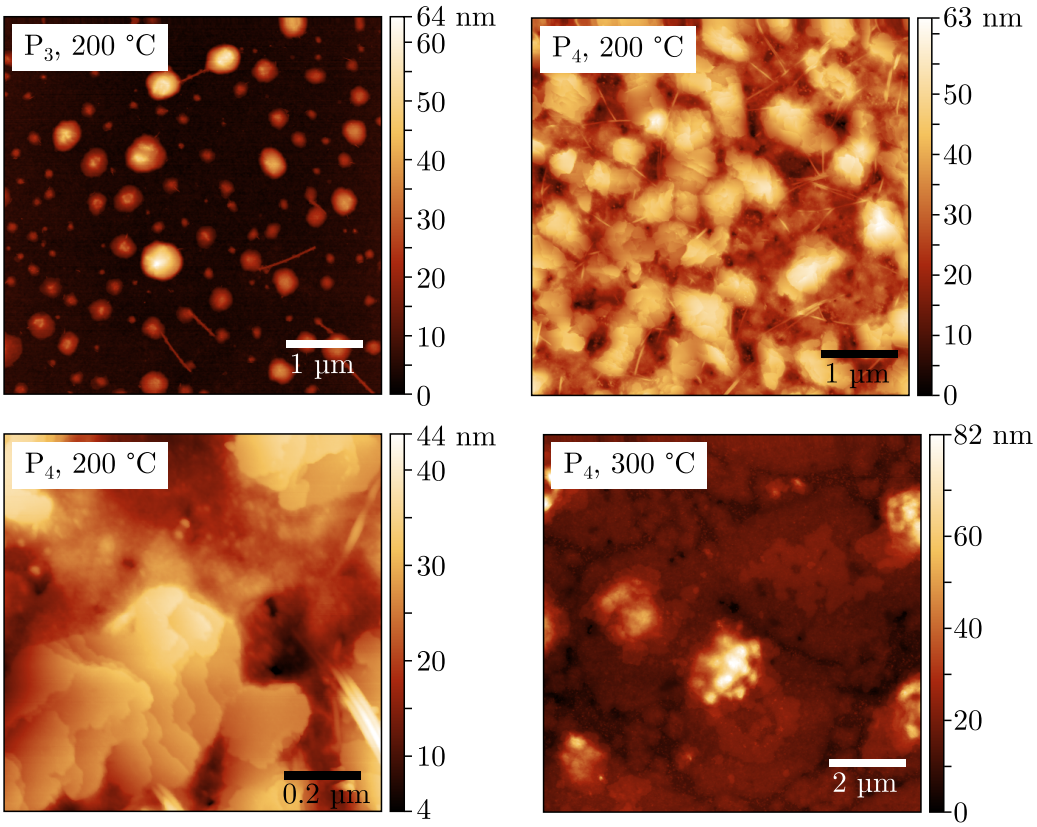

Figure 7.20: AFM images of annealed third generation precursor films. Films converted at 200 °C were annealed for 8 h while annealing at 300 °C was done for 1 h.

Thus the goal of an increased cristallinity was fully accomplished in the third generation precursor $\mathbf{P_1}$. It was accomblished to such an extend that the films were too crystalline for efficient charge carrier transport. Further studies into this material should thus employ a more complex annealing procedures increasing the size and connectivity of these aggregates to enhance the transport properties of these films. Alternatively a fourth generation precursor utilizing a slightly longer chain could decrease the cristallinity again while at the same time reducing the bandgap for better charge carrier injection.

7.4 Conclusion

Here various precursor routes to access pristine and unsubstituted Poly(*para*-phenylene) films were investigated regarding their conversion kinetics and semiconducting properties. Precursor conversion was carried out at elevated temperatures for different time periods while the conversion process was monitored through IR spectroscopy. The polimeric syn-precursor $\mathbf{P_1}$ was investigated in great detail first. Measurements in organic field effect transistors of fully converted films revealed only modest carrier transport properties (low mobility and high threshold voltage). This finding was attributed to the chemical structure of the precursor molecule. The big conformational change necessary from $\mathbf{P_1}$ to $\mathbf{PPP_1}$ was found as the underlying cause of the modest mobility observed. The combination of IR and transistor measurements revealed that already 80 % conversion is sufficient for fully saturated charge carrier transport properties, further illuminating the hypothesis of a suboptimal precursor molecule. $\mathbf{PPP_1}$ was further shown to be dopable with MoO_3 as observed through a change in transistor parameters and the formation of polarons as measured through IR spectroscopy. In conclusion it was clearly shown for the first time that unsubstituted PPP possesses indeed semiconducting properties although the here observed transport behaviour is far from ideal. While modifications of the precursors chemical structure towards anti-polymers achieved the goal of a reduced conversion temperature the charge carrier transport properties remained unchained. The films obtained from precursor $\mathbf{P_2}$ show a very modest increase in crystallinity, here believed to be far too modest to be translatable into improved charge carrier transport. Furthermore, this increase in order was bought at the price of a longer side-chain. This longer chain is suspected to possess a higher tendency to remain in the film where it can disturb intermolecular interaction and hamper the charge carrier transport. Thus, oligomeric syn- and anti-precursors were investigated next to achieve highly crystalline films. The syn-precursor was found to exhibit strong dewetting behaviour prior to conversion making him unsuitable for the fabrication of electronic devices. The oligomer-anti-precursor was found in the AFM to produce films of such high order that highly ordered aggregates were formed which were only weakly connected through much thinner amorphous layers. The resulting performance in transistors thus still bears room for improvements. Thus the aim of achieving a higher cristallinity material was fully accomplished. In conclusion, the here presented study gives valuable insights into the interplay between conversion kinetics and charge carrier transport properties of the obtained thin films. The oligomer-anti-precursor showed very promising structures in the AFM which can potentially lead to a high charge carrier mobility if properly optimized. Another approach would be to utilize a fourth generation precursor with a reduced crystallinity. These findings can further be applied easily for similar approaches to obtain insoluble films of different target molecules.

8 Cross-linking Organic Semiconductors through Electron Irradiation

The fabrication of efficient electronic devices requires precise control over the shape and location of the different functional layers involved (e.g. electrodes, semiconductors and insulators). For different material types and required spacial resolutions, various patterning techniques such as photo-lithography or thermal evaporation with shadow masks were developed. Electron-beam lithography (EBL) patterns materials through the controlled irradiation with electrons, offering resolutions in the nm range at the cost of a low processing speed. Here organic (semiconducting) materials featuring cinnamic acid derivatives shall be investigating regarding their response to electron irradiation. At the moment, patterning of organic semiconducting materials through electron beams is still in its early stages but could enable novel fabrication techniques and device layouts for electronic devices. After a brief introduction into the fundamentals of EBL the here used model system of cinnamic acid derivatives shall be presented. Then, electron induced cross-linking will be shown in a proof-of-concept study. Finally, a cinnamic acid functionalized semiconducting polymer is cross-linked and investigated in transistors.

This chapter is the result of collaboration of different research group, providing the necessary expertise for this project. Chemical synthesis was carried out by Maximilian Bojanowski from the research group of Prof. Bunz.[1] IR spectroscopy, EBL patterning and DFT calculations were carried out together with Christian Huck and Michael Tzschoppe from the group of group of Prof. Annemarie Pucci.[2] Lisa Veith from the group of Prof. Rasmus Schröder recorded the SEM images.[3] A publication describing this work is under preparation. [135]

8.1 Fundamentals of Electron Beam Lithography

Irradiating material with electron beams triggers a number of different processes where their nature is strongly influenced by the electrons energy. In the energy range of a typical EBL experiment (5 keV to 50 keV) the primary electrons do not strongly interact with matter due to their low cross sections at these energies but rather generate secondary electrons through inelastic scattering. These secondary electrons ($<$50 eV) are responsible for the majority of processes induced through the electron irradiation. [136] Secondary electrons are known to excite or ionize molecules or even break connecting

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[2] Kirchhoff-Institut für Physik, Universität Heidelberg
[3] Bioquant, Universität Heidelberg

bonds. As such, electron induced chemistry was studied in a variety of molecules in either mono or multilayers. [137, 138] Ethanol could be synthesized for example through the irradiation of a frozen water/ethylene mixture. [137] In Focused Electron Beam Induced Deposition (FEBID) organo metallic complexes are irradiated with hard electron radiation, resulting in quasi metallic structures of arbitraty shapes through complete elimination of the organic substitutions. EBL uses electron radiation to locally alter the solubility of a given resist generating a pattern in the process (see Figure 8.1). First, a thin layer of resist is deposited on a substrate and exposed to electron radiation. This changes the solubility of the materials so that a development step in a suitable solvent will either wash away the exposed/unexposed material depending whether a positive/negative tone resist was used. The amount of radiation needed to fully expose a given structure is dependent on the film thickness, the beam energy, the feature size and the resist itself and is usually given in $\mu C\,cm^{-2}$. As such tremendous work has been invested into the development of a wide variety of different resists for different EBL applications. [18]

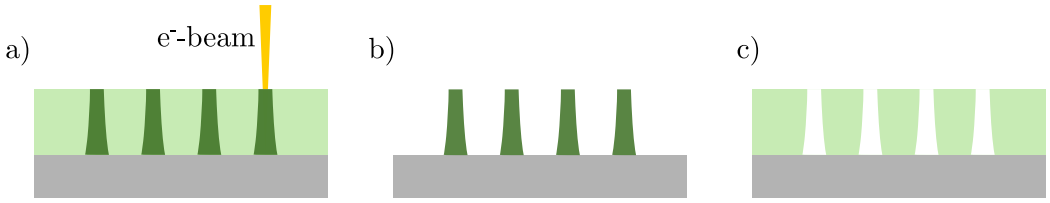


Figure 8.1: Sketch of a typical EBL Process. a) Irradiating a thin resist layer results in chemical changes where the sample was irradiated. After development, a negative tone resist (b) shows remaining material where at irradiated areas while a positive resist (c) results in the inverse pattern. Forward scattering of electrons may broadens the written pattern resulting in the here shown exemplary profiles (e.g. undercut in positive resists).

The quality of the written EBL structure depends on a number of factors. The primary energy of the electron beam directly influences the degree of forward scattering sharpening the structures for higher energies while increasing the necessary dose as a higher energy interact more weakly with matter. The shape and density of the structure written also influences the necessary dose as the proximity to an already written structure may result in a partial exposure through scattered electrons (this effect is called the proximity effect). Thus bigger structures usually require a smaller dose. Furthermore, charging of the thin film can alter the electron beams trajectory decreasing the overall resolution. As these numerous processes may adversely effect the resolution and quality of EBL written structures a lot of optimization is required for highly resolved lithography.

The main focus of this study was placed on the fundamental nature of the cross-linking process, the question weather organic functional materials can be cross-linked through electron beams and weather they retain their functionality in the process. In the field of EBL insulating resists are often used as a patterning stencil to structure another material (e.g. a therafter deposited metal film via a lift-off process). Thus, organic functional

materials have been patterned through electron beam irradiation very sparingly in the past. Persson et al. patterned in 1996 poly(3-octylthiophene) and doped the obtained structure resulting in ohmic conduction through the up to 50 nm thin channels. They proposed an unspecified cross-linking between the polymer chains but did not further investigate this process. [20] Similar but unstructured insoluble conductive thiophene films were obtained by Kock et al. in the same year. [21] Hikmet et al. fabricated multi coloured OLEDs through the irradiation of different Poly(p-phenylen-vinylen) (PPV) polymers. Cross-linking was explained through a radical process between the polymers side chains. [22] Here a more systematic approach will be taken studying the cross-linking process in greater detail where further (chemical) analysis of the cross-linked films will be done.

8.2 Cinnamic Acids and its Derivatives

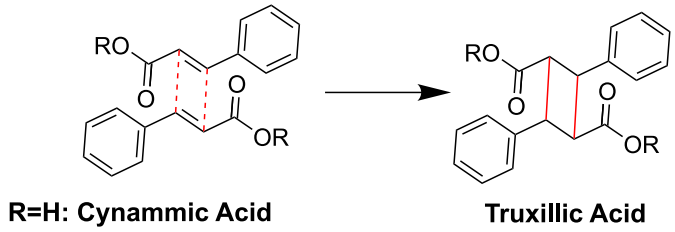
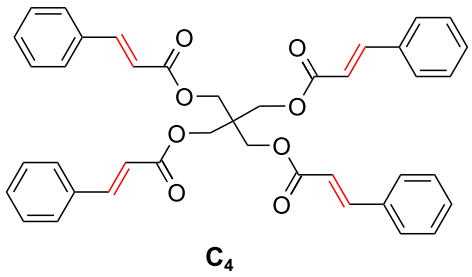


Figure 8.2: Cross-linking of cinnamic acid (R=H) into truxillic acid. Cross-linking is usually done through UV light. Cinnamic acids can be attached at position R to various functional building blocks.

Immobilization of organic functional materials can be achieved through a number of different mechanisms. [85, 139] The two most common approaches focus on the cleavage of a solubility mediating side group rendering the remaining material insoluable or on the cross-linking of the materials substituent to form an insoluble macromolecule. The two most common stimuli to trigger these reactions are either of thermal or photochemical nature. Here cinnamic acid derivatives shall be used for investigations into the cross-linking of organic functional molecules. Cinnamic acids are already very well understood in their light induced cross-linking behaviour. [140–142] Figure 8.2 shows the cross-linking of two synammic acid molecules through irradiation of light into truxillic acid. Cross-linking is done through a [2+2]-cycloaddition requiring one of the cross-linking partner to be in its excited state rendering these reactions thermally inaccessible. This adds the benefit that local heating through the electron beam can be excluded as a potential cause for cross-linking. Photon induced cross-linking of cinnamic acid derivatives was already investigated in the past in the research group of Prof. Bunz where such materials were applied as emissive and injection layers in OLEDs. [143, 144] The starting hypothesis of this project is that not only irradiation by light but also irradiation by electrons can excite these groups resulting in successful cross-linking. Then,

a vast number of different EBL pattern-able functional materials can be easily synthesized where the cinnamic acid group is responsible for the cross-linking while the desired functionality (e.g. conductive, semi-conductive, high optical absorption,...) can be introduced as a rest (R in figure 8.2). This approach is viable as long as the amount of (possible) additional reactions induced within the rest through the e-beam can be controlled.

8.3 Proof of Principle



C_4

Figure 8.3: Chemical structure of C4. The here in red shown double bonds can undergo [2+2]-cycloaddition to form extended macromolecules.

First, a proof of concept study was carried out to verify the hypothesis that cinnamic acids can indeed be cross-linked through electron irradiation. Initial investigations started from pure unsubstituted cinnamic acid. It was quickly discovered that this material use as a perfume ingredient comes form its low vapour pressure making it unsuitable for vacuum applications such as EBL. Thus, the simpel cinnamic acid tetramer (C4) was synthesized which is shown in figure 8.11. The double bond in each of the four arms can cross-link with its neighbouring molecule to form large macromolecules. We also expect that cross-linking to itself can happen to some extend forming a compound close to truxin acid. C4 was processed through spin-coating from a $6\,\mathrm{mg\,mL^{-1}}$ chlorobenze solution on plasma cleaned silicon substrates resulting in a film of around 50 nm thickness. First, the IR spectrum of a pristine C4 film was recorded by Christian Huck from the Pucci group (see figure 8.4). Via density functional theory (DFT) calculations, the individual peaks can be assigned to specific molecular vibrations.[4]

Cross-linking of C4 can be quantified by the a number of peaks of which some are identified in figure 8.4. The C=C stretching oscillation at around $1630\,\mathrm{cm^{-1}}$ will be completely suppressed in fully cross-linked films through the formation of the cyclobutane ring. Past work further found a shift of the C=O oscillation at $1710\,\mathrm{cm^{-1}}$ towards higher energies. [141] Here the double peak in the fingerprint region above and below $700\,\mathrm{cm^{-1}}$ shall be used as an additional metric for successful cross-linking of C4. [5]

[4] DFT calculations by Michael Tzschoppe, IR spektra measured together with Christian Huck.

[5] The peak at 980 nm from the out off plane twisting vibration of the C-H bonds located at the C=C bonds can be used as another indicator for conversion.

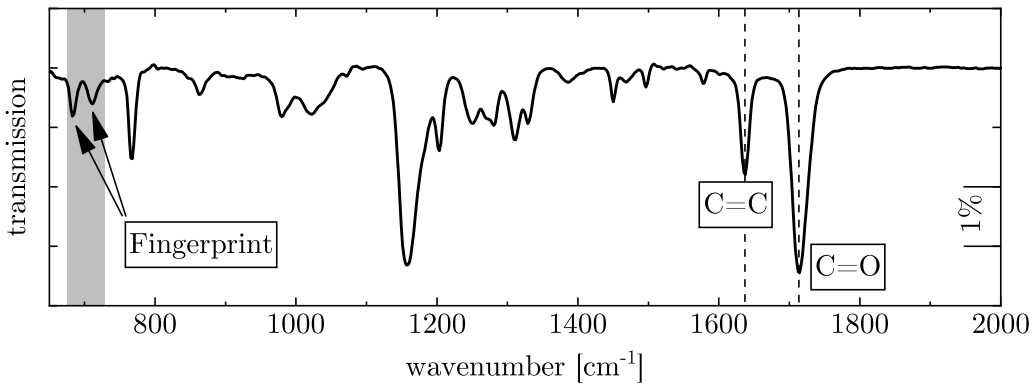


Figure 8.4: IR transmission spectra of a pristine C4 film. Both the C=C and C=O peaks (marked by vertical dashed lines) and the two peaks inside the shaded fingerprint area will be used as to track the cross-linking reaction.

8.3.1 Light Induced Cross-Linking

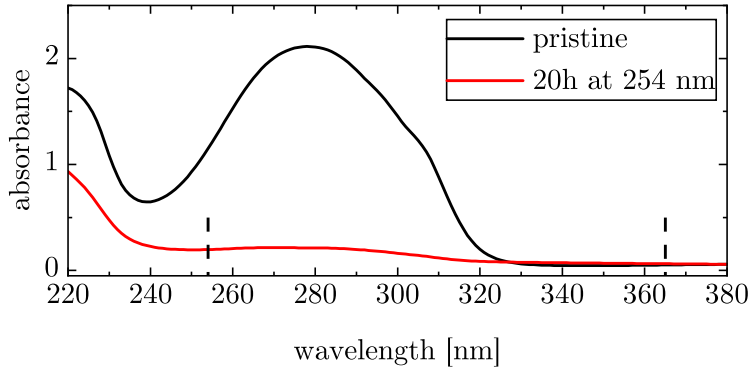


Figure 8.5: Absorption spectra of a C4 film in its pristine (black) and cross-linked form (red). The horizontal dashed line indicate the wavelength at which C4 was irradiated. Irradiating at 365 nm results in no cross-linking due to the lacking absorption at this wavelength.

Having understood the IR spektrum of pristine C4, light induced cross-linking of this material was investigated in order to obtain an IR spektrum of a successfully linked film. First, the absorption spectrum of C4 was measured (see figure 8.5), showing only an absorption band in the deep UV.[6] Next, films were irradiated by UV light to induce cross-linking. UV irradiation was done in a glove-box with UV light from a hand held UV tube (25 W electrical) of different energies (254 nm and 365 nm). It was found that irradiation with 365 nm did not result in any cross-linking as can be expected from the very low absorption at this wavelength. Irradiation at 254 nm resulted

[6] The absorption of C4 is close to the one of pure cinnamic acid. Extending the comparably small conjugated system of cinnamic acid can shift its absorption towards lower energies.

in successful cross-linking which disbands the conjugated system at the double bond strongly reducing the absorption peak at 280 nm.

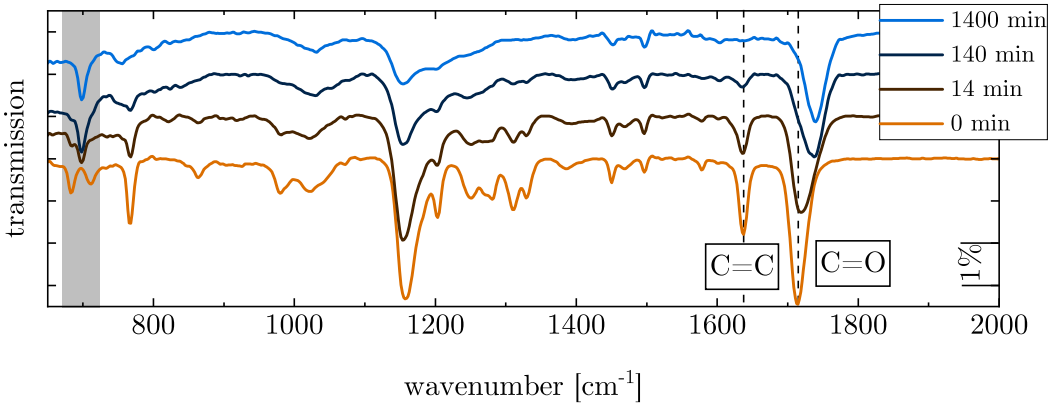


Figure 8.6: IR spectra of C4 films irradiated with UV light for increasing time periods. Irradiation at 254 nm for increasing time periods leads to the conversion of the double peak to a single peak in the fingerprint region (shaded area), a strong decrease of the C=C oscillation and a shift of the C=O oscillation (dashed lines) all indicating cross-linking.

Figure 8.6 shows IR spectra for different irradiation times at 254 nm. A clear decrease of C=C (1630 cm^{-1}) double bond upon irradiation can be seen as well as a small decrease an a shift to higher energies of the C=O oscillation. Furthermore the double peak (below and above 700 cm^{-1}) in the fingerprint region vanishes and is replaced by a single peak at 700 cm^{-1} further indicating successful cross-linking. The peak intensity of all peaks decreases which can be explained by the overall decreasing molecular order induced through the cross-linking. Furthermore, degradation through the UV light may also contribute to this finding.

Cross-linked films are believed to form large macromolecules reducing the films solubility untill completely insolubility is reached. Thus, the irradiated films were developed by washing them in room temperature chloroform for 10 s and drying them with a nitrogen gun, removing all non cross-linked material. Fully or nearly fully cross-linked films could not be washed away as can be seen from Figure 8.7. This finding is supported by film thickness measurements revealing that films irradiated for 140 min and 1400 min show thicknesses identical to pristine ones while irradiation for 14 min does not induce enough cross-linking so the films are completely washed away. The appendix shows the full film retention curve, which is the film thickness after development as a function of stimulus (here the UV-lights duration). Having established successful cross-linking of C4 through UV light irradiation with electrons can be investigated next.

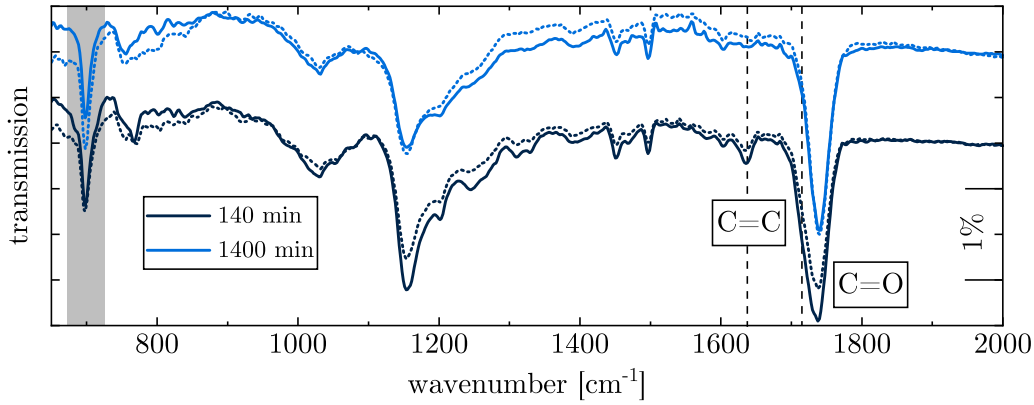


Figure 8.7: IR spectra of two UV irradiate C4 films before and after development. Films were cross-linked at 254 nm for 140 min and 1400 min, respectively (solid lines). After development these films exhibit only a small decrease in peak intensities (dotted lines). The shaded area and dashed vertical lines are the metrics indicating the degree of cross-linking (see figure 8.4 and text for more details).

8.3.2 Electron Induced Cross-Linking

Films processed identically to the before investigated samples were irradiated in an electron beam lithography setup with 10 keV. A broad interval of doses was chosen of $1\,\mathrm{mC\,cm^{-2}}$ to $5\,\mathrm{mC\,cm^{-2}}$. Two different patterns were written. First, a set of $250\,\mu\mathrm{m}^2$ pads with different doses were written for IR measurements. An area of $250\,\mu\mathrm{m}^2$ was chosen as a compromise between the required write time (increasing with pad area) and the signal intensity in the IR spectroscopy (decreasing with pad area). Second, the 1951 USAF resolution test chart was written with different doses to determine the achievable resolution.

First, the IR spectra of the pads were investigated via IR microscopy before and after development (see figure 8.8). Clear signs of cross-linking can be found in the spectra before development. First, the double peak in the fingerprint region vanishes and is replaced by a peak at $700\,\mathrm{cm^{-1}}$. Secondly, a strong decrease of the C=C at around $1630\,\mathrm{cm^{-1}}$ in combination with the shift of the C=O peak are further signs of cross-linking. Furthermore, a strong decrease in all peaks can be seen, stronger then in the previous spectra of films irradiated by UV light (UV spectra in figure 8.6). This stronger decrease is most likely the product of molecular degradation since high energy electron radiation can also cause bond fissure, partly destroying the investigated molecules. After development the pads with doses of $2.5\,\mathrm{mC\,cm^{-2}}$ and $5\,\mathrm{mC\,cm^{-2}}$ show identical film thickness (40 nm) but the IR spectra from figure 8.8 clearly reveal that soluble material remained before development subsequently removed through the development step. We attribute this behaviour to the formation of a cross-linked scaffold in which partly soluble material is incorporated which can be removed through development (see

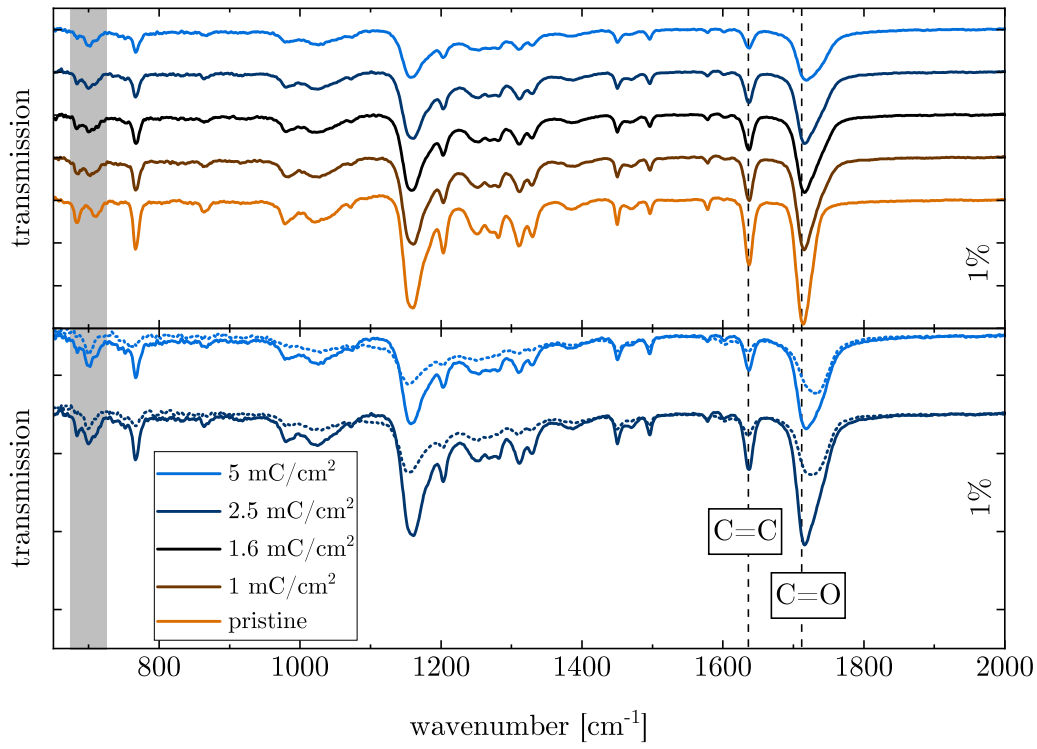


Figure 8.8: IR transmission spectra of C4 films irradiated with increasing electron doses (top) and comparison to spectra after development (bottom). IR spectra before development (solid lines) exhibit a conversion of the two fingerprint peaks into one (shaded area), a decrease of C=C peak and a shift of the C=O oscillation (see vertical dashed lines) for increasing doses, indicating an increasing amount of cross-linking. A comparison of IR spectra befor/after development (solid/dotted lines at the bottom) indicate a decrease among all peaks through development. Irradiation at 10 keV.

appendix for film retention curve). AFM investigations of this behaviour do not show a high porosity on the investigated scale (10 nm), indicating rather small pores.

8.3.3 Comparing UV and EBL Cross-Linking

Figure 8.9 shows a comparison of IR peak area of the C=C and C=O peak for different amounts of cross-linking.[7] Cross-linking via UV light results in an immediate strong decrease of the C=C while the C=O peak exhibits a slight decrease in peak area. Cross-linking via EBL conveys a mucher slower decrease of the peak area in the C=C peak with respect to the C=O peak. Furthermore, the peak area of the C=O reaches lower values in EBL than in UV and vice versa for the C=C peak. This behaviour is most likely the result of an interplay between conversion and degradation. In comparison to EBL, UV

[7] The calculation of the peak area was done by integrating the IR spektrum from 1615 cm^{-1} to 1670 cm^{-1} and 1675 cm^{-1} to 1800 cm^{-1} for he C=C and C=O peak, respectively

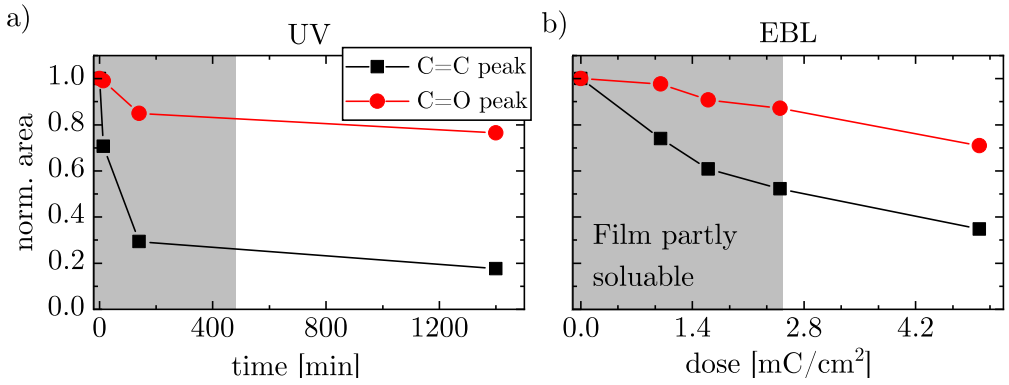


Figure 8.9: Normalized area of the C=O and C=C IR peak for increasing amount of UV (a) and EBL radiation (b). Both UV and EBL radiation lead to a strong decrease of C=C peak area while the C=O area is only weakly reduced. While the decrease in the C=C is much more pronounced for UV radiation, both UV and EBL show different decay rates for the C=C and the C=O peak indicating successful cross-linking. Calculated from figure 8.6 (UV) and figure 8.8 (EBL).

cross-linking with the here used wavelength is a resonant process where the exciting stimulus (UV light) is more or less in resonance with the required excitation (band gap) so that all of the energy is transformed into the formation of an excited state leaving little excess energy for degradation of the molecule. Formation of the excited state in EBL on the other hand is the result of a bombardment with a broad distribution of secondary electrons ($<$50 eV) leaving ample room for additional degradation processes. Calculating the normalized C=O to C=C peak ratio gives figure 8.10, further supporting this explanation. The Peak ratio can be seen as a measure of the conversion degree taking a value of 1 for unconverted films and ∞ for fully converted films. Cross-linking via UV and EBL leads to a linear increase in peak ratio in the here shown semi-logarithmic plot indicating the same common process. Since UV cross-linking is done via [2+2]-cycloaddition the same process can be assumed to be responsible for EBL irradiation, albeit their different degradation rates

8.3.4 Patterning C4 Films

Figure 8.11 shows the images of the 1951 USAF resolution test chart written with a dose of 5 mC cm^{-2}. Both SEM and AFM images indicate that sub 100 nm resolution can be achieved. Larger structures are better resolved as they need a smaller dose through the proximity effect. A test chart with dose 8 mC cm^{-2} more clearly resolves the smaller structures but leads to over-exposure of larger structures which results in a decresed resolution. This trend can be further proven when locking at the film thickness after development as a variation of dose which is given in the appendix. This film retention curve clearly shows that bigger structures need less dose.

In conclusion, it was clearly shown that cross-linking of C4 is possible not only possible via UV but also through electron radiation. It was found that EBL cross-linking leads to

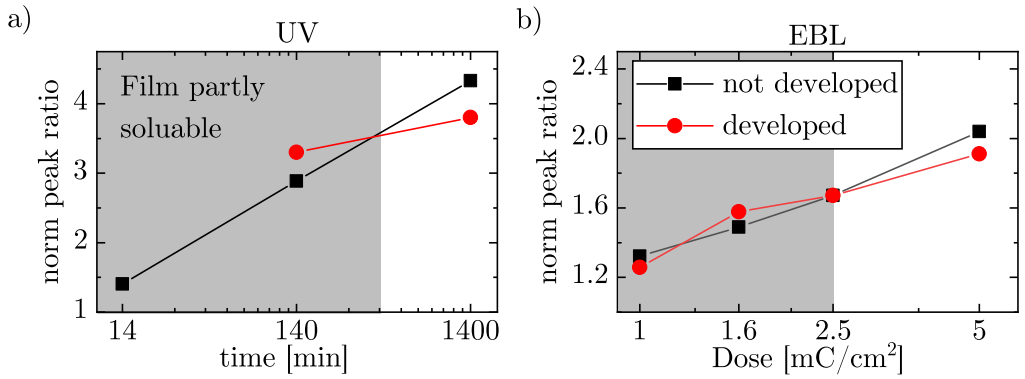


Figure 8.10: Normalized C=O to C=C peak ratio for increasing amounts of UV (a) and EBL dose (b) before and after development. Both types of radiation exhibit an increase in normalized peak area for increasing time/dose. Within the measurement window UV radiation reaches a much higher peak ratio. Normalized to the value at time/dose zero. See figure 8.9 for peak areas.

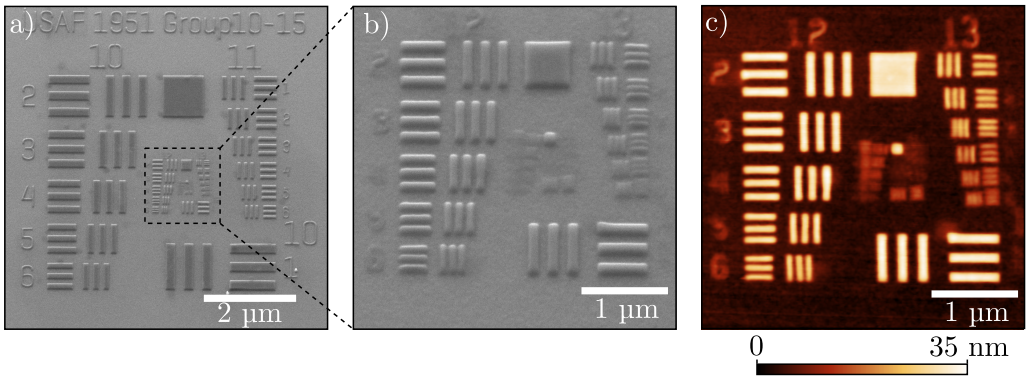


Figure 8.11: SEM (a/b) and AFM (c) images of an EBL written resolution test chart after development. Areas irradiated by electron beams can be seen on the substrate while those without irradiation were washed away, indicating successful de-solubilization. The test chart was written at $5000\,\mu C\,cm^{-2}$. b) and c) depict the same part of the structure.

much a stronger degradation of the material due to the broadly distributed energy of the secondary electrons triggering the cross-linking. Sub 100 nm pattern could be written in C4 films using EBL. The possibility of patterning in the nm-domain in combination with their ability for easy functionalization give cinnamic acid derivates the promise of a wide application as EBL processable funtional materials. Thus, a semiconducting polymer with cinnamic acid containing side-chains will studied next.

8.4 Cross-Linking Semiconductors

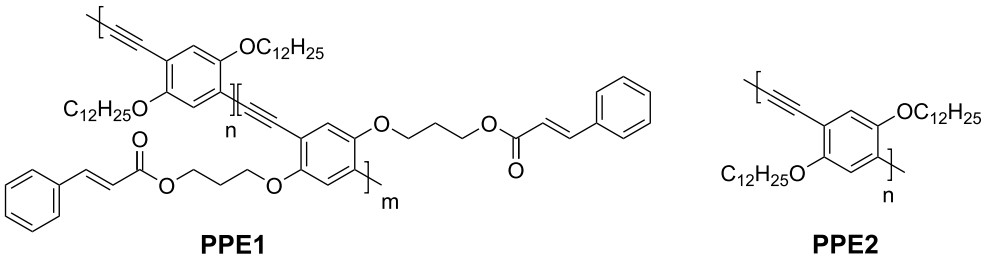


Figure 8.12: Chemical structure of the used Poly(*para*phenylene-ethynylene)s (PPEs). PPE1 is copolymer of a simple dodecyloxy side-chain and a cinnamic acid containing monomer. **PPE2** acts as a reference material with only dodecyloxy side-chains.

Poly(*para*phenylene-ethynylene)s (PPEs) are a class of semiconducting polymers widely studied in a variety of organic electronic devices ranging from field-effect transistors to light emitting diodes. [145–149] Melt annealed PPEs containing dodecyloxy side-chains are know to form nanowire structures which were highly investigated in transistors resulting in charge carrier mobilities of up to $0.1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. [150] Here such materials shall be investigated for patterning through EBL. Figure 8.12 shows the chemical structure **PPE1** a copolymer of a cinnamic acid containing monomer in combination with a dodecyloxy monomer. **PPE2** is a simple dodecyloxy PPE homopolymer serving as a reference material.[8] Both materials were readily solvable in toluene and were processed via spincoating into films of ≈40 nm thickness. **PPE1** was processed as far as possible in the dark to prevent premature cross-linking of the cinnamyl sidechains.

As dodecyloxy PPEs only show a high charge carrier mobility in melt annealed devices the melting point of both materials was investigated first. TGA/DSC measurements in combination with heat stage microscopic images revealed that tempering at 170 °C/205 °C results in completely molten films of **PPE1**/**PPE2**, respectively. Melt annealing was thus done at these temperatures for one minute to prevent material degradation and dewetting, two effects which can occure for prolonged heating. Figure 8.13 shows AFM pictures of the resulting nano-structures. Comparing the two images show a clear suppression of nanowire formation through the introduction of the more bulky cinammyl side-chain. Nevertheless, nanowire formation is still visible in **PPE1**. While thermally activated cross-linking of the cynnamic acid side-chains via [2+2]-cyloaddition is prohibited the occurrence of main-chain cross-linking of PPEs remains unclear. [147] As both material posses the same main chain this process is expected to happen in both materials.

[8] PPE1 was synthesized by Maximilian Bojanowski while **PPE2** was provided by Emmanuel Smarsly (both from the group of Prof. Uwe Bunz).

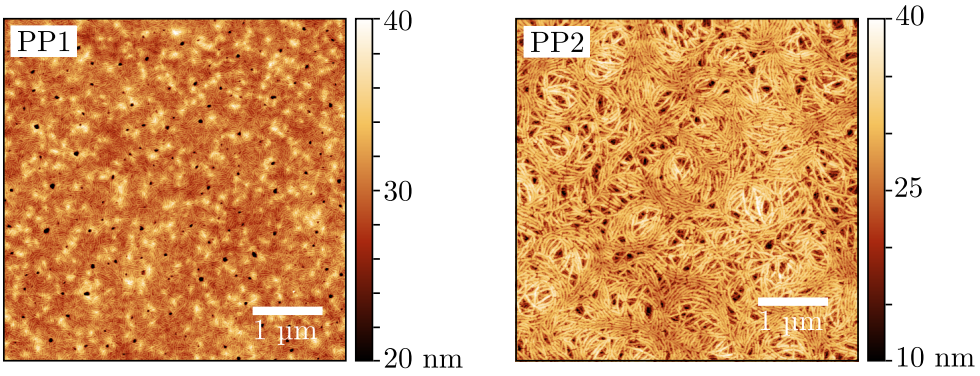


Figure 8.13: AFM images of melt annealed PPE1/PPE2 films. The introduction of the cinnamyl sidechains in **PPE1** has led to a significantly suppresses formation of nanowires. Pristine films of both materials do not show any signs of nano-structures.

8.4.1 Pristine Transistors

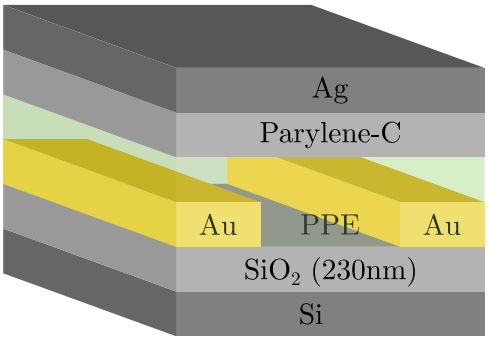


Figure 8.14: Dual gate layout of the here used transistors. A dual gate layout was chosen as it allows investigations into the charge carrier transport at both the top and the bottom interface.

To investigate the semiconducting properties of **PPE1** dual gate transistors were fabricated by using pre-patterned substrate and adding a second gate through the deposition of Parylene-C and Ag on top of the substrates (see figure 8.14). The prefabricated substrates consisting of interdigitating gold contacts ($W = 10\,\text{mm}$, $L = 20/10/5/2.5\,\mu\text{m}$) on top of a Si/SiO_2 (SiO_2 thickness: 230 nm). The results of an exemplary top gated transistor measurement with a melt annealed **PPE1** film as semiconductor can be found in figure 8.15. The high turn-on voltage in combination with the observed s-shape suggest the occurrence of a substantial injection barrier. Assuming that both **PPE1** and **PPE2** have similar ionization potential, the literature value for **PPE2** of 5.3 eV suggest an injection barrier as well. [148] The results of 19 measured **PPE1** transistors can be found in table 8.1. Two clear trends can be seen. The charge transport properties are significantly improved through melt annealing (1 min at 170 °C) while top-gated tran-

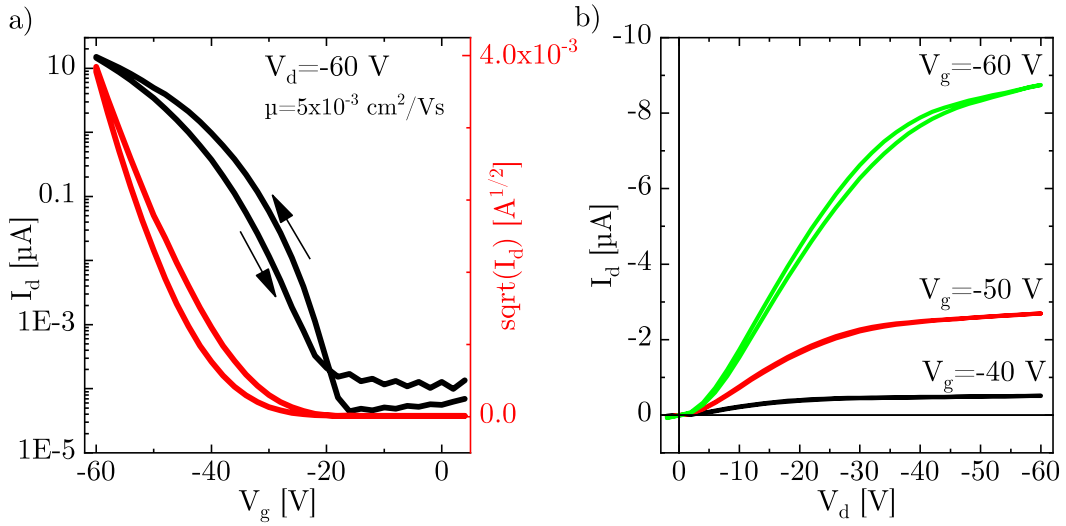


Figure 8.15: Exemplary transfer (a) and output (b) charateristic of a melt annealed PPE1 transistor. The high turn-on voltage ($-20\,\mathrm{V}$) and the s-shaped output curve indicate an injection barrier, very plausible from the assumed IP (L=$10\,\mu\mathrm{m}$).

Table 8.1: Parameters of PPE1 transistors for different annealing and gating. Melt annealing and top gating both improves transistor performance (V_d=$-60\,\mathrm{V}$).

gating	melt annealed	mobility [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	turn-on voltage [V]	max. current [μA]
top	yes	$(6 \pm 2) \times 10^{-3}$	-26 ± 3	13.9 ± 0.8
	no	$(11 \pm 3) \times 10^{-5}$	-42 ± 2	0.1 ± 0.1
bottom	yes	$(9 \pm 2) \times 10^{-4}$	-27 ± 3	6 ± 3
	no	$(2 \pm 1) \times 10^{-5}$	-45 ± 3	0.011 ± 0.006

sistors show a better performance than those gated from the bottom. The influence of gating on transistors performance is not surprising as bottom-gate transistors suffer from the same pitfalls as the ones investigated in chapter 7 in that the SiO_2 surface hampers charge transport. Bottom gate transistors show the same shift in turn-on voltage and hysteresis seen before (see appendix). Thus, the third measured transfer curve was evaluated for this table. The here observed mobilities are slightly inferior to those obtained from **PPE2** (see appendix for devices or Literature). [147, 148] The reduced mobility can be explained through the added cinnamic acid sidechain hampering the nanostructure formation.[9] Having established a baseline for the charge transport properties of **PPE1** the possibility of EBL cross-linking this material can be investigated.

[9] It was found that untempered PPEs or PPEs who do not form a nanostructure all exhibit mobilities in the range of $1 \times 10^{-5}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $1 \times 10^{-4}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$.

8.4.2 Cross-Linking via Electron Radiation

An initial test of the cross-linking behaviour of **PPE1** was done at 3 keV on a thicker then usual melt annealed film of 130 nm to increase the signal of the C=C and C=O groups in the IR. Irradiation was done in a standad scanning electron microscope.[10] Due to the low amount of cross-linkable side-chains we expected the IR spectrum to show only a low signal in the region used for conversion tracking. A too high film thickness on the other hand is very far from the final applications.

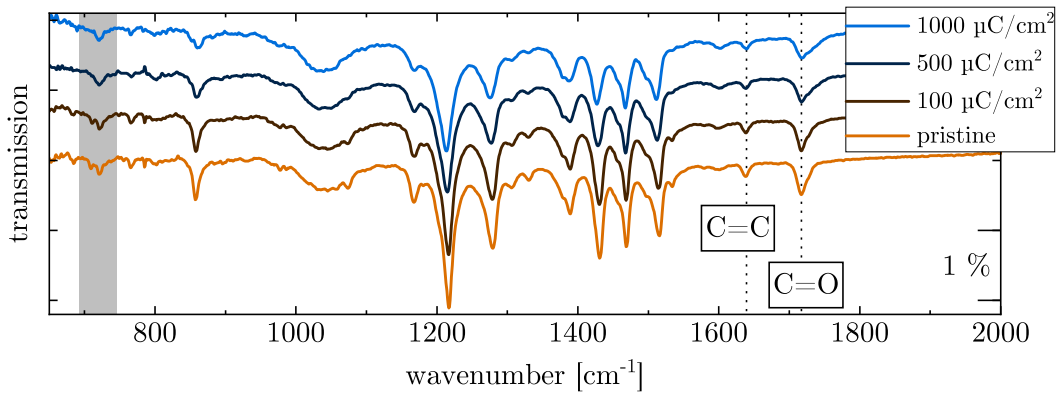


Figure 8.16: IR spectra of PPE1 films for increasing electron doses. Increasing electron doses leads to the conversion of a double peak to a single peak in the fingerprint region (shaded area), a strong decrease of the C=C oscillation and a shift of the C=O oscillation (dashed lines). These changes all indicate cross-linking of the cynammic acid side-chains.

Figure 8.16 shows the IR spectra of **PPE1** for increasing electron dose. Due to the small amount of cross-linkable groups the peaks of interest are rather weak. Nevertheless, a decrease of the C=C peak at 1630 cm^{-1} in combination with the broading of the C=O peak at 1720 cm^{-1} indicate some degree of cross-linking. Furthermore a change in the fingerprint region is also visible. Further irradiation with electrons (up to 10 $mC\,cm^{-2}$) leads to degradation of the material characterised by a monotonous decrease of all peak intensities. It is highly unlikely for all cinnamic acid groups to find a cross-linking partner due to the scarcity of this side-chain. Thus, it is very likely that some amount of unreacted groups will prevail. After a development for 10 s in room temperature chloroform AFM and Dektak measurements were carried out. It was found that even in unirradiated parts of the film roughly half of the film thickness (65 nm) remained. The pad with 100 $\mu C\,cm^{-2}$ already showed a post development thickness of 110 nm. Thus, 85 % of the previously 130 nm thick film remained. For the 500 $\mu C\,cm^{-2}$ and 1000 $\mu C\,cm^{-2}$ pads the full film thickness remained after development, indicating that only small doses are needed for full film retention. The fact that nearly half of the films thickness remained in non-irradiated samples be explained by the low solubility

[10] Together with Lisa Veith.

of **PPE1** which is even further decreased by the here done melt-annealing.[11] Melt annealed films of **PPE1** could not be removed by either hot toluene or hot N-Methyl-2-pyrrolidon (NMP). It was found that toluene in combination with ultrasonication for 5 min was able to fully remove the layer. While ultrasonication fully removes melt annealed films irradiated patches do not exhibit any loss of material hinting towards strong cross-linking through the electron irradiation.

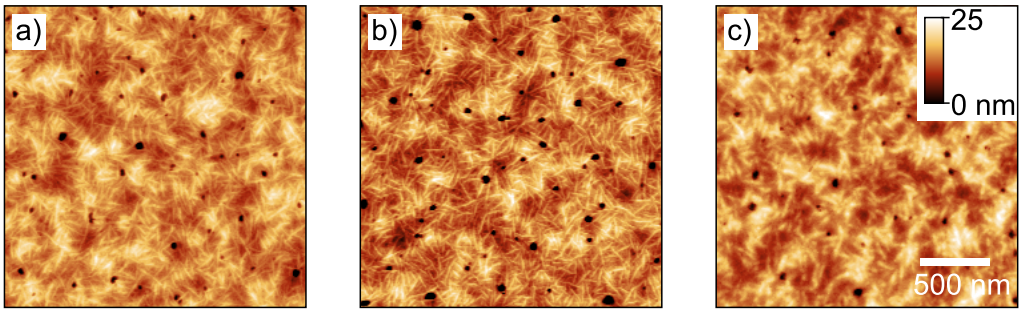


Figure 8.17: AFM images of melt annealed PPE1 films. a) Film previous to electron irradiation, b) after irradiation and c) after development. The clear change in "sharpness" indicates degradation of the top layers through ultrasonication, potentially hampering charge carrier transport at this interface.

Figure 8.17 shows AFM images of the same pad in its pristine state, irradiated by 500 $\mu C\,cm^{-2}$ and after a subsequent ultrasonication. While irradiation seems to have no effect on the morphology of the top layers the "sharpness" of the nano-structure is decreased through ultrasonication which we explain by irregular ablation of the top most layers. While irradiation of the reference material **PPE2** results in some film retention for normal development in chloroform these films are fully removed through ultrasonication (see appendix for IR spectra and AFM images). Thus, the here observed cross-linking behaviour is exclusively the result of the introduced cinnamic acid containing sidechain. In the next step the cross-linked layers will be invastigated in transistors.

[11] Melt annealing of **PPE2** was found to strongly increase its order suspected to prevent a rapid dissolution. [147] Furthermore, main-chain cross-linking may further decrease its solubility.

8.4.3 Patterning Transistors

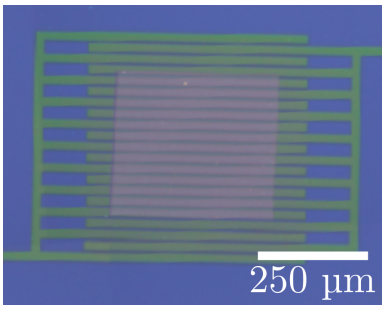


Figure 8.18: Cross-polarized microscopy image of a structured PPE1 transistor. The **PPE1** was structured through cross-linking at 3 keV with $500\,\mu C\,cm^{-2}$ followed by a development via ultrasonication in chloroform.

The influence of the cross-linking action was investigated in transistors fabricated identically to the devices shown in figure 8.14. Irradiation and development was done prior to the deposition of parylene-C/Ag with 3 keV. A dose of $500\,\mu C\,cm^{-2}$ was used which carried the previously investigated thicker films to total insolubility. The here used thinner films thus should be slightly overexposed ensuring complete insolubility as well. One sample was subsequently ultrasonicated for development (see figure 8.18) while the other sample was not developed. The maximum area which could be irradiated homogeneously without stitching was set to around $400\times400\,\mu m^2$ not enough to cover the active areas of the transistors entirely.[12] Thus, several patches were irradiated per active area of a transistor leaving some material unirradiated. This is of little interest for the ultrasonicated sample as unirradiated material is removed but requires a more complex analysis of undeveloped sample as charge transport between the irradiated and the unirradiated part has to be distinguished which shall be discussed first.

First, charge transport of the transistors under top gating was investigated. The undeveloped sample consists of 4×4 transistors channels of length L=20; 10; 5 2.5 µm where one of each group was irradiated while the remaining three were used as reference transistors. The calculation of the mobility from transfer curves was done in the following way: First, the reference transistors were used to calculate an average expected drain current $I_{ref.}(V_g)$ giving the avarage transistor response for unerradiated material (at a given chennel length). Then the irradiated transistor was measured giving $I_{irr.}(V_g)$. Optical microscopy was used to estimate the ratio R of unirradiated to irradiated channel area on the transistor. The drain current stemming from the pristine material can then be astimated as $R\cdot I_{ref.}$ with R taking values from 6 % to 10 %. The current carried by the irradiated area is then $I_{cor.} = I_{irr.} - R\cdot I_{ref.}$. The resulsts of such an analysis for L=20 µm can be found in figure 8.19. While the current decreases by roughly a factor of ten through the irradiation, the turn-on voltage and the general operation behaviour

[12] A higher area could be irradiated by increasing the distance between the single points which would then result in inhomogeneous irradiation.

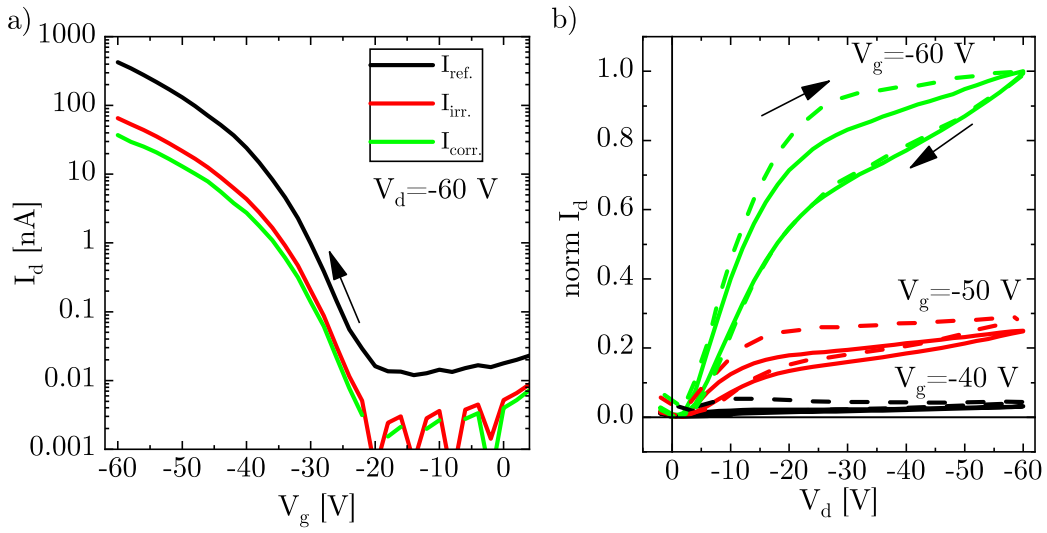


Figure 8.19: Transfer (a) and output (b) charateristic of a cross-linked PPE1 transistor. $I_{ref.}$ is the mean current of the reference transistors, $I_{irr.}$ is the current of cross-linked transistor as is (including contributions from both linked and unlinked material), $I_{corr.}$ is the transistor current stemming solely from cross-linked material. Output: Normalized $I_{ref.}$ (solid) and $I_{irr.}$ (dashed) plots indicating that the general operation behaviour of this transistor has not significantly changed. (L=20 µm)

seems to be weakly influenced as can be seen from the normalized output characteristic. The mobility of the reference devices fabricated here were found to be nearly an order of magnitude inferior to the previously fabricated devices of identical making. The origin of this decrease remains unclear as it can be caused by a number of factors such as the extended handling of the samples, fabrication errors or the prolonged time in the EBL setup which may damage non-irradiated devices as well. Table 8.2 shows a comparison of the charge transport properties for the 20 µm and the 5 µm group where R can be measured best.[13] While the turn-on voltage is only weakly influenced by the cross-linking the maximum current and the mobility decrease by an order of magnitude through cross-linking. Nevertheless This trend is supported by the other two groups of available channel length (L=2.5; 10 µm) not shown in the table.

Developed substrates do not shown any signs of charge transport when top gated which we attributed to the degradation of the interface through the necessary ultrasonication already apparent in the AFM investigations. The interpretation of these results indicates that cross-linking of **PPE1** hampers its charge transport properties but a clear semiconducting behaviour still prevails. The here presented findings are only a first piece of the puzzle to fully understand the degradation mechanism behind this decrease. The decrease in mobility of the reference transistors is another point for further investigations. Additional research should also focus on a different transistor layout in

[13] The transistors width of $W = 10$ mm was reduced for the mobility calculations from $I_{cor.}$ by R aswell (e.g. to 9.4 mm).

Table 8.2: Electrical parameters of undeveloped cross-linked top-gated PPE1 transistors. "only $I_{cor.}$" means that solely the current stemming from cross-linked material was used (see text).

L [µm]	device	mobility [$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]	turn-on voltage [V]	max. current [nA]
20	reference	6×10^{-4}	23	420
	only $I_{cor.}$	3.5×10^{-5}	24	37
5	reference	6×10^{-4}	14	2100
	only $I_{cor.}$	7×10^{-5}	20	250

which the active area of one transistor can be fully cross-linked rendering the complex correction via reference devices obsolete. Nevertheless, it could be clearly shown that **PPE1** is indeed an EBL cross-linking functional material.

8.5 Conclusion

Here, the viability of electron induced cross-linking of cinnamic acid derivatives and its application in the field of organic electronics was proven. A concept study with the insulating small molecule C4 clearly showed through a combination of IR spectroscopy and AFM measurements that cinnamic acid derivatives undergo a cross-linking reaction when irradiated with electron beams. Patterns with resolutions of up to 100 nm could be written using this material via EBL. This knowledge was applied to a semiconducting polymer backbone modified with cinnamic acid containing side-chains. Again electron beam induced cross-linking could be observed. It was found that the semiconducting properties of this polymer were deteriorated through the electron radiation to some extend but the overall semiconducting nature of this materials clearly prevailed. Further research is needed to better understand the cause of this degradation and develop novel semiconducting materials containing cinnamic acid groups. The here required use of ultrasonication for development of irradiated films for example is very detrimental to device operation. Thus, we see more solvable functional building blocks (e.g. the small molecular TIPS-PEN) or other stable semiconducting polymers to be an additional worthwhile starting point for future research. In Conclusion, cinnamic acid containing functional materials could enable novel approaches for nano-fabrication given the broad applicability of the approach and the fact semiconducting or even conductive films for EBL applications are to date very rare.

9 Summary and Outlook

The here presented work not only provides investigations into the more fundamental processes of charge carrier transport in thin films of organic p-type semiconducting materials but also offers a metrological contribution in the form of a novel robust approach to measuring the transport properties of modest mobility semiconductors. Furthermore, two classes of organic functional materials were studied in bigger detail. It was shown that the prototypical polymeric semiconductor Poly(*para*-phenylene) exhibits semiconducting properties in its unsubstituted form and a direct patternable EBL resist with semiconducting properties for nano-fabrication of the electronic devices was introduced.

Charge Carrier Transport in MIS-Capacitors

The first thematical chapter of this work was dedicated to the vertical charge carrier transport in MIS-Capacitors (featuring an unstructured semiconductor layer) with particular reference to charge carrier mobility and density of states width σ investigations. The devices were fabricated from the reference material P3HT in which an approach to calculate the vertical charge carrier mobility from capacitance frequency (Cf) measurements was validated twofold. Temperature-dependent measurements of the capacitors cut-off frequency from which the vertical mobility was calculated allowed the calculation σ via the gaussian disorder model proposed by Bässler. Next, this property was extracted via a sophisticated simulation of the potential distribution in such devices in combination with experimental capacitance voltage (CV) measurements. While the temperature-dependent Cf approach resulted in σ values lower than what was previously reported in literature the ones obtained through the simulated CV curves were higher than literature values. Furthermore, the simulations exhibited a strong inverse correlation between the capacitors active area and the σ value obtained. This finding could be mediated in parts by an ad-hoc addition to the model introduced in the following chapter. In conclusion measurements of unstructured MIS-Capacitors can give worthwhile insights into the vertical charge carrier transport properties but further research is needed when it comes to the extraction of σ. The simulation's approach, for example, assumes total steady state conditions which may be one of the reasons why this approach overestimates σ. Thus, future work into the theoretical description with special considerations for time-dependent phenomena may alleviate this issue. Additionally, the ad-hoc addition accounting for the accumulation induced parasitic capacitance could be further refined. Furthermore, the extraction of σ for the temperature dependent vertical mobility with another transport model may also lead to more accurate results.

A Kelvin-Technique for Mobility Measurements

The second chapter utilizes the previously detrimental effect of the accumulation induced parasitic capacitance for horizontal charge carrier mobility measurements. Applying a small perturbing voltage to an MIS capacitor with an extended and exposed channel results in charge carrier density oscillations along this channel. The resulting surface potential oscillations can be traced through a Kelvin-probe giving insights into the charge carrier transport properties of the employed semiconductor. First, a model describing the experimentally observed surface potential oscillations was derived through a simple drift-diffusion ansatz. It was found that the semiconductors charge carrier properties can be fully described through a relatively simple response function in Fourier space. The proposed model was experimentally verified and the thusly extracted charge carrier mobility closely matched the values calculated through complimentary transistors measurements. This model was further investigated through two-dimensional finite-element simulations to study experimentally hard to reach regions in a simple manner. These investigations fully proved the robustness of the model giving accurate predictions for the mobility as long as its small signal assumptions are met. The two common effects of interfacial trap states and doping were investigated and respective closely matching additions were introduced. Finally, the model was further simplified to only include a single fit parameter for the description of the charge carrier transport properties broadening its applicability window even further. In conclusion, a new method was proposed and verified to accurately measure the charge carrier properties of modest mobility materials which are especially insensitive to the often interfering injection barriers. All the objectives of this study have been fulfilled making the proposed method ready for application.

Local Electrical Property Investigations

The aim of this chapter was to prove the occurrence of injection barriers in TIPS-PEN transistors as suspected from its electrical characterization and to further investigate the transistors local electrical properties. To achieve this goal, a specially designed holed was fabricated which allowed contacting devices under the SKPM equipment. Through surface potentials measurements of such TIPS-PEN transistors under operation conditions, the existence of a significant injection barrier could be directly visualized. Furthermore, it was found that electron injection is possible during hole depletion in those devices. Having achieved these two goals, a further SKPM technique to measure the density of states with a high spatial resolution was presented next. Unfortunately, the necessary surface potential measurements proved to be too unstable for reliable measurements. The underlying cause for this behaviour is most likely the missing environmental protection so that water adsorption or desorption strongly influences the required high resolution measurements. These potentially very rewarding investigations to deepen the understanding between the morphological features of a semiconductor, its local electrical properties and its macroscopic transport behaviour remain undone. Future investigations into this field would thus need a different setup where ambient in-

fluences can be eliminated as far as possible be it in a glovebox or even under ultra-high vacuum conditions

Poly(*para*-phenylene)s for Organic Electronics

Although Poly(*para*-phenylene)s (PPP) derivatives were highly investigated as active materials in light emitting diodes, access to the unsubstituted polymer has been established just recently. The here presented route obtains PPP thin films through the conversion of an insulating precursor to the final PPP. The properties of this thermal conversion towards PPP as well as the establishment of the PPPs semiconducting properties were investigated in this chapter. First, it could be clearly shown that the obtained unsubstituted PPP is indeed a semiconductor. Its only modest performance in OFETs was rationalized by the chemical structure of the precursor requiring it to undergo a drastic conformational change when converting to PPP. Thus, different polymeric and oligomeric precursor materials were investigated aiming towards a higher crystallinity PPP to improve its charge carrier transport properties. One of the investigated oligomeric precursor molecules exhibited a remarkably high thin film order. It showed such a strong aggregation that its modest transistor performance was attributed to the lacking connectivity of the observed highly crystalline grains. In conclusion, valuable insights into the interplay of precursor structure, conversion speed, the morphology of the final film and charge carrier transport properties could be established. Future work should thus focus on two aspects: Further control of crystallinity in the obtained films could finally establish the break-through towards a high charge carrier mobility. The very promising behaviour of the investigated oligomeric precursor material could be tuned, for example, through a different processing or annealing procedure. In a competing approach, the lessons learned in the here presented studies could be applied to similar materials utilizing a different core with different transport properties. The observed high IP of PPPs, for example, will most likely always impede charge carrier injection as suitable electrode materials are not available. A significant reduction of this property could be achieved for example through the utilization of a low band gap push-pull core.

Cross-Linking Cinnamic Acid Derivatives through Electron Irradiation

The last chapter of this thesis investigated the cross-linking behaviour of cinnamic acid derivatives which could give access to novel ways for the direct nano-fabrication of organic functional devices. First, the viability of the proposed cross-linking mechanism was shown in a proof of concept study. An insulating cinnamic acid rich material could be cross-linked through electron radiation as shown through IR spectroscopy. Structuring via electron beam lithography was done where resolutions below 100 nm could be achieved. These findings were then applied to a semiconducting polymer bearing a cinnamic acid containing side chain. The polymer was shown to undergo cross-linking as investigated through IR spectroscopy. Irradiation of this material resulted in a decrease

of the materials charge transport properties but its semiconducting nature remained decisively intact. Thus, an electron beam processable functional material was presented in which the cross-linking can be attributed to the used cinnamic acid side chains. Future work should focus on a better understanding of the semiconducting properties in these materials after irradiation. For the moment, it remains unclear to which extend the π conjugation of the investigated polymer remains intact or which processes are responsible for its reduced hole mobility. Different characterization techniques (transistors, UV-VIS spectroscopy, IR spectroscopy) and approaches (e.g. dose-dependent measurements) could give valuable insights into this topic. Furthermore, the presently used material has some shortcomings already in its non-irradiated state (e.g. its low solubility post melt-annealing). Thus, the use of a different material could potentially render further investigations easier. Although some parts of the involved processes still remain in the dark, a promising route towards electron beam processable functional material has been established.

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A Appendix

A.1 Appendix to Chapter 4

Temperature Dependent Capacitance voltage measurements of reference capacitors

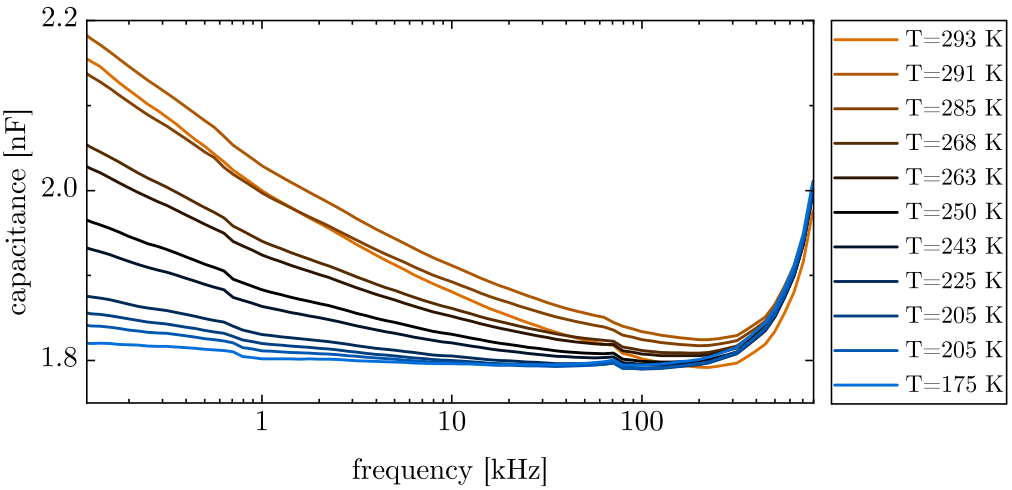

Figure A1: Temperature dependent capacitance frequency measurement of a reference capacitor. The capacitor consists only of ITO/Ag/Parylene-C/Au layers (no semiconductor). These measurements were used to normalize the temperature dependent Cf curves (see figure 4.7 and figure A2).

Different Cut-off Frequency Calculation

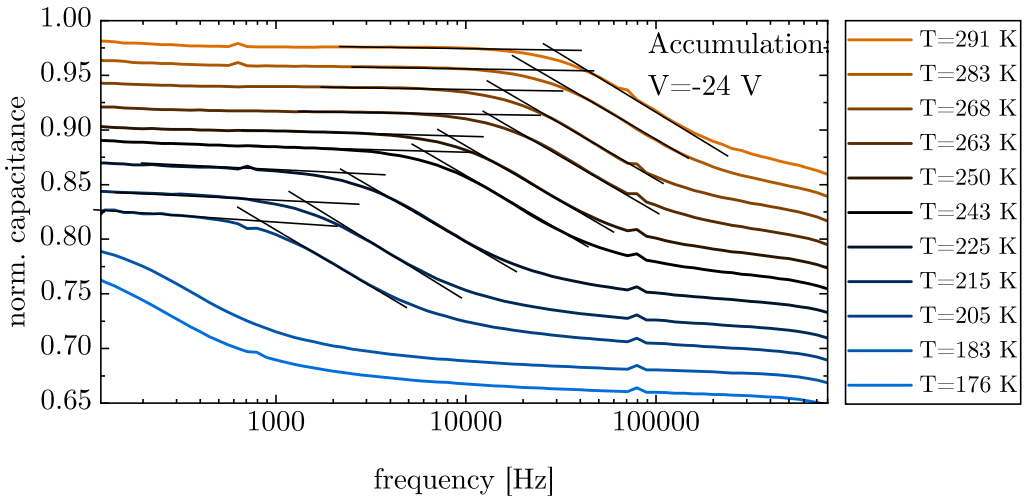

Figure A2: Temperature dependent capacitance frequency measurement of a P3HT MIS capacitor. In the main part f_c was calculated from the maximum of the dC/df curve (see figure 4.7). Here f_c is calculated by the intersection of two straight lines describing the the device in full accumulation and its transition towards the depletion capacitance for each temperature. Capacitance frequency measurements are shifted by 0.02 each for clarity reasons. At 183 K and 176 K the accumulation capacitance cannot be reach excluding them from further analysis.

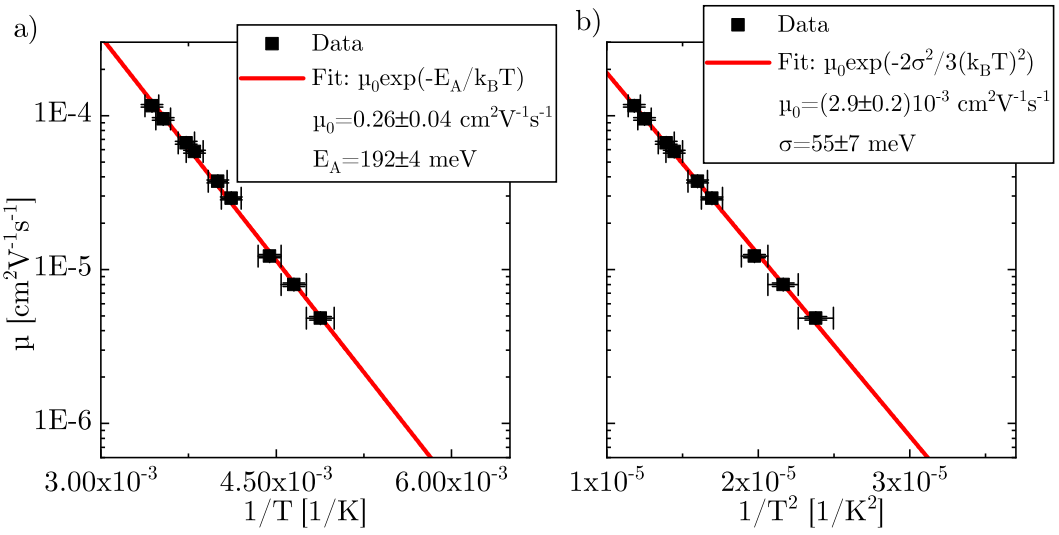

Figure A3: Charge carrier mobility as a function temperature measured in a P3HT MIS capacitor a) Hole mobility calculated from the critical frequencies extracted from figure A2 vs $1/T$ including a fit of an ARRHENIOUS model. b) Same data plotted vs. $1/T^2$ and a fit of the BÄSSLER-model. Both models give similar results to the main part (see figure 4.8 and figure 4.9)

MIS-Capacitor Simulations with Varying Device Area

In order to test the influence of device area on the extracted σ values, simulations with varying device area were carried out. The experimentally measured CV spectra of **1** at 1 kHz was taken as input data and simulations with device areas varied by up to $\pm 20\,\%$ were fitted to this data set. Figure A4 shows the five extracted fit parameters normalized to their value at 0 % tuning corresponding to the device area of $A_0 = 2.4 \times 10^{-5}\,\mathrm{m}$, the experimentally used device area. The results indicate no or very little influence on σ and V_{shift} while the d_{sc}, d_{ins} and c_{fix} are linearly influenced by the device area tuning. This behaviour is not surprising as d_{sc}, d_{ins} and c_{fix} determine the position of the curve in the capacitance voltage plane while σ and V_{shift} determines its shape. As the input data remained constant the CV shape should remain constant as well.

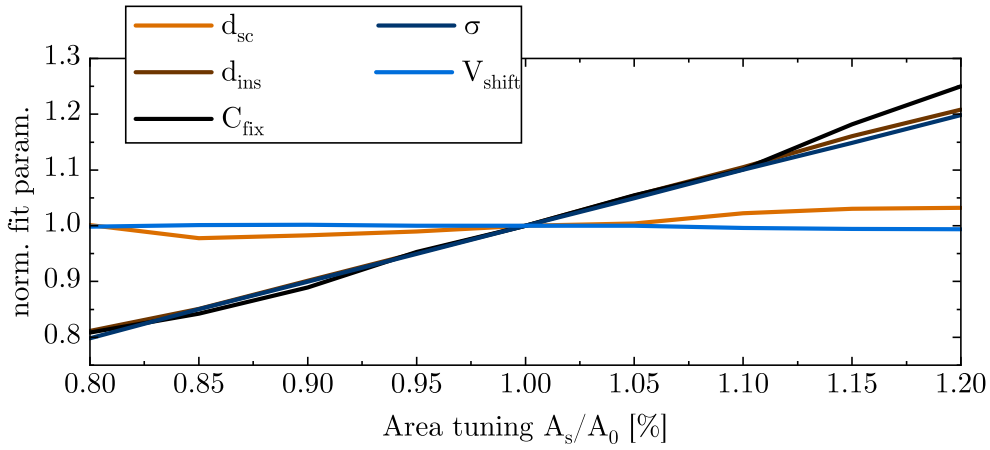

Figure A4: Influence of the input device area on the obtained fit results. The input device area A_s was tuned by $\pm 20\,\%$ from $A_0 = 2.4 \times 10^{-5}\,\mathrm{m}$. While d_{sc}, d_{ins} and c_{fix} exhibit a linear relationship with area tuning, σ and V_{shift} remain nearly unvaried.

A.2 Appendix to Chapter 5

Derivation of the ACKP Surface Potential Evolution for Triangular and Harmonic Bias

The fourier transform of a triangular bis is given by:

$$\nu(\omega) = \nu_0\sqrt{(2)} \sum_{n=-\infty}^{\infty} \frac{4\sin\left(\frac{\pi n}{2}\right)^2 - \pi\frac{\omega}{\omega_0}\sin(\pi n)}{\pi^{3/2}n^2}\delta\left(\omega - n\omega_0\right) \tag{A.1}$$

with ν_0 and ω_0 the amplitude/period of the applied bias and $\delta(w)$ the dirac delta function. The inverse Fourier transform into time space of the master equation (5.11) then results in:

$$\Phi(\hat{x},\hat{t}) = \sum_{n=-\infty}^{\infty} \Theta_n(\hat{x})\cos\left(\Omega_n\hat{t} + \delta_n(\hat{x})\right) \tag{A.2}$$

where the normalized length $\hat{x} = \frac{x}{L}$ and time $\hat{t} = \frac{t}{\tau}$ were used and $\Omega_n = (2n+1)\omega_0\tau$. The amplitude

$$\Theta_n(\hat{x}) = \nu_0\frac{8}{\pi^2(2n+1)^2}\sqrt{\frac{\cos\left(\sqrt{2\Omega_n}(\hat{x}-1)\right) + \cosh\left(\sqrt{2\Omega_n}(\hat{x}-1)\right)}{\cos\left(\sqrt{2\Omega_n}\right) + \cosh\left(\sqrt{2\Omega_n}\right)}} \tag{A.3}$$

and phase shift read:

$$\delta_n(\hat{x}) = -\arccos\left(\frac{\cos\left(\sqrt{\frac{\Omega_n}{2}}\hat{x}\right)\cosh\left(\sqrt{\frac{\Omega_n}{2}}(\hat{x}-2)\right) + \cosh\left(\sqrt{\frac{\Omega_n}{2}}\hat{x}\right)\cos\left(\sqrt{\frac{\Omega_n}{2}}(\hat{x}-2)\right)}{\sqrt{\left(\cos\left(\sqrt{2\Omega_n}\right) + \cosh\left(\sqrt{2\Omega_n}\right)\right)\cos\left(\sqrt{2\Omega_n}(\hat{x}-1)\right) + \cosh\left(\sqrt{2\Omega_n}(\hat{x}-1)\right)}}\right) \tag{A.4}$$

For a given harmonic bias of the $\nu_0\cos(\omega_0 t)$ the fourier transform is given as:

$$\nu(\omega) = \nu\sqrt{\frac{\pi}{2}}\left(\delta(\omega-\omega_0) + \delta(\omega+\omega_0)\right). \tag{A.5}$$

The solving the master equation then reads with the above given amplitude and phase shift:

$$\Phi(\hat{x},\hat{t}) = \frac{\pi^2}{8}\Theta_0(\hat{x})\cos\left(\omega_0\tau\hat{t} + \delta_0(\hat{x})\right) \tag{A.6}$$

Full Dataset of the finite element ACKP Simulations

Chapter 5 presents the results for a number of different simulations to validate the ACKP model. Here the full dataset of all the simulations carried out will be presented. The data is treated in a way to easily distinguish the deviation of a parameter form their expected value. As such, the four parameters extracted from the simulation (Φ_0, Φ_{AC}, τ and Δt) are normalized to their predicted values (V_0, V_{AC}, τ_i and P). The parameters are marked by symbols and their predicted values by solid lines. If a parameter significantly deviates from the solid line (the predicted value) the validity of the ACKP model has to be questioned. If the quantity varied in the simulation directly influences a parameters prediction this parameter is plotted in a separate axis to the right. The following two graphs treat first more simple simulations into parameters of the measurement setup (e.g. device length, see figure A5) and then more complex investigations into the details of the semiconductors transport properties (e.g. mobility, see figure A6). Further discussions and a more detail explanations of individual setup of the simulations can be found in the main text.

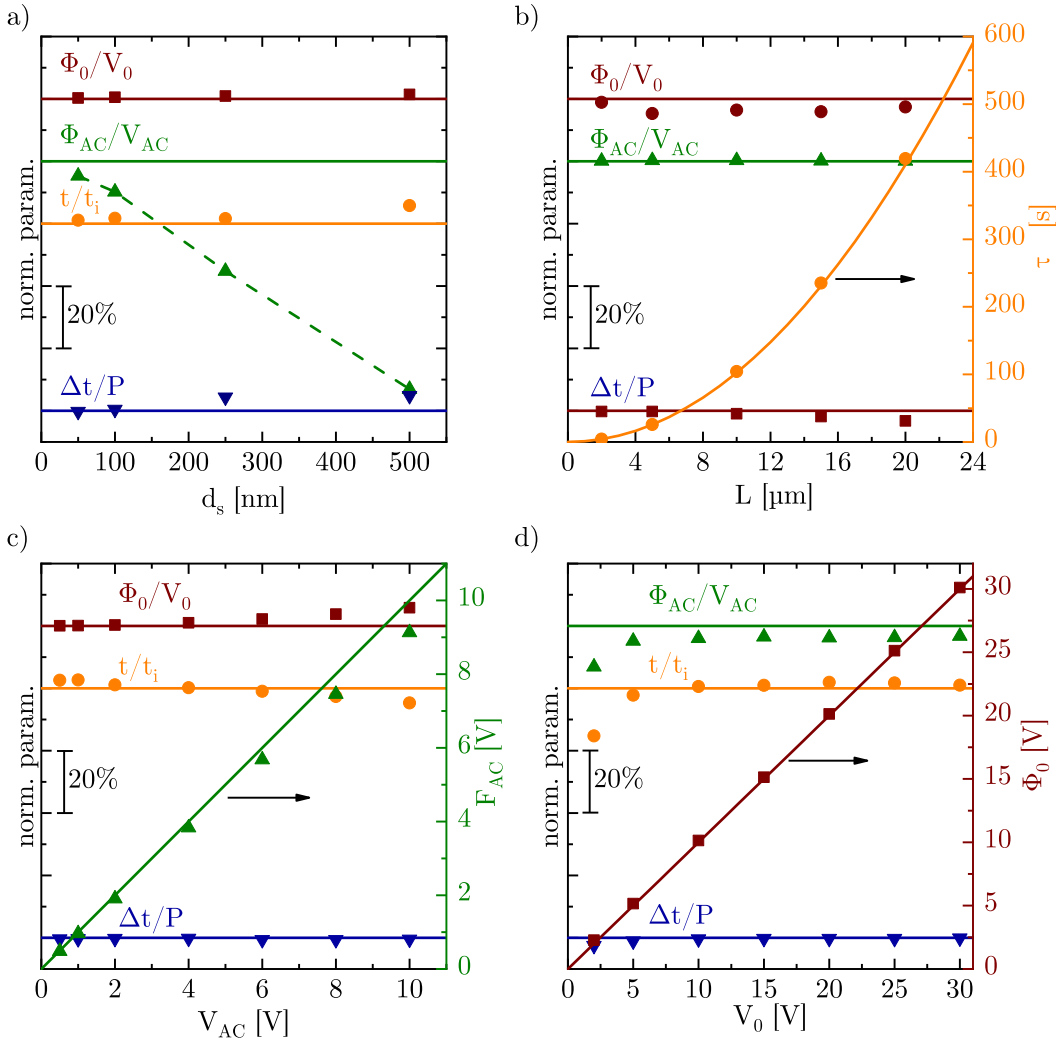

Figure A5: Simulation results for a variation of device thickness d_s (a), device length L (b), perturbing V_{AC} (c) and constant part V_0 (d) of the applied bias. The dashed line is a guide to the eye.

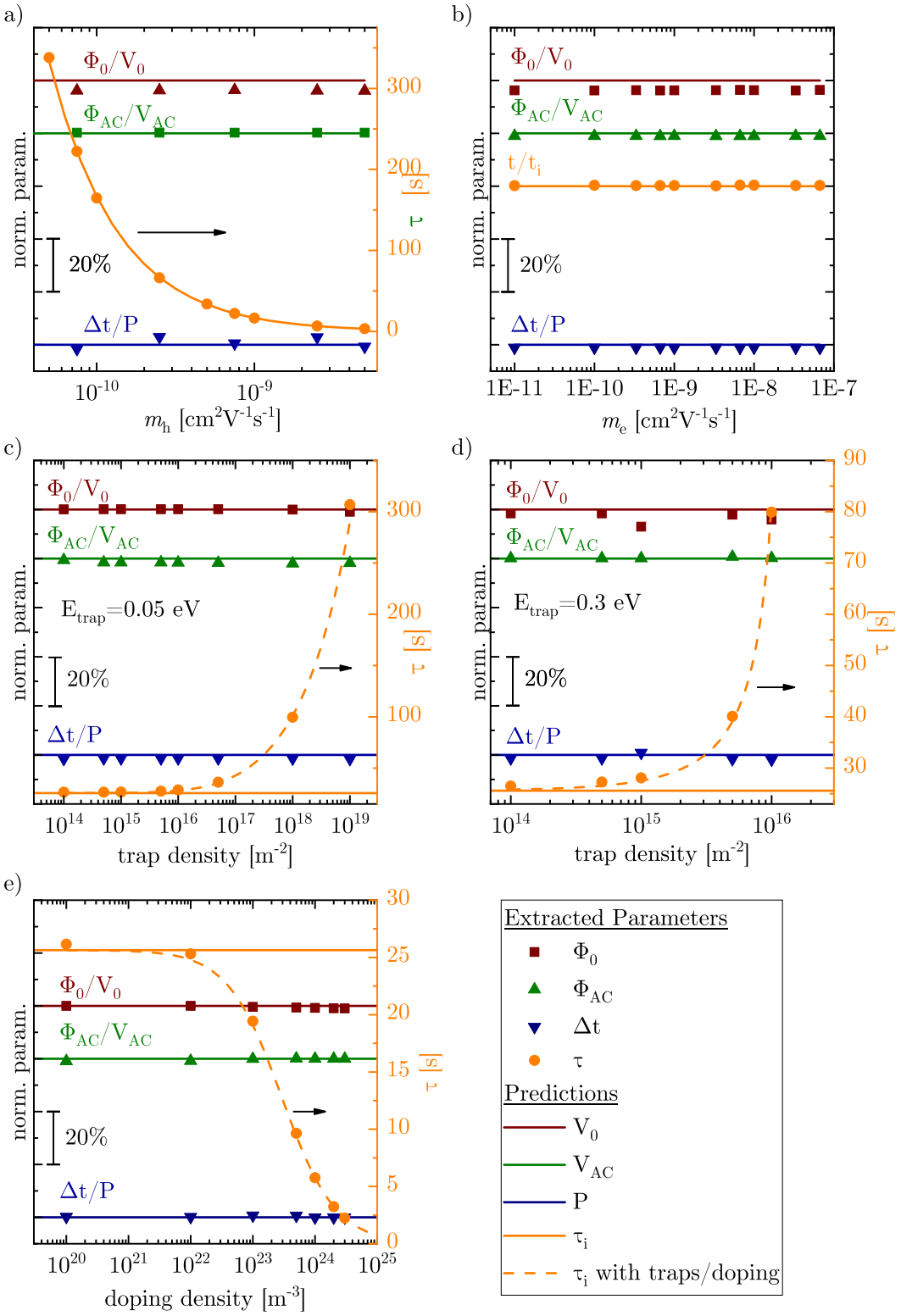

Figure A6: Simulation results for a variation of the mobility (a, b), trap density (c, d) and doping density (e) Symbols/lines stand for extracted parameters and their predictived values, respectively.

Derivation of the Parasitic MIS Capacitance in Unpatterned Devices

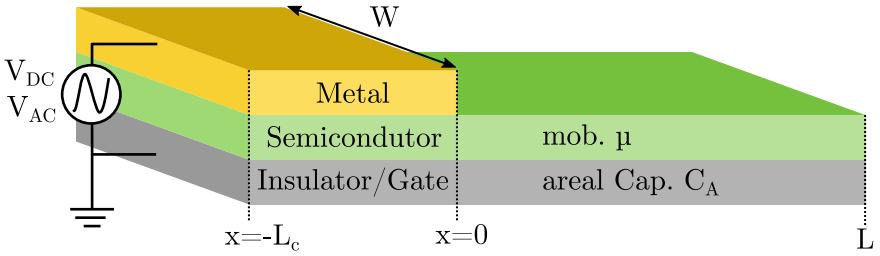

Figure A7: Sketch of a typical MIS capacitor experiment. The unpatterned semiconductor allows charge carriers to drift outside of the active area in x direction increasing the capacitance measured.

Consider the example of a simple capacitance measurement experiment given in figure A7. The capacitor of area WL_c is measured via impedance spectroscopy at constant bias V_{DC} in accumulation. As the semiconductor, insulator and gate electrode extend further then the top electrode, charge carriers can drift into the open channel increasing the overall capacitance measured. As derived in chapter 4 the response function for surface potential oscillations $\Phi(x,t)$ of such a system can be approximated in the limit of large $\omega\tau$ in Fourier space as (see equation (5.12)):

$$R(\hat{x},\omega) \approx \exp\left(\frac{i-1}{\sqrt{2}}\sqrt{\omega\tau}\hat{x}\right), \tag{A.7}$$

with the transit time $\tau = L^2/(\mu V_{DC})$, the frequency ω and the normalized x-coordinate $\hat{x}$. $\Phi(\hat{x},\omega)$ is given by the product of the response function and the Fourier transform of the applied bias. Thus, if the applied bias takes a form of $V_{AC}\cos(\omega_0 t)$ the amplitude of surface potential oscillation takes in time space the following form:

$$\Phi(x) = V_{AC}\exp\left(-\sqrt{\frac{\omega_0\tau}{2}}\frac{x}{L}\right) \tag{A.8}$$

The charge per area Q_A can be calculated with the areal capacitance C_A as

$$Q_A(x) = C_A\Phi(x) = C_A V_{AC}\exp\left(-\sqrt{\frac{\omega_0\tau}{2}}\frac{x}{L}\right). \tag{A.9}$$

Here, a reformultion of this equation using the definition of τ, the frequency $f_0 = \omega_0/2\pi$ and with the introduction of a threshold voltage V_{th} is in order:

$$Q_A(x) = C_A V_{AC} \exp\left(-\sqrt{\frac{f_0 \pi}{\mu(V_{th} - V_{DC})}} x\right). \tag{A.10}$$

The total additional charge stored in the channel reads then:

$$\Delta Q = C_A V_{AC} \int_0^L \int_0^W \exp\left(-\sqrt{\frac{f_0 \pi}{\mu(V_{th} - V_{DC})}} x\right) dydx. \tag{A.11}$$

In the case of high frequencies, low mobilities and typical DC voltages (e.g. $\mu = 1 \times 10^{-3}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$; $f_0 = 1\,\mathrm{kHz}$; $V_{DC} = 20\,\mathrm{V}$) the charge density drops on a µm scale, much faster then the extend of the exposed contact L (in the mm range). Thus the solution of the integral reads:

$$\Delta Q = C_A V_{AC} W \sqrt{\frac{\mu(V_{th} - V_{DC})}{f_0 \pi}} \tag{A.12}$$

The additional capacitance is then given by

$$\Delta C = \frac{\Delta Q}{V_{AC}} = C_A W \sqrt{\frac{\mu(V_{th} - V_{DC})}{f_0 \pi}} \tag{A.13}$$

One has to note that the given threshold voltag is not necessarily identical to the one measured in transistors as the MIS capacitors threshold voltage more closely resembles a built-in voltage while $V_t h$ in transistors is extracted from a fit of the SHOCKLEY-Model (e.g. in saturation regime of a transfer curve: $I_d \propto (V_g - V_{th})$). This equation can now be used to model the voltage and frequency dependence of the measured parasitic capacitance in accumulation.

A.3 Appendix to Chapter 7

UV-VIS spectra of P_1 and PPP_1

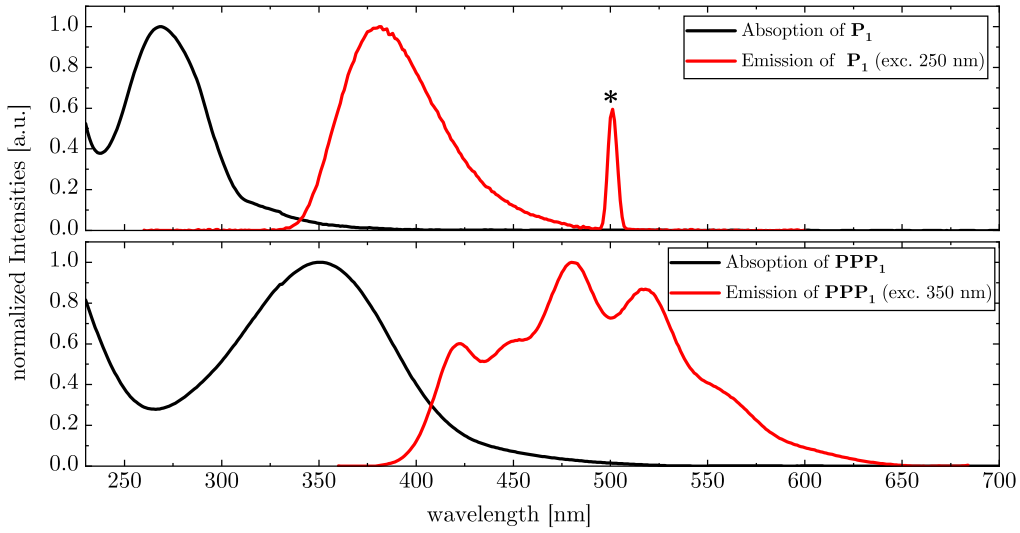

Figure A8: Absorption and Emission spectra of P_1 and PPP_1. Conversion of P_1 to PPP_1 leads to a strong shift of absorption towards smaller energies and photo-luminescence rich in features. Spectra measured on quartz substrates. The peak marked by * is located at twice the excitations wavelength.

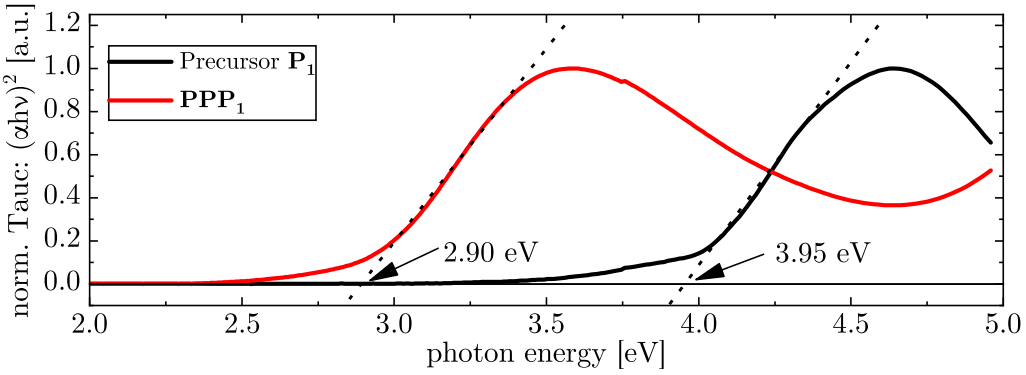

Figure A9: Tauc plot of P_1 and PPP_1. The Tauc plot is used to calculate the optical gap from absorption spectra.

UPS and X-ray diffraction of P_1 and PPP_1

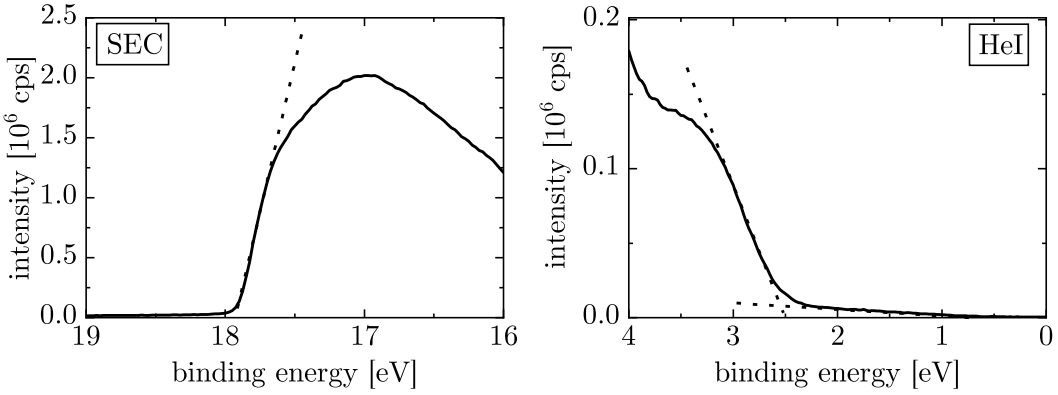

Figure A10: UPS spectra of PPP_1. Secondary electron cutoff (SEC) and HeI-line of a fully cured P_1 film. The SEC has been measured with an applied bias of V=-3V by which the spectrum was shifted. The workfunction can be calculated as $3.3\,\mathrm{eV}$ and the IP as $5.8\,\mathrm{eV}$.

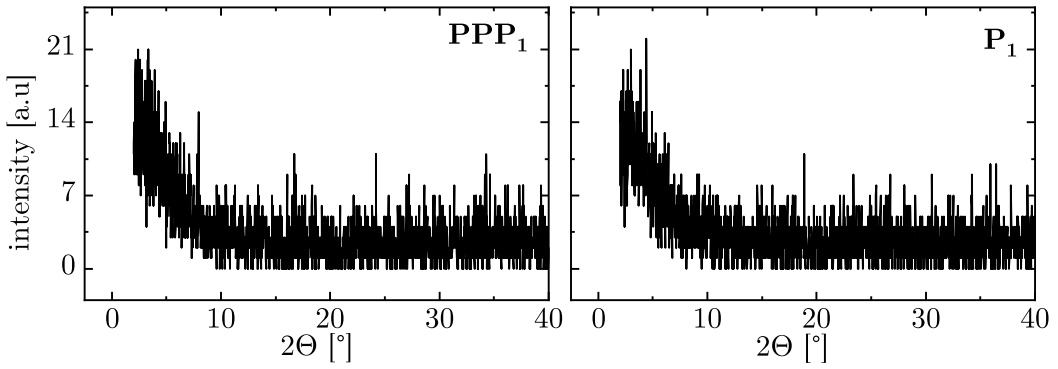

Figure A11: 1D-XRD measurement of a PPP_1 and P_1 film. The absence of clear peaks indicate no order in these films. Data recorded by Thomasz Marszalek. [124]

GIWAXS data of P_2 and PPP_2

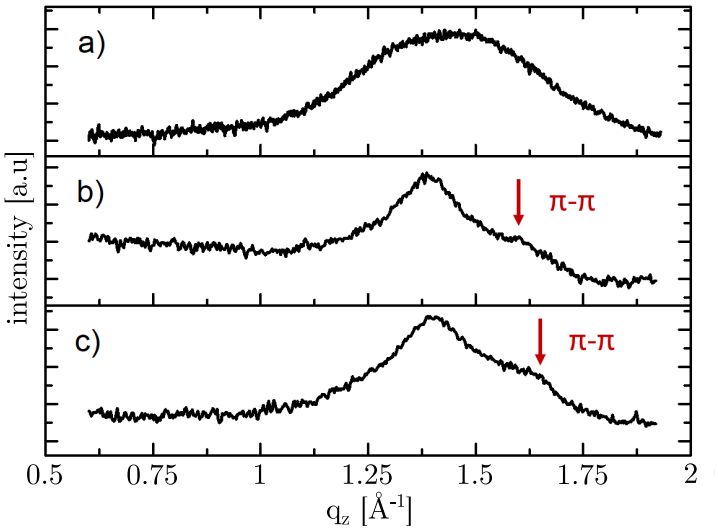

Figure A12: Meridional integration of GIWAXS patterns of differently annealed P_2 thin films. a) Pristine film, b) annealing at $250\,°C$ for $2\,h$ and c) annealing at $300\,°C$ for $2\,h$. The peak marked by the arrow (c) indicates a π-π-stacking distance of $0.39\,nm$. Data recorded by Thomasz Marszalek. [125]

A.4 Appendix to Chapter 8

Film retention curves for UV and EBL cross-linking of C4

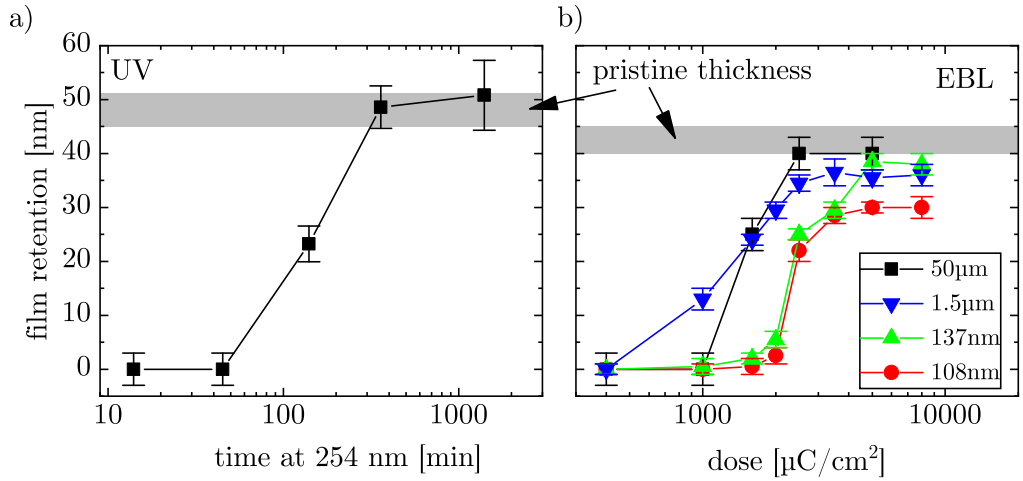

Figure A13: Film retention curves for crosslinking of C4 via UV (a) and electron radiation (b). For EBL cross-linking the feature size (given in the plot's legend) directly influences the amount of irradiation needed for full film retention. Furthermore, full film retention cannot be achieved for very small structures.

Bottom Gate Measurements of a PPE1 transistors

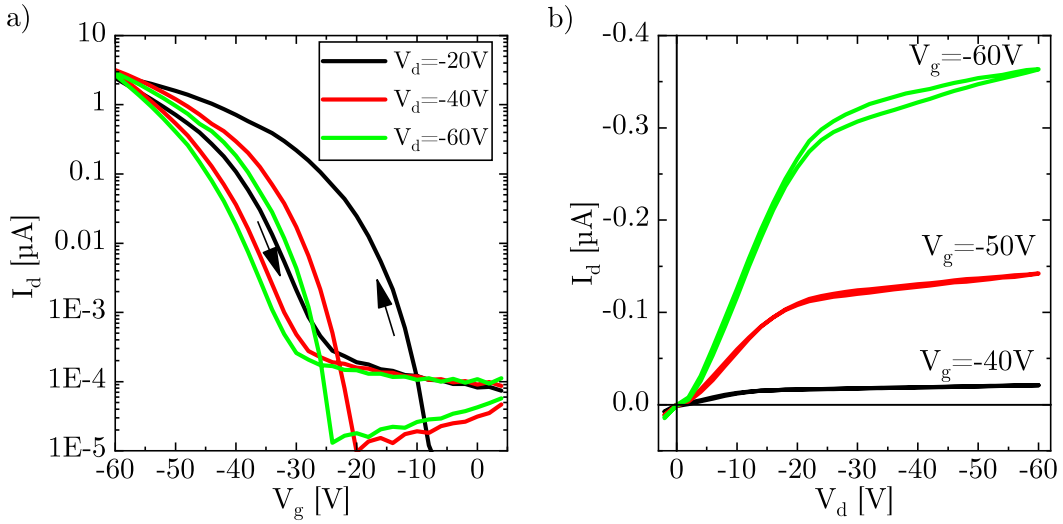

Figure A14: Transfer (a) ant output curve (b) of bottom gate melt annealed PPE1 transistor. First a transfer measurements ($V_d = -20\,\mathrm{V}; -40\,\mathrm{V}; -60\,\mathrm{V}$) were carried out (a) followed by a output measurement (b). The shift in turn-on voltage towards more negative values for repeated measurements indicates hole trapping analogously to chapter 7. See figure 8.14 for device structure.

Transistor, IR and AFM data of experiments with PPE2

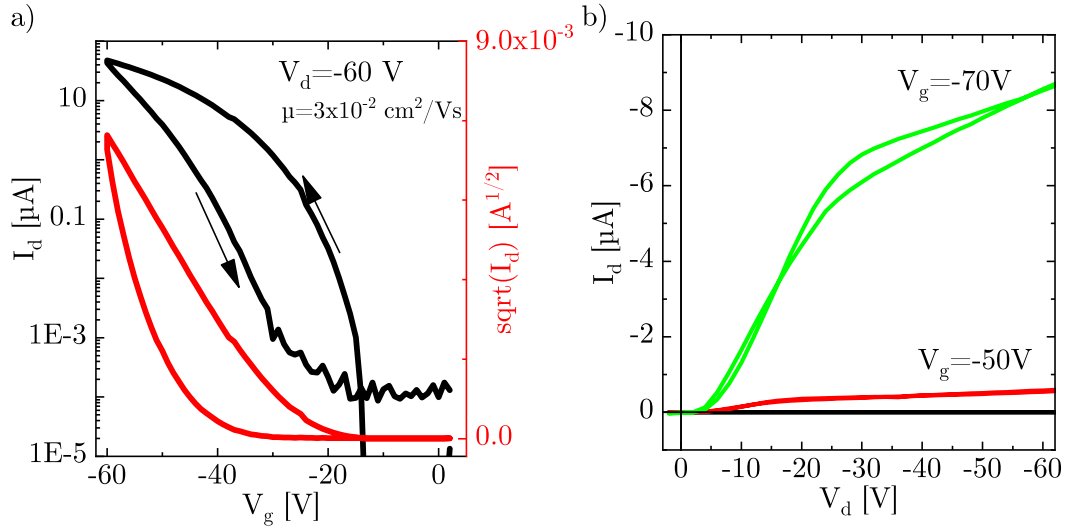

Figure A15: Transfer (a) and output (b) characteristic of an exemplary melt-annealed top gated transistor fabricated from PPE2. The device structure was identical to the one presented in chapter 8 with the exception that a 430 nm PMMA layer was used as the top dielectric instead of Parylene-C.

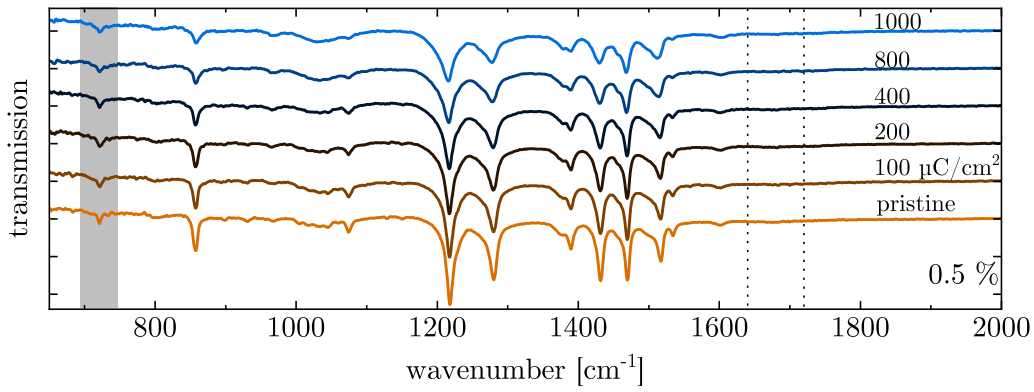

Figure A16: IR transmission spectrum of a melt-annealed PPE2 film irradiated with different electron doses. The monotonous decrease of intensity for all peaks does not indicate any form of cross-linking but instead indicates a non-specific degradation of the molecule. **PPE1** exhibited a strong change in spectra in the shaded area and at the two horizontal lines (see figure 8.16) which can also not be observed here. Irradiation was done at 3 keV.

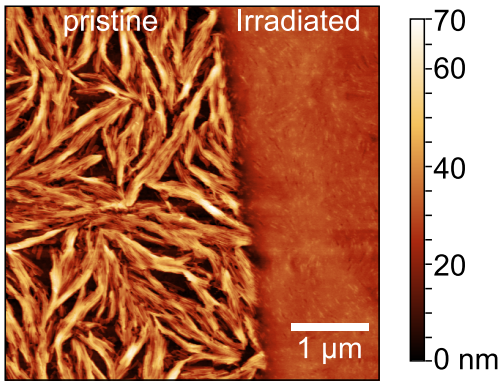

Figure A17: AFM image of a partly irradiated film of PPE2. A melt annealed film of **PPE1** was irridiated at $3\,\mathrm{keV}$ with a dose of $400\,\mu\mathrm{C\,cm^{-2}}$. Susequent development was done identically to chapter 8 without the use of ultrasonication. The picture clearly shows that also in the unirrediated part of the film some film retention can be observed. Development further results in a swelling of the pristine film locally increasing its thickness from around $30\,\mathrm{nm}$ to up to $70\,\mathrm{nm}$. Development with ultrasonication fully removes the irradiated and pristine layers.

List of Figures

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List of Publications

Accepted Publications

V. Milotti, M. Pietsch, **K.-P. Strunk**, and C. Melzer, "Measuring the lateral charge-carrier mobility in metal-insulator-semiconductor capacitors via kelvin-probe," *Review of Scientific Instruments*, vol. 89, no. 1, p. 013902, 2018.

K.-P. Strunk, A. P. Ullrich, S. Kebrich, and C. Melzer. "Kelvin-probe based carrier-mobility extraction reviewed by finite element simulation," *Synthetic Metals*, vol. 247, pp. 177-182, 2019.

K.-P. Strunk and A. Abdulkarim, S. Beck, T. Marszalek, J. Bernhardt, S. Koser, W. Pisula, D. Jaensch, J. Freudenberg, A. Pucci, U. Bunz, C. Melzer, and K. Müllen, "Pristine poly(*para*-phenylene): Relating semi-conducting behavior to kinetics of precursor conversion," *ACS Applied Materials & Interfaces*, in press, 2019.

Publications under Review

A. Abdulkarim, **K.-P. Strunk**, R. Bäuerle, S. Beck, H. Makowska, T. Marszalek, A. Pucci, C. Melzer, D. Jänsch, J. Freudenberg, U. Bunz, and K. Müllen,, "Small change, big impact: The shape of precursor polymers governs poly-p-phenylene synthesis," *Macromolecules*.

Publications in Preparation

K.-P. Strunk and N. M. Bojanowski, C. Huck, M. Bender, L. Veith, M. Tzschoppe, I. Wacker, R. Schröder, A. Pucci, U. H. F. Bunz and C. Melzer, "Electron-beam-induced cycloaddition of cinnamate for nano sized structuring," *Small*.

Co-supervised Master thesis

V. Milotti, "Transient Kelvin Probe Measurements on Organic Semiconductor Devices" Master's thesis, Università degli Studi di Padova, 2017.

Publications not related to this work

L. Ahrens, S. Schlisske, **K.-P. Strunk**, F. Hinkel, C. Melzer, U. H. F. Bunz, U. Lemmer, G. Hernandez-Sosa, D. Jänsch, J. Freudenberg, and K. Müllen, "Solubility modulation

of polyfluorene emitters by thermally induced (retro)-diels–alder cross-linking of cyclopentadienyl substituents," *Chemistry of Materials*, vol. 30, no. 12, pp. 4157–4167, 2018.

List of Acronyms

ACKP	Alternating current Kelvin-probe
AFM	Atomic force microscope
AIPC	Accumulation induced parasitic capacitance
Cf	Capacitance frequency
CPD	Contact potential difference
CV	Capacitance voltage
DFT	Density funtctional theory
DOS	Density of states
EA	Electron affinity
EBL	Electron beam lithography
GIWAXS	Grazing-incidence wide-angle x-ray scattering
HOMO	Highest occupied molecular orbital
IP	Ionization potential
IR	Infrared (spectroscopy)
IV	Current-voltage
MIS	Metal-insulator semiconductor
LUMO	Lowest unoccupied molecular orbital
OFET	Organic field-effect transistor
OLED	Organic light emitting diode
OPV	Organic photovoltaics
PPE	Poly(*para*phenylene-ethynylene)
PPP	Poly(*para*-phenylene)
SEM	Scanning electron microscopy
SKPM	Scanning Kelvin-probe microscope
UPS	Ultraviolet photo-emission spectroscopy
XRD	X-ray diffraction

Acknowledgement

First and foremost I would like to thank Christian Melzer for his excellent supervision during my thesis. I really enjoyed our little research group and the work we did. I am looking forward to working with you in the future.

Second, I would like to thank Prof. Dr. Albrecht Winnacker for being the second referee of my thesis and all the administrative help he gave.

I would like to thank Prof Dr. Annemarie Pucci for all the fruitful scientific discussions and for welcoming me into her group after Christian Melzer left for the innovationLab.

I want to express my thanks to Prof Dr. Uwe Bunz for all the support in scientific and non-scientific matters he gave me during my thesis.

My gratitude goes to the German Academic Foundation for their generous PhD scholarship and the very interesting summer schools.

I thank Silke Koser for being my labmate and the first person to talk to for experimental problems in our little underground lab. You always had an open ear for scientific discussions or music genres.

I thank all my collaboration partners for the possibility of interdisciplinary work and for broadening my horizon. I thank Ali Abdulkarim, Maximilian Bojanowski and Emmanuel Smarsly and Soh Kushida from the chemistry side for the close collaboration and all the interesting insights into their area of expertise. I thank Christian Huck, Sebastian Beck, Rainer Bäuerle and Michael Tzschoppe for our joint projects and fruitful discussions. I want to thank Lisa Veith and Stefan Kauschke for all the things I learned from you about SEM and EBL.

I extend my gratitude to all those who did proof-reading of this work: Susanne Nebl, Katelyn Goetz, Silke Koser, Christian Huck, Maximilian Bojanowski, Soh Kushida and Michael Tzschoppe.

I extend my thanks to all the students I supervised during my thesis be it for a Bachelor/Master thesis or a simple Forschungspraktikum. Thus I want to thank: Valeria Milotti, Maximilian Krings, Nico Balzer, Tobias Deprie, Claudia Legler, Kathrin Slota, Nicolas Daub, Sebastian Kebrich, Saskia Braun, Jakob Steidel, Ina Michalsky and Philipp Stein. I really enjoyed working with you and learned a lot along the way.

My thanks goes to all of the past and present members of the research group of Professor Bunz who accepted me as one of their own and with whom I spent a lot of pleasant time.

I want to especially thank my family and my partner Susanne for always supporting my during my life