

A smart CMOS mid-infrared sensor array

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We present a novel single-chip thermopile sensor array for mid-infrared room temperature imaging. The array is fabricated on a single complementary metal–oxide–semiconductor (CMOS) dielectric membrane, comprising of single-crystal silicon (Si) p^+ and n^+ elements, and standard CMOS tungsten metal layers for thermopile cold junction heatsinking, significantly reducing the chip size and simplifying its processing. We demonstrate a 16×16 pixel device with 34 V/W responsivity and enhanced optical absorption in the 8–14 μm waveband, with suitable performance for gesture recognition and people-counting applications. Our simple, low-cost sensor is an attractive on-chip array for a variety of applications in the mid-infrared spectral region. © 2019 Optical Society of America

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Infrared (IR) thermal imaging of near room temperature (T) objects[1] is increasingly important for many applications including smart homes[2], healthcare[3], security[4], or automotive[5]. For example, in building automation[2], systems like heating, ventilation, and air conditioning (HVAC), are controlled by using sensors employed to detect the presence of occupants and their motion[6]. Objects near room T , e.g., the human body, radiate energy in the mid-infrared (MIR) ($\sim 2\text{--}20\mu\text{m}$) spectral region, with an emission peak $\sim 10\mu\text{m}$ [1]. Detectors operating in this region are also highly relevant to spectroscopy[7], because many organic and inorganic molecules have fundamental vibrational and rotational energy transitions in the MIR[8]. In addition, with the emerging trend of miniaturization of optical systems on-chip[9], numerous possibilities exist for MIR sensors integrated into smart phones, watches, or wearables[7], to widen their appeal to a much broader consumer application area, where smart sensors (by use of integrated circuitry) are increasingly used for decision-making applications[2]. When deployed for such applications, or within the internet of things (IoT) environment[10], MIR detectors need to be low-cost (so they can be deployed in large numbers), and low-power consumption (so they can be battery or energy harvesting[11] operated)[2].

Low-cost IR image sensors typically consist of an array of bolometers[5, 12], or thermopiles[13, 14]. Bolometers are thermal detectors where T variations, caused by incident IR radiation, produce a change in resistance (ΔR) of a sensing element,

typically made of vanadium oxide (VOx)[15], or amorphous silicon ($\alpha\text{-Si}$)[16]. A voltage $V_B = I\Delta R$ can then be measured by constant current-biasing (I) the bolometer[17]. Thermopiles are another class of thermal detectors, typically composed of several thermocouples (i.e. junctions of two dissimilar conductive materials) connected in series[17]. An electromotive force $V_T = \alpha\Delta T$ [17] is produced across each thermocouple when its elements (conductive materials, e.g., poly-Si[18]) are presented with a temperature gradient ΔT , where the proportionality constant α is a T -dependent material property known as the Seebeck coefficient[19]. It follows that the output (measured voltage) of a thermopile is inherently insensitive to changes in the ambient T [1, 20], in contrast to a bolometer which generates a signal proportional to T . In addition, thermopiles need no electrical bias, leading to negligible $1/f$ noise[17], and have no voltage offset in their output signal[17]. Furthermore, compared to bolometers, which require process steps and materials that are often incompatible with standard fabrication methods[5, 12], thermopiles are easier to manufacture using standard CMOS fabrication processes[21, 22], which increases device fabrication flexibility, in addition to having economic advantages[7, 23].

A thermopile image sensor consists of an array (typically rectangular) of pixels (thermopiles) located at the focal plane of a lens[1]. An image is formed by displaying the ΔT s detected by the individual pixels in the X by Y array. Each pixel's thermocouples have their hot junctions thermally isolated, typically by a thin dielectric membrane[18, 22]. Therefore, when the membrane is heated by incoming IR radiation, a voltage $V_T = N\alpha\Delta T$, proportional to the number of thermocouples N and the ΔT across their elements, is generated[17]. An important figure of merit is the detector's responsivity R_V , defined as the change in voltage response due to incident optical power ($R_V = dV_T/dP$)[17], which is highly dependent on the thermal resistance of the device[17, 19]. Membranes with high thermal resistance are used to enhance IR heating and thus R_V , and can be formed by micromachining of the Si substrate[18, 24]. A typical array consists of thermopile pixel elements fabricated on isolated membranes, formed by bulk etching of the substrate[5, 14]. However, this fabrication method requires critical process control to minimize substrate etching tolerances and undercut. In addition, the space required between the membranes contributes to large chip areas and small fill factors[18]. IR sensor arrays fabricated on a single membrane have been reported, but employ non-standard structures above or below the membrane. Examples include bulk silicon layers[13], or additional gold

layers[25] acting as heatsinks. Gold is not fully CMOS compatible, which results in non-standard processes and increased fabrication costs[24]. To overcome these limitations and simplify chip processing and minimize manufacturing costs, we recently presented a fully CMOS compatible array design, based on a single membrane with aluminium (Al) layers for heatsinking of the thermopile cold junction elements[21].

Here, we present a CMOS based thermopile array fabricated on a single membrane, using only commercially available industrial fabrication steps, employing standard CMOS tungsten (W) layers and integrated control electronics. W is an interconnect metal found in high temperature CMOS processes, and can enable stable devices with excellent reproducibility and the possibility of a wide range of on-chip circuitry, at very low cost[23]. Compared to Ref.[21], silicon on insulator (SOI) technology is used to allow field-effect transistors (FETs) on the membrane which allows full on-chip pixel control and enables smart functionality. We use the IR sensor array for gesture detection and people-counting, showcasing its suitability as a smart sensor for the IoT and consumer electronics applications.

The thermopile array is fabricated using a commercial $1\mu\text{m}$ SOI-CMOS process on 6 inch Si wafers. The pixels are formed by highly doped p^+ and n^+ single-crystal Si formed within the SOI layer. Three devices, having array sizes of 8×8 , 16×16 and 32×32 pixels, were fabricated as a proof-of-concept. The interconnects between the p^+ and n^+ elements, and the heatsinking tracks between the pixels are formed by three W interconnect layers, with track widths of $10\mu\text{m}$ and total thickness of $1\mu\text{m}$ (for the 16×16 pixel sensor). The Si dioxide (SiO_2) based membrane is $\sim 5\mu\text{m}$ thick [see Fig.1(a)] and has an area of $1200\mu\text{m}\times 1200\mu\text{m}$ [see Fig.1(b)], leading to a $\sim 75\%$ fill factor if only the thermopile area is considered, and to a 100% fill factor, if the heatsinking tracks are considered as part of the pixels. The layers are grown on a $400\mu\text{m}$ thick Si substrate which was back-etched using deep reactive ion etching (DRIE) to form the membrane, with the first SiO_2 layer acting as an etch stop. Each pixel consists of a thermopile with 36 thermocouple pairs [inset of Fig.1(b)], connected in a differential arrangement, having their cold junctions placed adjacent to the surrounding heatsinking tracks, formed by the three W layers. Each pixel's differential output is connected in series to two metal-oxide-semiconductor FETs (MOSFETs). The gate and drain of the MOSFETs are connected to the column (X) addressing line and to the row (Y) differential read-line, respectively. The X-Y readout scheme is implemented by two 4-to-16 on-chip binary decoders that individually address the pixels to

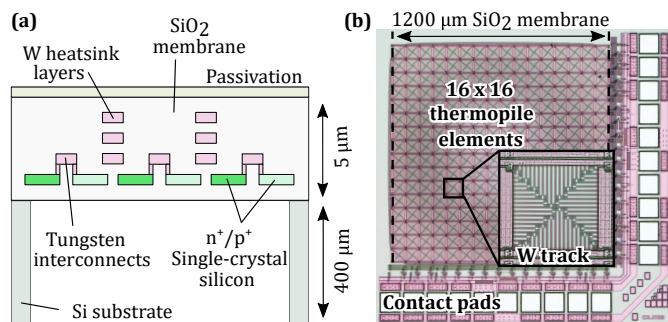


Fig. 1. (a) Cross-sectional view showing the single-crystal Si p^+/n^+ elements and tungsten (W) layers of the thermopile array. (b) Optical image of the thermopile array with a zoomed in individual pixel. Chip size = $1.76\text{ mm}\times 1.76\text{ mm}$.

allow reading of the generated V_T voltages. To address a pixel in the array, the X decoder selects the column by applying +5 V to all the MOSFETs within the column, while the Y decoder selects which row is connected to the output to be read. Each X/Y decoder input is connected to a separate pad at the edge of the thermopile array chip, where pads for the differential output and device bias are also available [Fig.1(b)].

The experimental configuration of our smart IR sensor is shown in Fig.2. The thermopile array chip is mounted and bonded to a 16 pin TO-8 type chip carrier, which is placed on a printed circuit board (PCB) and connected to an analogue-front-end (AFE) integrated circuit (LMP93601), interfaced to a microcontroller (MCU) (MSP430). The active pixel elements are accessed by selecting the corresponding XY address of the internal decoder circuits. An output frame (one sample from each of the pixels) consists of differential signals from the X by Y array which are amplified and digitized by the AFE.

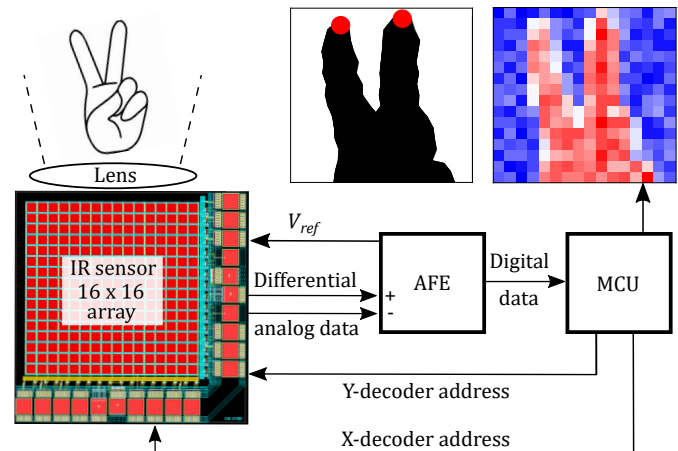


Fig. 2. Thermopile array system diagram. Each pixel is accessed by selecting the corresponding XY address via internal on-chip decoder circuits. An output frame consists of X by Y differential signals, each floating on a reference voltage (V_{ref}) provided by the analog-front-end (AFE). Each frame is transferred to the AFE via positive and negative output pins of the sensor in serial format, where it is amplified and digitized, and subsequently processed by the microcontroller (MCU). The thermal image and processing of a hand posture is shown.

The thermopile detector shows high optical absorption in the $8\text{--}14\mu\text{m}$ waveband [measured at room T using a Fourier-transform IR (FTIR) spectrometer], caused by the properties of the SiO_2 membrane[18], with an absorption peak of $\sim 90\%$ at $8.5\mu\text{m}$ [see Fig.3(a)], making it suitable for people presence detection[1]. For R_V tests, the device is mounted at a distance of 50 mm from a blackbody source (Fluke 4180) which is held at a constant T of 100°C . In our tests, the total emitted power from the blackbody is used for R_V calculations, which is extracted from the measured V_T . R_V varies with the wavelength[17], and is expected to be at a maximum in the 8 to 9 μm range [see Fig.3(a)]. The response uniformity to IR illumination per pixel for the 16×16 pixel array is shown in Fig.3(b). Pixel elements in the center of the membrane show a maximum 20% drop in signal level due to the lower efficiency of the thermopile cold junction heatsinking. At the edge of the membrane, the substrate acts as a more efficient heatsink, maximizing ΔT between the hot and cold junctions, thereby creating a higher V_T . Arrays with smaller

pixel areas show a drop in R_V due to the reduced conversion efficiency of each pixel, as shown in Fig.3(c). The cross-sensitivity of the sensor (a measure of the crosstalk between the pixels) was measured by electrically heating an individual pixel using an embedded micro-heater[23] and measuring V_T for both the heated and adjacent pixels. This is shown in Fig.3(d) for arrays with differing numbers of pixels. The 8×8 and 16×16 arrays show low thermal crosstalk (<2%); demonstrating the efficiency of the heatsinking between pixels. Arrays with smaller pixels show increased thermal crosstalk (>2.5%) due to increased thermal leakage, as the thermal path between pixels is reduced.

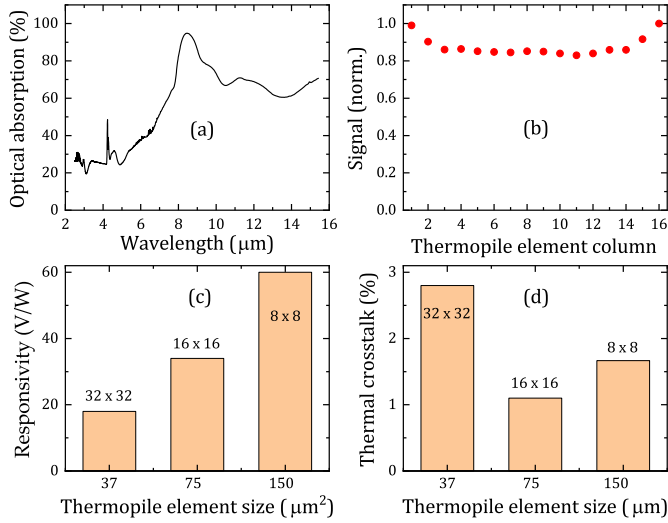


Fig. 3. (a) Infrared absorption spectrum of the 16×16 pixel array measured using FTIR spectroscopy, and (b) its pixel optical response uniformity. (c) Responsivity values shown for the 32×32 , 16×16 , and 8×8 arrays, and (d) the respective thermal crosstalk between pixels.

From the application perspective, a relevant figure of merit to characterize the thermopile array is the noise equivalent power (NEP), which corresponds to the lowest detectable power per square root bandwidth (f , typically normalized to 1 Hz)[17]. In a thermopile detector, the noise level is dominated by the thermal Johnson–Nyquist contribution $V_n = \sqrt{4kTR}$ [17], where k is the Boltzmann constant, and R the detector resistance. The NEP is then obtained dividing this value by R_V . The 16×16 pixel array has a R_V of 34 V/W , translating to a $NEP \sim 1.6 \text{ nW}/\sqrt{\text{Hz}}$. This gives a specific detectivity $D^* = \sqrt{A}/NEP$ [17] of $7 \times 10^5 \text{ cm}\sqrt{\text{Hz}}/\text{W}$, where A is the membrane area. These values are comparable to current state-of-the-art thermopile sensor arrays[13, 25]. A fuller range of specifications for our sensor is presented in Table 1.

To test our sensor in a real-world scenario, we use it to detect thermal images for a gesture recognition demonstration application. The system consists of the IR array, and an Umicore IR lens (focal length =6.8mm) with ~97% transmission in the 8–12μm range to form the images. The eight timing signals (X and Y), required by the thermopile array to output the pixel data, are generated by the MCU, with data being transmitted from the array one pixel at a time. We drive the system at a speed of 10 frames per second (fps), corresponding to ~300μs pixel sampling time. To compensate for R_V non-uniformity, we average 100 consecutive frames in a reference frame which is then subtracted from the normal frame to create a corrected frame. The reference

Table 1. Characteristics of the 16×16 pixel thermopile array.

Parameter	Value
Chip size	1.76 mm × 1.76 mm
Thermopile material	n^+ / p^+ Si
Membrane area	$1200 \mu\text{m} \times 1200 \mu\text{m}$
Pixel area	$75 \times 75 \mu\text{m}$
Membrane thickness	$5.17 \mu\text{m}$
Detector resistance	200 kΩ
R_V (100 °C, 1 Hz)	34 V/W
D^* (100 °C, 1 Hz)	$7 \times 10^5 \text{ cm}\sqrt{\text{Hz}}/\text{W}$
NEP	$1.67 \text{ nW}/\sqrt{\text{Hz}}$
V_n	$57 \text{ nV}/\sqrt{\text{Hz}}$
Thermal crosstalk	< 2 %

frame subtraction removes pixel-to-pixel offsets present in the thermopile array, and also the image of any warm objects that are stationary in the sensor’s field of view (FOV). The reference frame is taken after an initial ~10 min warm-up time, and then periodically to compensate for changes in ambient T . Thermal images of five different hand postures are presented in Fig.4(a-e).

To detect a hand posture, we use a low-complexity image processing algorithm based on an open-source computer vision and machine learning software library[26]. The algorithm uses the corrected frame to track a hand’s heat signature in the target area and estimate its posture. In our case, manually setting the threshold determines the temperature below which data is not considered, effectively setting the image background. The algorithm assumes that any pixel with a value above the threshold is a target of interest, while any pixel with a value below the threshold is not considered. An example is shown in Fig.4(f), where the background of Fig.4(e) was subtracted. The algorithm then finds the contour (convex hull[26]) of the thresholded hand posture and computes its extreme points [shown in red in Fig.4(f)], which are finally used to estimate the number of fingers shown in a posture. For more information on image processing see Ref.[26]. The system performs well for both tracking a moving object and detecting its posture. We also tested the system for people-counting in a room. For an operational test, the system was attached to the ceiling (in front of a door), and operated for several days continuously, with periodic connections to a host computer to command new reference frames. People entering and exiting the room were counted with a 100% accuracy. This shows that our device is beyond proof-of-concept and can already be used in a realistic setting, enabling posture detection and counting.

Our sensor could be improved in several ways. The overall optical absorption could be further enhanced by the addition of a high absorptivity coating, e.g., carbon nanotubes (CNTs) which have excellent optical absorption characteristics across the entire MIR range[7]. The processing software, including the R_V non-uniformity compensation could be implemented in an application-specific integrated circuit (ASIC), attached via face-to-face flip-chip bonding[7]. R_V could be further enhanced by vacuum packaging to minimize heat loss which would make higher resolution imaging possible[24]. The thermal crosstalk could be reduced by adding additional metal layers (to improve thermal isolation), thinner SOI and oxide layers, and/or optimization of the separating track widths. In addition, a set

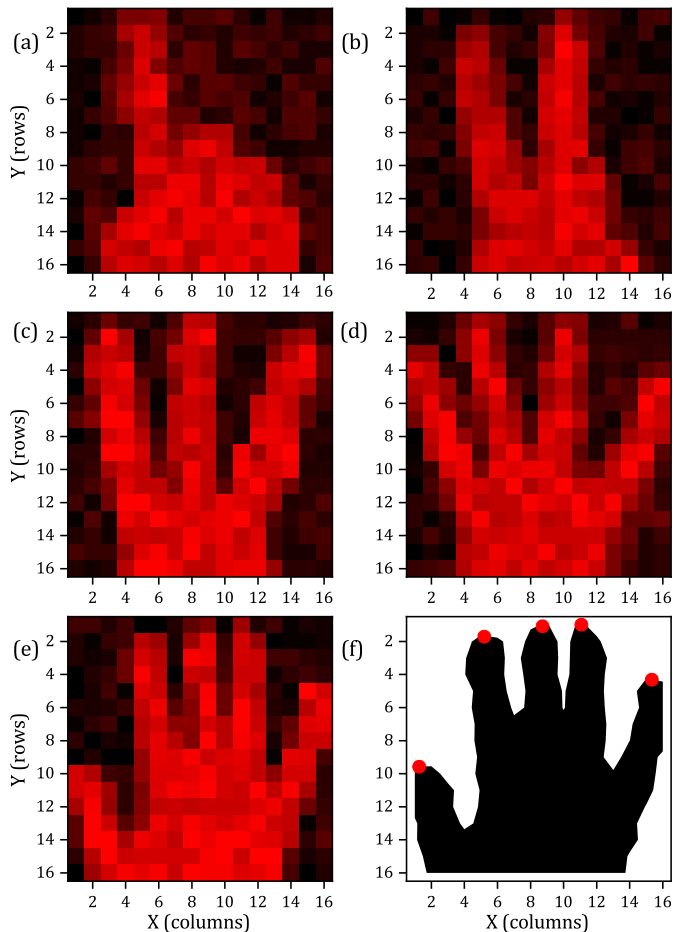


Fig. 4. Hand posture thermal images showing (a) one, (b) two, (c) three, (d) four, and (e) five fingers, respectively. (f) Image processing of Fig.4(e). The background is subtracted by manually setting a pixel threshold. Pixels below the threshold are not considered. An algorithm computes the extreme points (shown in red) of the thresholded posture, which are used to estimate the number of fingers, five in this case.

of stored coefficients to calculate initial pixel offsets based on ambient T , would enable the thermopile to be used without requiring a warm-up time. Faster scan rates are also possible, by optimizing the pixel settling time (e.g. by minimizing the total capacitance in the signal path). In our system, the thermopile array is being sampled continuously, leading to a power consumption close to 50mW. This could be significantly reduced by adding power cycling capabilities e.g., using a T correction algorithm to compensate the reference frame for ambient T changes that would allow the system to shut off the thermopile and the AFE. Compared to bolometer arrays, our thermopile array is manufactured using standard commercially available CMOS processes and can offer cost and power consumption compatible with the consumer electronics and IoT requirements.

In conclusion, we demonstrated a fully-compatible CMOS thermopile-based IR sensor array fabricated on a single SiO_2 dielectric membrane, significantly minimizing chip size and maximizing fill factor. Processing of the chip is also simplified by the use of a single membrane and standard CMOS tungsten layers for thermopile cold junction heatsinking. A 16×16 pixel array with enhanced optical absorption in the 8–14 μm band, low

crosstalk (<2%), and NEP ($\sim 1.6n\text{W}/\sqrt{\text{Hz}}$) is used for thermal gesture detection and people-counting applications. Our array is very flexible and can be adapted to many different situations, making it a promising candidate for a variety of low-cost, low-power-consumption, and high volume applications in the MIR spectral region.

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