HYBRID ELECTRIC AND THERMAL MODELLING OF SEMICONDUCTOR DEVICES USING THE TRANSMISSION LINE MATRIX (TLM) METHOD

By

AHMED ALDABBAGH, BEng. (Hons.)

Thesis submitted to De Montfort University

In partial fulfilment of the requirements for the degree of doctor of philosophy

June 2014

Dedication

To Imam Muhammad ibn Al-Hassan (AS)

To my father's soul Sahib Mohammad Ali

Abstract

Increasing the level of semiconductor devices' quality, reliability, and associated system safety is important as a fundamental contributor to overall technical advancement in the electronics sector. However, the growing requirements of optimizing device design for the broadest application areas need an enhanced level of understanding of thermal behaviour, and self-heating in particular, of semiconductor devices under harsh thermal operation conditions.

The aim of the research presented in this thesis is to develop and verify a numerical tool to assist in the understanding and the prediction of phenomena that contribute to the ageing and stressing of semiconductor devices. An aged semiconductor device can substantially adversely affect a system's electromagnetic compatibility (EMC) performance and reduce the desired functionality. The chosen method is a co-simulation approach for a linked electrical and thermal model, using the Transmission Line Matrix (TLM) method. This selection is based on having a single method that can simulate both domains, that is intuitive and flexible.

The method is enhanced by including electromigration and thermomigration mechanisms as an influential element in the calculation of material properties inside the hybrid solver.

The proposed model was subjected to a customized Thermal Cycling Test (TCT) in order to observe device behaviour and comprehend the degradation phenomenon that

appears after accelerated ageing test in RF LDMOS device. The research is a generic step forward, showing that a single TLM ‘engine’ can be used to model the linked factors in ageing and its effects, namely electrical, and thermal behaviour, that also allows for probabilistic events such as electro/thermo-migration.

Further, the method developed in this thesis is applied to two problem areas:

- Silicon nanowires, where the thermal radiation effects are addressed by adding an additional shunt conductance to a one-dimensional TLM node structure. The results demonstrate good agreement with previously published results and provide an appropriate tool to solve the internal heating problems and, hence, the degradation caused by thermal factors for future semiconductor devices.
- Silicon Carbide Metal-Semiconductor Field Effect Transistor (MESFET) and RF Laterally Diffused Metal Oxide Semiconductor (LDMOS) devices, which are approached as 2D structures, where the probability of occurring electromigration and thermomigration phenomenon in MESFET devices is investigated and the MTTF is shown when the model is subjected to thermal stress. The TCT is applied as a thermal acceleration factor in a MOS device, where the impact on the device IV (current-voltage) characteristic is studied. The results demonstrated good agreement with previous published results.

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List of main symbols

Symbol	Description
Af	Acceleration factor, kelvin
K_B	Boltzmann's constant, 8.63 $\times 10^{-5}$ ev/k
C_d	Capacitance per unit length, farad/m
N_d	Carrier density p- type, cm^{-3}
Z_{tl}	Characteristic impedance, ohm
N	Concentration of electron
P	Concentration of holes
G_{rad}	Conductance for radaition
L_d	Conductance per unit length, henry/m
σ	Conductivity, S/m
$\boldsymbol{C}$	Connect phase
A	Constant representing the dimensional problem
ρ	Density kg/ m^3
$\boldsymbol{E}$	Electric field as vector, volt/m
e	Electron charge, 1.6×10^{-19} coulombs
E_b	Emissive energy of black body
ε_m	Emissivity
λ_f	Failure rate
λ_{si}	Failure rate under stress tests conditions
λ_{ui}	Failure rate under use conditions

FE	Finite element method
J	Heat flux w/m^2
Q	Heat source, w/m^3
V^i	Incident voltage
${V^i}_L$	Incident voltage from left
${V^i}_R$	Incident voltage from right
N_i	Intrinsic carrier, cm^{-3}
$\mathbf{H}$	Magnetic field as vector, A/m
P	Maximum number of ports
$MTTF$	Mean time to failure
$NBTI$	Negative bias temperature instability
μ	Permeability, H/m
ε	Permittivity, F/m
V^r	Reflected voltage
R_d	Resistance per unit length, ohm/m
$\mathbf{S}$	Scatter matrix
S	Specific heat, j/kg k
R_{rad}	Surface resistance for radaition
Z^*	The effective charge number
Q^*	The heat of transport
E_a	Thermal activation energy, (joule/mole)
K_{th}	Thermal conductivity, w/m k
G_m	Transconductance, Siemens

ε_0	Vacuum permittivity, 8.85×10^{-12} f/m
$\emptyset$	Voltage or current

Publications

I. A. Al-Dabbagh, H. Sasse, M. Al-Asadi and A. Duffy, "*Modelling thermal radiation effects in nanowires using the TLM method*" Nanotechnology, IEEE Transactions on, vol. 12, issue 6, pp. 1118-1124, 2013.

II. A. Aldabbagh, H. Sasse, M. Al-Asadi, C. Oxley and A. Duffy, "*A review of the origin and modelling of non-linear behaviour in semiconductor devices*" in Proceedings of the 61st IWCS Conference Rhode Island-USA, pp. 366-372, 2012.

III. A. Aldabbagh and A. Duffy, "*Ageing effects on power RF LDMOS reliability using the Transmission Line Matrix method*", Microelectronics reliability Journal, Elsevier, 2014, under review.

IV. A. Aldabbagh and A. Duffy, "*The electromigration ageing effects on MESFETs using TLM method*", Micro and Nano systems letters, 2014, under review.

V. A. Aldabbagh and A. Duffy, "*Co-simulation approach in nanowires using TLM method*", Advanced Modelling and Simulation in Engineering Science Journal, 2014, under review

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Acknowledgment

All praise and thanks to my Lord God Almighty and peace and blessings be upon his messenger Muhammad and his progeny.

First and foremost, I would like to express my sincerely appreciations and gratitude to my first supervisor Dr. Alistair Duffy for his everlasting support, and encouragement. I am forever thankful for the guidance and help extended towards me to complete my PhD. I extend my thanks to Dr. Hugh Sasse for introducing me to the coding world, and for the long time of discussions.

I would like to thanks my second supervisors Dr. Chris Oxley and Dr. Muhammed Al-Asadi. My deep gratitude goes to Professor Farouk Shakib for his assistance and for the time he spent in checking my thesis.

Special thanks to my family:

To my lovely wife Jinan, my sons Yousif, Taha, and Ali for their patience, love, and endless encouragement.

Last but not least to my mother for her love, prayers and spiritual support.

Chapter 1 Introduction

Summary

The purpose of this research is to enhance the understanding and identification of ageing mechanisms in semiconductor devices using a combination of electrical and thermal modelling. In order to do this, a new tool is designed using the TLM method. Employing the method in this field of research provides valuable opportunities to explore more applications and capabilities that can be instrumental in indentifying a device ageing and its reliability in general. This chapter introduces the problem to be solved and a preliminary introduction to the solution space to help the reader set the context for later chapters.

1.1. Numerical Modelling

Numerical modelling is an important tool for the computation of physical phenomena using computers without the need to actually build something [1]. The numerical model helps in the computation and analysis of different scenarios mathematically, so as to predict what will occur in the same condition in the true operation condition. The modelling process can have different levels of complexity depending on the nature of the physical problem. The modelling methodology can be structured into the following steps [2].

- Conceptualization. Whereby observation and the analysis are related to relevant physical principle.
- Formulation. Describe the physical principle in a mathematical algorithm.
- Computation. Coding the algorithm.
- Validation. It is essential for the model to be tested for numerical and physical reasonableness.

There is wide range of possible modelling methods. Some of the most commonly encountered methods are:

- Method of Moments (MOM): This method originated in the 1960s [3] to solve linear partial differential equations of unknown function by solving the matrix equation resulting from the introduction of a certain set of basis functions to represent the unknown side of the function. One example that fit this method is the Poisson's equation. More details can be found in [4, 5].
- Finite Element (FE): Established in the early 1940's to study mechanical problems [6], later adapted for study electromagnetic applications. The principle of this method is to simplify a problem representing a complex structure by reducing it to a set of finite elements, i.e. small structures. The complex function controlling the behaviour of the whole structure is simplified over each one of these elements [1]. It can be used for arbitrary and irregular shapes, for more details see [7, 8].
- Transmission Line Matrix Method (TLM): First used to solve electromagnetic problems, it is based on finding the analogue between Maxwell's equations and

currents and/or voltages in one-, two- or three-dimensional space. Further details will be discussed in the chapter 2, also for more information see [9, 10].

- Finite Difference Time Domain method (FDTD): This scheme was originally developed to simulate electromagnetic environments by interleaving two grids: one used for calculating the magnetic fields and the other the electric fields. This interleaved grid ("Yee cell" approach is still very common). It discretises Maxwell's equations in time and space, thus allowing straightforward calculation and simple implementation. The drawback of this method is the difficulty in dealing with open boundaries, further details can be found in [11, 12].

  Generally, the methods can be divided into two groups based on the implementation of Maxwell's equations.

A. Integral methods, such as; MOM and FE
B. Differential methods, for example; FDTD and TLM

The advantages of time domain methods over frequency domain methods can be summarized in following points [13-15].

- Solutions able to cover a wide range of frequencies with a single simulation by using Fourier Transform solver.
- The time-animated movement of parameters such as, electric fields can be checked at any stage through the time progression. This active picture can be useful for observing the model behaviour.
- More suitable for time variation problems.

- More appropriate to deal with a wide range of frequencies and for transient problems.

On the other hand the Frequency domain methods, such as FE and MOM have advantages in.

- Obtaining results at a single frequency
- Dealing with frequency-dependent parameters

1.1.1 Selection of the simulation method

The choice of the TLM method was driven by the fact that it has the flexibility to model electrical, and thermal diffusion problems using the same basic solver, the internal and external environments can be modelled at the same time, the time–domain nature permits a change of parameters at each time step without considerably increasing computational difficulty, which is an important consideration when electro/thermo-migration is to be considered. The TLM implementation results in a solution that generally has a low level of complexity. Moreover:

As the electric field is a natural part of the TLM method, therefore, dealing with ageing problems that attributed to high electric field, i.e. electromigration will be more reliable.

- TLM is considered as a one-step technique, meaning that the field parameters are defined at the any point in the model. While in FDTD, such versatility is not applicable given that electromagnetic fields are spatially separated [16, 17].

- TLM uses an equivalent transmission line circuit to solve the physical problem, which is more familiar to the engineer. This 'visualisation' in the FDTD method falls in the discretization of Maxwell's equation rather than the model.

1.1.2 Why co-simulation approach?

The hybridized model will provide an integrated system that has the capability to deal with thermal factors that have the key role in degradation and ageing of semiconductor devices. Furthermore, it is

- More accessible, in that it deals with both electric and thermal parameters.
- Allows better accuracy, as the internal heating effects will account for all regions in the problem space.

By packaging the electrical and the thermal parameters together, i.e. having them communicate within a shared simulation engine, a continuous updating process will occur to maintain any changes in the material properties; such as mobility, permittivity, and resistivity. Recently, this approach has been used in [17] for a power delivery network to get accurate calculation for internal thermal effects.

1.1.3 Is the ageing phenomenon important in electronic devices?

Ageing is the expected consequence of any semiconductor device under frequent or continued usage. However, the possibility of failure will increase over time leading to catastrophic failure, due to the degradation processes inherited from the material used.

The recently significant development in semiconductor devices technology and the exponential demand on such devices to meet the requirements of continuous tasks that could be in use for many years, would weigh in on a positive side of the above question.

1.2 Research motivation

The list of questions developed in the previous sections can be seen as a prelude to the main motivation behind this research. This can be summarised in the following points.

- 65% of electronic failures are thermo-mechanical in origin [18] and with most electronic systems relying on semiconductor devices, ageing and failure in semiconductors is a major contributor to electronic system reliability
- A better understanding of the relationship between current, heat and electromigration in existing semiconductor systems could, ultimately, be used to help design more resilient devices.
- Understanding heating in nano-structures could be a key to designing reliable emerging nano-enabled transistor devices

This research project addressed these factors by developing an electro-thermal co-simulation tool in 1D and 2D.

1.3 Research objectives

The ultimate objective of this research is to verify the suitability of the TLM method in dealing with the ageing aspects through, electromigration failure mechanism, and thermal cycling tests using a hybrid solver. Furthermore, in this thesis we aim to delve into the nanoscale field through a one dimensional model to deal with the problem of heat dissipation. Concentrating interest towards nanowires, or semiconductor nanowires will provide an important tool for future semiconductor devices en route for solve the internal heating problems, and thus, the degradation of emerging devices by thermal causes. This target has been effectively achieved by modelling heat diffusion problem in silicon nanowires, in particular modelling the heat radiation aspect forming an additional contribution for TLM applications.

1.4 Organisation of the thesis

A discussion of the modelling principle and the importance of simulation in designing, also the motivation behind the choice of TLM, is presented in this introductory Chapter.

In the first part of Chapter 2, the simulation method principles are discussed, and a substantive review of the electric and the thermal diffusion modelling is presented. Additionally, the modification that have been introduced to the TLM node to express any changes for material properties will be highlighted, and the co-simulation approach in TLM will be discussed. In the second part, a literature review regarding the ageing in semiconductor devices is presented.

Chapter 3 gives a presentation for the nonlinearity phenomenon in semiconductor devices, and the convenient means to solve this problem in a 1D unified solver to model charge diffusions and in two dimensional models by the proposed new set of equivalence between the model and the device parameters.

Chapter 4 expresses the TLM simulator and the advantages from linking two solvers in one engine. The hybrid solver offers the benefits of a reduction in problem complexity, the development in simulation, making the model more accessible, and accelerating the simulation process despite the temporal difference between the electric and thermal diffusion. Moreover, the results generated from the 2D model are shown.

Chapter 5 describes the nanostructure: future semiconductor devices as a possible application for the 1D TLM model, where the thermal diffusion problem is presented, and the heat radiation aspect is included in the heat dissipation calculations.

In Chapter 6, ageing is the main topic in this chapter. A review and detailed explanation of the most important mechanisms to investigate device reliability and the important factors that reduce the lifetime of semiconductor devices. This is accompanied with effective steps to include TCT, electromigration and thermomigration mechanism as an influential element in TLM solver to model ageing problem.

Chapter 7 concludes the results and the advantages that have been achieved, and presents potential opportunities to extend the work by suggesting a plan for future research.

Chapter 2 Introduction to Modelling in TLM and Semiconductor Ageing

Summary

This chapter is in two parts:

- Part one is the main outline of simulation methodology, starting with the basis of the transmission line matrix (TLM) method. In section 2, the Huygens principle is described. An outline of homogenous and inhomogeneous modelling is discussed in section 3. In section 4, the thermal diffusion modelling in the TLM method is illustrated for one and two dimensional problems. Section 5, the co-simulation approach is presented together with the TLM examples.
- Part two, gives a description of ageing in semiconductor devices. Finally, the conclusion for this chapter shows that dealing with any changes in material properties can be resolved by adding a stub to the node structure, and the same principle is applicable in modelling the thermal diffusion problem, which paves the way to a more efficient modelling for the ageing problem in semiconductor devices, this is summarised in section 7.

Part I:

2.1. Introduction

Accurate simulation is a necessity for reducing costly repetitions in design in order to minimize the total cost and the concept-to-production lag [19, 20]. The transmission line matrix method is a time-domain numerical modelling technique. It is an unconditionally stable method, using the concept of a network of interconnected transmission lines. It is based on the analogy between an electric network and fields [21]. TLM has been used for electromagnetic simulation since the early 1970s [22]: it was originally developed to solve Maxwell's equations [23]. More recently, this method was employed in multiple areas to model many physical phenomenon such as, charge diffusion in semiconductors [24], laser diodes, vocal tract acoustics [25, 26], and recently in nanoscale applications [27]. A conceptual analysis of this method can be formulated in two different ways [28]:

- Firstly, it can be considered as an electric-circuit equivalent of electromagnetic-field phenomena where solutions are concluded by employing the isomorphism between the circuit and field (e.g. thermal and electromagnetic) equations.
- Secondly, it can be formed as a discrete structure of the Huygens's principle where the wave propagation is a product of countless isotropic wave scattering actions along a wave front.

The unconditional stability, simplicity, and the precise nature of the TLM are significant strengths of this method. In the following sub-sections, a review of the key elements that form this technique will be detailed.

2.1.1 Scatter and Connect phases

The time delay for the pulses travelling between the points in the electrical network can be considered the most important property of the transmission line, which provides the temporal discretization. While the distribution of mesh points in the modelled space gives the spatial discretization [29].

The TLM method is based, fundamentally, on the network of transmission line, where in this technique the transmission line can be divided into repeated small sections and each section will contain a "node". When the pulses approach these nodes they will scatter, either being transmitted with transmission coefficient (τ) , or get reflected back to the same transmission line with the reflection coefficient (Γ). The reflected and transmitted pulses from the nodes act as incident pulses on the neighbouring nodes for the next time step [25]. Two main processes involved are, the scatter phase $\boldsymbol{S}$ as in equation (2.1) and the connect phase $\boldsymbol{C}$ as in equation (2.2) [9].

$$V^r{}_k = \boldsymbol{S}\ V^i{}_k \tag{2.1}$$

$$_{k+1}V^i = \boldsymbol{C}\ V^r{}_k \tag{2.2}$$

where; V^r is the reflected voltage, V^i is the incident voltage, and $_{k+1}V^i$ is the incident voltage for the next time step.

When modelling any physical problem, it is necessary to choose appropriate spacing between the nodes. It is generally accepted that the spacing should not exceed one tenth of the wavelength to minimize the calculation error introduced by discretization, see [9] for more details. Then the determination of the time step is dependent on transmission line velocity v and node spacing Δl, which is given by (2.3).

$$\Delta t = \frac{\Delta l}{v} \tag{2.3}$$

2.1.2 Matrix

The relation between the incident and the reflected signals for each node is controlled through the scattering matrix. The matrix takes account of any changes that may take place in material properties (inhomogeneities) by an introduced stub. The stub represents an additional port for the TLM node, executing a similar job as a standard port, where any pulse entering the stub lines will be transmitted and reflected back to the node. The stub can be represented in three different forms.

a. Stub inductance
b. Lossy stub
c. Stub capacitance

As illustrated in Figure 2.1 for 2D node as an example for the above three forms. More details will be discussed in section 2.3.

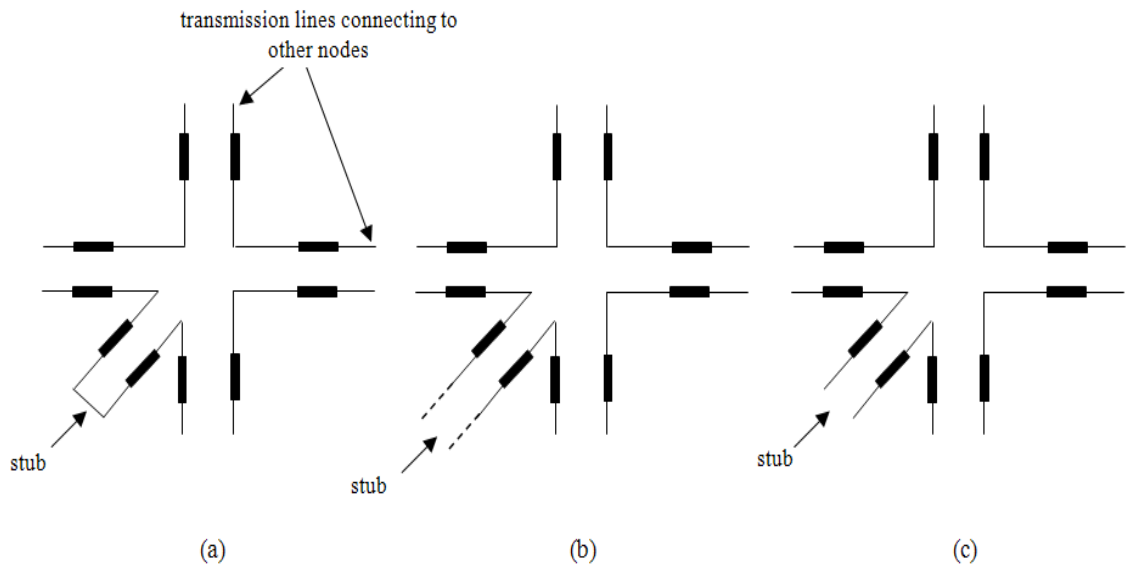


Figure 2.1: 2D node with a stub as (a) inductor, (b) lossy and (c) capacitive stub

The spatial resolution of the results can be increased by reducing the timestep. The stub is represented by an additional-port transmission line, where the length is adjusted so that the voltage pulse enters the stub and reflects back to the node at the next time step. At this point, a short circuit termination is required when modelling an extra inductor (for a 1D model see Figure 2.2), while an open circuit is required in case of extra capacitance, as shown in Figure 2.3 [9].

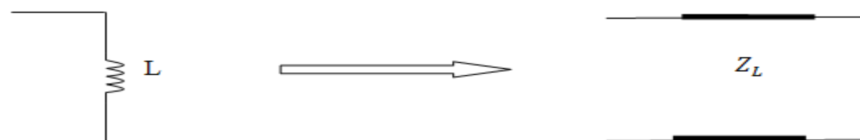


Figure 2.2: an inductor and the stub model

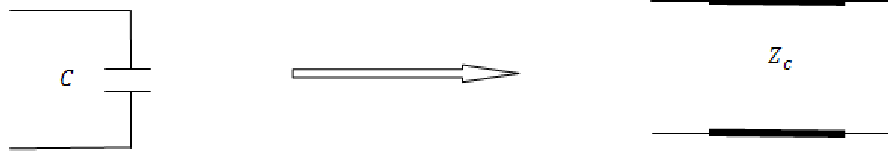


Figure 2.3: capacitor and the stub model

2.1.3 Boundary conditions

Most physical problems that cope with the electromagnetic simulation technique have a defined space as pulses scattered at the boundaries need to be terminated appropriately for stability to be preserved. The boundary condition can be classified into three types [9, 30].

I. Perfectly matched layer (PML): or absorbing boundary where all pulses are absorbed, $R=Z$ (where; R is the resistance and Z is the characteristic impedance of the transmission line)

II. Perfect Magnetic Layer: the boundaries are perfect conducting surfaces, the pulses return with same polarity and reflection coefficient equal to 1, and the resistance is an infinite $R \rightarrow \infty$ (open circuit). This is often used to represent a symmetry plane in the model.

III. Perfect Electric Layer (PEL): the boundaries are perfectly insulated, the pulses return with inverted polarity and reflection coefficient equal to -1, and the resistance is very low $R \rightarrow 0$ (short circuit).

2.2. Huygens principle

The propagation of the electromagnetic radiation as a series of propagating wavelets was first discussed by Christian Huygens [31]. The same wave nature of Huygens model was used by Johns and Beurle [22] which was initially a development of the physical circuit model proposed by Kron [32]. It presented a new two dimensional numerical simulation technique, by modelling the scattering of electromagnetic problems. The Huygens model can be briefly described as a wave front consisting of a number of sources of radiation that each generate new spherical wavelets - see Figure 2.4. By combining these wavelets, a new wave is produced continuing to propagate in the same manner. The continuous nature of the model in propagation and the scattering of the electromagnetic waves represents the main principle of the scatter and connect phases in the TLM method.

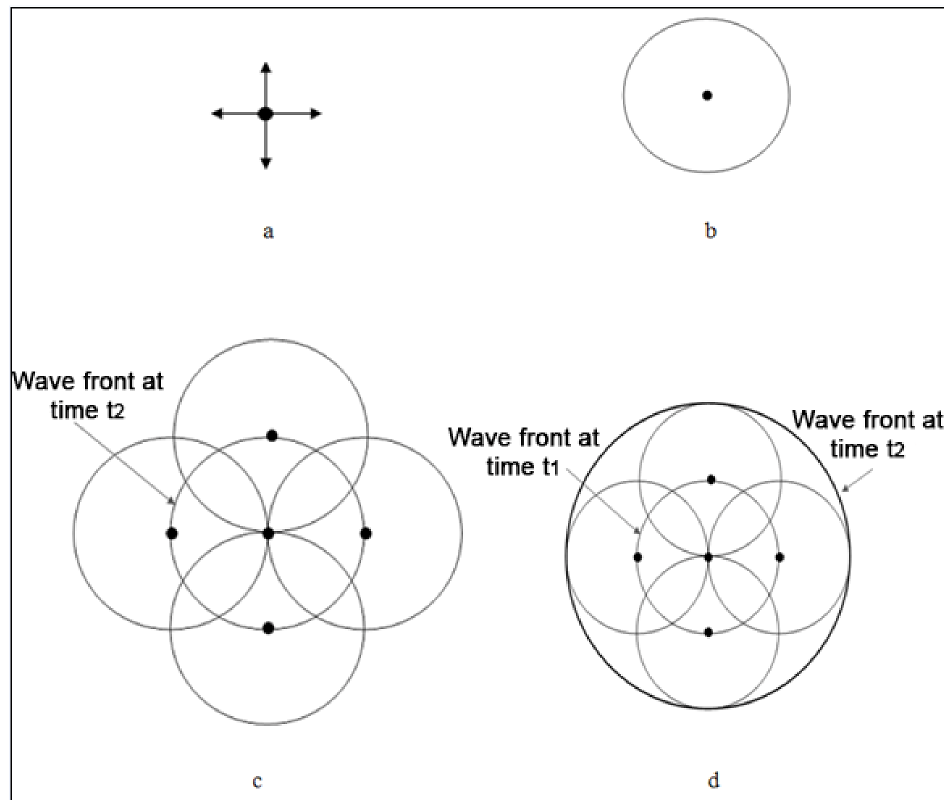


Figure 2.4: a) the source point for scattering wave, b) wave at t_1, c) four points in wave front each one representing a new point source and d) wave front at t_2

In TLM, to achieve a digital model for the wave propagation as explained in Huygens model, the discretization of the space and time take the following form.

$$\Delta t = \frac{\Delta L}{v} \tag{2.4}$$

where: Δt is the sampling time, ΔL is an element of discretized space, and v is the wave speed in the medium. For instance, in a two-dimensional TLM model the wave propagation on a mesh of transmission lines can be described by an excitation pulse of value 1V magnitude at one node (as shown in Figure 2.5), where part of the wave will propagate (transmit) towards the neighbouring four nodes; while the other part will

reflect back as reflected voltage. The propagation process will form secondary rings around each node, as a result from the transmitted and the reflected waves, leading to the formation of the overall waveform. The TLM model behaviour shows agreement with Huygens model, and provides a good implementation for Huygens principle: see Figure 2.6.

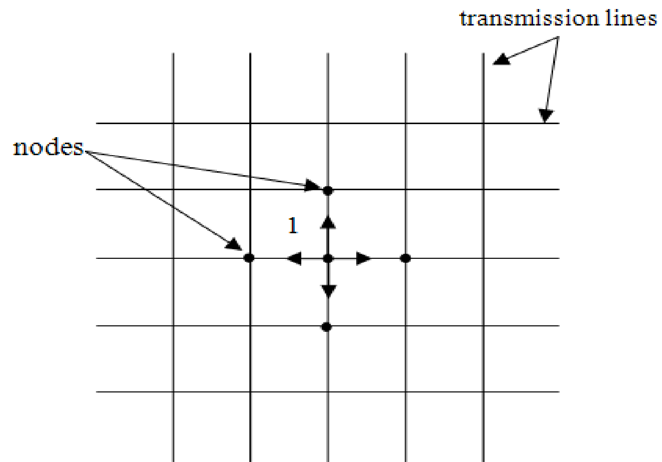


Figure 2.5: TLM mesh and the result of impulse excitation of 1V after the first scattering phase

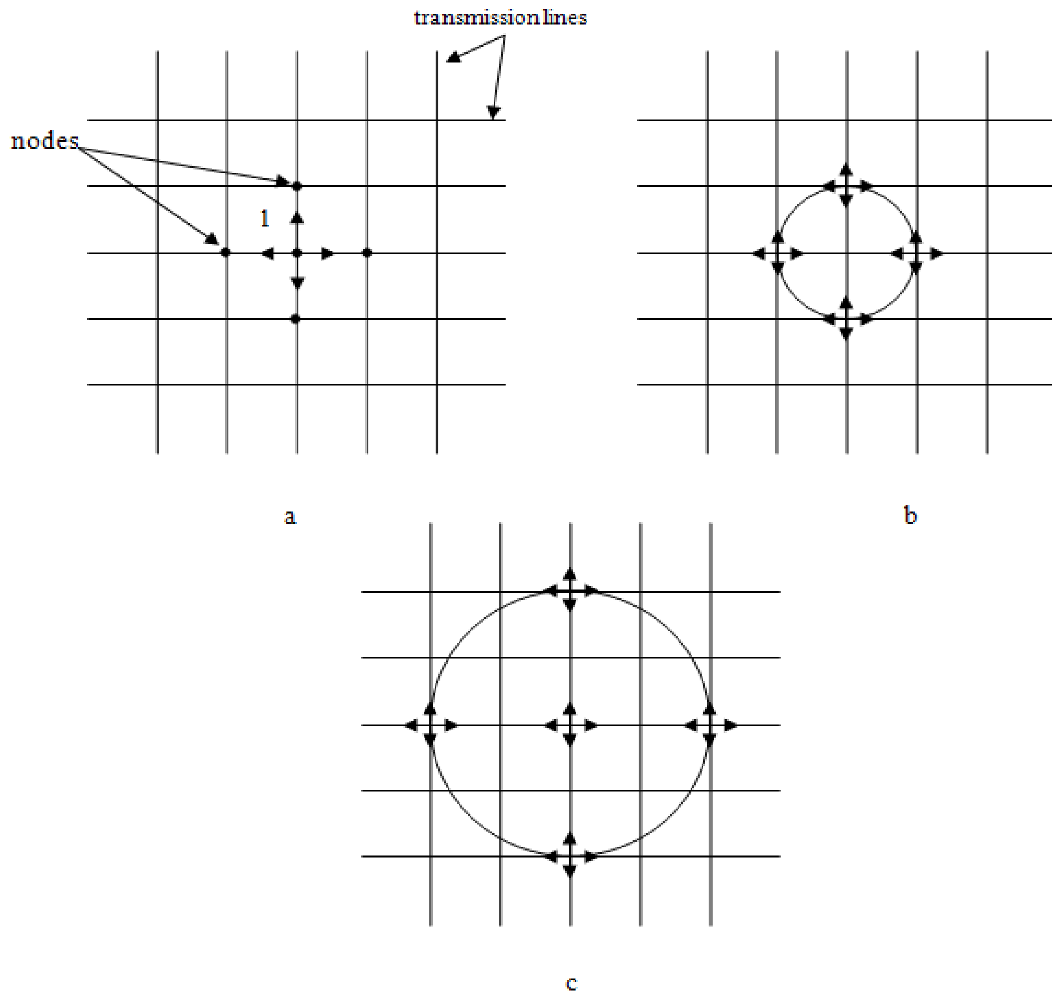


Figure 2.6: scatter results

2.3. Homogeneous and inhomogeneous medium

A homogeneous medium is any medium having the same properties such as, permittivity, permeability, conductivity, meaning the medium has the same material properties along the whole structure, and the wave propagation will not suffer from any speed changes thanks to a constant characteristic impedance, since this is a function of the series inductance, resistance, conductance and shunt capacitance of the transmission

line, as explained in equation (2.5). This is illustrated in Figure 2.7 for a basic line segment, [33] and in Figure 2.8 when it is represented in TLM form.

$$Z = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{2.5}$$

If losses G and R are neglected ($R \ll \omega L, G \ll \omega C$) then equation (2.5) get simplified form for characteristic impedance as in equation (2.6) [9].

$$Z = \sqrt{\frac{L}{C}} \tag{2.6}$$

The velocity of propagation in an homogenous medium can be described as a function of inductance and capacitance, as illustrated in equation (2.7) [9].

$$v = \frac{1}{\sqrt{LC}} \tag{2.7}$$

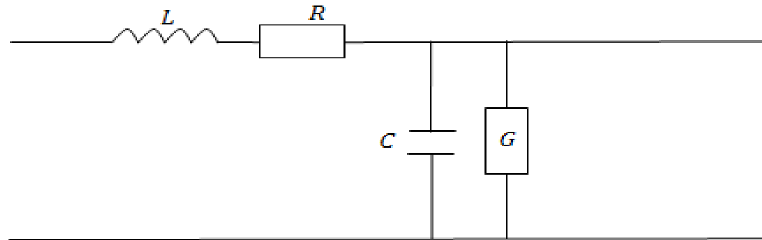


Figure 2.7: basic line segment 1D

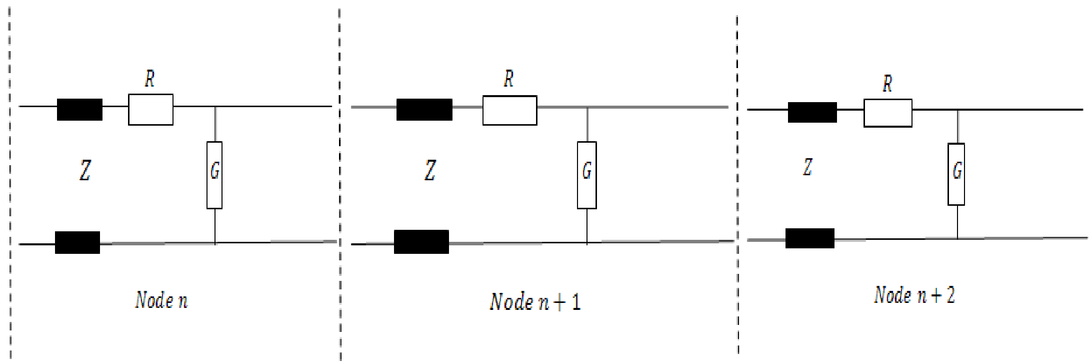


Figure 2.8: TLM nodes in 1D model

This simple relationship will not last in the case of the inhomogeneous medium when different material properties are introduced. Inductance or capacitance stubs will need to be introduced on the TLM node to model these changes in material properties for each different material region. Adjustment of circuit parameters is required to account for magnetic permeability and dielectric permittivity values, as given in equation (2.8). Therefore, the speed of propagation will be controlled by the material properties.

$$v = \frac{1}{\sqrt{\varepsilon\mu}} \tag{2.8}$$

Changing the inductance and capacitance to calculate the changes in permeability μ and permittivity ε will have effects on the simulation synchronism [30].

2.4. Thermal diffusion

Thermal diffusion is defined as energy transferred from a hotter body to a cooler body due to temperature difference. It can be described by equations which relate the energy

transferred in unit time to the temperatures and physical properties such as, specific heat and thermal conductivity of the bodies involved in the transfer.

There are three basic modes of heat transfer: conduction, convection and radiation. These can occur separately or simultaneously [34]. The diffusion process is a dominant mechanism for the movement of heat, where this mechanism is governed predominantly by two basic laws of diffusion [35]. The first law accounts for the difference in heat flux or flow across the element and that accumulation of heat corresponds to an increase in temperature with time, so for one dimension, one can express that by the following equation (2.9).

$$\frac{\partial T}{\partial t} = \frac{1}{S}\frac{\partial J}{\partial x} \tag{2.9}$$

where: T is the temperature, t is the time, S is the specific heat in $J\,K^{-1}\,m^{-3}$, and J is the heat flux.

While the second of these basic laws says that the heat-flux density J across the element is related to the gradient of the temperature across it, and can be represented as follow.

$$q = -k_{th}\frac{dT}{dx} \tag{2.10}$$

where: $\frac{dT}{dx}$ is the temperature gradient, q is the heat transfer per unit area and k_{th} is the thermal conductivity.

Since the heat diffusion is considered an important factor in the modelling of any semiconductor device, where reliability issues are concerned, it was imperative to address this problem in TLM. There has been some work to simulate thermal diffusion

problem from the early years of the emergence of TLM [23, 36]. The implementation has been used to model the heat diffusion in, one dimensional [37], two dimensional [38], and three dimensional problems [39]. Thermal diffusion expressed in equation (2.11) has received much attention [38, 40, 41] and recently in [42] using FE method. It has been possible to address many aspects in the TLM method using an equivalent formulation in equation (2.12). Using the isomorphism between equations (2.11) and (2.12), the temperature in the thermal domain can be represented using voltage in the electric domain [9]:

$$\frac{\partial \theta}{\partial t} = \frac{k_{th}}{S}\frac{\partial^2 \theta}{\partial x^2} + \frac{Q}{S} \tag{2.11}$$

$$\frac{\partial V}{\partial t} = \frac{(\Delta x)^2}{RC}\frac{\partial^2 V}{\partial x^2} + \frac{I}{C} \tag{2.12}$$

where: θ is the temperature, k_{th} is the thermal conductivity, Q is the heat source, I is the current.

A one dimensional circuit implementation is shown in Figure 2.9. Kirchhoff's voltage and current laws can be applied to give the relationships in equation (2.12)

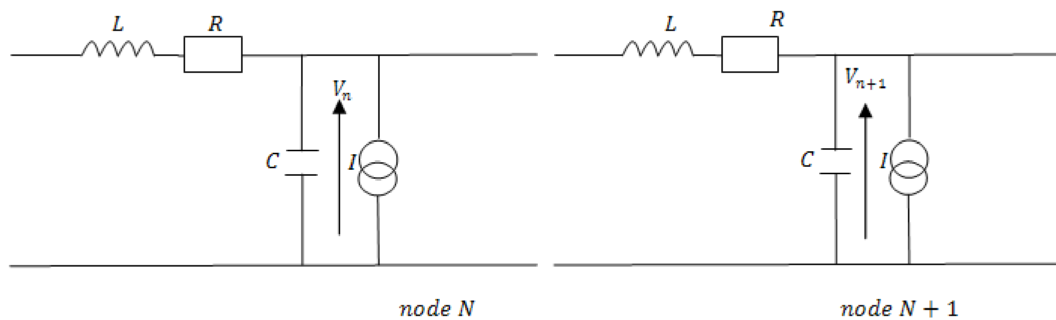


Figure 2.9: electric circuit to 1D thermal diffusion model

By comparing equation (2.11) with (2.12), the following equivalences can be obtained from the isomorphism:

$$V \leftrightarrow \theta, R \leftrightarrow \frac{\Delta x}{k_{th}A},\ C \leftrightarrow S\Delta x\mathrm{A},\ i \leftrightarrow JA,\ I \leftrightarrow Q\Delta xA \tag{2.13}$$

Equation (2.13) describes how the electric circuit parameters are employed to model the heat diffusion problem.

For a 2D problem, the characteristic impedance for the transmission lines will be [43].

$$Z = \frac{2\Delta t}{C} \tag{2.14}$$

The nodal temperature for Figure 2.10, can be found using the parallel generator (Millman's) theorem [44], as follows.

$$V_n = \frac{\sum_0^P 2V^i + I}{\frac{4}{R+Z}} \tag{2.15}$$

where: *n* is the node, *P* is the maximum number of ports. The scatter matrix can be described by the following equation.

$$\begin{bmatrix} V^{r1} \\ V^{r2} \\ V^{r3} \\ V^{r4} \end{bmatrix}_k = \frac{1}{(2R+Z)} [\boldsymbol{S}] \begin{bmatrix} V^{i1} \\ V^{i2} \\ V^{i3} \\ V^{i4} \end{bmatrix}_k + \frac{I(Z+R)}{4} \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} \tag{2.16}$$

$$\boldsymbol{S} = \begin{bmatrix} (2R+Z) & Z & Z & Z \\ Z & (2R+Z) & Z & Z \\ Z & Z & (2R+Z) & Z \\ Z & Z & Z & (2R+Z) \end{bmatrix} \tag{2.17}$$

where: *k* is the time step.

The connect matrix works on the reflected voltage pulses that travelled back to the nodes to use as incident pulses for the next time step, as follow.

$$V^{i}_{k+1} = C\, V^{r}_{k} \tag{2.18}$$

Then for 2D, the equation (2.18) can be written for the four ports – see Figure 2.10 [9].

$$V^{i1}{}_{k+1}(x, y) = V^{r3}{}_{k}(x, y-1)$$

$$V^{i2}{}_{k+1}(x, y) = V^{r4}{}_{k}(x-1, y)$$

$$V^{i3}{}_{k+1}(x, y) = V^{r1}{}_{k}(x, y+1)$$

$$V^{i4}{}_{k+1}(x, y) = V^{r2}{}_{k}(x+1, y) \tag{2.19}$$

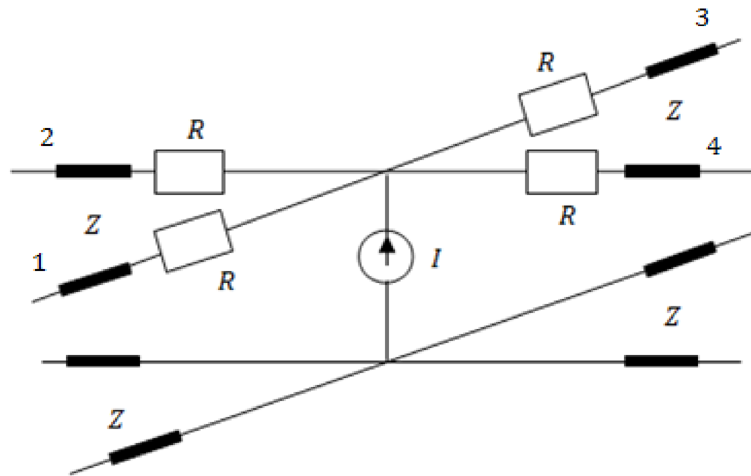


Figure 2.10: 2D TLM node for thermal diffusion problem

2.5. Co-simulation approach in TLM method

The co-simulation technique has been used in different systems with success; see references [43, 45, 46]. In [43], the 2D TLM co-simulation model was employed to model microwave heating, the results showed that this approach can provide optimization in reducing power consumption. It also offers a set of solutions to overcome the problem of the large difference in temperature within the load used. Furthermore, an enhanced 2D software package was introduced in [21] for modelling microwave heating, which is mainly suited for the high temperature heating of ceramics. The results from [21] showed that combining the polynomial terms for thermal and electrical parameters provides the means to model load materials in a more sophisticated manner.

These topics faced the difficulty of combining two physical problems, and handling the propagation speed difference at the same time in one engine. In coupling the electric and the thermal models, there is a need for interaction between the variables of the two solvers by exchanging parameters such as; resistivity, permittivity, temperature, heat losses, and thermal conductivity. Such changes are modelled in the TLM method, through adjusting the parameters of each single node in different regions [47]. Therefore, it was necessary to find homogeneity between the two processes and to maintain a “common language” between the two solvers. A sequencing mechanism is used in running both models based on the time difference. Consequently, this effect will translate into a heat source in the thermal solver; therefore the thermal model will start the heat diffusion process without any external heat generator. Thus, a new set of initial temperature for each node is proposed, and passed as a new feed to the electrical model

to be a new start condition for the second round, including an update for the material resistivity dependent on the amount of temperature change.

In this thesis, the hybridized engine will combine electric and the thermal solver, as illustrated in Figure 2.11, where the use of power dissipation in the electric solver as a heat source in thermal solver will maintain the updating process for nodal temperature and alter the material properties depending on temperature differences. More details for the TLM simulator and implementation will be discussed in Chapter 5.

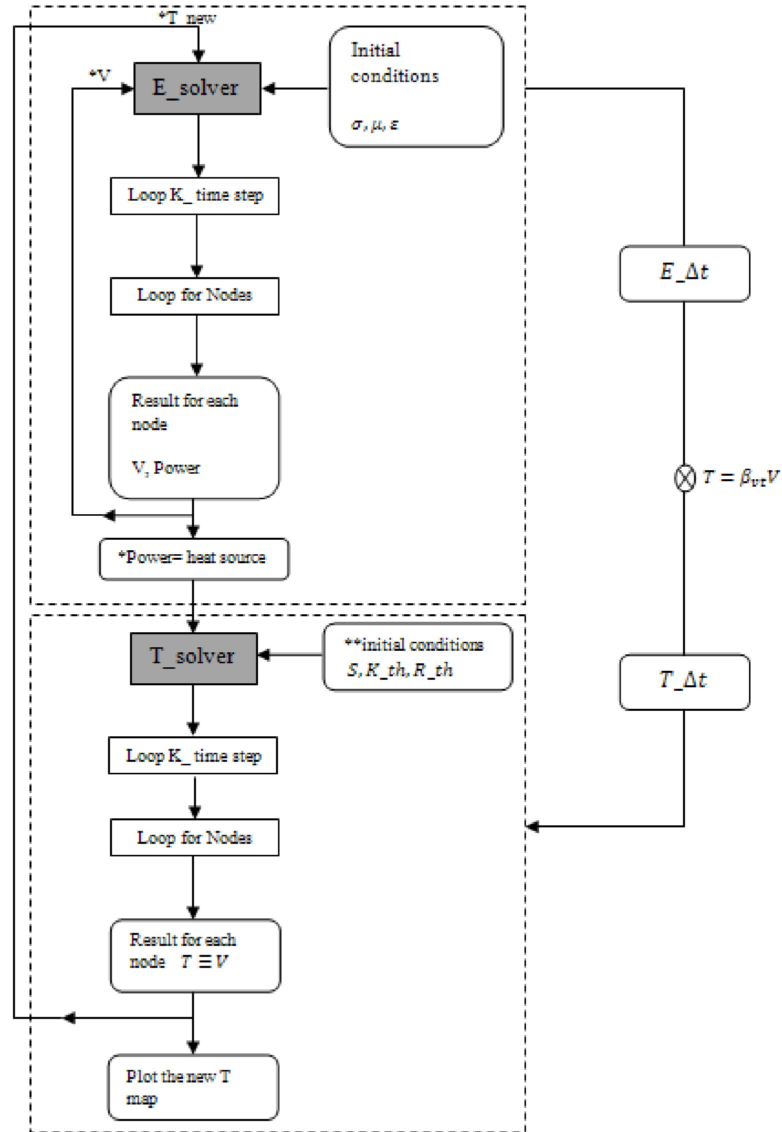


Figure 2.11: co-simulation process

2.5.1 Device of interest

The selection of 4H-SiC MESFETs was driven by the availability of data, in order to validate the TLM model results. The Metal-Semi Conductor Field Effect Transistors (MESFET) have been used in the microwave industry for many decades, particularly

Silicon Carbide based devices, and are considered to be very good candidates for high frequency and high power applications. These devices have received considerable attention due to their exclusive physical and electric properties such as; high saturated electron velocity, wide band-gap, high breakdown electric field strength, and high thermal conductivity [48-51].

Previous studies addressed the problem of self-heating in SiC MESFETs [52-55]. Recently, Feradji et al [52] have developed a numerical model of self-heating in multi-finger 4H-SiC MESFETs using a 3D TLM model and the results showed that increasing fingers spacing will significantly reduce the hot spots temperature. In [55], an enhancement for the breakdown voltage of 4H-SiC by 180% was demonstrated using floating metal strips (FMS) between the gate and the drain of the device. The improvement took another aspect in [56] by an increase in RF performance and reduction in cut-off frequency in an improved dual-channel layer 4H-SiC MESFET, using a 2D simulation model. While in [49] the power performance of SiC MESFETs improved by controlling the thickness of the buffer layer and the results urged an increase in the thickness of the buffer layer or making it highly doped to avoid the conductive path from occurring. The results shown from the last article confirm that changing the physical structure may help to improve the functionality, and longevity, of the device.

Self-heating effects are due to electric current flow in any semiconductor device. The current flow process increases electrons' kinetic energy.

Hence, the collision rate between the lattice and the energetic electrons will increase, leading to an increase in the channel temperature, which can dramatically worsen the I-

V characteristics [54]. Thus, knowledge of the temperature profile in the active region is essential to evaluate the device reliability and performance. More details about the solver results will be shown in Chapter 5.

Part II

2.6. Background to modelling ageing phenomenon

One of the essentials of understanding device reliability requires an understanding of the failure rate. In fact, degradation can be described as a cumulative process, this fact can be true for a single reliability effect, and for multiple reliability effects in a certain device.

The traditional method of determining a device's failure is by using the acceleration process, where the device is subjected to a series of tests under high temperature and/or high voltage. The failure rate is obtained for each case and compared with end-use conditions to give an estimate of the failure rate. The process also involves applying a high level of the stress condition (temperature and/or voltage) for a short period of time in order to accelerate the damage rate for relevant failure mechanism. A recent industrial practice in dealing with semiconductor devices ageing "guardbanding" is to test the device under the worst degradation that the device may suffer during the lifetime, due to worst voltage, worst temperature, and worst percentage of time the device is on. However, the worst-case need to account for the standard deviations

(spread) of ageing distributions, as the same device under similar workload and environmental conditions may suffer ageing at different rates [57].

The ageing mechanisms are varied in their dependency on the impact factors, such as for HBTs, the Bipolar Beta ageing mechanism is usually used, which is based on a degradation factor that is due to raised resistance of emitter ohmic contact and/or degradation due to base leakage current [58]. While for FET transistors, the transconductance ageing is more commonly used to calculate degradation rate, depending on the change of the gate leakage current and/or the drain-source resistance, which is affected by the scattering process inside the drain-source channel [59].

However, some methods can be used in general such as; Negative Bias Temperature Instability (NBTI), which degrades the voltage (threshold voltage) of a transistor with time [60] depending on voltage and/or temperature profiles, workload time, and elapsed time. The failure rate of semiconductor devices can be classified into the following terms:

Table 2.1: failure rate terms

Terms	Descriptions
Failure in time (FIT)	It calculates the failure rate in 10^9 device hours
Failure rate (λ_f)	It is based on measuring failure rate per unit time
Mean Time To Failure (MTTF)	It measures the life distribution for the population of semiconductor devices under operation or expected lifetime on single device. MTTF= $1/\lambda_f$
Total Device Hours (TDH)	It is based on calculating the summation of units in operation multiplied by the time of operation. TDH= no. of units × hrs under stress.
Confidence Level or Limit (CL)	The possibility level of estimated failure rate is driven from sample life test.
Acceleration factor (AF)	It is derived from test data

However, there are some factors that control the reliability [61].

a) **Thermal effects (temperature)**: temperature rises have a dramatic effect on the device lifetime, since the rapid changes in temperature will cause deterioration of the device's *IV* characteristics, and may lead to malfunction. Arrhenius's

general formula established the relation between life (L) and the absolute temperature (T), as follows in equation (2.20).

$$L = exp\left(\frac{E_A}{K_B T}\right) \tag{2.20}$$

where; E_A is the activation energy and K_B is the Boltzmann's constant 8.63×10^{-5} eV/K.

b) **Electric load**: has a great influence on the device's lifetime; the load includes the operation condition, such as electric current, voltage, and electric power dissipated. Therefore, any exceed for electric current can cause increase in the junction temperature and in turn may elevate failure rate.

c) **Mechanical stress:** when excessive force is applied, or the device is strongly vibrated, the device may suffer mechanical damage, and leads to device failure.

d) **Repeated stress:** For example**,** because of the internal heat generation cycle, and low to high temperature cycle induced stresses. These effects increase failure rate.

In this research, the interest was focused towards the thermal repeated stress as will be examined in section 6.3, since the main interest in this thesis is to address the ageing problem caused by thermal causes.

2.6.1 Co-simulation approach in ageing

One of the common difficulties in ageing simulation is the necessity to deal with different time scales, namely [62].

a. time scale of electric solver in microseconds or less

b. thermal solver in seconds

c. Ageing time scale, this ranges from days to months using the acceleration tests.

For instance, in [63] a new tool is designed by hybrid electrical and optical characterization and stress testing in AlGaN/GaN HEMTs. The proposed model identifies three main categories that affect the devices lifetime. i) contact degradation, ii) inverse piezoelectric, and hot electron effects. Similarly, Maneux et al [64] anticipated a 2D model to evaluate degradation on Hetrojunction Bipolar Transistor HBT dc characteristics on a GaAs substrate, using two types of stresses (current-bias or temperature), under three different technological processes: double mesa AlGaAs/GaAs, self-aligned GaInP/GaAs, and fully planner GaInP/GaAs. The results revealed that after 300h and 220℃, HBTs fail owing to thermally activated physical mechanisms, also increased contact resistance of the AuGeNi on n-type GaAs by 25% due to interdiffuaion.

In [65] a scalable ageing model for a MOSFET was proposed using HCI and P/NBTI mechanisms the model integrates HSPICE and HSIM circuit simulators to perform electric stress computation under particular operation conditions and to carry out the stress and the actual device degradation. Using the same means, the RF performance degradation in n/p MOSFET, was investigated by Yi Liu [66] through combining the NBTI, HCI, and the oxide breakdown effects.

The complete description for the whole process containing electric and the thermal solvers with the ageing solver is illustrated in Figure 2.12.

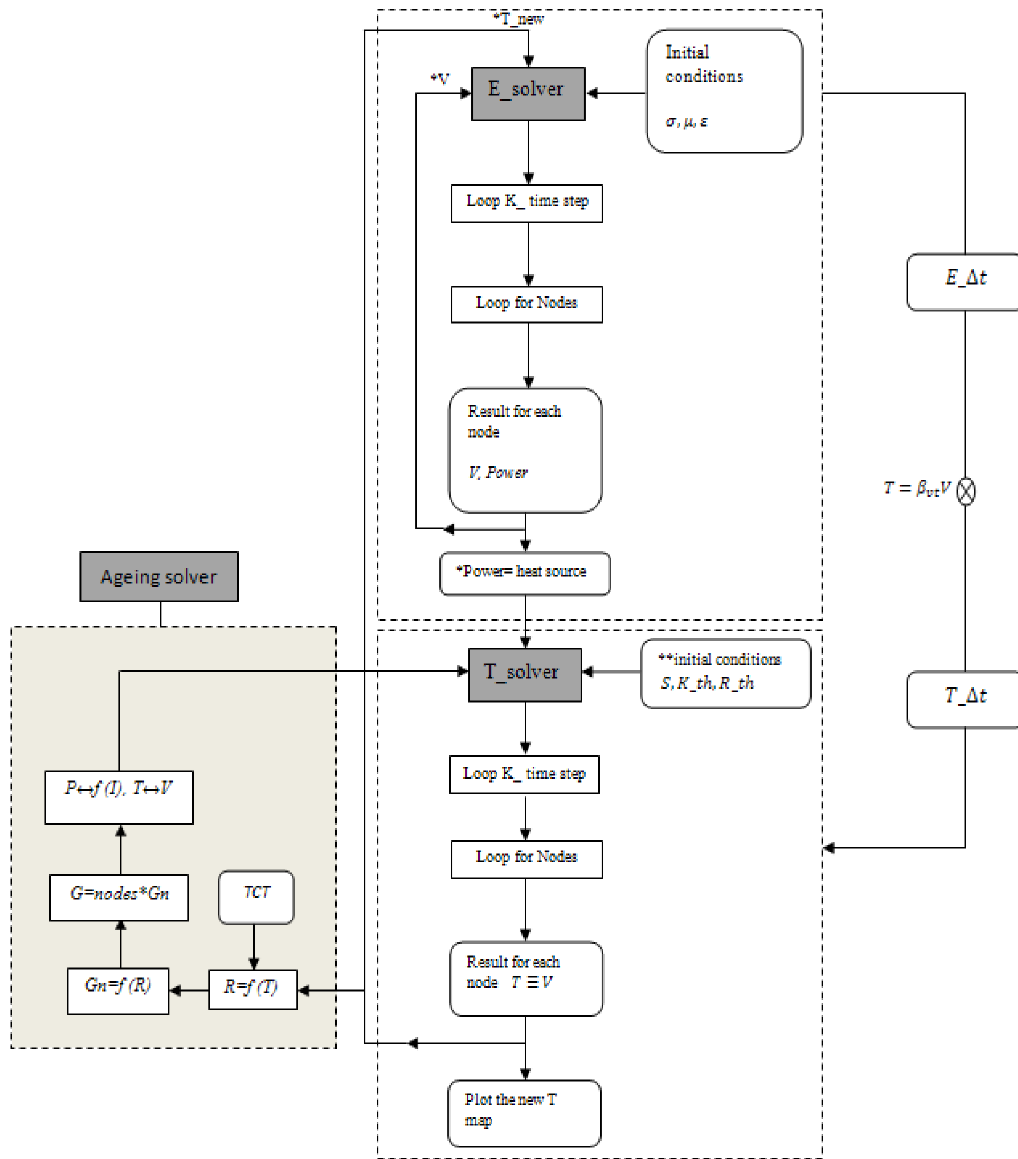


Figure 2.12: The co-simulation process with ageing solver

This early preview in modelling ageing problem from different prospective showed that the importance of device reliability and the ageing effects on device performance i.e. IV characteristic. More details together with TLM results will be discussed in Chapter 6.

2.7. Conclusion

The principle of TLM modelling has been presented, and the main key factors that control the mechanism of calculation such as, scatter matrix, scatter phase, connect phase, and the boundary conditions are highlighted. Dealing with different material properties in TLM is explained by introducing a stub in the model node using capacitance, conductance, and inductance. Furthermore, the thermal diffusion modelling is illustrated in one and two dimensional models providing a comprehensible implementation for modelling a physical problem in terms of electric circuit parameters using TLM technique. Furthermore, the principle of co-simulation in TLM model and the general specification for the device chosen for 2D model is presented. Finally, a literature review in ageing problem and the impact on device performance is briefly described.

Chapter 3 Nonlinear behaviour of semiconductor devices

Summary

In this chapter, the nonlinearity phenomenon in semiconductor devices is described. The negative impact on the performance of semiconductor devices is reviewed briefly in the first section. Section 2 describes the background to dealing with non-linearity using the TLM method. In section 3, charge carrier modelling and its influences on the current flow in semiconductor devices using 1D and 2D TLM model is described, and a new approach is introduced to find a set of equivalence between the device and circuit parameters in a 2D model. Lastly, in section 4 the conclusion from this chapter is summarised.

3.1. Introduction

Diodes and transistors form the basis of semiconductor circuits, non-linear behaviour is an important, and frequently undesirable, property of semiconductor devices and is a limiting factor in optical devices [67, 68]. For instance, nonlinearity in semiconductor devices under large signal conditions may introduce unwanted signal waveform distortions and degrade the quality of the signals, and, of course, introduce

intermodulation [69]. As a result, this will reduce the signal integrity and adversely affect the overall system performance. Nonlinearity may have a positive influence in some applications, such as in the frequency-doublers and in mixers to obtain frequency translation in the output signals. However, in amplifier design under large signal conditions non-linearity will introduce waveform distortion and reduce the overall power added to the efficiency of the amplifier [70].

In this chapter the modelling of non-linear phenomena in semiconductor devices using the TLM method is investigated. This method enables the inclusion of interaction between charge carriers and electromagnetic fields in semiconductor devices. Therefore, Maxwell's equations and semiconductor transport equations need to be combined in the device simulation process.

The occurrence of nonlinear effects in semiconductor devices is due to nonlinear changes of charge distribution under an external electric field and the variations in the carrier mobility [71]. These changes can be attributable to temperature inhomogeneities [72], photogeneration, and space redistribution [73]. Consequently, this manifests as non-linearity in the IV characteristics [74].

Non-linearity can be defined as "a dynamic non proportional relation between the input and the output variables" [73]

The nonlinear equation (3.1) can be used to describe the relation between electrical current flux density, material conductivity, and electrical field applied in semiconductors, equation (3.1) [74] , as illustrated in Figure 3.1.

$$J = \sigma(E)E \tag{3.1}$$

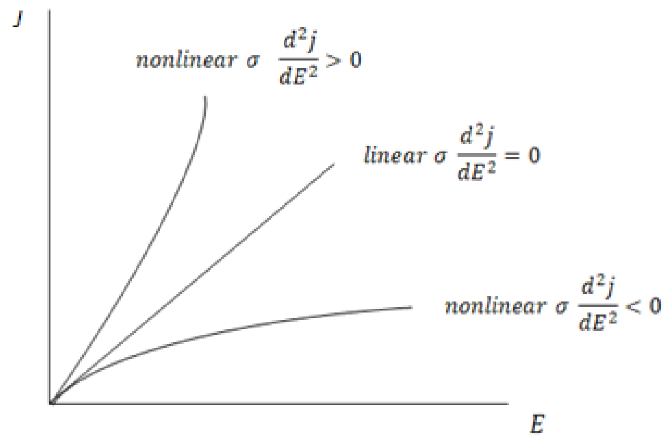


Figure 3.1: Electric field vs. current flux density [74]

3.2. Nonlinearity phenomenon in TLM

Nonlinearity in semiconductor devices has been widely addressed using the TLM method such as modelling non-linear photonic structure and modelling non-linear dispersive 2D media, see [75-78]. For instance, in [75] the approach presented adopts a Z-transform method that deals with different forms of nonlinearity, where the resulting nonlinear field is solved using the Newton-Raphson iteration scheme equation (3.2).

$$x: f(x) = 0 \quad x_{k+1} = x_k - \frac{f(x_k)}{f'(x_k)} \tag{3.2}$$

where: x_k is the initial value, $f(x_k)$ is the function of x, $f'(x_k)$ is the first derivative.

In [79] the application of TLM is used in the analysis of nonlinear phenomenon in optical devices, the proposed model used capacitive stubs and the Newton-Raphson method to solve a 1D problem, for more details see references [80, 81].

3.3. Charge carriers

Knowledge of the movement of charge carriers ($e^+$and e^-) in semiconductor devices under the influence of an external electric field is of considerable technological importance for device operation [82]. The rate of change in the number of electrons and holes across a PN junction will determine the amount of current flow. Consider a simple structure as in Figure 3.2, which shows an infinitesimal slice of semiconductor [83] where the increasing number of electrons in the slice is due to two factors, the net current flow into the slice $J_n(x)$ and, the net carrier generation in the slice G_n [83].

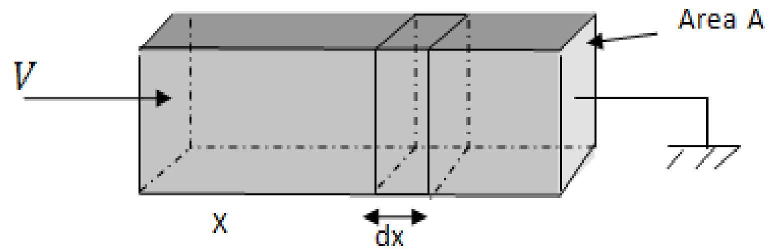


Figure 3.2: An infinitesimal slice of semiconductor

The continuity equation (3.3) [84] can express the relation among carrier drift rate, carrier diffusion, carrier generation rate, and the carrier recombination rate, as follows.

$$\frac{\partial n}{\partial t} = \nabla \cdot J_n + G - R \tag{3.3}$$

where: n is the minority carrier density (*cm*$^{-3}$*sec*$^{-1}$), J_n is electron current density, *G* is the generation rate (*cm*$^{-3}$*sec*$^{-1}$), and *R* is the carrier recombination rate(*cm*$^{-3}$*sec*$^{-1}$). The

continuity equation (3.3) governs the overall rate of change in the holes or the electrons. For one a dimensional model, the relation can be expressed in the following form.

$$\frac{\partial n}{\partial t} = \left[\frac{J_n(x)A}{-q} - \frac{J_n(x+dx)A}{-q}\right] + (G_n - R_n)Adx \tag{3.4}$$

And for a two dimensional model in an equilibrium state [85].

$$\frac{\partial^2(n_p - n_{p0})}{\partial x^2} + \frac{\partial^2(n_p - n_{p0})}{\partial y^2} - \frac{n_p - n_{p0}}{D\tau} = 0 \tag{3.5}$$

where: n_{p0} is the thermal-equilibrium minority carrier density, τ is the life time, and D is the diffusion constant.

To get good representation of the problem, the solution of the electromagnetic field is required, where the TLM method offers efficient solutions at this stage. The interaction between the charge carriers and the electromagnetic fields can be simulated by the isomorphism of Maxwell's equations and the charge diffusion equations. Maxwell's equations are given by.

$$\frac{\partial E_z}{\partial y} = -\mu\frac{\partial H_x}{\partial t} \tag{3.6}$$

$$-\frac{\partial E_z}{\partial y} = -\ \mu\frac{\partial H_y}{\partial t} \tag{3.7}$$

$$\frac{\partial \mathrm{H_y}}{\partial \mathrm{x}} - \frac{\partial \mathrm{H_x}}{\partial \mathrm{y}} = \varepsilon\frac{\partial \mathrm{E_z}}{\partial \mathrm{t}} \tag{3.8}$$

$$\frac{\partial^2 E_z}{\partial x^2} + \frac{\partial^2 E_z}{\partial y^2} = \mu\varepsilon\frac{\partial^2 E_z}{\partial t^2} \tag{3.9}$$

With an external electrical field applied, the continuity equation for minority carriers (electrons in n-type semiconductor) becomes.

$$\left(\frac{\partial^2(n)}{\partial x^2} + \frac{\partial^2(n)}{\partial y^2}\right) - \frac{\mu}{D}\boldsymbol{E}.\left(\frac{\partial n}{\partial x} + \frac{\partial n}{\partial y}\right) - \frac{n}{D\tau} = \frac{1}{D}\frac{\partial(n)}{\partial t} \tag{3.10}$$

$$\nabla^2 n - \frac{\mu}{D}\left(\boldsymbol{E}\cdot\left(\frac{\partial n}{\partial x}i + \frac{\partial n}{\partial y}j\right)\right) - \frac{n}{D\tau} = \frac{1}{D}\frac{\partial n}{\partial t} \tag{3.11}$$

$$\nabla^2 n - \frac{\mu}{D}(\boldsymbol{E}\cdot\nabla n) - \frac{n}{D\tau} = \frac{1}{D}\frac{\partial n}{\partial t} \tag{3.12}$$

Equation (3.12) can be used as the transport equation in the 2D TLM model.

To compare the equivalences with the TLM parameters by considering the electric circuit in 2D with additional leakage resistance to model the recombination term and an additional current source to model the drift term. A Similar approach has been achieved in [82] for one dimensional TLM diffusion problems for an infinite and homogenous n-type semiconductor.

The equivalences between the transport equation for 1D minority carriers equation (3.13) and the transmission line circuit for TLM diffusion node equation (3.14) showed that the model parameters R_L, Z_0, R can be used as an equivalences for their counterpart parameters in semiconductor device, as in equation (3.15) [24].

$$\frac{\partial^2 P}{\partial x^2} - \frac{\mu\, E_x}{D}\frac{\partial P}{\partial x} - \frac{P}{D\tau} = \frac{1}{D}\frac{\partial P}{\partial t} \tag{3.13}$$

$$\frac{\partial^2 V}{\partial x^2} + R_d\, g_m \frac{\partial V_x}{\partial x} + G_d R_d V_x = R_d C_d \frac{\partial V_x}{\partial t} \tag{3.14}$$

$$P \leftrightarrow V_x\,, D \leftrightarrow \frac{1}{RC}\,, \tau \leftrightarrow \frac{C_d}{G_d}, -\mu E_x \leftrightarrow \frac{g_m}{C_d}\,,\ \frac{\partial P}{\partial x} \leftrightarrow -I_x R_d \tag{3.15}$$

To derive a new set of equivalences, a two dimensional shunt TLM model is used. The node illustrated in Figure 3.3, and the Thevenin equivalent circuit is described in Figure 3.4, where the characteristic impedance (*Z*) has been normalized to 1 (for both

simplicity of calculation and convention), then the voltage across the node can be found from the following form [9]:

$$\left(\frac{\partial^2 V}{\partial x^2}+\frac{\partial^2 V}{\partial y^2}\right)-4RC\left(\frac{\partial V}{\partial t}\right)+2\frac{RI_m}{\Delta l}=2CL\frac{\partial^2 V}{\partial t^2} \quad (3.16)$$

$$\left(\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 v}{\partial y^2}\right)-2CL\frac{\partial^2 V}{\partial t^2}+2\frac{RI_m}{\Delta l}-GR=4RC\left(\frac{\partial V}{\partial t}\right) \quad (3.17)$$

Where: I_m is the current generator and GR represents the recombination term.

$$\nabla^2\vec{\boldsymbol{V}}-2CL\left(\frac{\partial^2 u}{\partial t^2}+\frac{\partial^2 v}{\partial t^2}\right)+2\frac{RI_m}{\Delta l}-GR(u+v)=4RC\left(\frac{\partial V}{\partial t}\right) \quad (3.18)$$

Comparing equation (3.18) with equation (3.12) yields the following new set of equivalences for 2D model:

$$n\leftrightarrow V, D\leftrightarrow\frac{1}{4RC}, \tau\leftrightarrow\frac{C}{G}, \ \nabla n\leftrightarrow -4R\boldsymbol{I} \quad \frac{g_m}{2C}\leftrightarrow -\boldsymbol{E}\mu \quad (3.19)$$

Further details about the implementation of 2D model on MESFET and MOSFET devices will be presented in Chapters 4 and 5.

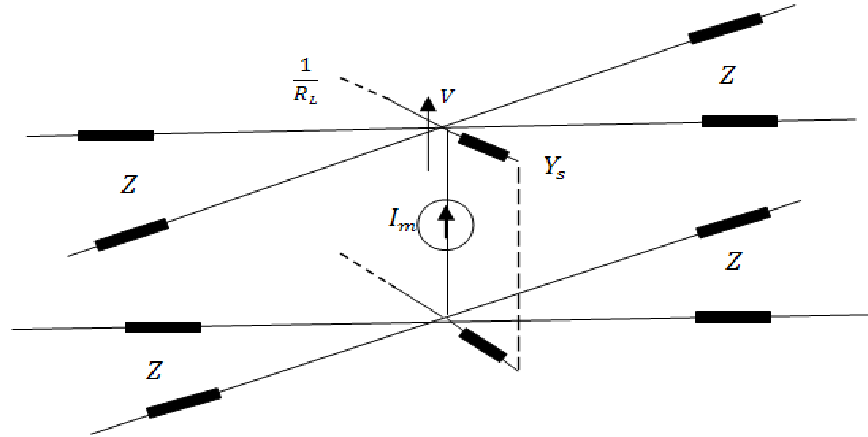


Figure 3.3: 2D shunt TLM model with current source and leakage resistance

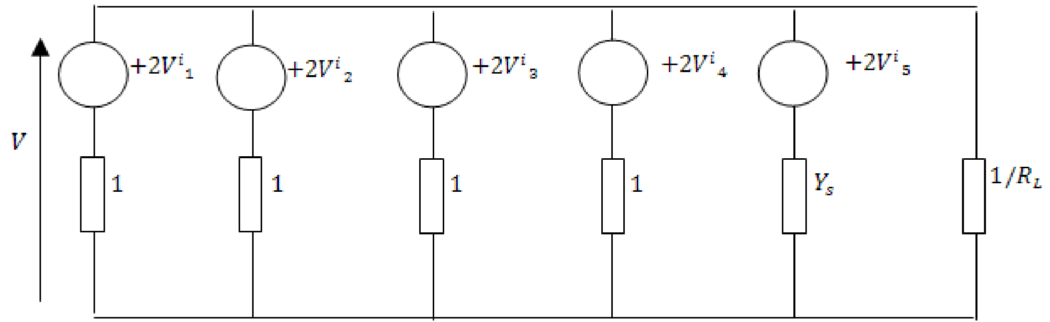


Figure 3.4: Thevenin equivalent for circuit at Figure 3.2

The charge carriers are modelled in a 1D TLM solver, to investigate the behaviour under an excitation source, and to show the possibility of combining the circuit parameters and the semiconductor transport parameters. This is done by taking an n-type silicon sample, as in [24] (Length $0.1\mu m$), with a node size 0.01 μm, $\Delta t = 0.5 \times 10^{-8}\ sec$, and diffusion constant=50 $cm^2V^{1}s^{-1}$ with excitation input of 10 V cm^{-1} at node 2. The model was run for 100 time steps to ensure stability and the uniform distribution of charge carriers. The results for the minority carrier concentration against the distance with different time steps ($0.5\mu s, 1.0\mu s\ , and\ 1.5\mu s$) are shown in Figure 3.5. A good agreement is obtained, when these results are compared with those from [82], as can be seen from Figure 3.6.

To verify the reflection coefficient effects on the charge diffusion process, two types of boundary conditions are used as shown in Figure 3.7, for absorbing boundaries with a reflection coefficient value=0, as illustrated in (a), and with an insulating boundary,

with reflection coefficient value =-1, as in (b). The results show noticeable increase in carrier concentration with isolated walls.

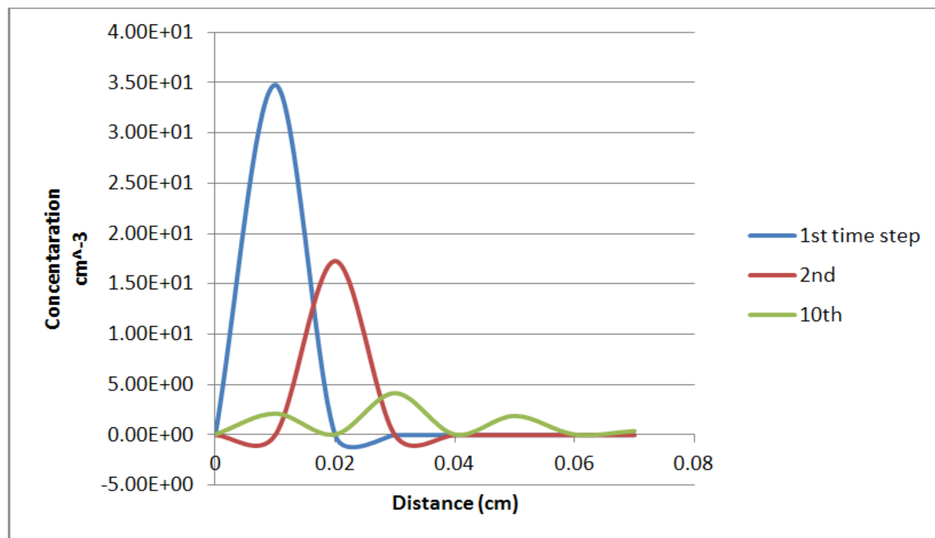


Figure 3.5: 1D TLM results for minority carriers' diffusion in three time steps

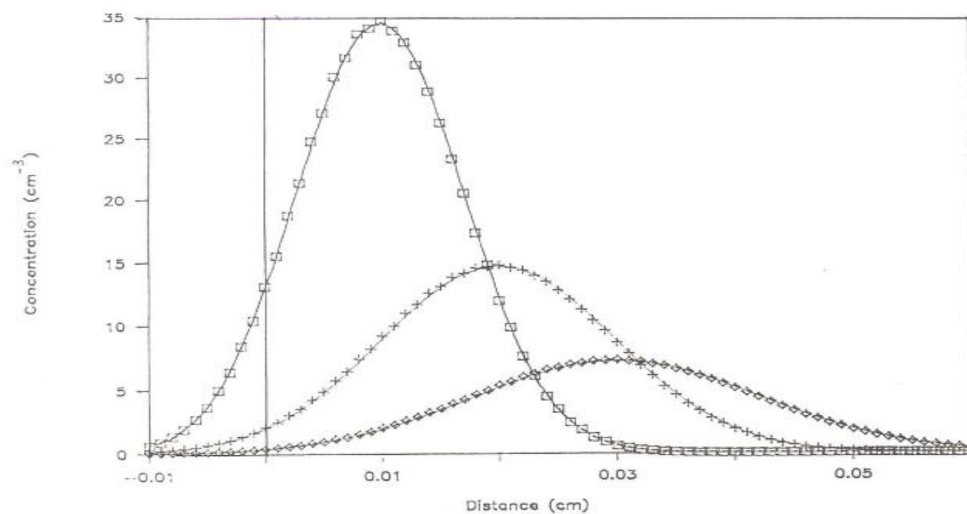
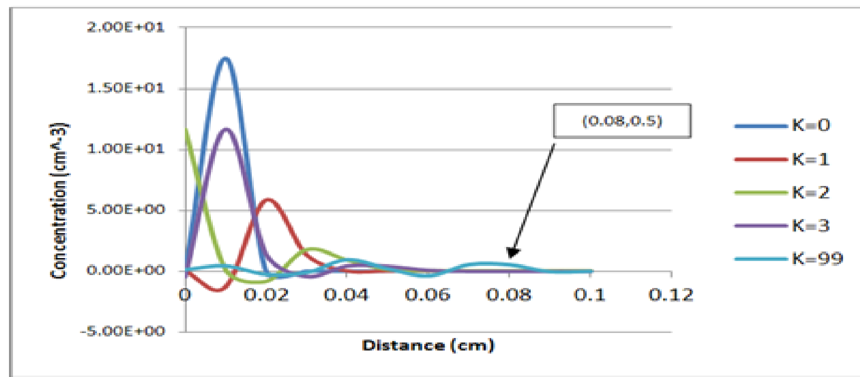
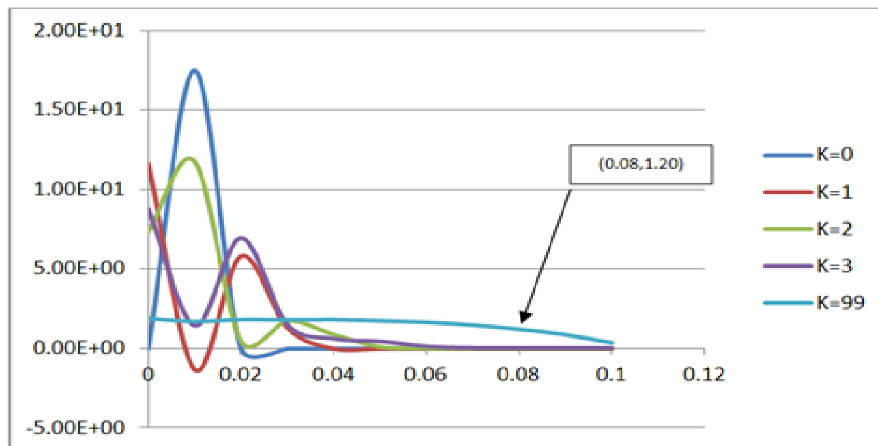


Figure 3.6:Alzeban et al [82] results, concentration vs. distance in different time steps



(a)



(b)

Figure 3.7: a-Carriers diffusion with two different reflection coefficients values (0, 1), and b- with (1, -1)

3.4. Conclusion

Nonlinearity in semiconductor devices has been discussed, including review of the common disadvantages and the minor advantages. Clearly, an understanding of semiconductor device nonlinearities is important in understanding inter alia communication channel limitations and electromagnetic compatibility effects. Modelling this phenomenon using the TLM method was derived from a 2D model. The charge diffusions are modelled in a 1D unified solver, to assess the capability of

modelling the semiconductor transport equation and circuit parameters in one solver, the results showed good agreement with published work [24].

Chapter 4 Nanowires and nanotubes: future semiconductor devices

Summary

In this chapter, as an appropriate application for one-dimensional model, nanowires have been used for the first time in TLM method. The heat diffusion in Silicon nanowires has been described. The thermal radiation effects are included by adding an additional conductance to the TLM node structure to represent the emissivity of the circuit. In section one; a brief description is given for nanowires and their applications. In section two, the heat radiation aspect in nanowires is described, and the new modification on TLM node is shown. In section three, the co-simulation approach of electric and thermal modelling in Silicon nanowires is proposed. Section four contains the conclusions from this chapter.

4.1. Introduction

In this chapter, the TLM model will be implemented in the nanotechnology zone, to address the problem of heat dissipation. Focusing the research at this stage on nanowires, or semiconductor nanowires such as silicon nanowire field effect transistors

(SiNW FET), will provide an important tool for these promising devices to solve the internal heating problems, and hence, the degradation caused by thermal factors in emerging semiconductor devices.

Nanowires and nanotubes are developing into important engineering materials. Size reduction, speed increase, and improved storage in nanoscale electronics due to the application of nanotubes and nanowires opens up opportunities for a wide range of applications, such as: solar cells, increased miniaturization of electronic circuits, quantum devices, spectroscopic sensing, memory devices, biological sensors, communications systems, and alternative energy [86, 87]. The following section shows that thermal nanowire behavior is sufficiently different to the bulk material performance to warrant separate studies.

A Nanowire is a structure that has limited diameter around a tenth of a nanometre (10^{-9}meters) or less and an unconstrained length (usually much greater than the diameter), Figure 4.1 illustrates examples of silicon nanowires with different diameters [88]. Generally the synthesis of nanowires can be classified into four categories [89]:

- Template-based synthesis: electrophoretic deposition, conversion with chemical reaction, and electrochemical deposition.
- Spontaneous growth: dissolution condensation, Vapour-Liquid-Solid growth (VLS), and evaporation condensation.
- Electro-spinning
- Lithography

In 1991 the first experimental evidence of Carbon Nanotubes (CNTs) has been presented by Iijima [90] in the form of multi wall nanotubes [91]- see Figure 4.2. The nanotubes have cylindrical nanostructure, where the length-to-diameter ratio is similar to those in nanowires. The synthesis of nanotubes can be broadly divided into two categories depending on the process used to extract atomic carbon.

- Chemical method: Used catalytic decomposition
- Physical method : Used high energy sources, such as plasma, or laser

The properties of carbon nanotubes can vary greatly depending on how they are rolled up, a property called chirality. Silicon nanotubes have many similarities with a carbon nanotube including a band gap at half-filling and conducting behavior which is dependent on structure.

Nanotubes in the forms, single and multi walled are used in a wide range of application for instance chemical sensors, energy storage, conducting paints, and composite materials (heat exchanger, reinforced material).

Thermal ageing and devices reliability problems in nanotubes have been addressed recently [92, 93]. For example, in [93] the thermal ageing problem in carbon nanotubes has been investigated, when the model was subjected to thermal treatment, the results showed that the presence of Multi-walled Carbon Nanotubes (MWCNT) had a major effect on electric conductivity stability and on thermal ageing. These research indicated the importance of the ageing in the future semiconductor devices, and emphasizes the importance of preparing a design tool, which confirming the right direction of this study.

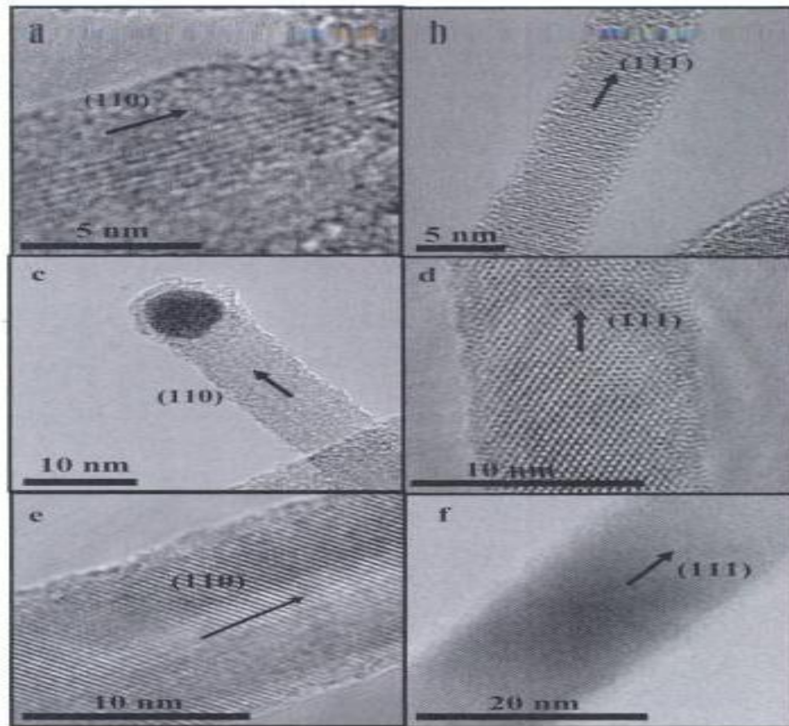


Figure 4.1: Si nanowires with different diameters, the growth direction is marked with arrows [88]

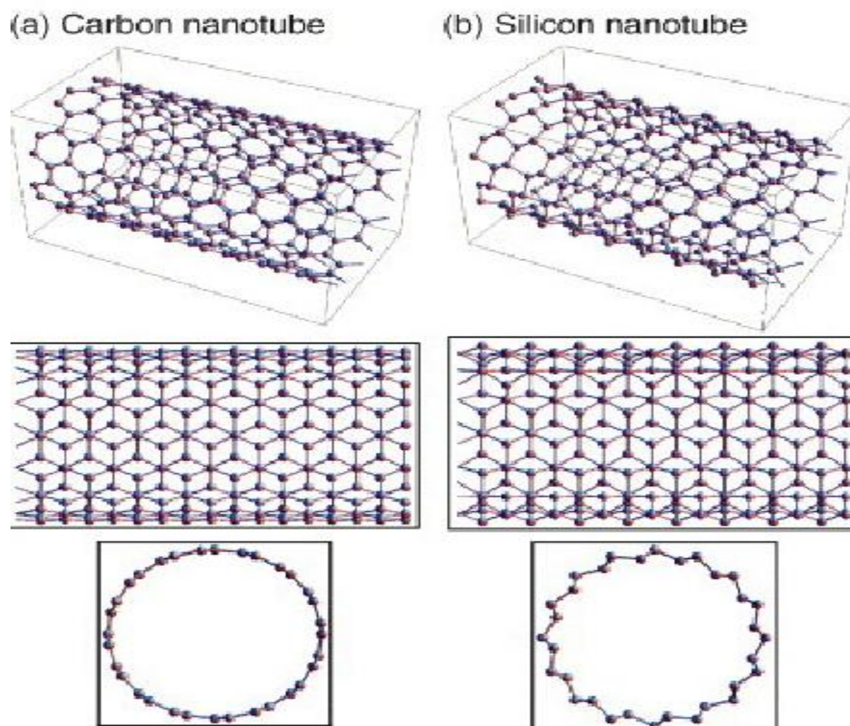


Figure 4.2: a-carbon nanotube, b-silicon nanotube [94]

Because of enhanced phonon surface scattering and quantum confinement effects, nanowires have lower thermal conductivity than their bulk counterparts. This exclusive property opens up a large range of applications such as thermal barrier coatings and thermoelectric energy converters.

Generally, thermal properties of nanowires can be investigated in three ways: measurement, analytical studies, and/or numerical simulation. In terms of measurements, because of the difficulties in heat flow control at microscopic scale and temperature measurements the experimental methods are still difficult to undertake reliably [95]. Numerical methods are providing a useful contribution to evaluating nanowire performance. Recently the Finite Element Method (FE) has been used in [96] to simulate plasmonic nanostructures. The proposed numerical algorithm is based on hybridizing the Surface-Integral Equation (SIE) method and the Finite-Difference-Time-Domain (FDTD) method to present an efficient, accurate, and fast electromagnetic method.

In this thesis, the Transmission Line Matrix (TLM) based approach uses the electromagnetic wave equation and the thermal diffusion equation in nanostructure SiNWs, to find a set of equivalences to model temperature rise and radiation. In [97] the thermoelectric performance was studied in silicon nanowires using (FE) simulation. Through accounting for the cooling temperature, coefficient of performance, and cooling power density, the results in [97] showed that SiNWs have a great potential in hot spot removing in ICs.

Analytical approaches have been adopted to calculate thermal conductivity as a function of temperature, alloy concentration, and nanowire diameter, for SiGe alloy nanowires

[98]. Here, the differences in thermal conductivity values of non-alloy and alloy structures were reported as another factor in evaluating thermal properties in nanostructures.

Undoubtedly, simulation methods are an important approach in raising the level of understanding of nanowire thermal behaviour. For example, in [99] the Boltzmann Transport Equation (BTE) was used to obtain the thermal profile for silicon nanowires in transient and steady state regimes. By simulating interactions and phonon movement through a Monte Carlo model which is a simulation method that relays on repeated random sampling to obtain numerical results, thermal conductivity has been studied [100] and the results provide a good description of the phonon heat transport interaction with boundaries in nanostructures. The Molecular dynamics (MD) simulation technique of physical movement of molecules and atoms, was employed by [101] to calculate the thermal properties of (Au_3Ni) nanowires, where the effects of diameter size on the melting temperature and the energy, were observed.

Clearly, developments in simulation methods help in understanding, predicting and analyzing the thermal behaviour of nanowires and can present important advantages to the designers of downscaled electronic devices, data storage, and sensing applications [102-104].

Understanding the thermal behaviour of nanowires is an important part of designing and analyzing systems in which they are used. Measurements are challenging, representing the behaviour as a system of equations is equally challenging and full wave simulation can be costly in terms of time and computational resource. The aim of this model is to develop a first order approximate method based on a 1-dimensional Transmission Line

Matrix (TLM) method that accounts for the main behavioural attributes of nanowires, including thermal radiation effects. As will be discussed, radiation effects are generally ignored in analysis. The current TLM model demonstrates how this property can be introduced into simple 1D TLM model. It does confirm that the radiation effects are only of the order of a few percentage points of power dissipation but this, in itself, can be used as a basis for investigating system temperature rises and the potential for thermal runaway conditions under situations where large numbers of nanowires, all radiating small power levels, exist in a confined space with minimal or no convection cooling.

4.2. Heat radiation in Nanowires

One of the important aspects in the heat transfer process in electronic devices is thermal radiation. Conceptually, this type of heat transfer does not need a propagation medium as with convection and conduction. By means of electromagnetic wave (photon) emission, the energy can be transferred across the system boundary due to difference in temperature. This property allows its inclusion in a 1D framework, allowing nanowires to be treated as pseudo-1D structures. One approach to including radiation effects would be to use 2D or 3D modelling [105]. Incorporation of emissivity in a 1D node overcomes the resulting problem of excessive computational resource required in 2D or 3D solutions. Mostly, thermal radiation occurs in wavelengths of 10^{-1}-10^{2} μm, meaning that the wavelength of radiation is generally greater than the dimensions of the structures being considered. The upshot of this is that, even when only a handful of

nodes are used per nanowire, each node will be short compared with the wavelength of radiation, which lends itself to the distributed approach adopted in this work.

In this chapter, thermal radiation effects are approached with an additional conductance to the transmission line structure to represent the emissivity of the circuit as shown in Figure 4.3. The emissivity is one of the important factors in heat radiation, it is a ratio of the radiation of a given material to that of a "black body" under the same conditions, as illustrated in equation (4.1).

$$\varepsilon_m = \frac{E}{E_b} \tag{4.1}$$

where, E is the emissive energy from the surface of a body, and E_b is the emissive energy of an equivalent black body.

The existence of the parallel conductance in the model leads to a clear expression of emissivity in a TLM node. The equivalent circuit in Figure 4.4 shows the additional current source *I*, and shunt conductance G_{rad}. The capacitance and the inductance may be replaced by the characteristic impedance of the line *Z,* while the voltage at the node will be the sum of two incident voltages approaching from the right side of the node $2V^i{}_R$, and $2V^i{}_L$ from the left. From the equivalent Thevenin model, the voltage source is equal to the open circuit voltage, and this will add to the incoming propagating pulse. Thevenin equivalents can be used to describe these parameters as shown in Figure 4.4. To ease the calculation, the resistor is assumed to be divided across the node as shown in Figure 4.5. Afterward, the voltage across the node can be obtained using Millman's theorem [44]. Accordingly, the lumped current source and the conductance will model the heat dissipation and thermal radiation respectively.

The electric analogy with radiation can be expressed in terms of the conductance, surface resistance, and the emissivity as follows [106].

$$G_{rad} = \frac{1}{R^{rad}}, \; R^{rad} \leftrightarrow \frac{1-\varepsilon_m}{\varepsilon_m A} \tag{4.2}$$

where; G_{rad} conductance in radiation, R^{rad} is the surface resistance, and A is the surface area. The analogy between the conductance and the material emissivity enables the modelling of the thermal radiation dissipation in each node along the wire leading to a reduction in the calculated temperature. Equations (4.5-4.9) provide the entire description for the TLM solver, taking into account all the issues discussed above.

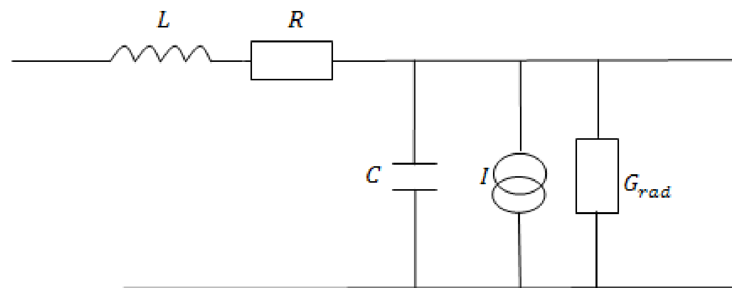


Figure 4.3: Lumped circuit to model thermal diffusion with radiation effects

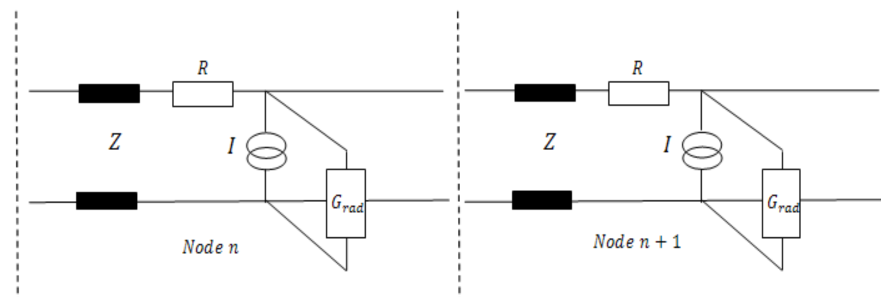


Figure 4.4: TLM shunt node with current source and resistor in parallel

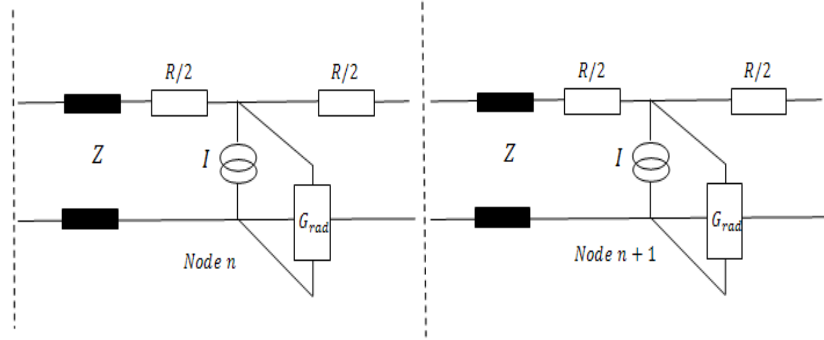


Figure 4.5: TLM node with divided resistor

The voltages across the node can be found using the parallel generator theorem [44] as follows:-

$$V_n = \frac{\frac{2Vi_L}{Z+\frac{R}{2}} + \frac{2Vi_R}{Z+\frac{R}{2}} + \frac{V^{rad}}{R^{rad}}}{\frac{1}{\frac{R}{2}+Z} + \frac{1}{\frac{R}{2}+Z} + \frac{1}{R^{rad}}} \tag{4.3}$$

where: V^{rad} is the voltage across the stub. While the current flow to the left and right hand sides are as follows.

$$I_L = \frac{(V_n - 2Vi_L)}{Z+\frac{R}{2}} \tag{4.4}$$

$$I_R = \frac{(V_n - 2Vi_R)}{Z+\frac{R}{2}} \tag{4.5}$$

Then the voltage to left and the right of the node can be found from.

$$V_L = 2Vi_L + I_L Z \tag{4.6}$$

$$V_R = 2Vi_R + I_R Z \tag{4.7}$$

After completing the scatter phase, the reflected voltages can be calculated to represent the incident voltages for the next time step.

$$V_L{}^r = V_L - Vi_L \tag{4.8}$$

$$V_R{}^r = V_L - Vi_R \tag{4.9}$$

These equations can be implemented to update for every small increment of time.

4.2.1 Results

Figure 4.6 shows the temperature profile for electron-etching-grown (EE) SiNW of size 50nm diameter × 2.5 μm length, thermal conductivity 1.6 *W/m K* with applied electric current of 3.5 μA, the material properties and nanowire size were obtained from references [97] and [107]. The contact with the hot side of 300K is at node 1 and the simulation was run for 150 time steps. The 3D plot explains the distribution of temperature (Y-axis), along the nanowire nodes (X-axis), as a function of time (Z-axis), the gradual increasing of nodal temperature starts to become obvious after 60 timesteps until it reaches to uniform distributions at the end of the 140th timestep. In Figure 4.7, the longitudinal temperature distribution for EE-SiNW 50 nm in contact with the hot side fixed at 300K, and applied current 3.5 μA, is shown against time, where the progression of heat diffusion process is observed at (a) 50 time steps, and (b) 100 time steps.

Similarly, when the applied current was increased to 9 μA as in Figure 4.8, the average temperature along the nanowire after 150 time steps was 286 *K*, i.e. it had increased by nearly 3 degrees *K* from the previous test, due to the increasing current that raises the

Joule heating. The thermal behaviour of the silicon nanowire when changing the thermal conductivity to 7 *W/m K*, shows limited changes on the total average temperature along the nanowire after the same period.

To validate the TLM results, and thereby the suitability of this method as a general approach for calculation of heat radiation in one-dimensional nanostructure, a comparison was made with the results from [97], that employed COMSOL MULTIPHYSICS [108] and FE simulation. The first comparison is illustrated in Figure 4.9, with a temperature profile of 50nm EE-SiNW and a 3.5μA applied current. The outcomes from the FE presents the longitudinal temperature distribution when one of the nanowire sides contact the hot source with a fixed temperature of 300K and the other end is in contact with a cold silicon island.

Results from the TLM solver agreed with the reference results (ignoring the heat radiation effects). Introducing the radiation effects demonstrated comparable results with the lower temperature, reported by Zhang, G., et al [97] for each node. This is due to using each node as a single emitting object in TLM model. Nevertheless, the amount of temperature difference between the two approaches was restricted to the range (0.1-4) Kelvin.

A second example used a 50nm vapor-liquid-solid-grown (VLS) SiNW with similar applied current and higher thermal conductivity of 20 *W/m K*, the effect of the thermal conductivity has a visible impact on the temperature range.

The results are in reasonable agreement with the reference temperature distribution, as shown in Figure 4.10, with relatively small differences between the TLM and FE

methods (0.3-2.1 *K*). Note also that the TLM results do not account for the silicon island in this example, which may contribute to some of the differences.

To assess the model, and to confirm our assumption about the effects of cross sectional area, a smaller node length was used ($0.001\mu m$), as shown in Figure 4.11. The results obtained showed better agreement. Similarly, in Figure 4.12, when the radiation effect is considered, the results show matching behaviour with FE results despite a nodal temperature decline along the nanowire. The comparison of the TLM and the FE results can be seen in Figure 4.9 to Figure 4.12. The percentage of error in TLM results for VLS-SiNW with applied current 3.5 μA with and without radiation effects when compared with FE results, are shown in Figure 4.13 and Figure 4.14 respectively, where the results shows that the error percentage for the both cases not exceed 1.4%.

There is a general agreement between the two approaches; any differences may be explained at least in part by the end-loading of the FE model due to the silicon island. Introducing the radiation in the heat diffusion calculation produced results with lower temperature along the nanowire. The overall differences in nodal temperature showed that the heat radiation has limited effects, within the range (0.1 – 9) degree Kelvin. The fact that a temperature difference of 1% -1.5% can be attributed to radiation can correctly be considered as a minor loss when the operation conditions are severe (i.e. high temperature). This conclusion agrees with the assumptions made (often without supporting evidence) in previous publications [95, 97, 109] about the possibility of neglecting the heat radiation in some applications of nanowires.

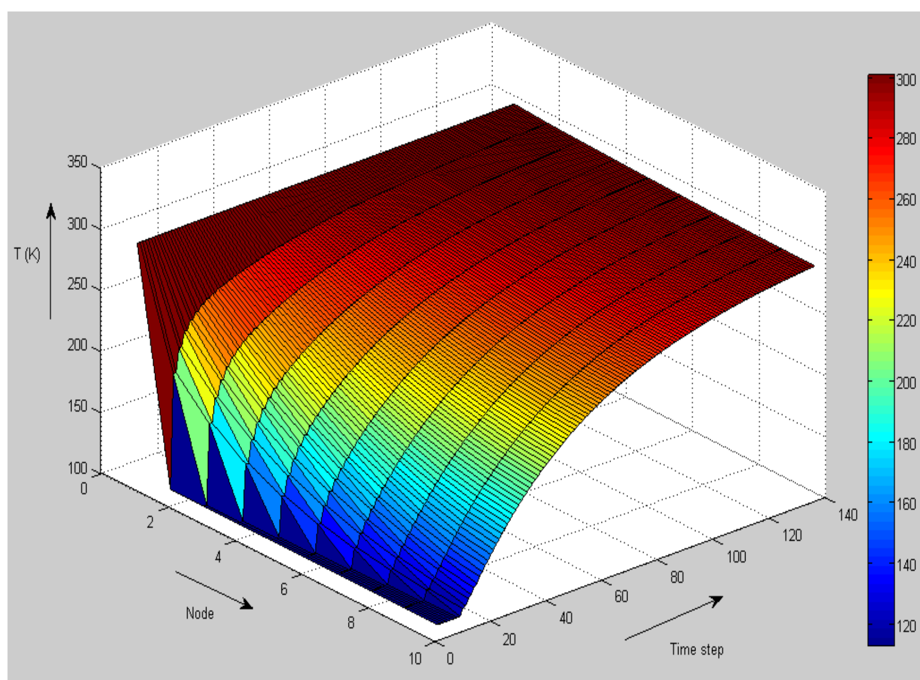
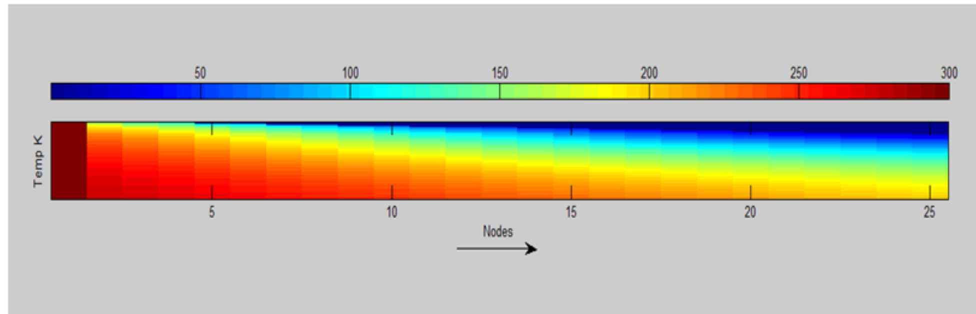
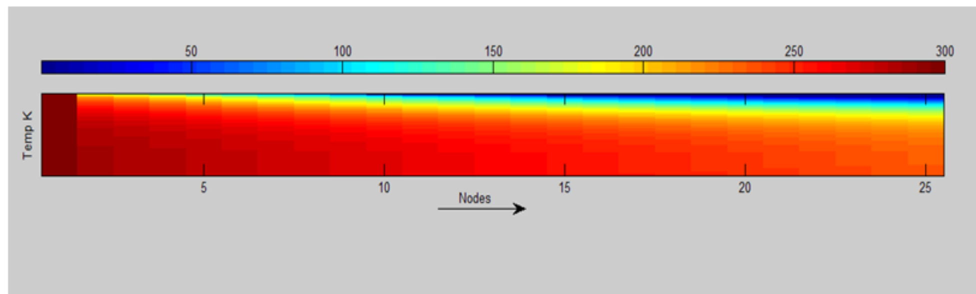


Figure 4.6: Temperature distribution with radiation effects for EE-SiNW 50nm in contact with hot side fixed at 300K, and applied current 3.5 μA



(a)



(b)

Figure 4.7: Longitudinal temperature distributions for EE-SiNW 50nm in contact with hot side fixed at 300K, and applied current 3.5 μA (a) after 50 time step, (b) after 100 time step

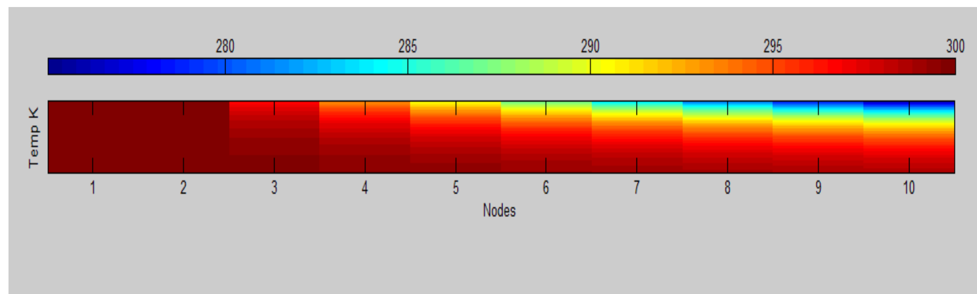


Figure 4.8: Longitudinal temperature distributions for EE-SiNW 50nm in contact with hot side fixed at 300K, and applied current 9.0 μA

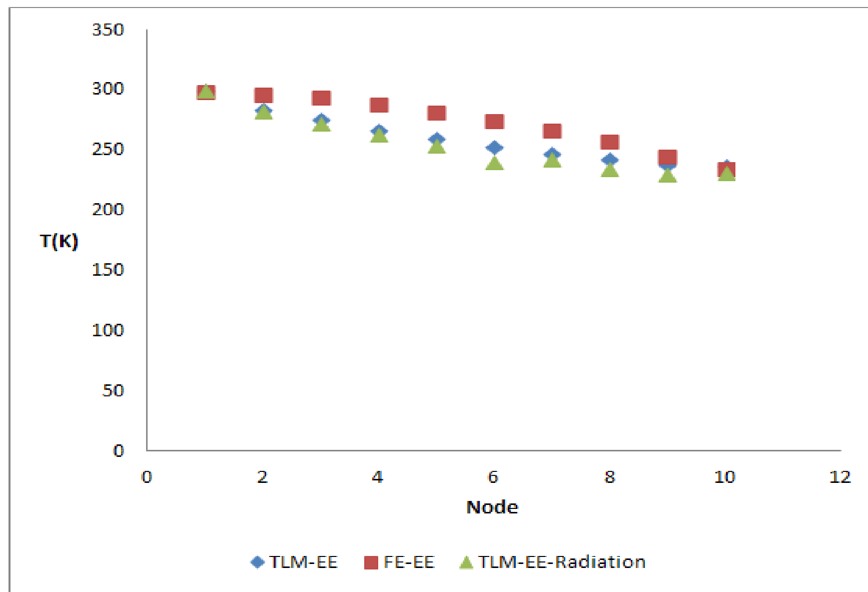


Figure 4.9: TLM results for 50nm EE-SiNW compared with FE results [97] with applied current 3.5 μA

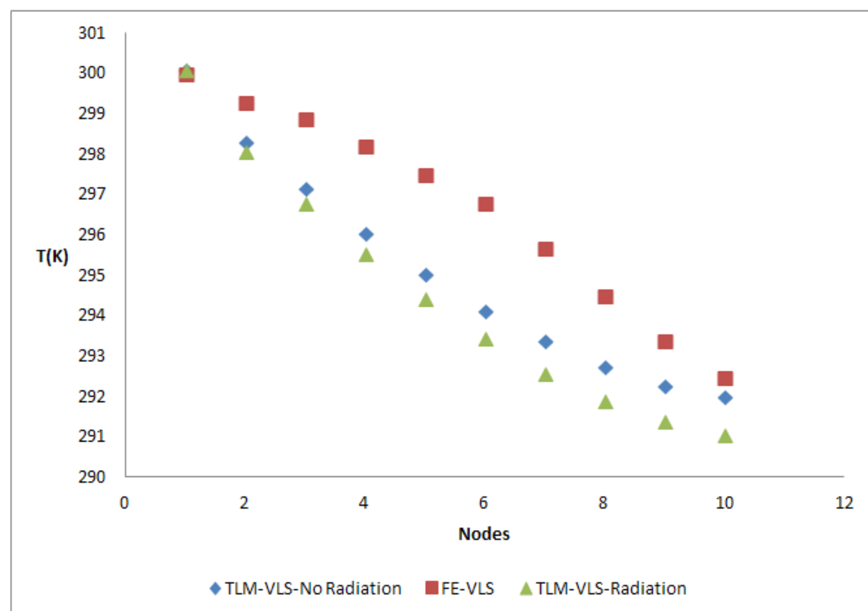


Figure 4.10: TLM results with FE simulation results, for VLS-SiNW with applied current 3.5 μA with and without radiation effects

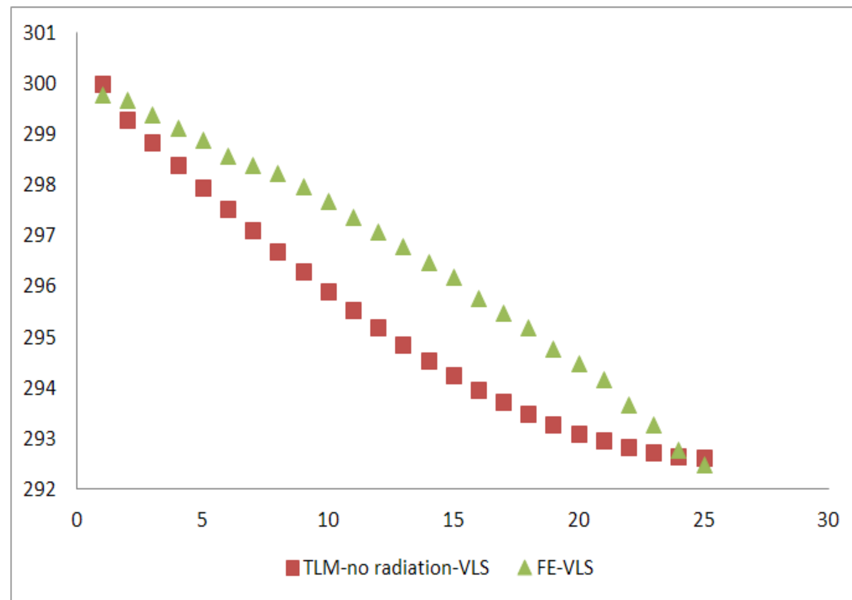


Figure 4.11: simulation results for VLS-SiNW with applied current 3.5 μA, and node length (0.001μm) without radiation effects (x-axis nodes, y-axis temperature)

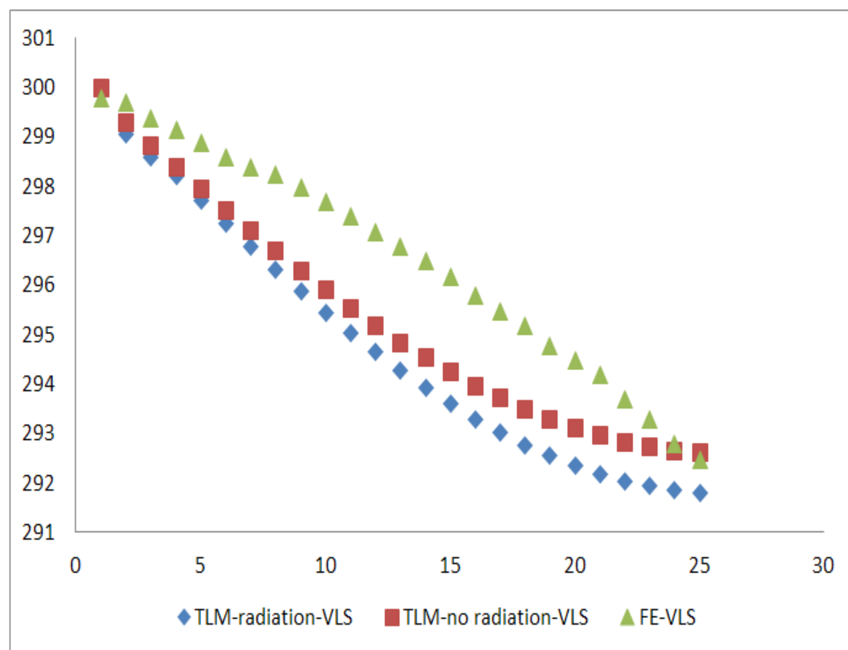


Figure 4.12: simulation results for VLS-SiNW with applied current 3.5 μA with radiation effects (x-axis nodes, y-axis temperature)

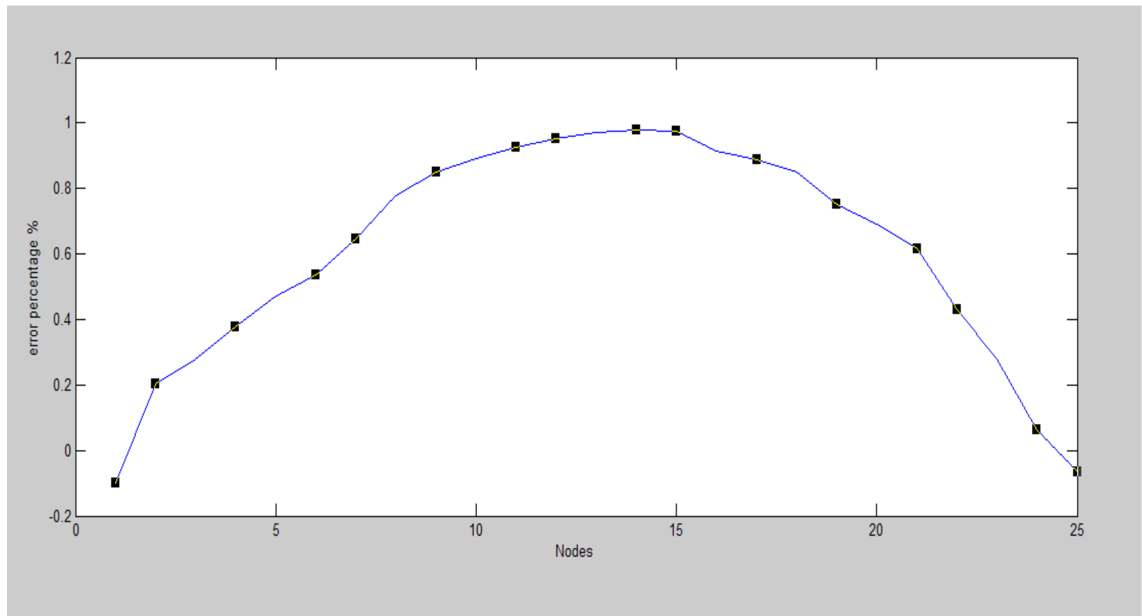


Figure 4.13: error percentage for TLM results compared with FE simulation results, for VLS-SiNW (without radiation)

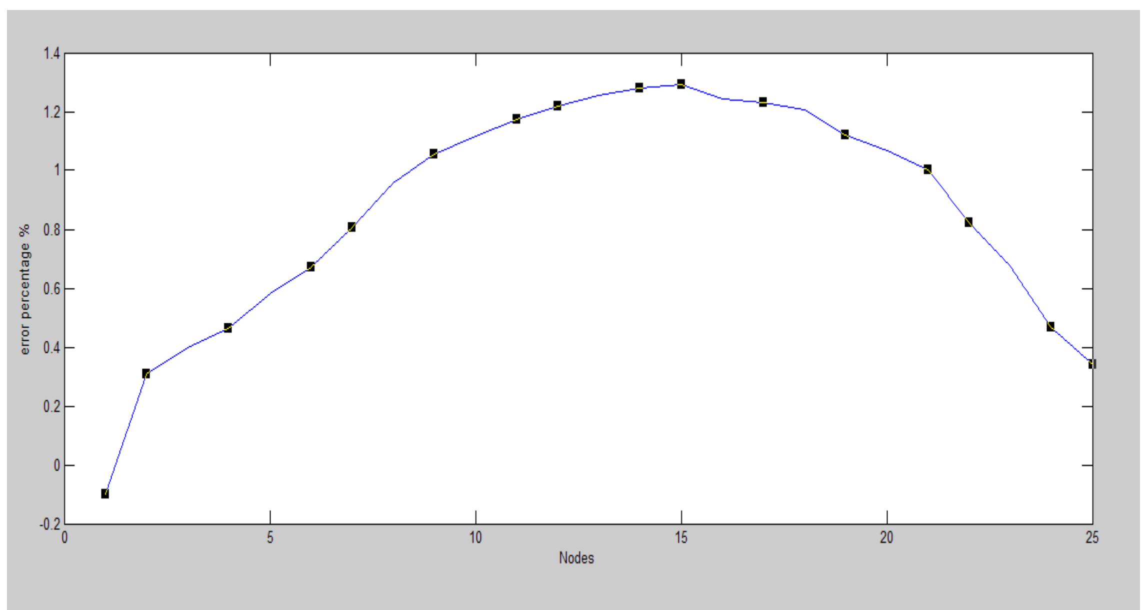


Figure 4.14: error percentage for TLM results compared with FE simulation results, for VLS-SiNW (with radiation)

4.3. Co-simulation approach in nanowires

The electric and thermal performance of nanowires is of great importance for designing and fabricating nanowires. However, there is a limitation to the further enhancement of nanowires due to the power dissipation problem. For instance, [110] examines the effects of surface passivation and source-drain contact annealing on key transistor properties. The results show that the silicon nanowire Field Effect Transistor (SiNW FET) performance can be improved by increasing the average transconductance and the average mobility. Enhancing the power output and the efficiency of a roughened silicon nanowire array was undertaken in [111] through integrated heat collection, where the transport properties of nanowire arrays is obtained by modelling the heat and the charge transport in individual silicon nanowire. The performance evaluation in [112] focused on the intrinsic properties of nanowires, the article provides an optimization for structure parameters, i.e., the configuration of the NW array and the spacer layer thickness in a vertical III-V NW transistor architecture. The thermoelectric performance of silicon nanowires has been investigated in [97] using finite element (FE simulation), and analytical modeling; the results show that the SiNW has a good potential in future integrated circuit applications.

In this section, an enhanced 1D TLM model is presented to investigate the interlocking influences of the electric propagation caused by a voltage source on the thermal diffusion process. One of the main obstacles that should be taken into consideration in combining the two models is the propagation speed, as the time for a signal to propagate through the model is in the range of femtoseconds in the electric model, but microseconds in the heat model. Due to this difference, it was necessary to find

homogeneity between the two processes and maintaining a common language between the two solvers. A sequencing mechanism is used in running both models based on the time difference. Subsequently, this effect will be translated into a heat source in the thermal solver; therefore the thermal model will be able to start the heat diffusion process without any external heat generator. Thus, a new set of initial temperature for each node is proposed, and passed as a new feed to the electrical model to acts as a new start condition for the second round, including an update for the material resistivity dependent on the amount of temperature changes.

4.3.1 Method and results

Five samples of silicon nanowires with different diameters 20, 30, 40, 50, and 60 nm were used with fixed length of $30\,\mu m$ were examined. The material resistivity is $R=8.7\times10^{-9}$ $(\Omega\, nm^{-1})$ [97], and the variation of resistivity in equation (4.10) with temperature assumed to be linear, due to the small range of temperature used [113].

$$R_T = R_0[1 + \alpha(T - T_0)] \tag{4.10}$$

where; R_0 is the resistance at initial temperature 300 K, α is the thermal coefficient of the material, T_0 is the initial temperature and R_T is the calculated resistance for the new temperature. The time step can be found from equation (4.11) [9].

$$\Delta t = \frac{\Delta l}{C} \tag{4.11}$$

The thermal time step is obtained from equation (4.12) by using the material properties and the advantage of TLM equivalences between circuit and thermal parameters to calculate the thermal diffusion time step.

$$\Delta t = \sqrt{RC} \tag{4.12}$$

The initial temperature setup was at 273K. The simulations for (electromagnetic) EM-engine run for 50 time steps for the first cycle to minimize the time gap between the two solvers and hence, reduce the numerical error. This resulted in obtaining the value of the overall average value of the voltages in each wire after this period as in Figure 4.15, in addition to the amount of power dissipated from each sample as a result of the passage of the electric current as in Figure 4.16.

The nanowire diameter has direct influence on the diffusion process, as the changes in resistance alter the reflection and transmission coefficients values. This will, in turn, specify the time delay for each pulse. In the 20nm wire, the average value for the voltage was less than the other samples by (0.3%-0.6%), in spite of using the same excitation value of 20V. This is due to the effects of nanowires diameter, as the nanowires properties are strongly dependent on their diameter [114].

The average power dissipated for each sample is illustrated in Figure 4.16. The results show the diameter size effect on energy losses and it can be seen that the highest value is for the 10nm wire, with higher resistance, and the least value of $0.01\,mW$ for the 60nm sample, with less resistance.

The thermal response for the model is described in Figure 4.17 for 60nm wire, where the heat source in the thermal solver is based on the amount of power dissipated from

each node in the electrical model. In Figure 4.18, one can see the heat response for 50nm wire under similar condition to the previous figure, taking advantage of the combined electric and thermal model being in one solver.

Figure 4.19 shows the thermal diffusion for 20nm wire and it can be seen that the temperature limit is increased in the last sample, where the upper temperature limit was 274.15 K, while this limit kept under 273.1 K for the 50nm and 60nm wires. These results can be attributed to the differences in the amount of power dissipated by each wire, also the small temperature difference is due to the limitation of the excitation source and the time of simulation. Figure 4.20 shows the variation of average temperature along the 50 nodes in each nanowire after 480 time steps. The variable initial temperature at each cycle showed noticeable effects that were diverse in each wire due to several factors. Those factors were: a different transient current path for each wire according to the wire diameter, a low transmission coefficient, a high refection coefficient, and the insulated boundary. These factors will work jointly to elevate the initial temperature for each node over time at different rates depending on the size of nanowire.

In Figure 4.21, the results from TLM approach are compared with a thermal model for 50nm vapor-liquid-solid-grown (VLS) SiNW from reference [27], it shows a good agreement. A higher temperature is demonstrated in the co-simulation model due to inclusion of the power dissipation effects.

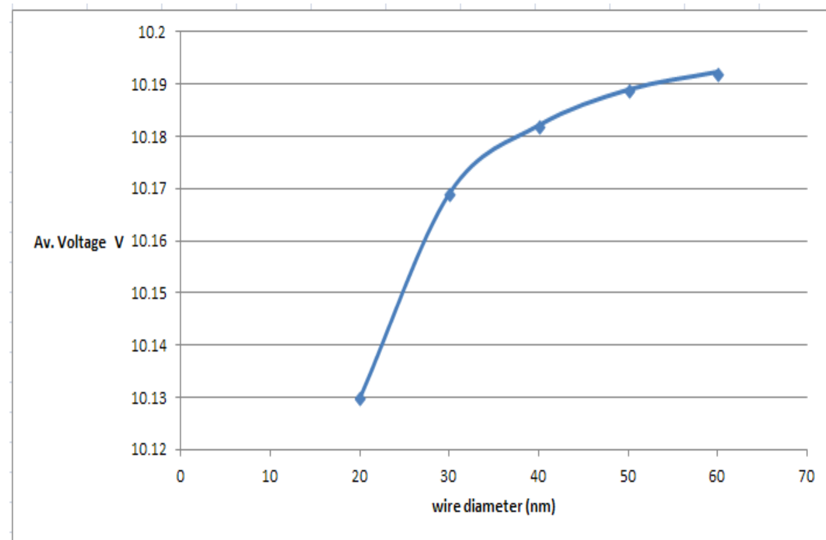


Figure 4.15: Average voltage in nanowires of different diameters after 50 timesteps

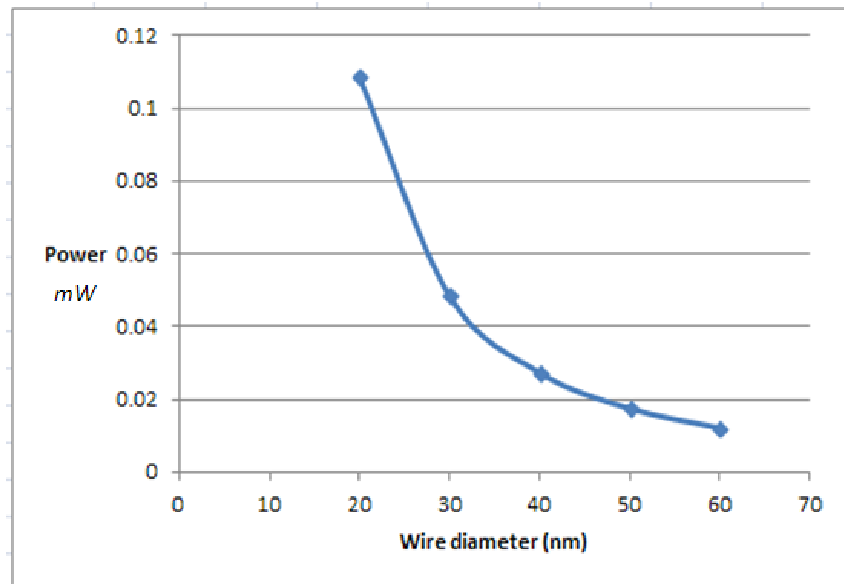


Figure 4.16: average power dissipated in different nanowire diameters after 50 timestep

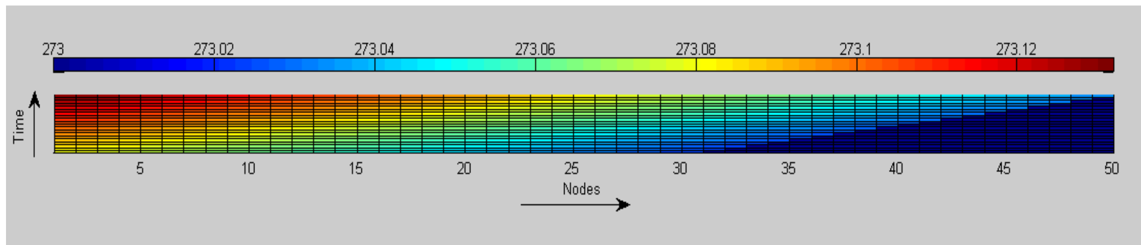


Figure 4.17: thermal response in 60nm wire vs. time, after 50 timestep

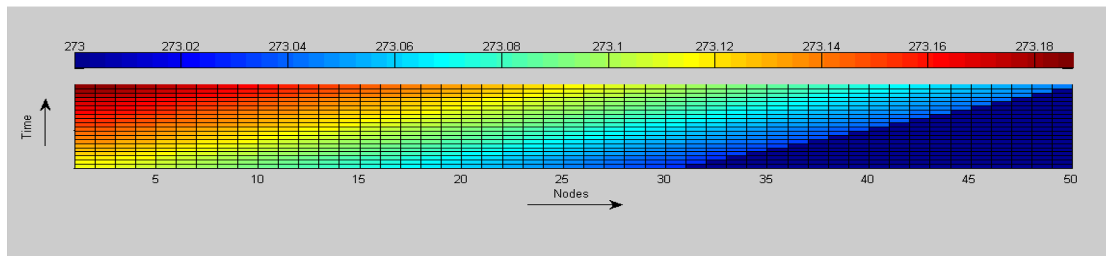


Figure 4.18: thermal response in 50nm wire vs. time, after 50 timestep

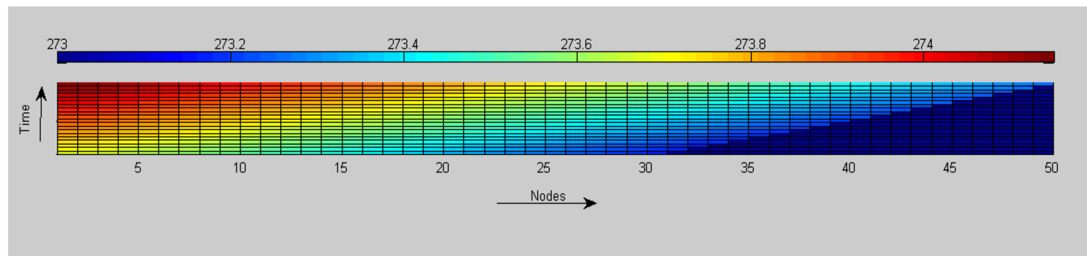


Figure 4.19: thermal response in 20nm wire vs. time, after 50 timestep

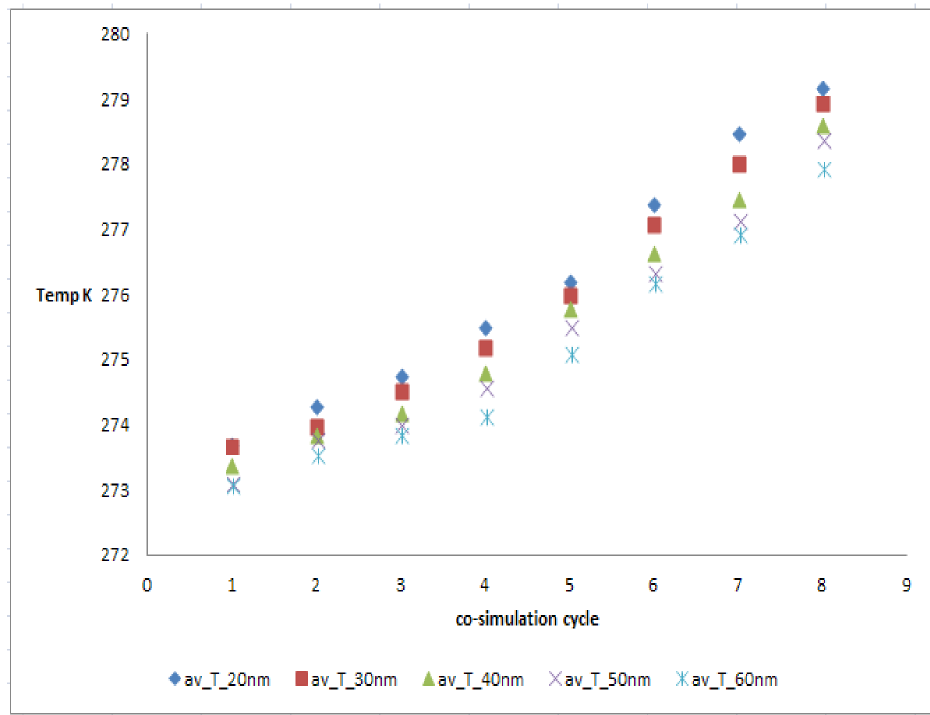


Figure 4.20: Average temperature along nanowires after 8 cycles (co-simulation), equivalent to 8.1×10^{-4} *sec*

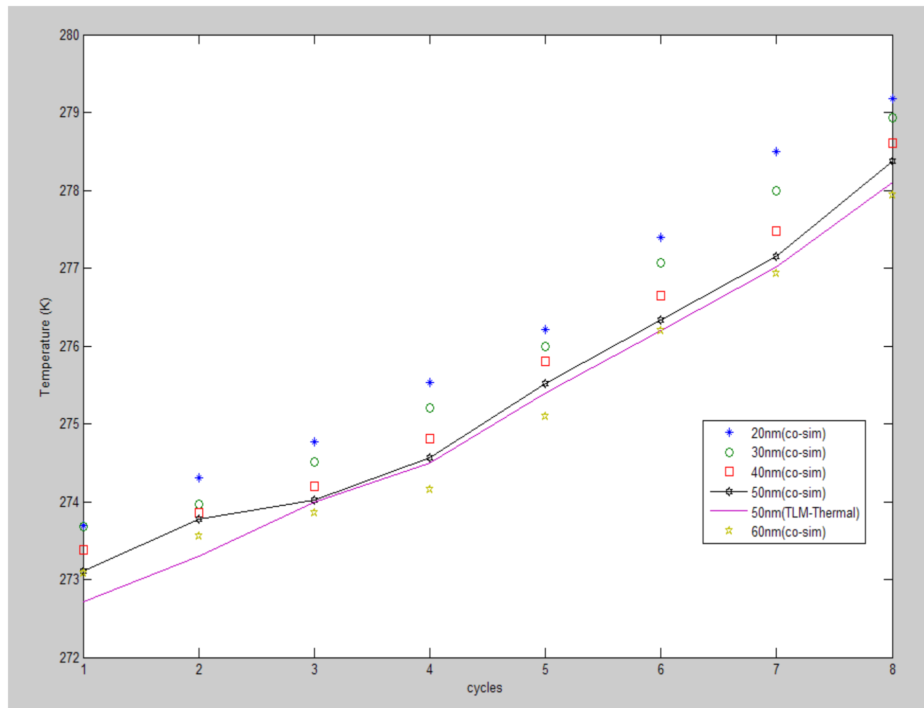


Figure 4.21: Average temperature along nanowires compared, in the legend, which is reference [27] for 50nm nanowire, reference labelled (TLM-Thermal)

4.4. Conclusion

A new node structure was derived to model heating effects in nanowires, including emissivity, by using a one dimensional TLM solver [27]. This approach provides a simple technique to model the thermal behavior of nanowires, which also includes the radiation effects in this thermal analysis, by the use of a shunt conductance. The application to vapor-liquid-solid (VLS) - grown, and electroless-etching (EE) - grown nanowires was examined. The models were well behaved and demonstrated good agreement with a previous publication [97]. The proposed model presents a potentially useful additional tool for thermal analysis of nanowires: in particular for application to future transistor technology. The approach used to model the emissivity in this 1D model may be extended to 2D or 3D systems to explicitly include emissivity effects in 'surface' nodes. Furthermore, the co-simulation approach is used for nanowires through a hybrid electro-thermal model to investigate the electrical and thermal behaviours of silicon nanowires. The hybrid model is well behaved and demonstrated good agreement with previous publication and is the basis of work presented later in this thesis.

Chapter 5 2D TLM simulator, description and implementation

Summary

In this chapter, a hybrid electric and thermal TLM model of semiconductor FET devices is described. The proposed solver combines the electric and the thermal behaviour for semiconductor devices in one engine using the power dissipation from the former as a key-link in the latter to use it as a heat source. Section 1 clarifies the mechanism of this approach under the title of TLM solver, where the electric and the thermal solvers are explained in two sub-sections, followed by the main results from the 2D model in section 2. Finally, the conclusions from this chapter are listed in section 3.

5.1. TLM solver

In this chapter, a two dimensional hybridized model is employed to examine the interrelated electrical and thermal behaviour of semiconductor devices, which leads to a better understanding of power dissipation and the self-heating problem. Additionally, the proposed model will introduce an integrated system that has the capability to deal with thermal factors that have the key role in degradation and ageing of semiconductor devices, which is the main topic in this research. Hence, preliminary assessment for FET devices is presented in this chapter.

5.1.1 Electric Solver

For inhomogeneous lossy materials, a shunt node as in Figure 5.1 is considered to model the electric problem for the first solver, where the introduced stub will represent any variation in permittivity from the background material. The nodal voltage can be calculated from equation (5.1), and the scatter matrix for this node is given in equations (5.2) and (5.3).

$$V_n = \frac{\sum_0^P 2V^i + Y_S 2\,V^i{}_S}{Y} \tag{5.1}$$

$$\boldsymbol{S} = \frac{1}{(4+Y_S+G)} \begin{bmatrix} 2-Y & 2 & 2 & 2 & 2Y_s \\ 2 & 2-Y & 2 & 2 & 2Y_s \\ 2 & 2 & 2-Y & 2 & 2Y_s \\ 2 & 2 & 2 & 2-Y & 2Y_s \\ 2 & 2 & 2 & 2 & 2Y_s - Y \end{bmatrix} \tag{5.2}$$

$$\mathrm{Y} = 4 + Y_s + G \tag{5.3}$$

where: V^i is the incident voltage, Y_s is the stub admittance, G is the conductance, and Y is the normalized admittance. The power dissipation calculated at each node from equation (5.4) will be used as the source of heat in the thermal model as expressed in equation (5.5).

$$P = I^2 R \tag{5.4}$$

$$P \leftrightarrow Q \tag{5.5}$$

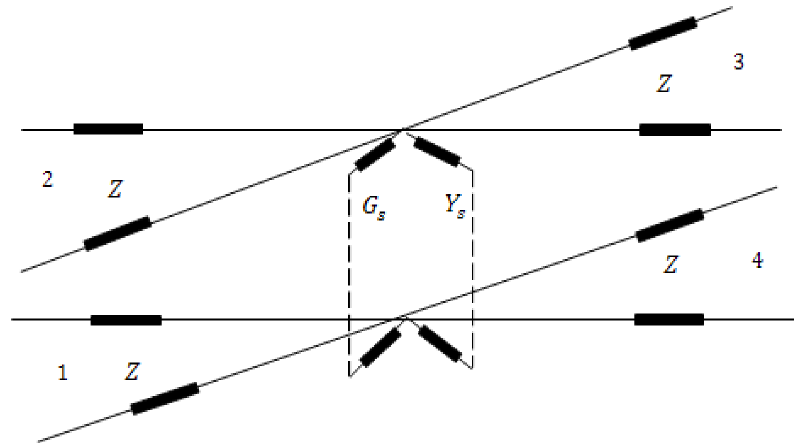


Figure 5.1: 2D shunt node for electromagnetic problem

5.1.2 Thermal solver

Heat diffusion problems are addressed in a wide range of applications, such as semiconductor lasers, power semiconductor devices, and optoelectronics [23, 115-117]. The thermal diffusion equation in two-dimensional problems can be expressed by (5.6) - see Figure 2.10. Adopting the analogy mechanism between this equation and the telegrapher's equation for two-dimensional problems as in equation (5.7), leads to the fact that the temperature can be represented using voltage, heat generation by current, specific heat by capacitance, and thermal conductivity by resistance, as in equation (5.8).

$$\nabla^2 T = D \frac{\partial T}{\partial t} \tag{5.6}$$

$$\nabla^2 = a[R_d\, C_d \frac{\partial V}{\partial t} + L_d C_d \frac{\partial^2 \emptyset}{\partial t^2}] \tag{5.7}$$

$$V \leftrightarrow \emptyset, R \leftrightarrow \frac{\frac{\Delta x}{2}}{k_{th} A}, C \leftrightarrow S\Delta x\mathrm{A}, \mathrm{I} \leftrightarrow \mathrm{Q}\Delta\mathrm{xA}, \mathrm{i} \leftrightarrow \mathrm{JA} \tag{5.8}$$

The characteristic impedance for the transmission lines is given by [43].

$$Z = \frac{2\Delta t}{C} \tag{5.9}$$

Upon this set of equivalences, the nodal temperature in Figure 5.1 can be found using the parallel generator (Millman's) theorem, as follows [43].

$$V_n = \frac{\sum_0^n 2V^i + I}{\frac{4}{R+Z}} \tag{5.10}$$

$$V = U_{VT}\, T \tag{5.11}$$

Where, U_{VT} is a unit factor (volt/temp). The temperature increment due to power update from electromagnetic model is found from [21].

$$\Delta T = K \frac{1}{n} \sum {V_n}^2 \tag{5.12}$$

K is a constant [21].

$$K = G \frac{\Delta l^2}{4} \left[\frac{1}{2\Delta l K_{th}} + \frac{2\Delta_{th}}{c\rho \Delta l^3}\right] \tag{5.13}$$

where; Δl is the node distance, Δ_{th} is the thermal time step, n is constant, ρ is the density, and K_{th} is the thermal conductivity. The scatter phase can be covered by equation (5.14) and the scatter matrix by equation (5.15).

$$\begin{bmatrix} V^{r1} \\ V^{r2} \\ V^{r3} \\ V^{r4} \end{bmatrix}_k = \frac{1}{(2R+Z)}[\boldsymbol{S}]\begin{bmatrix} V^{i1} \\ V^{i2} \\ V^{i3} \\ V^{i4} \end{bmatrix}_k + \frac{I(Z+R)}{4}\begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} \quad (5.14)$$

$$\boldsymbol{S} = \begin{bmatrix} (2R+Z) & Z & Z & Z \\ Z & (2R+Z) & Z & Z \\ Z & Z & (2R+Z) & Z \\ Z & Z & Z & (2R+Z) \end{bmatrix} \quad (5.15)$$

Repeating equations (5.1-5.14) give the mathematical structure for the co-simulation process.

5.2. Results for 2D hybrid model

The device structure is illustrated in Figure 5.2, and doping concentration are: $N_a=5.2 \times 10^{16}\ cm^{-3}$ p-type buffer layer, $N_d= 1.6 \times 10^{17}\ cm^{-3}$ for active layer and $N_d=1.1 \times 10^{19}\ cm^{-3}$ for N^+ layer (values obtained from references [50, 52]).

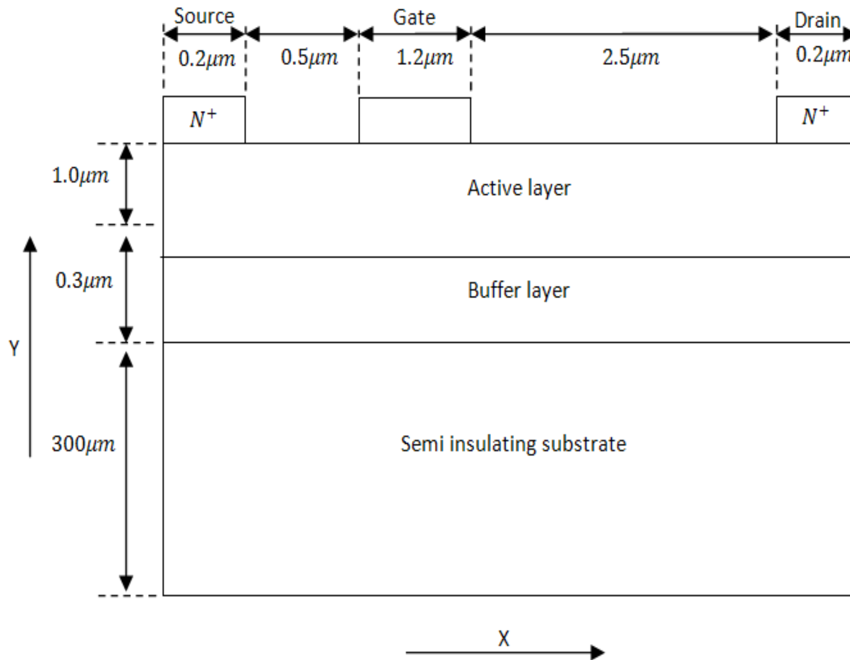


Figure 5.2: device structure in XY plan

Figure 5.3 shows the simulation results for SiC MESFET in xy plane, when Vds = 20 V and Vgs = 0V were applied, the model divided into 46 nodes in the x-direction with 54 nodes in the y direction, node size ($0.1 \times 0.05\,\mu m$). According to the variation of resistance value for each layer, the current flow will effected. It can be seen that the current flowing well in low resistance regions, i.e., the active layer, and with less in high resistance regions. The results also show that there is a higher current density underneath the gate area.

The device is subjected to some structural tests to examine the thermal behaviour, such as, the effect of the substrate and buffer layer thickness on the device performance, as a similar proposed by Song et al.[49]. This test will help to link the electromigration effects such as, hillocks formation, later in chapter 6.

In Figure 5.4, the average voltage across the channel for two values of Vds (20V and 40V) against the semi-substrate layer thickness is shown. In Figure 5.5, the maximum temperature was calculated along the active region, with thickness variation in semi-substrate layer, the heat sink used was 273K, and the heat generated taken into consideration in all nodes. The results show agreement in behaviour with Feradji et al's results [52], regardless of some differences between the two approaches, such as. The assumption by Feradji et al of uniform power dissipation underneath the gate and no heat generation elsewhere, while power losses were considered in all nodes in the current model. In addition, [52] adopted 3D TLM model, using 300K as fixed temperature for the heat sink, and using a constant power density of 3.8 Wmm^{-1}. The

model results show that the general behaviour is complies with results in [52] as it can be seen in Figure 5.5.

In Figure 5.6 the temperature increased with Vds when the buffer layer is doubled in thickness. It can be seen that the higher temperature recorded was 328.1 K for 1 μm buffer layer when Vds=100V applied, while the lowest was 275 K with Vds=20V when the buffer layer increased to 2 μm.

In Figure 5.7, the current flow is shown for the device when the thickness of the buffer layer increased to double (18 nodes), the results show there are signs of conducting areas outside the active region. In Figure 5.8, the buffer layer thickness is increased to 24 nodes. The results demonstrate less current outside the active region and provide an obvious boundary for the channel area. This results agree with previous research [49] about the effects of buffer layer size on the device performance and the points towards an increased buffer layer thickness to avoid the occurrence of the conducting path. The combination of the two models in one engine will simplify the calculation and the updating process for the electric and thermal properties, where the thermal diffusion results in Figure 5.9 show the temperature distribution in the 3D plot viewing the temperature in z-axis while the device described in x, and y-axis, it can be seen that the active layer is under the influence of energised electrons from the Vds input of 20V.

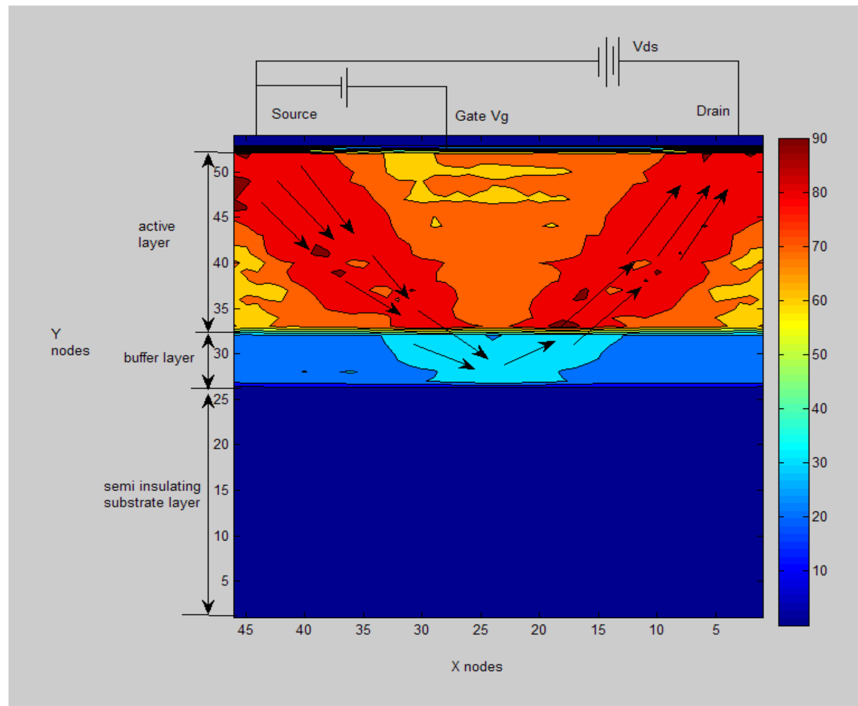


Figure 5.3: simulation result for voltage transient $\times 10^{-1}\,V$ in SiC MESFET with Vds=20V and Vgs=0

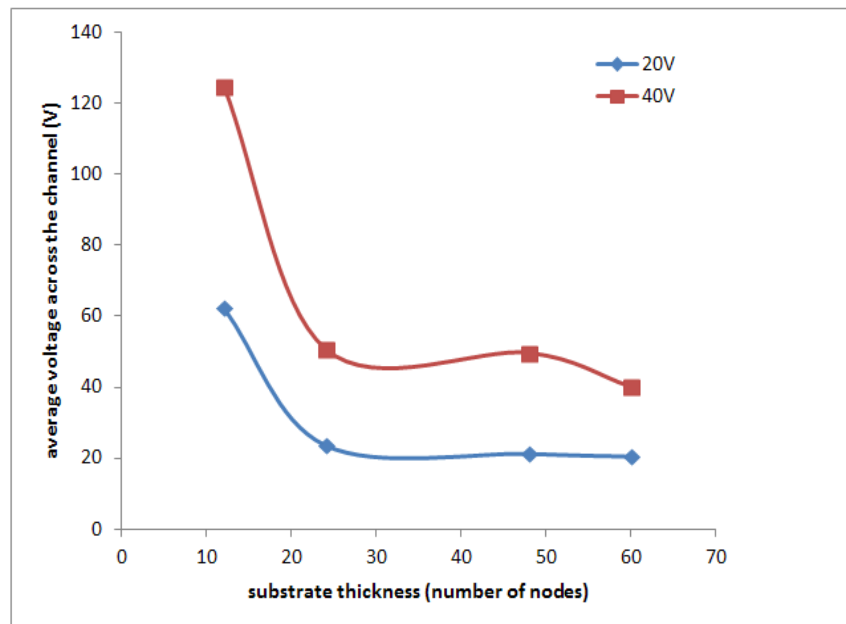


Figure 5.4: average voltage across the channel as a function of substrate thickness, nodes size $(0.1 \times 0.01)\,\mu m$

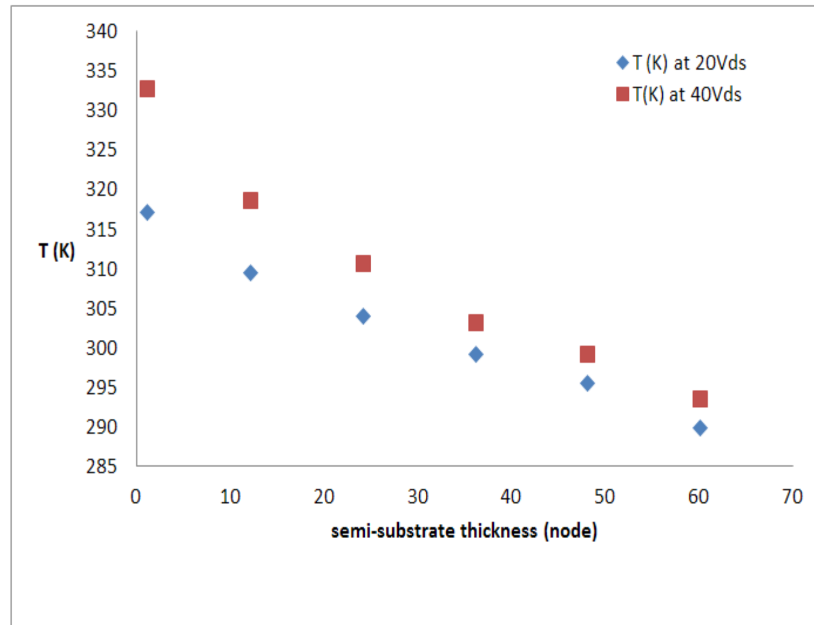


Figure 5.5: Maximum temperature for SiC channel region in 2D TLM model as a function of substrate thickness in contact with heat sink 273K

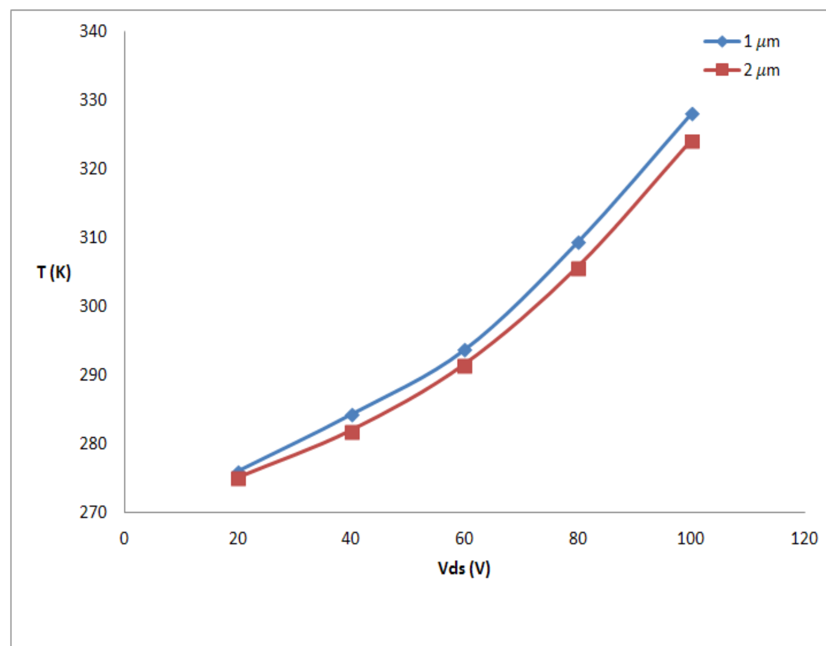


Figure 5.6: average temperature along the active layer with changes in buffer thickness doubled, with response to Vds=20, 40, 60, 80, and 100V

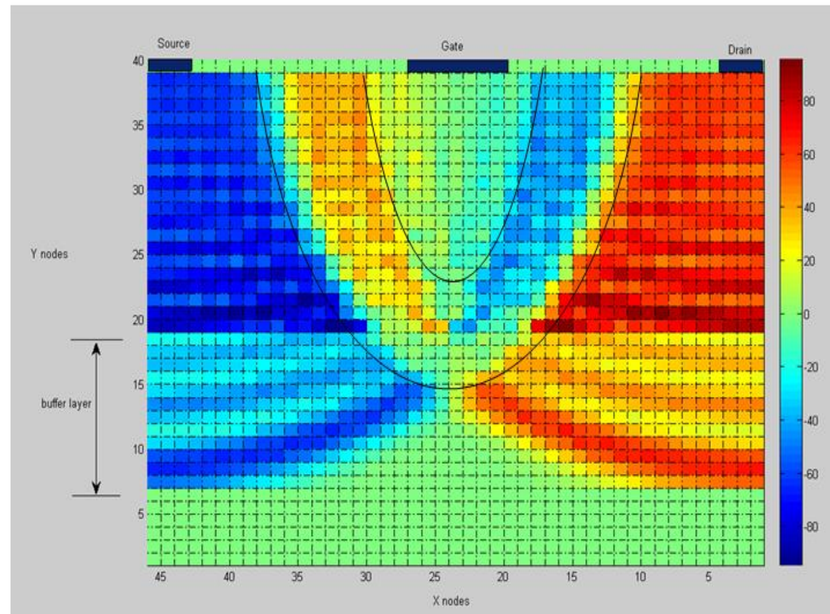


Figure 5.7: current flow in mA with changes to buffer layer thickness (double- 18 nodes)

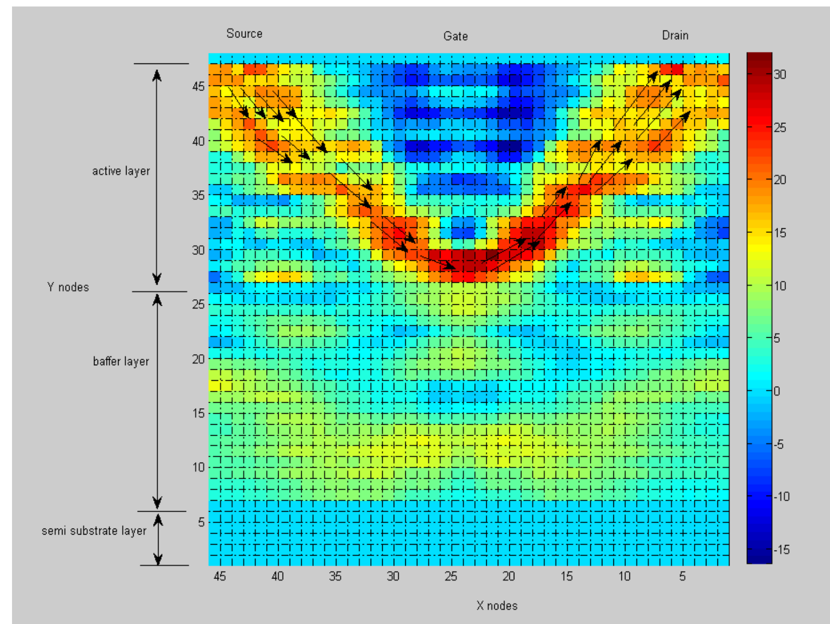


Figure 5.8: current flow in mA after increased buffer layer thickness to 24 nodes for 4H-SiC MESFET device

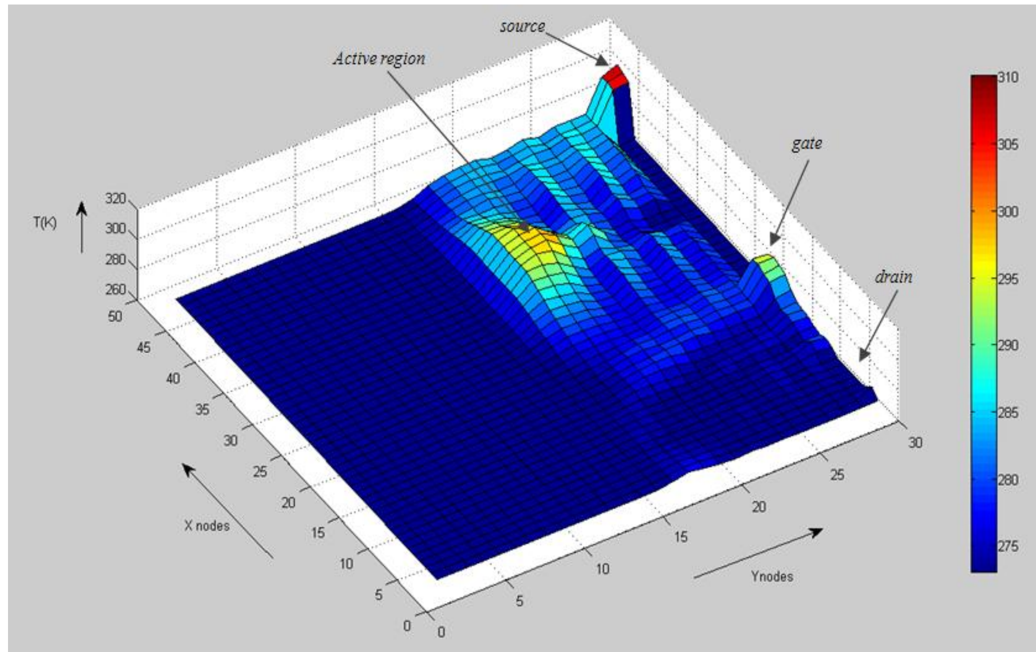


Figure 5.9: co-simulation result showing the temperature distributions in MESFET device

5.3. Conclusion

In this chapter, a hybrid approach is presented using the TLM method, through a combination of electro-thermal model, to investigate the electrical and the thermal behaviours for SiC MESFETs. The combined model offers better understanding for the power dissipation problem, and allows more information in both solvers at any stage during the simulation. The material resistivity was updated frequently with temperature variation, this resulted in noticeable changes in the current flow with different rates in each area according to the region resistivity. A combination of electro-thermal solvers, enabled the thermal simulator to start without introducing an external heat source, as the process is built on an interlock of both effects together. Buffer layer thickness in a 2D

model shows observable effects on device temperature, confirming the previous finding of Song et.al [49] and Arulkumaran et.al [118]. Conversely, maximum temperature for the channel rose to 325K when the buffer layer is doubled, with various inputs of the drain-source voltages up to 100V. This model is well behaved and demonstrates a potentially useful additional tool for the electrical and the thermal analysis of semiconductor devices can be used to deal with degradation parameters (thermal) in the field of semiconductor ageing.

Chapter 6 Ageing in Semiconductor Devices

Summary

In this chapter, the operational life of semiconductor devices is described. Moreover, examining the key factors that control failure rate are illustrated in the first section. Section 2 discusses common degradation mechanisms and the causes of failure in FET devices are discussed. In section 3, a new TLM approach is introduced to model the ageing phenomenon, this is done in two sub-sections, the first involves the probability of occurring electromigration effect, and the second involves thermomigration effects. In section 4, the TLM engine formulation is given, which includes, thermal reflection coefficient, device performance, acceleration factor and main time to failure. In section 5, the degradation in MOSFET devices is explained. Lastly, in section 6 the conclusion from this chapter is summarised.

6.1. Lifecycle in Semiconductor Devices

The probability of reduction in operational quality (failure) of electronic devices is a growing area of concern for semiconductor device based systems, as the life-times of these devices are seriously limited by factors such as: high voltage, high current,

temperature, and pressure differences. The lifecycle of a semiconductor device can be classified into three stages, as shown in Figure 6.1 [119]:

Early-life phase: the possibility of failure at this stage is a little higher, commonly caused by manufacturing process, based failure mechanisms.

Middle-life phase (constant failure rate): in this stage, devices subjected to different levels of stress, do degrade but still perform the desired functionality within their standard performance specifications, the failure rate remains reasonably constant.

Wear-out (end of life): this stage represents the final phase in the devices life, the device now has deteriorated and there is no guarantee for this to continue with the same performance, with time progressing the failure rate increases due to degradation processes inherent to the material used in the technology.

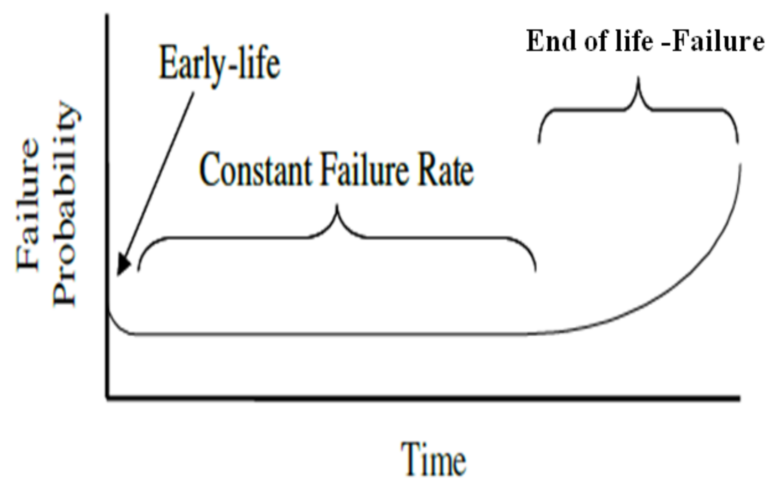


Figure 6.1: The reliability bathtub curve explains the lifecycle for semiconductor devices

Material ageing is an important cause of the failure. The ageing in material is usually understood as "altering in material properties with time, due to different causes" [120] such as, thermal effect, thermal treatment, corrosion, stress ageing.

Therefore, the device reliability is more comprehensive title for this phenomenon, as it defines the ability of the device to maintain its desired functionality under different conditions during the lifecycle. Generally, the reliability of semiconductor devices depends on their resistance to the stress applied to the device for instance, mechanical stress, thermal stress, electrical stress, and external stress (such as humidity).

To find a simple failure rate for a single acceleration-test [121].

$$\lambda_f \propto \frac{1}{TDH \times AF} \tag{6.1}$$

where; *TDH* is the total device hours, and *AF* is the acceleration factor. The acceleration factors are usually used to lower the failure rate from the thermally accelerated test conditions to a failure rate investigative of real use temperature. By using the Arrhenius Law which describes thermal acceleration in semiconductor devices and physio-chemical reaction rates, it can be represented by equation (6.2) [121]. This equation will be employed in calculate the acceleration factor for the TLM model in section 6.3.

$$AF = exp\left(\frac{E_A}{K_B} * \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \tag{6.2}$$

where E_A, K_B, T_1 and T_2 are as follows: thermal activation energy, Boltzmann's constant (8.63 $\times 10^{-5}$ eV/K), the operational temperature, life test stress temperature in degree Kelvin.

6.2. Degradation mechanisms

In this chapter, interest is focused on FET devices due to the availability of necessary data for validation. The applied gate voltage in FET devices will control the amount of current flow between the drain and the source terminals. In spite of the presence of the dielectric layer that insulates the gate, the electric field will cause some changes to the electric conductivity of the device channel. Moreover, these faults are placed under two categories [122]. First, are the main intrinsic faults which are more relevant to device physics, such as (hot-carrier, dielectric-breakdown, and electromigration). Second is major faults, which are related to device packaging, such as wire fragments and die solder degradation [123].

I. Hot-Carrier Injection (HCI): It is a process of the movement of the energetic charge carriers (electrons or holes) outside the device active channel and gets trapped in the dielectric insulating layer.

II. Bias Temperature Instability (BTI): It is caused by build-up of charge in insulating layer when a voltage is applied at the gate terminal, in this case the current flow is not necessary to make the charge trapped in the dielectric.

III. Oxide Breakdown (OB): When a voltage applied at the gate, an electrical active defect is generated within the dielectric, this can form a complete short circuit linking the channel current with the gate. This ageing mechanism can lead to catastrophic failure due to the breakdown of dielectric.

IV. Electromigration: It occurs due to high current density in silicon interconnects causing migration of metal atoms, meaning that when a flow of current collides with metal atoms, will cause drift of these loose atoms with

the electron flow. This diminishes the metal part of its atoms upstream, whilst causing a build-up of metal downstream. The upstream reduction, increases the resistance of the connection, to the degree that it may become a high resistive path or even an open circuit. At the same time, downstream may cause metal to "bulge" out of its designated track.

V. Wire left: It usually occurs when the bond between the package wires connecting to silicon die fail. It is considered as a dominant failure mode in high power IGBTs.

VI. Die solder degradation: It is a package related fault, the solder attaching to the die and packaging heat sink increase voids and cracks as a result of thermal expansion mismatch between contraction and materials during expansion.

6.2.1 Electromigration

One of the key reliability challenges in micro-semiconductors is electromigration [124]. In electromigration, the failure is mainly caused by high-energy electrons effecting the atoms in a material and causing them to shift position, where this failure mechanism is considered as the most problematic in regions of high current density [125, 126], it will be shown later in this chapter. Consequently, this failure mechanism has direct impact on a system's reliability, which can be measured in terms of *MTTF*, using Black's ageing equation (6.3) [127].

$$MTTF = A\,J^2 \exp\left(-\frac{E_a}{K_B T}\right) \tag{6.3}$$

where; j is the current density.

The accurate description for the mass transport of the ions may be very difficult due to the possibility of the mobile carriers being able to transfer their momentums to ion cores [128]. In turn, the ions are affected by accompanying forces: temperature gradient, mechanical stress, and electric field [128]. The transport phenomenon under the effect of applied current (electromigration) is quite similar to a diffusion process. In each case, the flux of ions or (atoms) along the channel, can be described as the product of the mobility and the force that is affecting the moving atoms, as in equation (6.4) [129].

$$J_a = \mu F \tag{6.4}$$

where; $\mu = D/kT$ and D is the diffusion coefficient of the moving atoms at which the transport occurs at temperature T. In the electromigration case, the force F can be used as a product of electric field and an effective charge for the moving atoms and/or resistivity of the metal multiplied by current density, as in (6.5) [130].

$$J_a = \frac{D}{k\,Tz^*\,e\rho J} \tag{6.5}$$

Or in terms of electric field, as in (6.6).

$$J_a = \frac{D}{k\,Tz^*\,eE} \tag{6.6}$$

The relationship expressed in (6.5) shows the proportionality between charge carrier flux and atomic flux. It also expresses the electric field as directly responsible for part of the factors acting on the moving atoms.

To show the transition probability for atomic ion cores Figure 6.2 illustrate the potential energy profile for atomic ion, where; j is the current flux density, E_b is the activation energy for an ion-vacancy exchange, E is electric field applied, $E_b = qE$, and T is the temperature. Therefore, the probability of transition of the atomic ion cores Figure 6.3 at $x - \Delta x$ to move to x, and for the vacancy to move from x to $x + \Delta x$ position, can be described as follows.

In case of current flow in the positive x-direction

$$f^{-\Delta x} = \exp\left(\frac{-(E_b - E_a)}{KT_{-\Delta x}}\right) \quad (6.7)$$

While, in electric field E_a less than electrons flux, the transition probability becomes.

$$f^{+\Delta x} = \exp\left(\frac{-(E_b + E_a)}{KT_{+\Delta x}}\right) \quad (6.8)$$

where; $f^{+\Delta x} and\ f^{-\Delta x}$ are the transition probability.

As the scattering and the connect phases are the two main processes in TLM method, and since the resultant electrons from the scattering event will suffers from direction change, this leads to divergence in atomic flux. Hence, the scatter phase in TLM can be employed to describe this phenomenon and control the collision rate through the scatter coefficient. This will be discussed in section 6.3.4. The unequal rate between the flux entering a specific region and the leaving flux will form the voids or the hillocks. When the leaving rate is greater than the flux entering the region, the depletion of matter ultimately leads to the formation of voids (open circuit), and elevated tensile stresses [128]. While in the opposite case, when the entering flux rate is much higher than the

leaving flux in the region, it will produce the whisker or hillock (lead to increase or decreased resistance), reduce path width, and relieves compressive stresses.

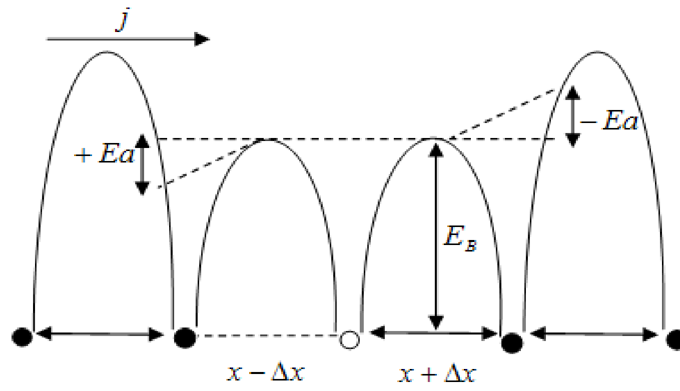


Figure 6.2: transition probability

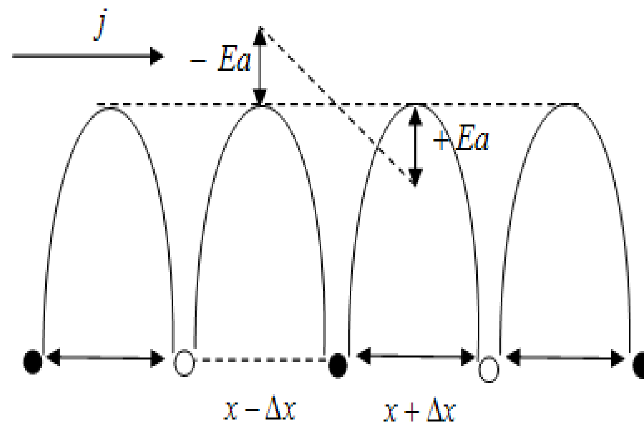


Figure 6.3: transition directions for metal ions

Briefly, we can identify two driving forces that control electromigration [131]:

a) Electrostatic force, due to the direct force of the external field on diffusion species (the charge of the migrating atoms). A charged ion (+) has a tendency to move in the direction of the applied field, and therefore the mass accumulation occurs at the cathode side.
b) Electrons force, caused by scattering of conducting electrons (i.e., momentum exchange between the diffusion atoms and the moving charge carriers).

6.2.2 Thermomigration

Miniaturization of electronic devices to micro and nanoscale leads to considerably higher current density levels and greater thermal gradient. In this case, the thermomigration phenomenon can be the dominant migration process. Thermomigration is a mass transfer of component material attributable to temperature gradient [132]. Despite the fact that the thermomigration phenomenon was identified some time ago, much of the subsequent research in semiconductor failure neglects the effects of thermomigration in electromigration failure of electronic devices. This is possibly due to the assumption of the magnitude of thermomigration flux is much smaller than the electromigration. Moreover, scientists have shown both theoretically and experimentally that thermomigration (TM) can be the dominant mass transport when the thermal gradient is high enough [133-135]. In metals the dominant force acting on the diffusion of ions is the momentum exchange caused by the collisions of the valence electrons. This driving force will change when there is no electric current flow, as the energy of electrons at higher temperature region is larger than the electrons energy at

the cold region. Therefore, the scattering electrons will collide with ions and transfer part of their momentum to ions, this process will generate a driving force for mass or heat transfer Q*.

In contrast, the atomic flux owing to thermomigration can be expressed as in equation (6.9) [130, 136].

$$J_{th} = N \frac{D}{K_B T} \frac{Q^*}{T} (-\frac{dT}{dx}) \tag{6.9}$$

And for electromigration, can describe as in (6.10).

$$J_{em} = N \frac{D}{K_B T} Z^* \, e\rho J \tag{6.10}$$

where; *D* is the diffusivity of the dominant diffusion species, *N* is the atomic concentration, *Z** is the effective charge value, ρ is the resistivity, and *J* is the current density. It is probable that thermomigration accompanies the electromigration process, as electromigration plays the key role, particularly when the temperature gradient is small.

In the next section, the possibility of electromigration and thermomigration phenomena occurring in FET device is investigated, where the atomic flux relationship in equations (6.9) and (6.10) is used, also the *MTTF* is shown when the model is subjected to a thermal stress. Afterwards, in section 6.4, the Thermal Cycle Test (TCT) will be applied as thermal acceleration factor in MOS device, where the impact on IV characteristic is studied. By presenting these two approaches, a new contribution will add to TLM and expand the area of applications for this method, and at the main time the ageing in

semiconductor devices will be tackled by a hybridized TLM engine taking the account of the internal heating effect using a time domain scheme.

6.3. TLM engine integrated with ageing function

In this section, two approaches are presented. The first model deals with a MESFET device to investigate electromigration and/or thermomigration effect in device performance. The second model deals with an RF-LDMOS device to study the effect of TCT on device performance.

The dimensions and material properties with doping concentration for 4H-SiC MESFET are taken from [50, 52]. The two dimensional TLM model is adopted in this study, thus the effects of device fingers (depth) is not considered in our calculations, the depth is considered sufficiently large compared with cross sectional dimensions to allow this 2D approximation. The device was represented by 46 nodes in the x-direction, and 88 nodes in the y-direction. As explained before the electric and thermal effects are linked together using the power loss factor.

6.3.1 Model development

The updating process for material resistivity will be effectively dependent on the amount of temperature difference. This alteration in temperature variations will lead to direct effect on electromigration through the atomic flux, as the resistivity will considered as variable parameter [137, 138]. The initial temperature was set to 273K, with an excitation voltage source of 20V to start the simulation. Due to the fact that the active regions in the semiconductor devices are usually under the influence of continuous high electric field in a short-channel, the existing charge carriers in the

channel and the active region will reach non-equilibrium energy distributions. The generation of these energized carriers is the primary cause of several reliability problems such as, hot carrier degradation [139].

Therefore, such large amount of energy in this small place will encourage the atoms to transport from the conductance zones or metal parts (drain, gate, and source) to the active region (energetic region). This increases the probability of forming hillocks or causing voids in the transition path. The hybridized engine will treat the temperature rise as a variable factor to update resistivity, hence, updating atomic flux.

6.3.2 Thermal reflection coefficient

The adoption of a co-simulation technique, and the frequent updating process for material resistivity in this model, will lead to a direct effect on the reflection coefficient values. Therefore, the boundary conditions are used with a different level of heat exchange. In Figure 6.4 the temperature distribution in device regions is shown, the results illustrates that the gate-source region is experiencing high temperature than the other layers. The reflection coefficient effects on the active region temperature are shown in Figure 6.5, the results show that with a lower reflection coefficient value such as 0.7, more reduction in device temperature occurs, providing an indication for the importance for the type of material or alloy may be used in device structure to ease the self-heating problem, thus reducing failure rate.

Similar behaviour is obtained when the range of time steps is extended to 10000 timesteps as shown in Figure 6.6. The results show that the average temperature across the active region reduced by (5-10) degrees *K* compared with the results obtained when insulated boundary used ($\Gamma = 1$).

6.3.3 Device Performance

One of the important signs in FET devices ageing is the reduction in *IV* characteristic, which leads to a decline in device performance and in a long term ending by catastrophic failure. In Figure 6.7, the device characteristic is expressed when Vds=20V applied, with four different Vgs values, the result shows the capability of the TLM circuit parameters to demonstrate *IV* plot for the first time without the need to use usual analytical methods. Also in Figure 6.8 the *IV* characteristic is plotted when higher value of Vds=40V is used, the results shows a rise in drain-source current by 80-100%. These results will be used as a reference to compare with, when the device expose to thermal stress conditions in the next section.

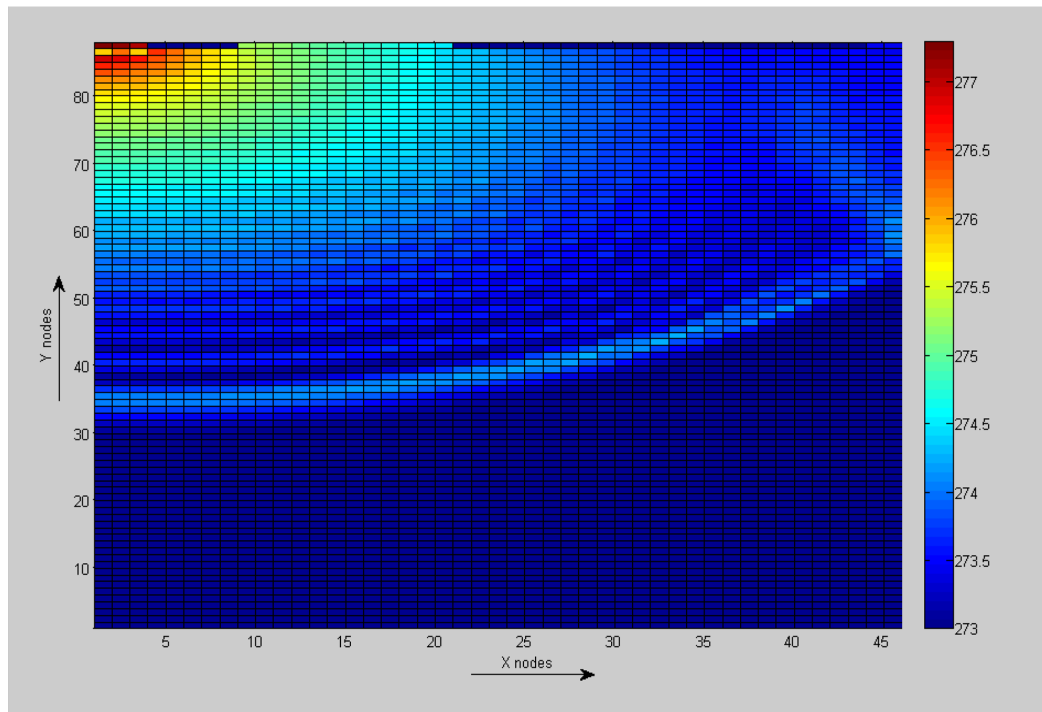


Figure 6.4: Temperature distribution with reflection coefficient 0.9

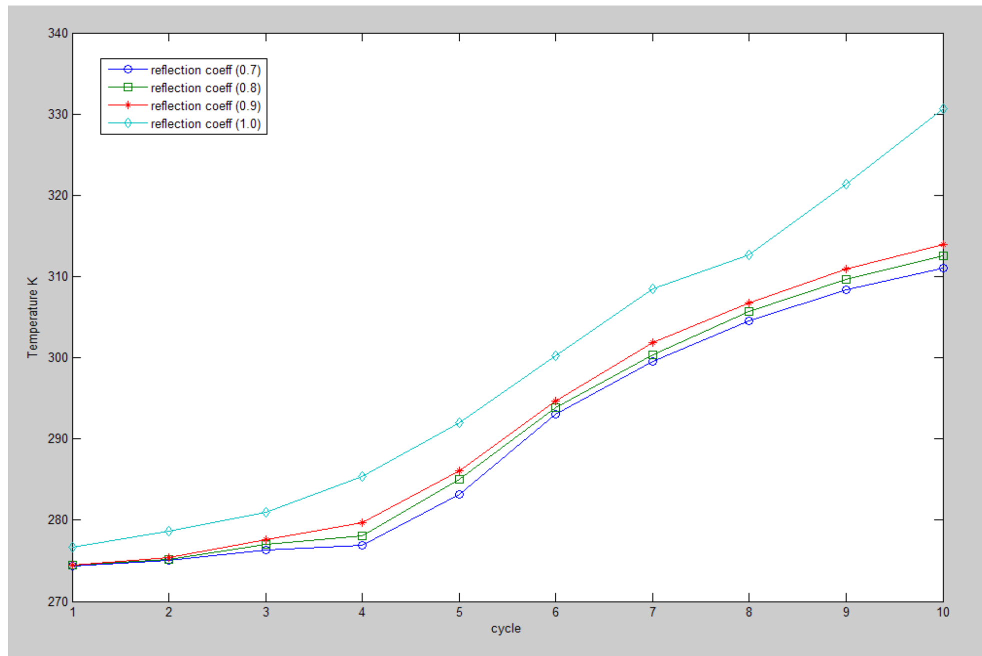


Figure 6.5: channel temperature vs. electro-thermal cycles (2000 time steps), with different reflection coefficients compared with channel temperature when reflection coefficient is 1

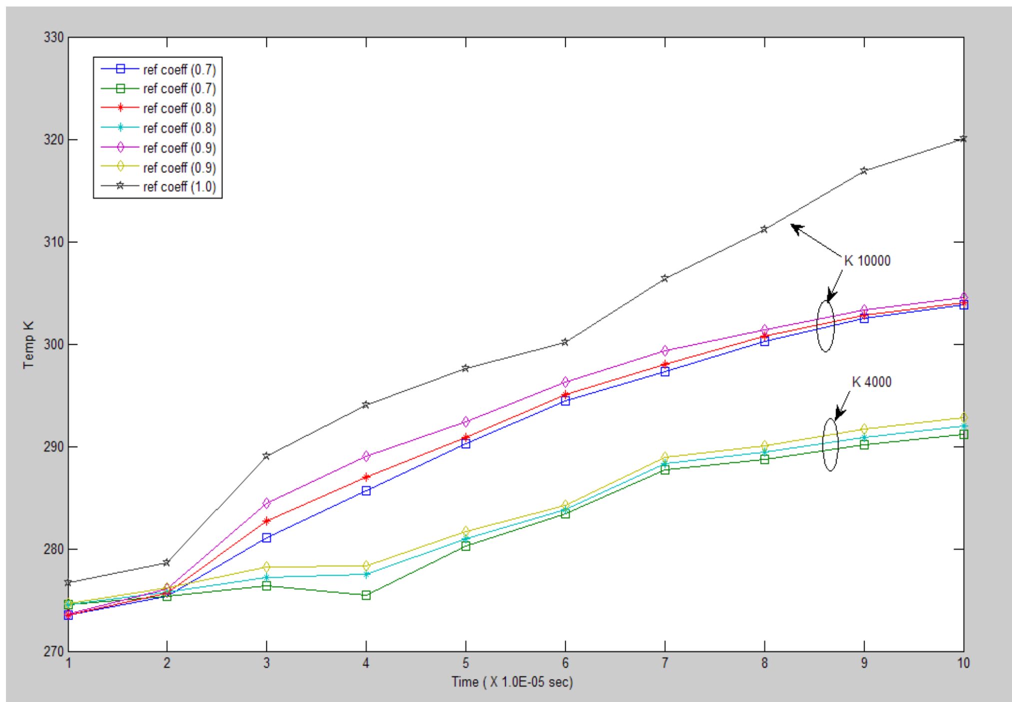


Figure 6.6: channel temperature vs. electro-thermal cycles with different reflection coefficients compared with channel temperature when reflection coefficient is 1.

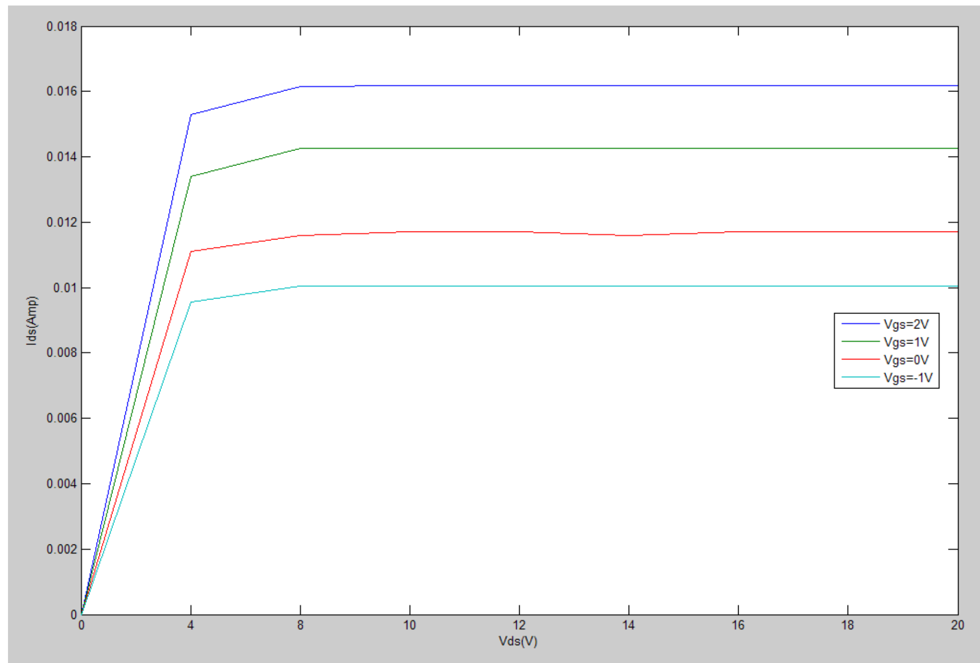


Figure 6.7: IV characteristics with Vds=20, and four cases of gate-source voltage applied - 1, 0, 1, and 2 V

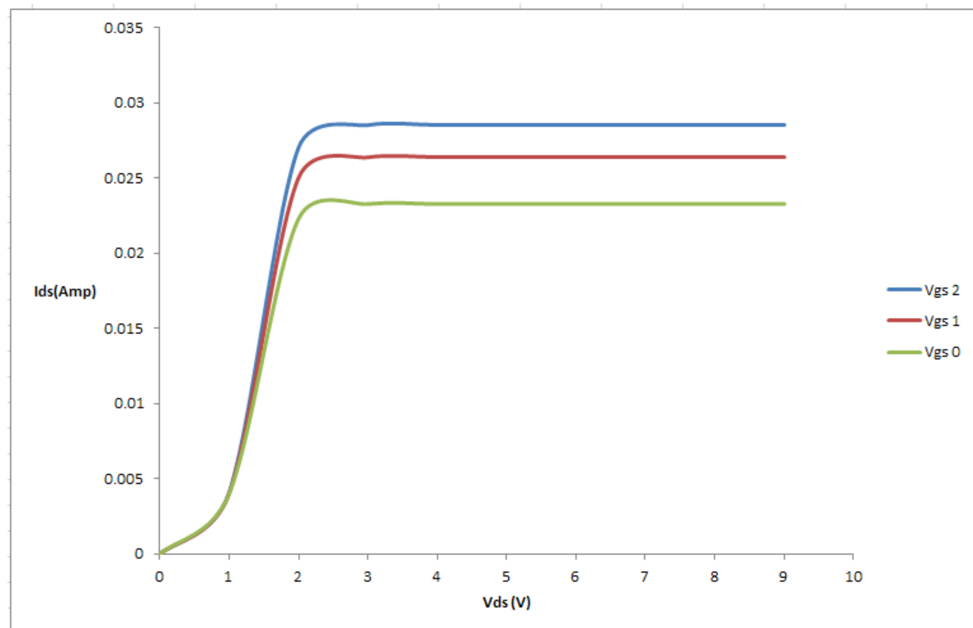


Figure 6.8: IV characteristics with Vds=40 for three cases of gate-source voltage applied 0, 1, and 2 V

6.3.4 Acceleration factor and MTTF: Discussion

In this section, the results generated from TLM engine is discussed, and the formulation of ageing parameters within the simulator is presented.

Figure 6.9 shows the temperature distributions after 8 cycles, and after 9 cycles is illustrated in Figure 6.10, the results in both figures shows that the active region is the mostly effected area by the high temperatures. The cumulative effects are shown clearly in Figure 6.11 after 10 cycles (176 seconds) when the average temperature at the active region rises to $330K$ caused by the type of boundary conditions ($\Gamma = 1$) and the continuous Vds source. These changes in device temperature, and particularly the active region temperature, will specify the amount of changes in material resistivity for the next time step. In Figure 6.12, the gradual incline in channel temperature with co-simulation cycles is shown, where these changes will be considered as the variable factors in calculating the electromigration when the *MTTF* is reduced by 10% as shown in Figure 6.13 due to increasing operation temperature by 60 degrees, as explained in section 6.3.1 (see Figure 6.14).

Similarly, Figure 6.15 show the *MTTF* for 6-10 cycles loops in a more understandable way. The rapid changes in channel temperature are considered as stress temperature in calculating the acceleration factor, and *MTTF* for each individual cycle. It is noteworthy that measuring the acceleration factor, as an important indicator, helps in showing the probability of increasing failure rate [140].

$$\lambda_{si} = \lambda_{ui} \cdot AF \tag{6.11}$$

The acceleration factor demonstrates significant increases at the 10th stage as illustrated in Figure 6.16 when the stress temperature reached to the range of 330 *K*. Another side for the temperature changes is shown in Figure 6.17 when the material resistivity was updated for each start in co-simulation cycle, as explained in chapter 4.

The (drain-source) current is shown in Figure 6.18, when the device is subjected to different drain-source voltages Vds (20, 40, 60, and 80V). The active region current demonstrates a rise proportional to the applied source after passing the non-linear phase (between cycle 2-3) down to the steady state. Meanwhile, the results presented in Figure 6.7 and Figure 6.8 can be considered as a proper test for the TLM solver to exhibit the semiconductor device functionality without using the usual analytical methods, where the drain-source current behaviour confirms this partial validation process.

Furthermore, in Figure 6.19 the atomic flux due to electromigration is linked to the excitation values (Vds). It can be seen that the atomic flux has recorded higher value of 5126 $atoms/cm^2$ with 80 Vds, this is due to dependency of electromigration on current density as it is explained in equation (6.10). In Figure 6.20, the drain-source current against time shows the probability of current reduction due to electromigration, where there is an increased in active region temperature for each cycle is shown when an insulted boundaries were used, which in practice represents an insulated device with no heat-sink. This leads to an increase in material resistivity, thus reducing the current flow, which in the case of Vgs=80 case, is ~8%, and with lower, but non-trivial, reduction for the other three Vgs values.

While in Figure 6.21, the drain-source current against time shows the effect of ageing on overall channel resistivity when the average temperature increases of 5.76 degrees

Kelvin is considered. It can be noticed that the differences are less compared with the results of Figure 6.20. These two figures confirm that with severe operation conditions (i.e. high temperature) the device may possibly demonstrate a degraded performance.

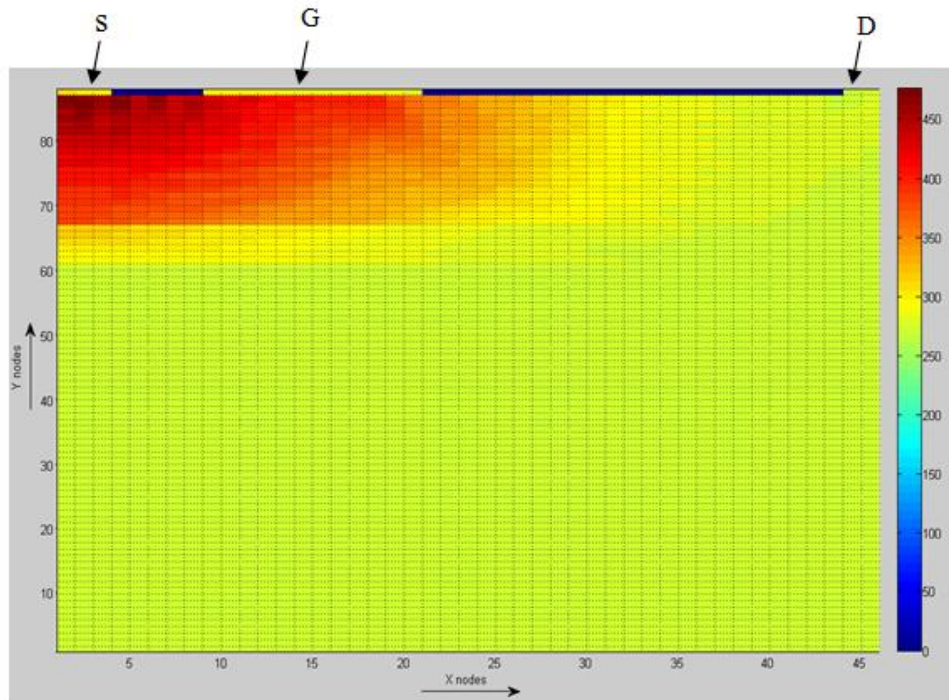


Figure 6.9: Temperature distribution after 8 cycles

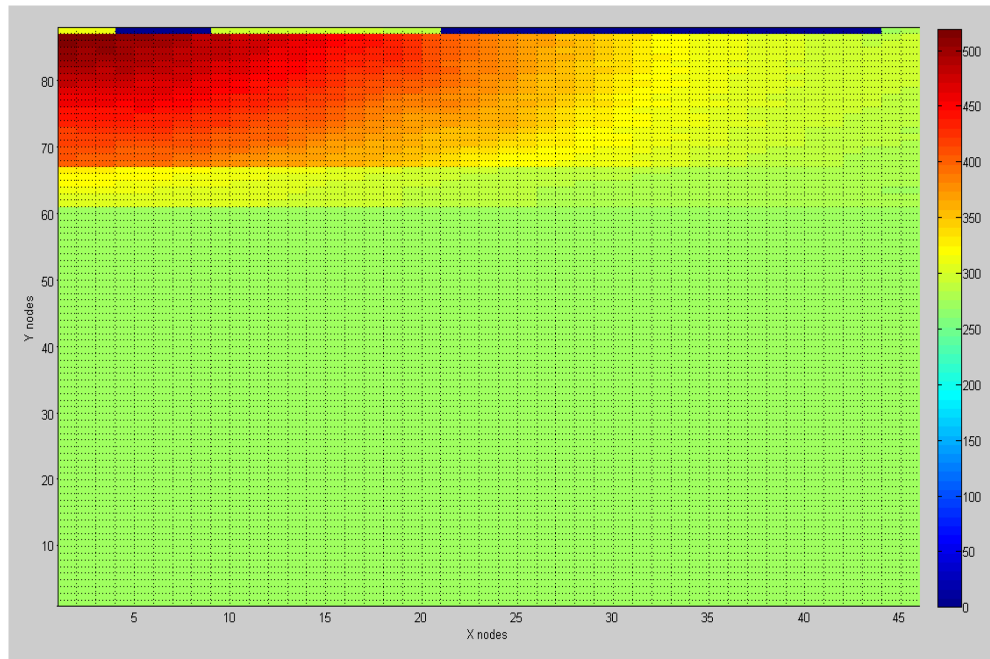


Figure 6.10: Temperature distribution after 9 cycles

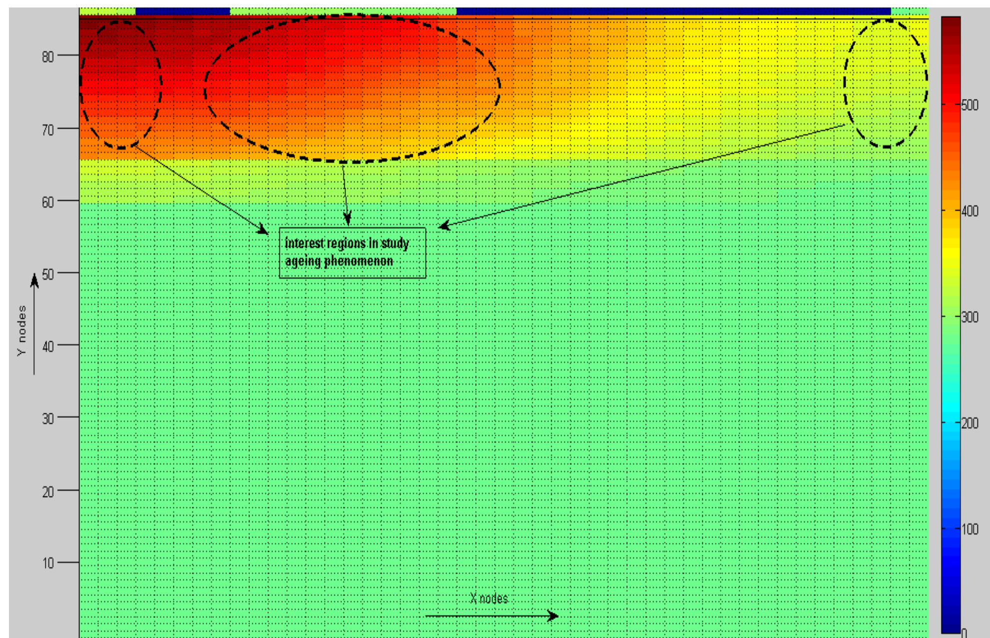


Figure 6.11: Temperature distribution after 10 cycles, showing regions of interest in study ageing phenomenon in TLM solver

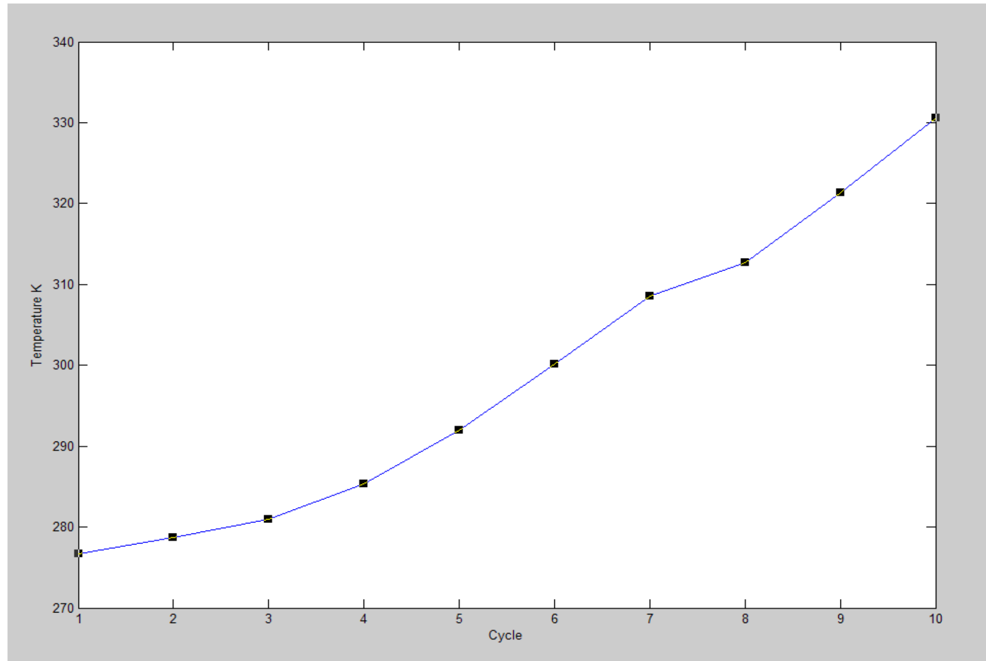


Figure 6.12: channel temperature vs. electro-thermal cycles

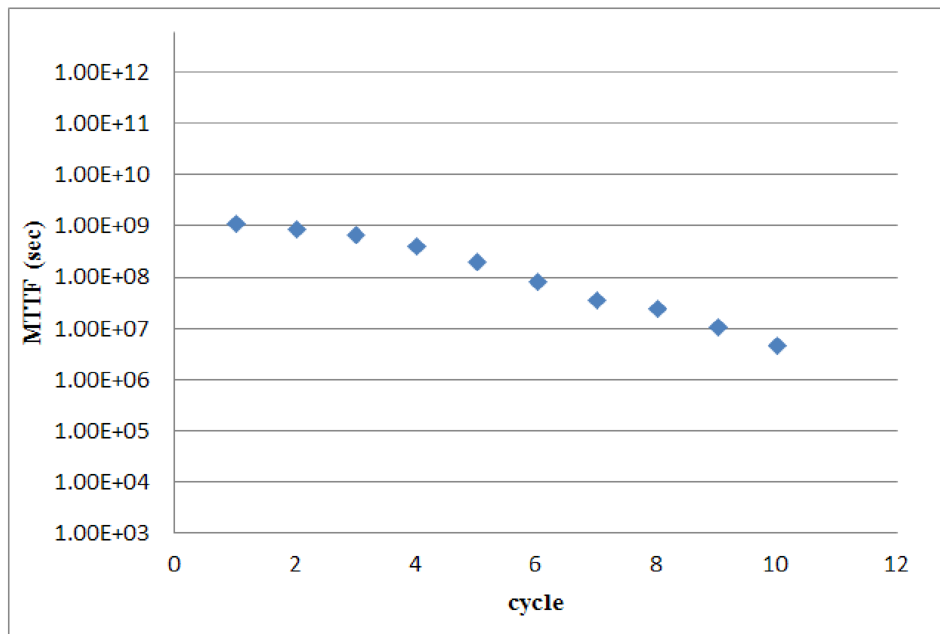


Figure 6.13 MTTF due to electromigration vs. temperature

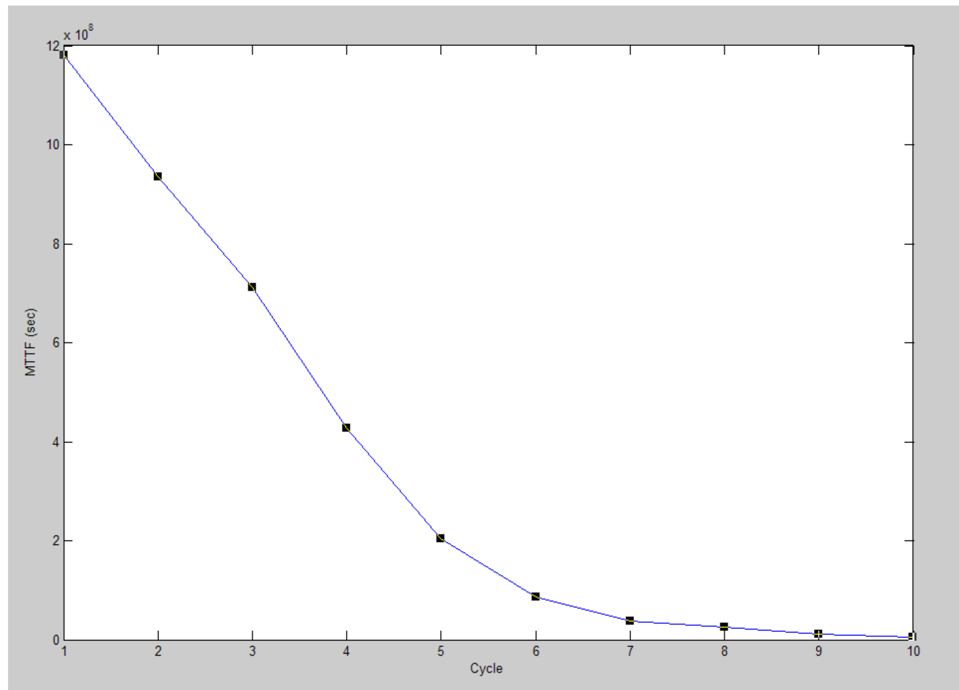


Figure 6.14: MTTF due to thermomigration vs. electro-thermal cycle

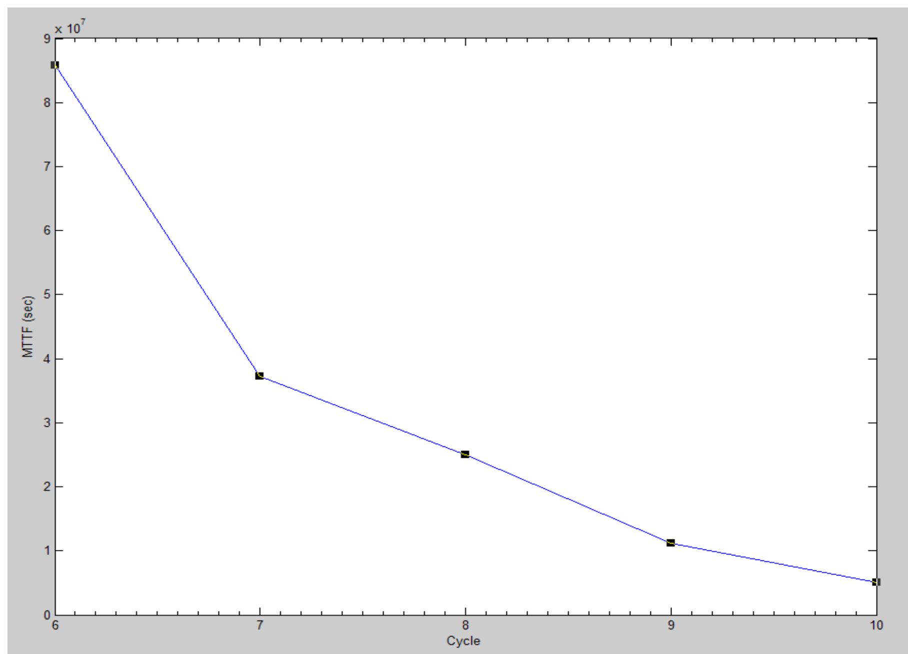


Figure 6.15: MTTF due to thermomigration for the second five cycles (clarification)

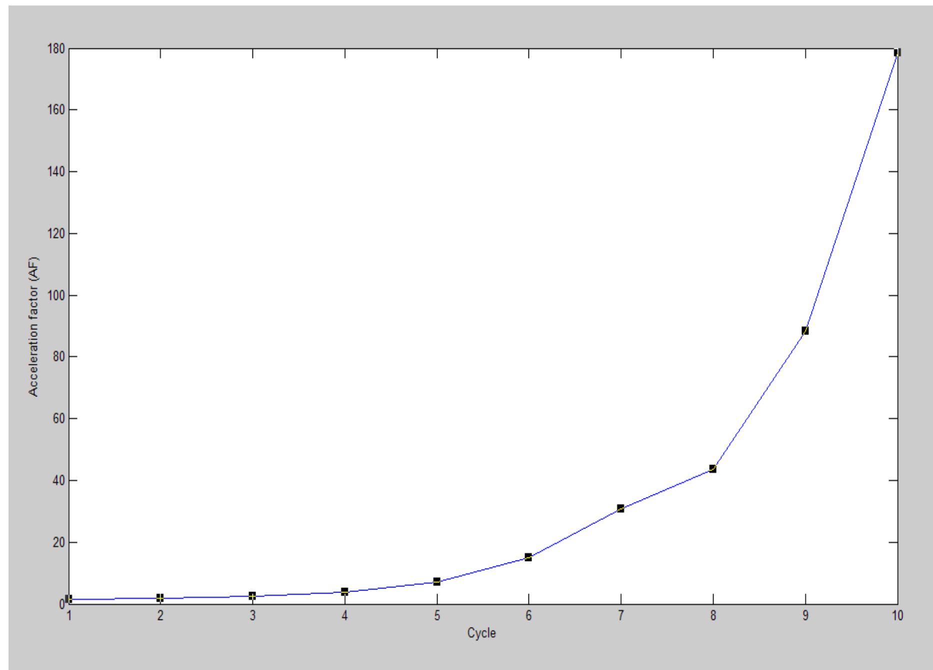


Figure 6.16: The acceleration factor vs. cycles, using reference temperature 273K

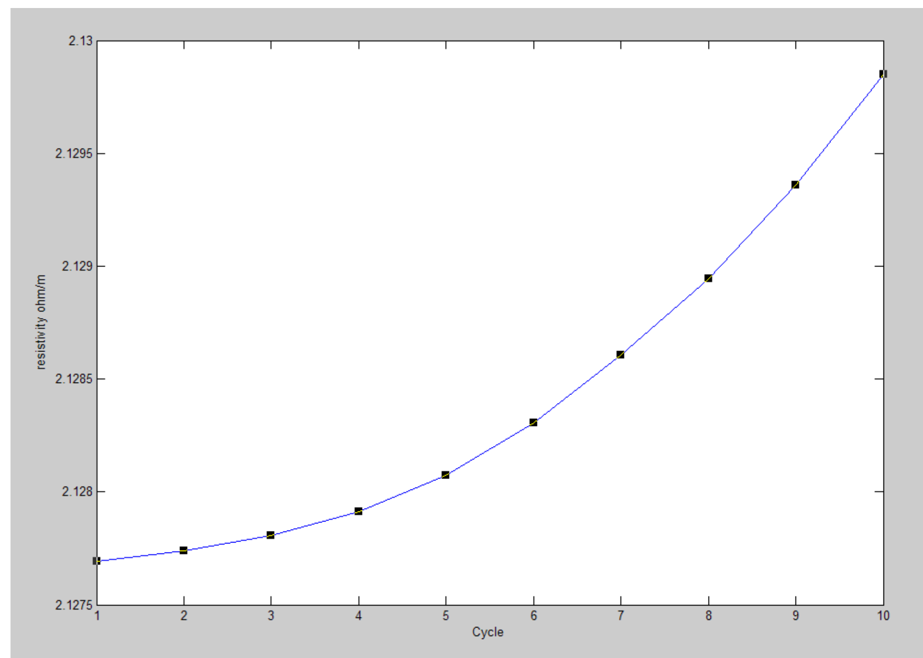


Figure 6.17: material resistivity with temperature difference vs. cycles

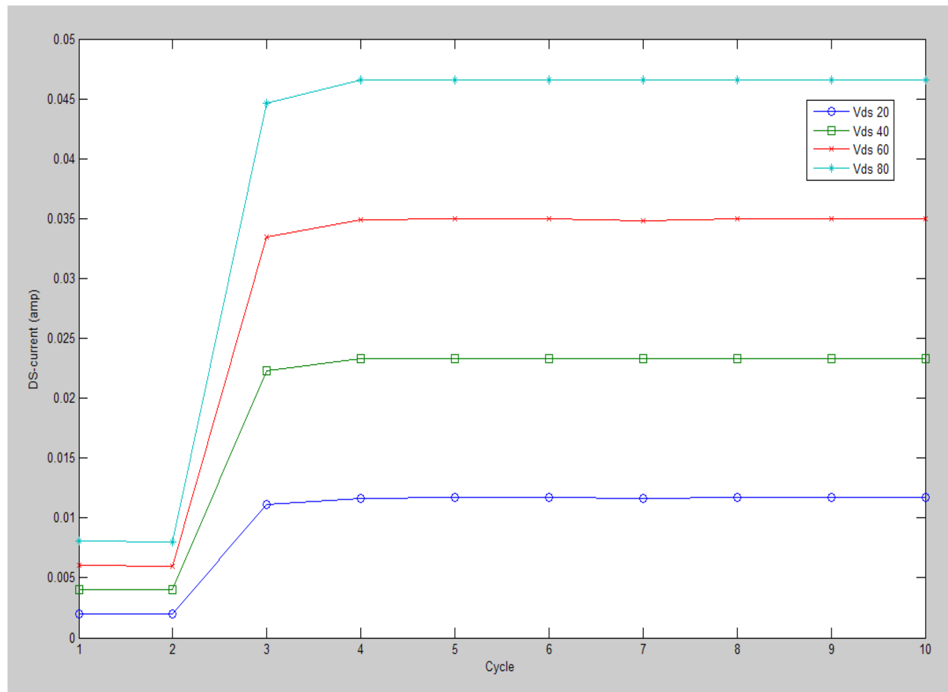


Figure 6.18: (drain-source current in amps) vs. cycles for MESFET device with 20, 40, 60, and 80 Vds (V)

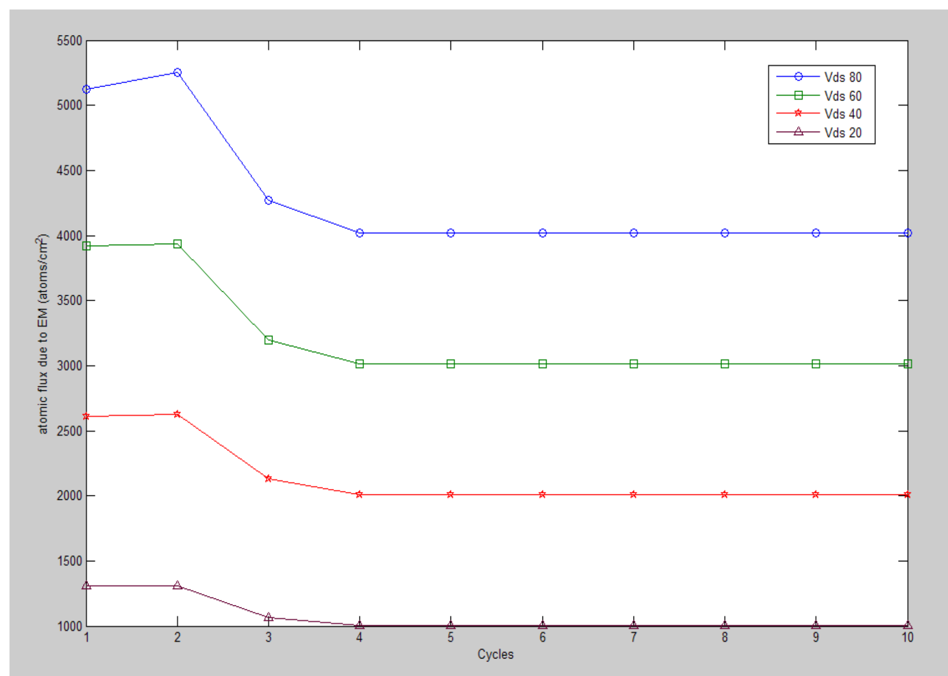


Figure 6.19: atomic flux due to electromigration vs. cycles under 20, 40, 60, and 80 (drain-source) voltage

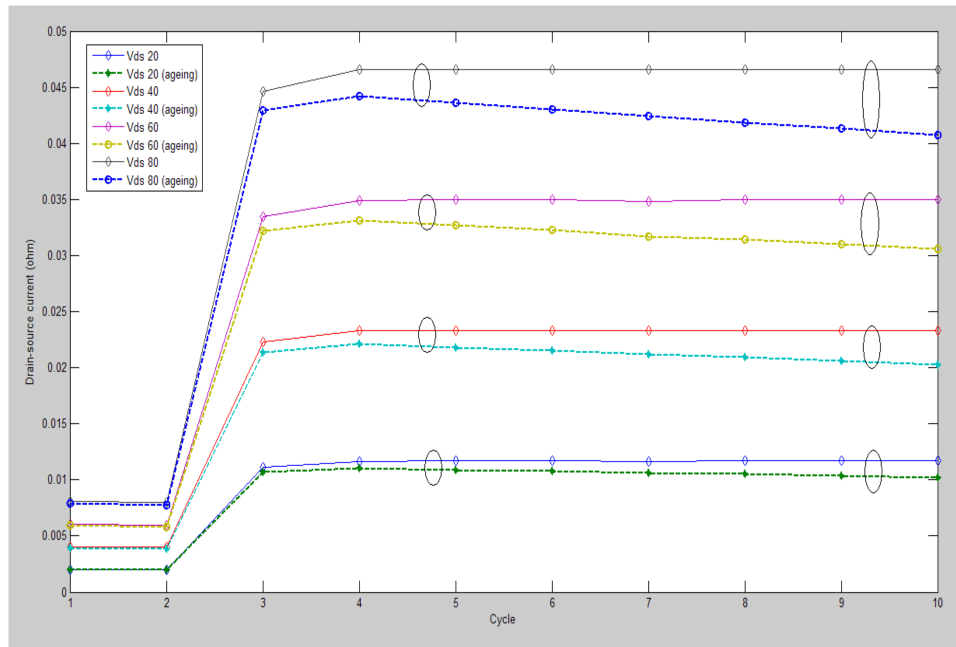


Figure 6.20: (drain-source current) Ids against time (cycles) for MESFET device with 20, 40, 60, and 80 Vds (V)

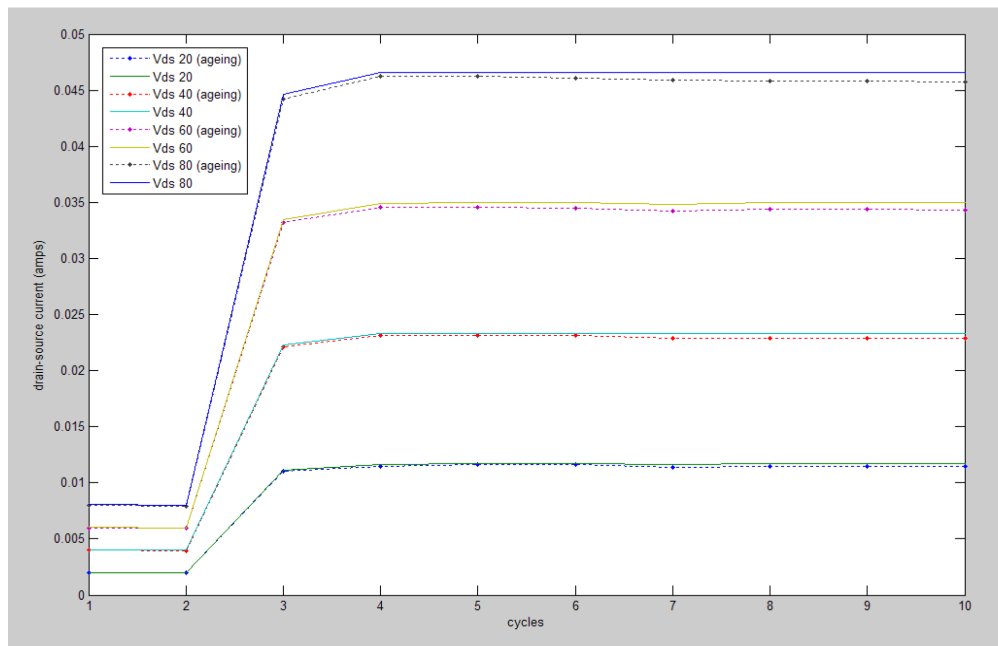


Figure 6.21: (drain-source current in amps) with ageing effects vs. cycles for MESFET device with 20, 40, 60, and 80 Vds (V), with average temperature increase by 5 degree Kelvin from the start temperature 273K

6.4. Degradation in MOSFET

In this section, the TLM solver has been validated with RF N-LDMOS device, by introducing TCT: thermal cycling test and transconductance in ageing measurement. The proposed test will subject the device to a cycle of stress conditions, in these cycling tests, the device is repeatedly put under electric and/or thermal overload over periods of time (subjecting the device to a repeated thermal overload over an extended period of time) [141]. As illustrated in Figure 6.22, consisting and starting with ambient temperature 273 K, then proceeding to cold (198K) then dwell time (44 seconds) to hot temperature (348K) for (90 seconds) for each cycle, as in [142]. The results are compared with results presented in [142] and [143], for the three values of Vds used as shown below in detail.

The device dimensions are taken from [142] as shown in Figure 6.24 in the XY plan, and the device main characteristics are: breakdown voltage 65V, output power 10 Watts, doping concentration for the drain and source are $1.0\times10^{20}\ cm^{-3}$ [144]. The model is divided into 70 nodes in x direction with 50 nodes in y direction, where each node size is ($0.1\times0.1\mu m$).

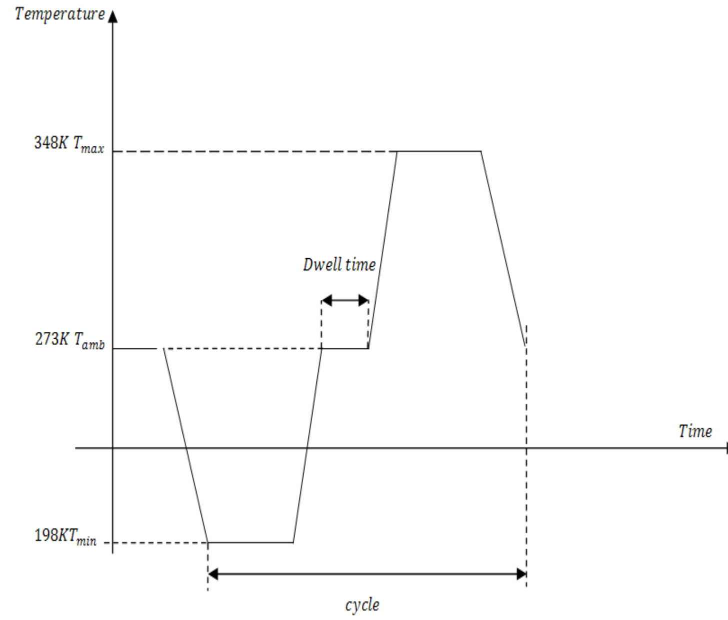


Figure 6.22: description for thermal cycle test

Figure 6.23 shows the relation between resistivity (R_s) for node n in source region and the drain-source current I_{ds}, where the transconductance for this node G_n can be expressed as follows.

$$G_n = \frac{\Delta I_{ds}}{\Delta V_{gs}} \tag{6.12}$$

For source region

$$\frac{\Delta V_s}{\Delta I_{ds}} = \frac{\Delta V_{gs}}{\Delta I_{ds}} + \frac{\Delta I_{ds} R_s}{\Delta I_{ds}} \tag{6.13}$$

Then R_s can be found from

$$\frac{1}{G_s} = \frac{1}{G_n} + R_s \tag{6.14}$$

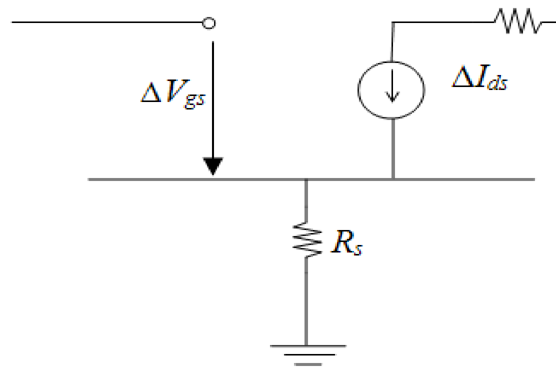


Figure 6.23: resistivity at node n in source region

Figure 6.25 shows the output characteristic for the device using the TLM solver with Vgs = 5.3V, both before and after the ageing test. The result shows a downward trend for the IV characteristic after the TCT due to an increase in resistivity and the threshold voltage, hence reduced electron mobility. The results from TLM model before ageing (green line) and after ageing (red line) were compared with measured data (blue line) from Belaid et al [142] when ATLAS SILVACO 2D simulation model was used.

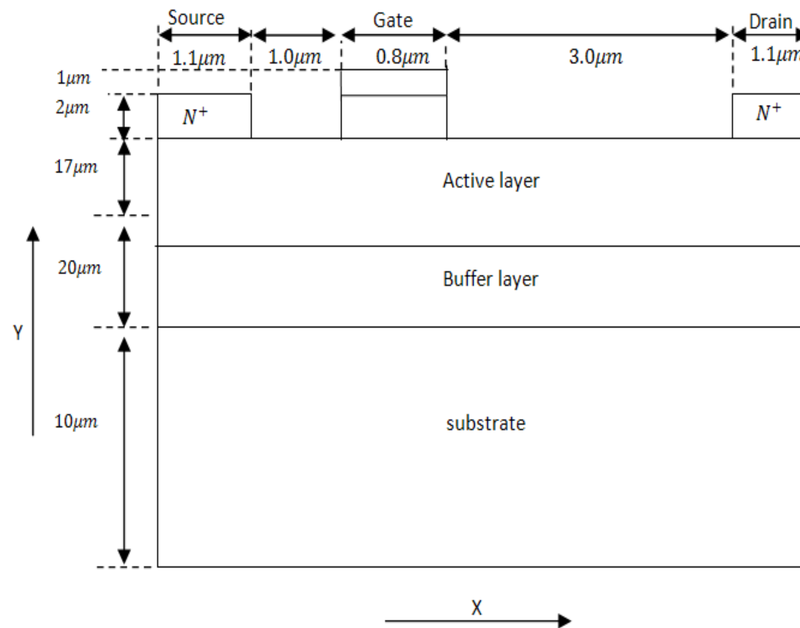


Figure 6.24: device structure in XY plane

In Figure 6.26 the TLM results are shown when the device was subjected to thermal stress test with Vgs=4.8V applied. This shows that the output characteristics from the TLM solver (red line) demonstrated comparable behaviour and shifts downward by 1% from the unaged data results (blue line). The comparison with measured results (green line) from [142] shows good agreement.

Figure 6.27, 5.8V was used as a new input voltage, the model demonstrated similar behaviour to SILVACO 2D simulator, were the results showed a drift in output characteristics by 5-7% from the original data generated from [142]. The total difference between the two approaches can be attributed to the use of different stress periods in the test conditions used in this approach to mimnize the numerical error that

could be caused by different time scales, hence reducing the transfer time that is needed for the device to reach the ambient degree before starting the new condition.

Breifly, the results obtained for the output charactristics for the three Vgs values are given in Figure 6.28 before and after the cycle thermal stress test. They highlight the shifts downward with variable rates rising with the higher gate-source voltage applied. The model results shows a reduction in the drain-current values caused by the thermal stress used which works together with the frequent updated for material resistivity for each node in the co-simulation process, to raise the threshold voltage and reduce electron mobility.

In the FET device, the transconductance parameter is the key factor in device reliability [58]. It was necessary to introduce this parameter in the TLM solver to develop the validation and to verify that the solver is able to deal with the device's parameter under various tests. Figure 6.29 combined with data in Table 6.1 shows the form of the relationship concluded for the transconductance parameter at different ageing tests with Vds=30mV and Vgs=4V. The results show good agreement with [143] findings. It can be observed that the general approach is the reduction in G_m values in the three tests, where the higher downward shift was with (Thermal Shock Tests) TST cold, starting at 273K and proceeding to 248K. While less reduction was observed for TST hot, which started at 273K and proceeding to 348K with a transfer time from cold to hot not exceeding 5 mintues. The TLM results were in good agreement with TST hot, as the variation ranging (0.5% - 1.0%), and (1.5% - 2.5%) with TST cold. The effect of reduction in transconductance value can be attiributed to an increase in resistivity of the drain-source region and a decrease in electron mobility.

These results allow some comparison between the test type and the amount of reduction in device functionality, where the thermal effect seems to be influential, and noticeable. This effect shows that it can form a combined load when it works with the electric voltage applied, confirming that any increase in the voltage applied may cause increases in the device internal temperature with different rates and that may elevate the failure rate, as shown in Figure 6.28 for three different applied voltages. Furthermore, the results from the transconductance in Figure 6.29 showed that there is a possiblity of establishing a relation between the aged parameters, the TLM parameters, and the ageing conditions by the updating mechanism for the material properties for each node, according to the stress temperature applied, which affects the resulted voltage and the current flow, hence the output characteristic for the device.

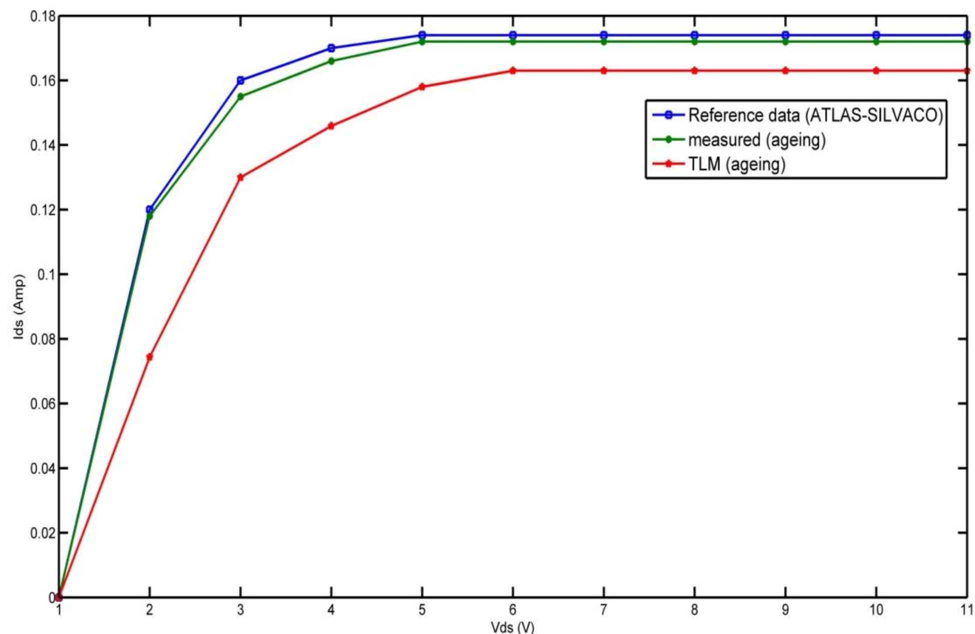


Figure 6.25: Output characteristics before and after ageing for TLM, with Vgs=5.3V

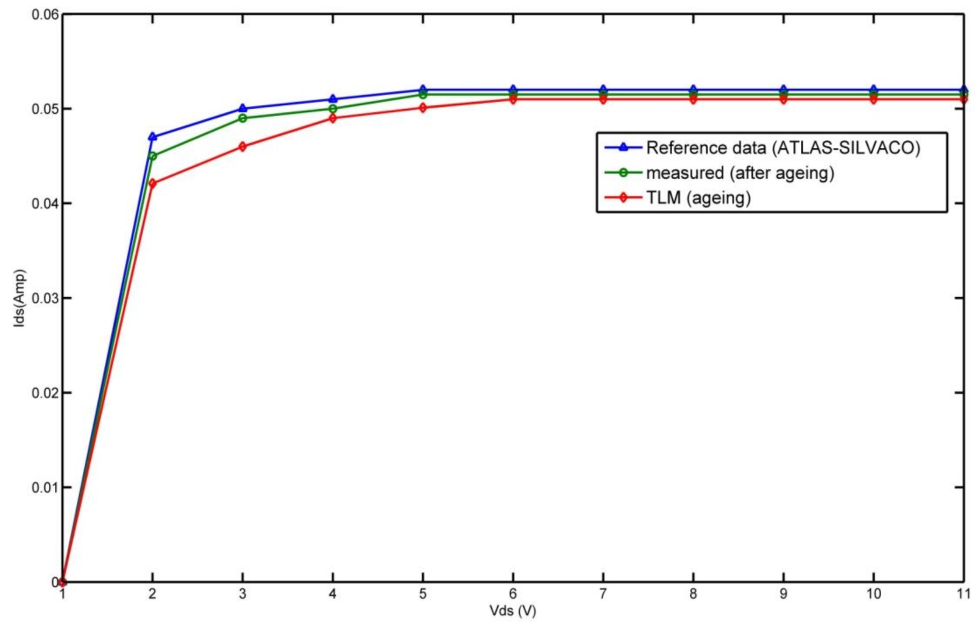


Figure 6.26: Output characteristic for RF LDMOS device before and after ageing, with Vgs=4.8 V

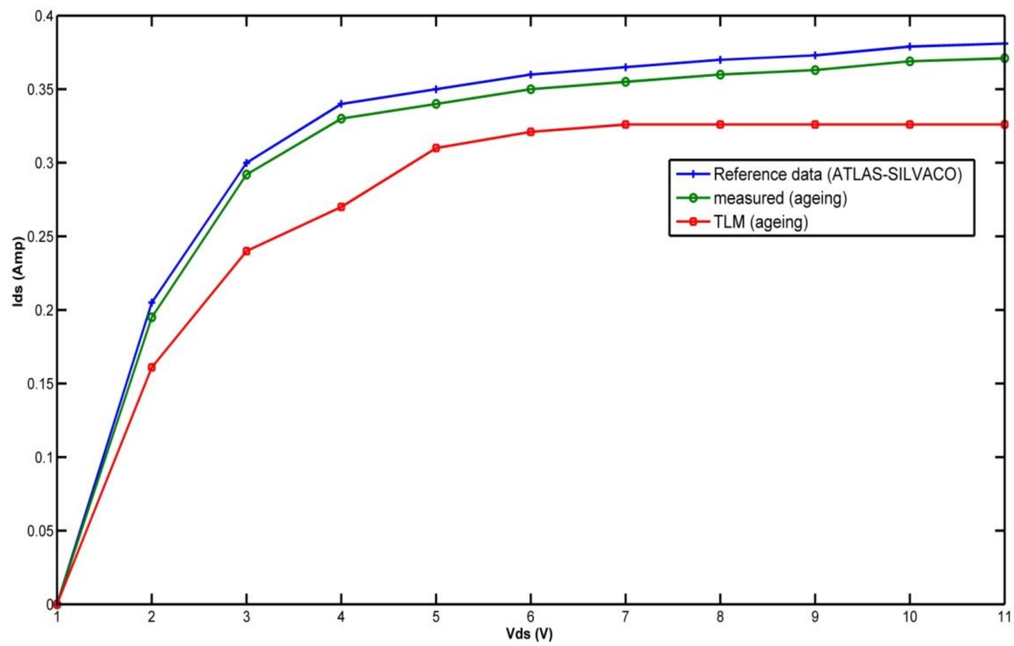


Figure 6.27: Output characteristic for RF LDMOS device before and after ageing, with Vgs=5.8 V

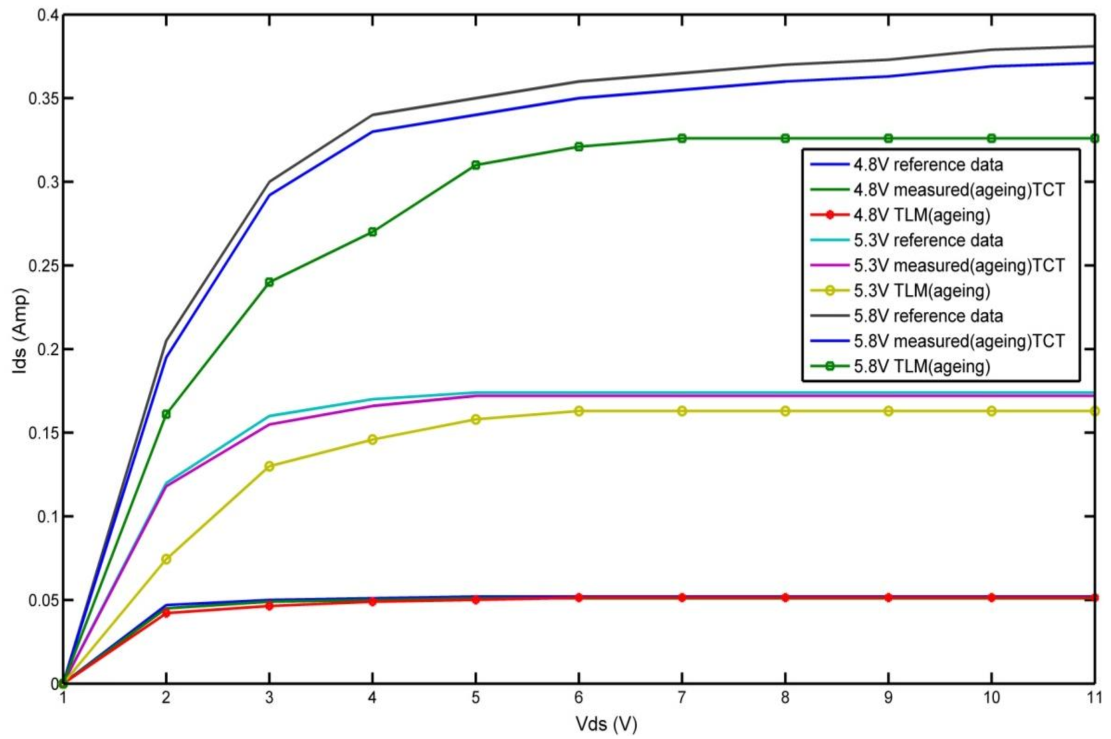


Figure 6.28: Output characteristic for RF LDMOS device before and after ageing, with Vgs=4.8V, 5.3V, and 5.8V

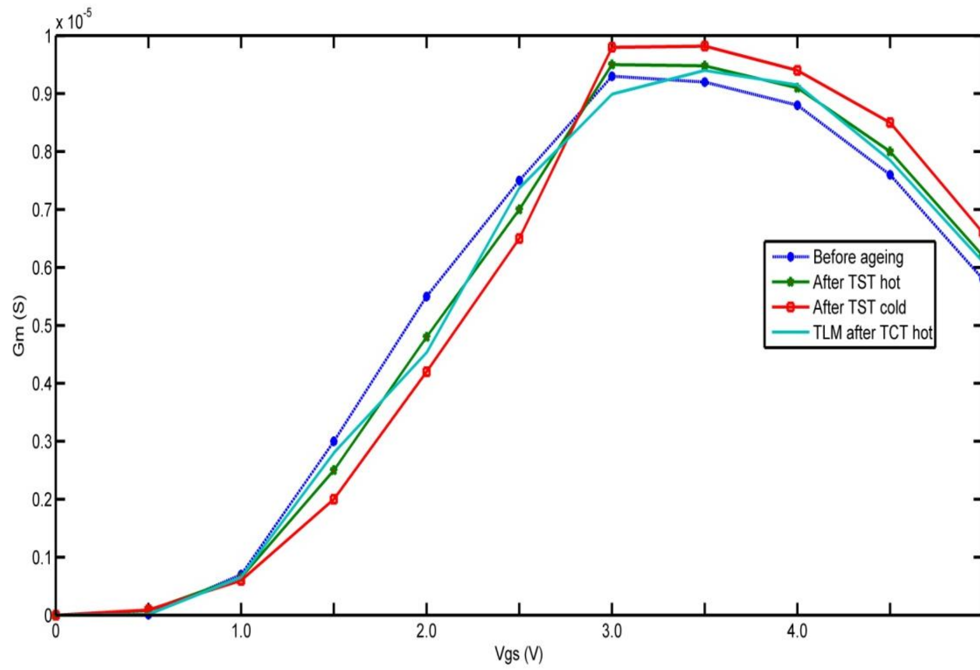


Figure 6.29: Transconductance results compared with [143] at different ageing conditions with Vds=30mV and Vgs=4V

Table 6.1: Transconductance values for the device in the four cases; fresh, TST hot, TST cold and TLM results

Fresh data	After-TST hot	After-TST cold	TLM-TCT
0.00E+00	0.00E+00	0.00E+00	0.00E+00
1.00E-08	8.00E-08	9.00E-08	1.00E-07
7.00E-07	6.50E-07	6.00E-07	6.55E-07
3.00E-06	2.50E-06	2.00E-06	2.81E-06
5.50E-06	4.80E-06	4.20E-06	4.51E-06
7.50E-06	7.00E-06	6.50E-06	7.34E-06
9.30E-06	9.50E-06	9.80E-06	8.96E-06
9.20E-06	9.48E-06	9.82E-06	9.40E-06
8.80E-06	9.10E-06	9.40E-06	9.22E-06
7.60E-06	8.00E-06	8.50E-06	7.79E-06
5.80E-06	6.20E-06	6.60E-06	6.10E-06

6.5. Conclusion

A generic approach to semiconductor device ageing was introduced into the ageing domain, by using a two dimensional TLM hybrid solver.

This was applied to two examples structures: SiC MESFETs and LDMOS transistors. This approach provides a simple technique in MESFETs to model the device parameters under influence of temperature rise and anticipated ageing behaviour when the probability of electromigration is taken into account. Acceleration factor is shown under stress conditions, and the mean time to failure indicates an obvious reduction in device's life time against temperature increases. Moreover, the model in the LDMOS case provides a simple technique to model the device parameters under customized thermal acceleration test. The model demonstrated good agreement with previous publications.

The TLM presents a potentially useful additional tool for ageing analysis to assist in the understanding and the prediction of phenomena that contribute to the aging and stressing of semiconductor devices, where the results showed device parameters such as: transconductance and resistance, can be used to evaluate the device reliability; and provide a link to be established between the electric parameter drift and the applied ageing.

Chapter 7 Conclusions and Suggestions for Future Work

Summary

The research presented in this thesis is aimed at exploring additional capability and initiate the TLM method to new applications, i.e., nanotechnology. Furthermore, to address the problem of ageing in semiconductor devices by counting ageing as a key function embedded in the hybrid cycle for TLM solver.

In this chapter, a description of the outcomes resulting from the study of nonlinear behaviour of semiconductor devices, is given in the first section. In section two, a description of the results obtained from the 1D solver for silicon nanowires is presented together with the conclusion from adopting a co-simulation approach in nanowires. Section four, describes the main conclusion from the hybrid model for SiC MESFET's device, as well as the thermal behaviour.

Section five presents the conclusions from studying the ageing problem and the main factors affecting device reliability and the results gathered from including the electromigration, thermomigration mechanism and the repeated thermal stress test in the TLM solver. Finally suggestions for future work are summarised in section six.

7.1. Nonlinearity using TLM

Based on the equivalent principle, the proposed 2D TLM solver was successful in finding a simple means to simulate nonlinearity, and presents a set of equivalences between the semiconductor device parameters and the circuit parameters for 2D model. This contribution will simplify the determination of the effects of nonlinearity in semiconductor devices.

7.2. Modelling thermal radiation in nanowires

One of the prominent results from this thesis is the competence to model thermal radiation aspect in nanowires. This has been achieved by introducing a shunt conductance in the one dimensional TLM node structure. The application to vapor-liquid-solid (VLS)-grown, and electroless-etching (EE)-grown nanowires grown nanowires was examined. The models were well behaved and demonstrated good agreement with a previous publication [97]. In the meantime, the results constructed for the first step to address the heat diffusion problem for future semiconductor devices using the TLM method, and provide a good tool that can be used to deal with ageing problems caused by thermal factors.

7.3. Co-simulation technique

A hybrid electro-thermal model was presented using the TLM method, to investigate the electrical and thermal behaviours of 1D and 2D variants. The combined model offers more information in both solvers at any stage during the simulation. The material resistivity is updated frequently with temperature variation, this resulted in noticeable changes in device temperature with different rates.

7.4. Hybrid 2D model for SiC-MESFET

To link the forgoing achievements, a 2D model has been proposed for silicon carbide 4H-MESFET to investigate the electrical and the thermal behaviour. The process is built on an interlock of both effects together. Power dissipation was employed as a common element between the two simulation schemes. Buffer layer thickness showed visible effects on device temperature. Moreover, the substrate layer plays a noticeable effect in the channel temperature confirming the previous finding of Song et.al[49]. This model provides an appropriate tool for the electrical and the thermal analysis of semiconductor devices can be used to deal with degradation parameters (electromigration) in ageing.

7.5. Modelling the ageing phenomenon using TLM method

A new contribution has been presented by employing the TLM method for the first time in the study of ageing problems in semiconductor devices. The choice of electromigration and thermomigration mechanisms were based on a probability base of migration of the metal atoms to the active region causing an increase in resistivity, reduced current flow, and ending with a decline in device *IV* characteristic. Moreover, the proposed solver has been used in an RF_LDMOS device to investigate the thermal acceleration test on device performance through a customised TCT (repeated thermal stress), the results came in agreement with previous publication [143] findings, as another way of validation.

7.6. Suggested future work

The presented work in this thesis has built the basis for the TLM method in the ageing field for semiconductor devices, and suggested ways of extending the work to 3D models. The hybrid solver enables the analysis of the ageing effects in each individual section of the model, based on the signals from the nodes. Also, in the TLM solver, the possibility to introduce different ageing mechanisms such as Hot-Carrier, and dielectric-breakdown represents an opportunity for new applications with certain modifications. Several further investigations would be beneficial for a fuller understanding of the ageing phenomenon modelling in the TLM method. However, there are some questions which arise, where further work is needed.

- To investigate the ageing in nanoscale applications, a reduction in semiconductor nanowires performance would be expected.
- Exploring the volume of power dissipated during the degradation.
- To study the coupling between the TLM method and other simulation methods as another way to investigate the benefits from using a hybrid approach. This will provide another opportunity to address the ageing problem by combined solvers.
- To apply the proposed engine into a 3D model which will reveal more facts about the first regions which experience high temperature stress. This will enable designers to find effective solutions in a short period.
- To expand the implementation devices to include photocells, photodiodes, and laser diode, helping in designing a TLM solver that can deal with a wide range of semiconductor devices.

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Appendix

I. TLM HYBRID SOLVER_E

```
#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <fstream>
#include <math.h>
#include <stdlib.h>
#define Delta_L
#define X_max
#define Y_max
#define X
#define Y
#define IMPULSE_INPUT 0
#define CONTINUOUS_INPUT 1
#define SINE_INPUT 2
#define COSINE_INPUT 3
#define NO_MORE_INPUTS (-1)
#define FILENAMELEN 30
#define r 5                          //Represent maximum number of rows in matrix //
#define c 5                          //Represent maximum number of Columns in matrix //
#define P 5                          //Is the number of ports foe each node //
#define dy                           //Dimension for the node in y direction in block of space //
#define dx                           //Dimension for the node in x direction in block of space
#define MAX_INPUT_POINTS 10          //Arbitrary maximum number of input points.
#define C_light 2.997925E+08         //Speed of light in vacuum in m/sec
//*************************************************************************************
const float PI (3.1415926536);       //PI value
const float epsilon_0 = 8.854E-12;   //Vacuum permittivity  farad/meter
const float Mu_0 = 4*PI*1.0E-07;     //Vacuum permeability  henry/meter
const float q = 1.6E-19;             //Electrons charge in coulombs
const float Blotz_man= 8.63e-05;     //Blotz-man constant
const float E_a=0.7;                 //Activation energy
const float diffusivity=1.7;         //Diffusivity of silicon
const float effective_ch=1;
//*******************************************************************************//
double Ref,Ref2,Ref3,Ref4;           //  Reflection coefficients
float Vi_elm[X][Y][P]={};            //  Incident voltage in electromagnetic
float Vr_elm[X][Y][P]={};            //  Reflected voltage in electromagnetic
float Vn_elm[X][Y]={};               //  Nodal voltage in electromagnetic model
float g_n[X][Y]={};                  //  Transconductance for each node-ageing function
float delta_V[X][Y]={};              //  Difference between two node in voltages
```

```
float delta_I[X][Y]={};                       // Difference between two node in voltages
float R_s[X][Y]={};                           // Resistivity of the gate-source
float R_d[X][Y]={};                           // Resistivity of the drain-gate
float L,C,Z,Z_c,C_c,Y_s,T,Y_adm,I,;           // TLM model parameters
float Mu_r,epsilon_r,Area,R;                  // Material parameters
float J_electro_mig,G_s,g_m;                  // Ageing parameters
void vacuum_value (void);                     // Function to specify the vacuum regions
void set_Vds_stimulus(void);                  // Function to set voltage applied for D/S
void excitation__input(void);                 // Function to specify excitation type and place
void source_input(void);                      // Function for source type and value
void test_files (void);                       // Function to test files
void read_regions(void);                      // Function to read regions in the device
void ageing_calc(float *Vn_elm,int x,int y);  // Function to calculate ageing in the device
void g_m_transconductance(int x, int y);   // Function to calculate transconductance for the device
void set_Vgs_stimulus(void);                  // Function to read Vgs value
void reflection_coeff(void);                  // Function to read reflection coefficients
void compute_nodal_voltage(float *Vi_elm, int x, int y);     //  Function to calculate nodal voltage
void readinput(int i, float Y_s);                            //  Function to read material properties
void M_Matrix(float *Vi_elm,float *Vr_elm,float S[r][c]);    //  Function for matrix multiplication
void _connect (float *a , float *b);                         //  Function for connect phase stage
void connect_phase(void);                                    //  Function for connect stage
float drain_resistivity();
float source_resistivity();
//******************************************************************************************
typedef struct {
                float epsilon_r;
                float Mu_r;
                float Y_s;
                float Y_adm;
                float R;
                float doping;
                float mobility;
                float Z_c;
                float G_s;
                float density;
                }materials_type;
materials_type material[X_max][Y_max];
materials_type *this_material;                // Points at material[x][y];
typedef struct {
                float S[r][c];
                         }s_matrix;
typedef struct {
                int x;
                 int y;
                double port_values[P];
                } dc_point_input;

s_matrix scatter_phase(int x,int y);            //  Function required to modify the scatter matrix //
s_matrix s_m;
```

```
int n_impulse_inputs = 0;
int n_continuous_inputs = 0;
int source;
double a_voltage;
void test_corner_of_S(int x, int y, s_matrix sm );
dc_point_input impulse_input_points[MAX_INPUT_POINTS];
dc_point_input continuous_input_points[MAX_INPUT_POINTS];
dc_point_input *the_input;
// Input files and the generated excel and txt files from each cycle
FILE *fp;
FILE *infp     = fopen("device_structure.txt","r");
FILE *outfp1 = fopen("power_loss_E1.txt","w");
FILE *outfp2 = fopen("result_E1_Volt.csv","w");
FILE *outfp3 = fopen("last_timestep_E_1.txt","w");
FILE *outfp4 = fopen("EM_1.csv","w");
FILE *outfp5 = fopen("Current_E_1.csv","w");
FILE *outfp6 = fopen("EM_E_1.csv","w");
FILE *statsfp = NULL;

//********************************** Main source   ********************************
int  main ()
{
  float Ez_plane[X_max][Y_max];
  float Z_c;
  float Mu;
  int Regions,n,i,K,x,y,p,excitation_type;
  float dt,Power,R;
//***********************************************************************************
     test_files ();                          // tests for files
     excitation__input();                    // read excitation co-ordinates
     reflection_coeff();                     // setup boundary conditions
     read_regions();                         // reading material properties
 //*******************************     starting scatter phase *******************************
for(K=0;K<MK;K++)
                        {source_input();
                                    for(x=0;x<X_max;x++){
                                  for(y=0;y<Y_max;y++){
                        this_material = &material[x][y];
                                          Mu = this_material->Mu_r * Mu_0;
                                          Z=sqrt((Mu)/(epsilon_0*this_material->epsilon_r));
                                          R =this_material->R = 1/(q*this_material->doping *
                                          this_material->mobility);
                                   Y_s = this_material->Y_s = 4* (( this_material->epsilon_r-1)/Z);
                                           this_material->G_s=(1/R)*dx*Z;
                                          G_s=this_material->G_s;
                                          Y_adm =this_material->Y_adm = (4+ Y_s+G_s);
                                           C_c=(epsilon_0*(this_material->epsilon_r-1)*dx);
                                            Z_c=dt/(2*C_c);
```

```
// Starting scatter phase as the first part of TLM method //
s_m = scatter_phase(x,y);
test_corner_of_S(x,y,s_m);
M_Matrix(&Vi_elm[x][y][0],&Vr_elm[x][y][0], s_m.S);
compute_nodal_voltage(&Vi_elm[x][y][0],x,y);
vacuum_value ();
set_Vds_stimulus();
set_Vgs_stimulus();
I=(2*Vi_elm[x][y][0]/(R+Z))+(2*Vi_elm[x][y][1]/(R+Z))+(2*Vi_elm[x][y][2]/(R+Z))+(2*Vi_elm[x][y][
3]/(R+Z))+ (2*Vi_elm[x][y][4]/Z_c);
Power=(I*I*R);
I_plane[x][y] = I;
drain_resistivity();
source_resistivity();
g_m_transconductance(x,y);
ageing_calc(&Vn_elm[x][y],x,y);
fprintf (outfp1," %g \n",Power);
fprintf (outfp7," %g, ", g_m);
fprintf (outfp4," %g, ", J_electro_mig);
fprintf (outfp5," %g, ",I_plane[x][y]);
if (K==(MK-1)){
fprintf(outfp3,"%g \n",Vn_elm[x][y]);}
                                        else;
                                            } fprintf(outfp2, "\n");
                                              fprintf(outfp4, "\n");
                                              fprintf(outfp5, "\n");
                                              fprintf(outfp6, "\n");
                                              fprintf(outfp7, "\n");
} fprintf(outfp2,"k=%d\n",K);
  fprintf(outfp4,"k=%d\n",K);
  fprintf(outfp5,"k=%d\n",K);
  fprintf(outfp6,"k=%d\n",K);
  fprintf(outfp7,"k=%d\n",K);

connect_phase( );
}
return(0);
}
   //****************************** End of the main source          **********************
  //******************************** Sub functions                   ***********************
 //******************************** 1- Matrix Multiplication function ***********************

void M_Matrix(float *Vi_elm,float *Vr_elm, float S[r][c])
        {
        int i,k;
        for(i=0;i<r;i++){
                    Vr_elm[i]=0;
                    for(k=0;k<c;k++){
                                Vr_elm[i]+=(S[i][k]*Vi_elm[k]);
```

```
                                            }
                                        }
                                        return;
 }

// ******************************** 2-Reading input    ******************************
void readinput(int i, float Y_s)
 {
  char string[50];
  int success;
  success=get_named_string("material", string);
  if (success==1)
                  {
                   printf("Warning the materials name failed");}
char xmin_keyword[]="xmin";
char ymin_keyword[]="ymin";
char xmax_keyword[]="xmax";
char ymax_keyword[]="ymax";
char density_keyword[]="density";
char epsilon_r_keyword[]="epsilon_r";
char Mu_r_keyword[]="Mu_r";
char doping_keyword[]="doping";
char mobility_keyword[]="mobility";
char sigma_keyword[]="sigma";
int x,y,xmin,xmax,ymin,ymax;
float density,C,epsilon_r,Mu_r,doping,mobility;
Area=dx*dy;
// These define the limits of the region for this block of material.
   xmin=get_named_int(xmin_keyword);
   ymin=get_named_int(ymin_keyword);
   xmax=get_named_int(xmax_keyword);
   ymax=get_named_int(ymax_keyword);

// These define the materials properties //
   density=get_named_double(density_keyword);
   epsilon_r=get_named_double(epsilon_r_keyword);
   Mu_r=get_named_double(Mu_r_keyword);
   doping=get_named_double(doping_keyword);
   mobility=get_named_double(mobility_keyword);
   sigma=get_named_double(sigma_keyword);

   for(x=xmin;x<xmax;x++)
                              {
                              for(y=ymin;y<ymax;y++)
                                                {
                                                material[x][y].epsilon_r= epsilon_r;
                                                material[x][y].Mu_r=Mu_r;
                                                material[x][y].density=density;
                                                material[x][y].doping=doping;
```

```
                                        material[x][y].mobility=mobility;
                                       material[x][y].sigma=sigma;
                                        }
                                        }printf("readinput done\n");
                                        return ;
 }

//*********************** 3- Function to read reflection coefficients ***************************
 void reflection_coeff()
 {
 char Ref_keyword[]="Ref";
 char Ref2_keyword[]="Ref2";
 char Ref3_keyword[]="Ref3";
 char Ref4_keyword[]="Ref4";
 Ref=get_named_double(Ref_keyword);
 Ref2=get_named_double(Ref2_keyword);
 Ref3=get_named_double(Ref3_keyword);
 Ref4=get_named_double(Ref4_keyword);
}
//*************************** 4- Function to read regions  *********************************
 void read_regions()
{
 int Regions,i;
 char Regions_keyword[]="Regions";
 Regions=get_named_int(Regions_keyword);
 for(i=0;i<Regions;i++){
                          readinput(i,Y_s);
                         }}
//********************** 5- Function to set_Vds_stimulus ********************************
void set_Vds_stimulus()
{
int x,y ;
int xmin,xmax,ymin,ymax,p,xmin1,xmax1,ymin1,ymax1;
xmin=0;xmax=10;ymin=47;ymax=49;
xmin1=58,xmax1=70,ymin1=47,ymax1=49;
            for(x=xmin;x<xmax;x++)
                                    {
                                    for(y=ymin;y<ymax;y++)
                                            {
                                           Vi_elm[x][y][2]=30e-03;
                                                                            }
                                                                            }
for(x=xmin1;x<xmax1;x++)
                              {
                              for(y=ymin1;y<ymax1;y++)
                              {
                               Vi_elm[x][y][2]=0;
                                          }
                                          }
```

```
}

//**************************** 8- Function to set_ ageing_cal***************************
void ageing_calc(float *Vn_elm,int x,int y)
 {
  float j,AF,T_use,T_stress,Part_1,Part_2,MTTF,A,j_MTTF,n=1;
  j=I/Area;
  Part_1= material[x][y].doping*(diffusivity/(Blotz_man*273));
  Part_2= effective_ch*q*material[x][y].R*j;
  J_electro_mig=Part_1*Part_2;
  MTTF=A/(pow(j,n))* exp(E_a/(Blotz_man*T_use));
  AF=exp((E_a/Blotz_man)*(1/T_use-1/T_stress));
  fprintf (outfp6," %g, ",J_electro_mig);
  return ;
  }
//************************* 9- Function to set_Vgs_stimulus ********************************
void set_Vgs_stimulus()
 {
 Vi_elm[20][49][2]=4;Vi_elm[21][49][2]=4;Vi_elm[22][49][2]=4;Vi_elm[23][49][2]=4;
 Vi_elm[24][49][2]=4;Vi_elm[25][49][2]=4;Vi_elm[26][49][2]=4;Vi_elm[27][49][2]=4;
 }
//********************** 10-Transconductance function ******************************
void g_m_transconductance(int x,int y)
  {
  delta_I[x][y]=I_plane[x][y]-I_plane[x+1][y];
  delta_V[x][y]=Vn_elm[x][y]-Vn_elm[x+1][y];
  if (delta_V[x][y]==0){g_n[x][y]=0;
  }else
  g_n[x][y]=delta_I[x][y]/delta_V[x][y];
  if (R_s[x][y]==0){R_s[x][y]==0;
  }else
  g_m=g_n[x][y]/(1+(g_n[x][y]* R_s[x][y]));
  return;
  }
//********************** 11- Update source-resistivity **********************************
float source_resistivity()
  {
intxmin=0,xmax=11,ymin=46,ymax=49;
        for(x=xmin;x<xmax;x++)
                    {
                    for(y=ymin;y<ymax;y++)
                    {
                     R_s[x][y]= R;
                    } }
 return  R_s[x][y];
  }
//********************** 12- Update source-resistivity ****************************
 float drain_resistivity()
  {
```

```
int xmin1,xmax1,ymin1,ymax1;
 xmin1=58,xmax1=70,ymin1=46,ymax1=49;
   for(x=xmin1;x<xmax1;x++)
                              {
                              for(y=ymin1;y<ymax1;y++)
                              {
                             R_d[x][y]=R;
                                           }
                                           }
return R_d[x][y];
}

//******************** 13- Function to compute nodal voltage ******************************
 void compute_nodal_voltage(float *Vi_elm, int x, int y)
  {
   float current,conductance,port_1,port_2,port_3,port_4,port_5,R;
   port_1 =(2*Vi_elm[0])/(R+Z);
   port_2 =(2*Vi_elm[1])/(R+Z);
   port_3 =(2*Vi_elm[2])/(R+Z);
   port_4 =(2*Vi_elm[3])/(R+Z);
   port_5 =(2*Vi_elm[4]*Y_s);
   current =port_1+port_2+port_3+port_4+ port_5;
   conductance =Y_adm;
   Vn_elm[x][y]=current/conductance;
   return;
   }

//************************ 14- Function scatter matrix  **************************
s_matrix scatter_phase(int x,int y)
{
  int i,j;
  float tmp,Y_adm;
  s_matrix s_m;
  Y_s=material[x][y].Y_s;
  Y_adm=material[x][y].Y_adm;
  for (i=0;i<r;i++)
                    {
                    for(j=0;j<c;j++)
                                    {
                                    s_m.S[i][j]=(2.0/Y_adm);
                                                            }
                                                            }
  for(i=0;i<=3;i++)
                    {
                    s_m.S[i][i]= tmp = (2.0-Y_adm)/Y_adm;
                    s_m.S[r-1][i]=(2.0*Y_s)/Y_adm;
                    }
                     s_m.S[r-1][c-1]=((2.0*Y_s)-Y_adm)/Y_adm; return s_m;}
```

```
//************************** 15- Function for connect phase ** ******************************
void _connect (float *a , float *b)
        {
        *a=*b;
         return;
        }
//********************** 16- function to exclude vacuum regions  ****************************
void vacuum_value ()
{
int x,y ;
int xmin,xmax,ymin,ymax,p,xmin1,xmax1,ymin1,ymax1,
xmin2,xmax2,ymin2,ymax2,xmin3,xmax3,ymin3,ymax3;
 xmin=11;xmax=20;ymin=47;ymax=50;
xmin1=28,xmax1=58,ymin1=47,ymax1=50;xmin2=0,xmax2=21,ymin2=49,ymax2=50;
xmin3=28,xmax3=70,ymin3=49,ymax3=50;
        for(x=xmin;x<xmax;x++)
                        {
                        for(y=ymin;y<ymax;y++)
                        {
                        for(p=0;p<P;p++){ Vi_elm[x][y][p]=0;
                                                    }
                                                    }
                                                    }
  for(x=xmin1;x<xmax1;x++)
                     {
                     for(y=ymin1;y<ymax1;y++)
                     {
                     for(p=0;p<P;p++){ Vi_elm[x][y][p]=0;
                                                  }
                                                  }
                                                  }
 for(x=xmin2;x<xmax2;x++)
                    {
                    for(y=ymin2;y<ymax2;y++)
                    {
                    for(p=0;p<P;p++){ Vi_elm[x][y][p]=0;
                                                }
                                                }
                                                }
for(x=xmin3;x<xmax3;x++)
                    {
                     for(y=ymin3;y<ymax3;y++)
                    {
                    for(p=0;p<P;p++){ Vi_elm[x][y][p]=0;
                                                 }
                                                 }
```

```
                                    }


  return;
}

//****************** 17- function connect-phase ******************************
void connect_phase(void)
        {
        int x,y;
        for (x=0;x<X_max;x++){
                        for (y=0;y<Y_max;y++)
                                {
 if( y>0 && x>0 && x<(X_max-1)&& y<Y_max-1)
                                {
                                 _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
                                 _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
                                _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
                                _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
                                 }
 if((y==0)&&(x<X_max-1))
                    {
                     if(x==0)
                         {
                          _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
                          _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
                          Vi_elm[0][0][1]=Ref2*(Vr_elm[0][0][1]);
                          Vi_elm[x][y][0]=-1*(Vr_elm[x][y][0]);
                          }
 else
    {
        Vi_elm[x][y][0]=-1*(Vr_elm[x][y][0]);
        _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
         _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
         _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
        }
        }
if (x==0 && y>0 && y<Y_max-1)
                       {
                          _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
                          Vi_elm[x][y][1]= Ref2 * Vr_elm[x][y][1];
                          _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
                          _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
                          }
if((y==(Y_max-1))&&(x<X_max))
                          {
                          if (x==0)
                          {
                          Vi_elm[x][y][1]=Ref2*Vr_elm[x][y][1];
```

```
                                        Vi_elm[x][y][2]=-1*Vr_elm[x][y][2];
                                        }
else{
    _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
   }
   if(x==X_max-1)
            {
            Vi_elm[X_max-1][Y_max-1][3]=Ref4*Vr_elm[X_max-1][Y_max-1][3];
             Vi_elm[X_max-1][Y_max-1][2]=-1*Vr_elm[X_max-1][Y_max-1][2];
             }else{
            _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
            Vi_elm[x][y][2]=Ref3*Vr_elm[x][y][2];
            _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
            }
            }
  if((y<Y_max-1)&&(x==(X_max-1)))
                                         {
                                        Vi_elm[x][y][3]=Ref4*Vr_elm[x][y][3];
                                        _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
                                        _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
                                         _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
   if(y==0)
            {
            Vi_elm[x][y][0]=-1*Vr_elm[x][y][0];
            }
            }
            }
      }
return;
}
//*******************18- function to read int type  ***** **********************************
int get_input_type()
{
 char keyword[186];
 fscanf(infp,"%s",&keyword[0]);

 if((keyword,dc_input_keyword)==0){
                                     printf("DC INPUT");
                                     return CONTINUOUS_INPUT;
                                      }
 if((keyword,impulse_input_keyword)==0) {
                                     printf("IMPULSE INPUT");
                                     return IMPULSE_INPUT;
                                       }
 if((keyword,no_more_input_keyword)==0){
                                     printf("INPUTS DONE");
                                     return NO_MORE_INPUTS;
                                     };
 return -1;
```

```
  }

//****************19- function to read string character *************************************
int get_named_string(char *expected_keyword, char *string)
{
  char keyword[186];
  fscanf(infp,"%s",&keyword[0]);
  if(stricmp(keyword,expected_keyword)==0)
                                        {
                                          fscanf(infp,"%s",string);
                                          printf("%s :%s\n",expected_keyword,string);
                                          } else
//**************** 20- function to test corner of the matrix ******************************
void test_corner_of_S(int x, int y, s_matrix sm )

{

  float Y_adm, Y_s;expected;

  Y_s =(material[x][y].Y_s);

  Y_adm =(material[x][y].Y_adm);

  expected = (((2*Y_s)-Y_adm)/Y_adm);

  if ((sm.S[4][4] - expected) > 0.00001)

    {exit(-1);

            }

            return;}

int vertex_index(int x, int y)

            {return (x * Y_max) + y + 1;

            }

//***************************************************************************//
```

II. TLM HYBRID SOLVER_TH

```
#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <fstream>
#include <math.h>
#include <stdlib.h>
#define X_max
#define Y_max
#define X
#define Y
#define IMPULSE_INPUT 0
#define CONTINUOUS_INPUT 1
#define SINE_INPUT 2
#define COSINE_INPUT 3
#define NO_MORE_INPUTS (-1)
#define FILENAMELEN 30
#define r 5                          //Represent maximum number of rows in matrix //
#define c 5                          //Represent maximum number of Columns in matrix //
#define P 5                          //Is the number of ports foe each node //
#define dy                           //Dimension for the node in y direction in block of space //
#define dx                           //Dimension for the node in x direction in block of space
#define MAX_INPUT_POINTS 10          //Arbitrary maximum number of input points.
#define C_light 2.997925E+08         //Speed of light in vacuum in m/sec
//*********************************************************************************
const float PI (3.1415926536);       //PI value
const float epsilon_0 = 8.854E-12;   //Vacuum permittivity  farad/meter
const float Mu_0 = 4*PI*1.0E-07;     //Vacuum permeability  henry/meter
const float q = 1.6E-19;             //Electrons charge in coulombs
const float Blotz_man= 8.63e-05;     //Blotz-man constant
const float E_a=0.7;                 //Activation energy
const float diffusivity=1.7;         //Diffusivity of silicon
const float effective_ch=1;
//***************************************************************************//
double Ref,Ref2,Ref3,Ref4;        //  Reflection coefficients
float Vi_elm[X][Y][P]={};         //  Incident voltage in electromagnetic
float Vr_elm[X][Y][P]={};         //  Reflected voltage in electromagnetic
float Vn_elm[X][Y]={};            //  Nodal voltage in electromagnetic model
float g_n[X][Y]={};               //  Transconductance for each node-ageing function
float delta_V[X][Y]={};           //  Difference between two node in voltages
float delta_I[X][Y]={};           //  Difference between two node in voltages
float R_s[X][Y]={};              //   Resistivity of the gate-source
float R_d[X][Y]={};               // Resistivity of the drain-gate
```

```
float L,C,Z,Z_c,C_c,Y_s,T,Y_adm,I,;          // TLM model parameters
float Mu_r,epsilon_r,Area,R;                 // Material parameters
float J_electro_mig,G_s,g_m;                 // Ageing parameters
void vacuum_value (void);                    // Function to specify the vacuum regions
void set_Vds_stimulus(void);                 // Function to set voltage applied for D/S
void excitation__input(void);                // Function to specify excitation type and place
void source_input(void);                     // Function for source type and value
void test_files (void);                      // Function to test files
void read_regions(void);                     // Function to read regions in the device
void ageing_calc(float *Vn_elm,int x,int y); // Function to calculate ageing in the device
void g_m_transconductance(int x, int y);   // Function to calculate transconductance for the device
void set_Vgs_stimulus(void);                 // Function to read Vgs value
void current_flow(void);                     // Function to void current flow in vacuum region
float gm_flow(void);                         // Function to void transconductance in vacuum region
void stress_test_1(float *Vn_elm);           // Function for stress test-first part-cold
void stress_test_2(float *Vn_elm);           // Function for stress test-second part -hot
float drain_resistivity();                   // Function to update drain resistivity region value
float source_resistivity();                  // Function to update source resistivity region value
void reflection_coeff(void);                 // Function to read reflection coefficients
void compute_nodal_voltage(float *Vi_elm, int x, int y);         //  Function to calculate nodal voltage
void readinput(int i, float Y_s);                                //  Function to read material properties
void M_Matrix(float *Vi_elm,float *Vr_elm,float S[r][c]);        //  Function for matrix multiplication
void _connect (float *a , float *b);                             //  Function for connect phase stage
void connect_phase(void);                                        //  Function for connect stage

typedef struct {
                float K_th;
                float Mu_r;
                float epsilon_r;
                float Y_s;
                float Y_adm;
                float R;
                float C;
                float doping;
                float mobility;
                float Z;
                float S;
                float density;
                }materials_type;
materials_type material[X_max][Y_max];
materials_type *this_material;               // Points at material[x][y];

typedef struct {
                        float S[r][c];
                        }s_matrix;

typedef struct { int x; int y;
            double port_values[P]; } dc_point_input;
```

```
s_matrix scatter_phase(int x,int y);    // Function required to modify the scatter matrix //
s_matrix s_m;
int n_impulse_inputs = 0;
int n_continuous_inputs = 0;
int source;
double a_voltage;
void test_corner_of_S(int x, int y, s_matrix sm );
dc_point_input impulse_input_points[MAX_INPUT_POINTS];
dc_point_input continuous_input_points[MAX_INPUT_POINTS];
dc_point_input *the_input;
// Input files and the generated excel and txt files from each cycle
FILE *fp;
FILE *infp   = fopen("thermal input.txt","r");
FILE *infp2  = fopen("power_loss_E1.txt","r");
FILE *outfp1 = fopen("last_T1_60node.txt","w");
FILE *outfp2 = fopen("result_Th1_Temp.csv","w");
FILE *outfp3 = fopen("Th_1.txt","w");
FILE *outfp4 = fopen("Thermo_Th1.csv","w");
FILE *outfp5 = fopen("New_R1.csv","w");
FILE *outfp6 = fopen("Current_T1.csv","w");
FILE *outfp7 = fopen("Th1_gm.csv","w");
FILE *statsfp = NULL;


//********************************   Source code ***********************************//

int  main ()

  {

  int Regions,n,i,K,x,y,p,excitation_type;
  float dt,Power,R;
//**********************************************************************************
     test_files ();                           // tests for files
     excitation__input();                     // read excitation co-ordinates
     reflection_coeff();                      // setup boundary conditions
     read_regions();                          // reading material properties

//********************************      starting scatter phase ********************************

 for(K=0;K<Max_timestep;K++){
                          for(x=0;x<X_max;x++) {
                                  for(y=0;y<Y_max;y++){
                                  I_G = set_stimulus();
                                  this_material = &material[x][y];
                                   C=(this_material->S*this_material>density*Area*dx);
                                  R=this_material->R=(dx/2)/( this_material->K_th*Area);
                                  dt=sqrt(R*C);
                                  Z=(2*dt)/C;
                                   rpz=(R+Z);
                                  s_m = scatter_phase(x,y);
```

```
                                        M_Matrix(&Vi_elm[x][y][0],&Vr_elm[x][y][0], s_m.S);
                                        compute_nodal_voltage(&Vi_elm[x][y][p],x,y);
if (K>50&&K<70){
            stress_test_1(&Vn_elm[x][y]); }
 if (K>80&&K<100){stress_test_2(&Vn_elm[x][y]); }
                                      Resistivity_update(&Vn_elm[x][y],R);
                                      R=R_new;
                                      vacuum_value ();
                                      Temp_grad=Vn_elm[x][y]-Vn_elm[x+1][y];
                                      fprintf(outfp2,"  %g , ",Vn_elm[x][y]);
                                      fprintf(outfp3,"  %g \n",Vn_elm[x][y]);
                                      fprintf(outfp5,"  %g , ",R);
                                      current_flow();
I=((2*Vi_elm[x][y][0])/(R+Z))+((2*Vi_elm[x][y][1])/(R+Z))+((2*Vi_elm[x][y][2])/(R+Z))+((2*Vi_elm[
x][y][3])/(R+Z))+I_G;
                                      Power=(I*I*R);
                                      ageing_calc(&Vn_elm[x][y],x,y);
                                      I_plane[x][y] = I;
                                      fprintf(outfp6,"  %g , ",I_plane[x][y]);
                                      drain_resistivity();
                                      source_resistivity();
                                      gm_flow();
                                      g_m_transconductance(x,y);
                                      fprintf(outfp7,"  %f , ",g_m);
if(K==Max_timestep-1) {fprintf(outfp1," x=%d y=%d K=%d %g   \n",x,y,K,Vn_elm[x][y]);
}
}                                         fprintf(outfp2, "\n");
                                          fprintf(outfp4, "\n");
                                          fprintf(outfp5, "\n");
                                          fprintf(outfp6, "\n");
                                          fprintf(outfp7, "\n");
                                          }

connect_phase();
                                          fprintf(outfp2,"k=%d\n",K);
                                          fprintf(outfp5,"k=%d\n",K);
                                          fprintf(outfp6,"k=%d\n",K);
                                          fprintf(outfp4, "k=%d\n",K);
                                          fprintf(outfp7, "k=%d\n",K);
                                        }
return(0);

}

//****************************** End of the main source          *************************
//********************************** Sub functions                *************************
//********************************** 1- Matrix Multiplication function  *******************

void M_Matrix(float *Vi_elm,float *Vr_elm, float S[r][c])
        {
        int i,k;
        float AO,BO;
        AO=(I_G*(Z+R))/4;
```

```
            BO=1/((2*R)+Z);
            for(i=0;i<r;i++){Vr_elm[i]=0;
                        for(k=0;k<c;k++){
                                    Vr_elm[i]+=(BO*S[i][k])*(Vi_elm[k]+AO);
                                    }
            }
            return; }
// ********************************  2-Reading input    ********************************
void readinput(int i, float Y_s)
 {
  char string[50];
  int success;
  success=get_named_string("material", string);
  if (success==1)
            {
             printf("Warning the materials name failed");}
   char xmin_keyword[]="xmin";
   char ymin_keyword[]="ymin";
   char xmax_keyword[]="xmax";
   char ymax_keyword[]="ymax";
   char density_keyword[]="density";
   char K_th_keyword[]="K_th";
   char S_keyword[]="S";
   char doping_keyword[]="doping";
   char mobility_keyword[]="mobility";
   int xmin,xmax,ymin,ymax,x,y;
   float doping,mobility,density,C;Area=dx*dy;
// These define the limits of the region for this block of material.
   xmin=get_named_int(xmin_keyword);
   ymin=get_named_int(ymin_keyword);
   xmax=get_named_int(xmax_keyword);
   ymax=get_named_int(ymax_keyword);
// These define the materials properties //
  density=get_named_double(density_keyword);
  K_th=get_named_double(K_th_keyword);
  S=get_named_double(S_keyword);
  doping=get_named_double(doping_keyword);
  mobility=get_named_double(mobility_keyword);
  for(x=xmin;x<xmax;x++)
                        {
                        for(y=ymin;y<ymax;y++)
                                    {
                                    material[x][y].S= S;
                                    material[x][y].K_th=K_th;
                                    material[x][y].density=density;
                                    material[x][y].doping=doping;
                                    material[x][y].mobility=mobility;
                                    }
                                    }
                                    printf("readinput done\n");
```

```
 return ;
 }

// ******************************** 3-Resistivity update ********************************
float Resistivity_update(float *Vn_elm,float R)
 {
 float diff;
 diff=(*Vn_elm)-273;
 if (diff<=0){diff==1;}else
 R_new= R*(1+(Temp_coeff*diff));
 return R_new;
 }
// ******************************** 4- Current Void regions ******************************
void current_flow(void)
{
int x,y;
int xmin,xmax,ymin,ymax,p,xmin1,xmax1,ymin1,ymax1,
xmin2,xmax2,ymin2,ymax2,xmin3,xmax3,ymin3,ymax3;
xmin=11;xmax=20;ymin=48;ymax=50;xmin1=28,xmax1=58,ymin1=48,ymax1=50;
xmin2=0,xmax2=21,ymin2=50,ymax2=51;xmin3=28,xmax3=70,ymin3=50,ymax3=51;
for(x=xmin;x<xmax;x++)
                    {
                    for(y=ymin;y<ymax;y++)
                                        {
                                        I_plane[x][y]=0;
                                        }
                    }
for(x=xmin1;x<xmax1;x++)
                    {
                    for(y=ymin1;y<ymax1;y++)
                                        {
                                        I_plane[x][y]=0;
                                        }
                    }
for(x=xmin2;x<xmax2;x++)
                    {
                    for(y=ymin2;y<ymax2;y++)
                                        {
                                        I_plane[x][y]=0;
                                        }
                    }
for(x=xmin3;x<xmax3;x++)
                    {
                    for(y=ymin3;y<ymax3;y++)
                                        {
                                        I_plane[x][y]=0;
                                        }
                    }
return;
```

```
}

// ************************** 5-Transconductance void regions   ********************

float gm_flow(void)
{
   int x,y;
  int xmin,xmax,ymin,ymax,p,xmin1,xmax1,ymin1,ymax1,
  xmin2,xmax2,ymin2,ymax2,xmin3,xmax3,ymin3,ymax3;
  xmin=11;xmax=20;ymin=48;ymax=50;
  xmin1=28,xmax1=58,ymin1=48,ymax1=50;
  xmin2=0,xmax2=21,ymin2=50,ymax2=50;
  xmin3=29,xmax3=70,ymin3=50,ymax3=50;

for(x=xmin;x<xmax;x++)
                    {
                    for(y=ymin;y<ymax;y++)
                                        {
                                          g_m[x][y]=0;
                                         }
                     }
for(x=xmin1;x<xmax1;x++)
                      {
                      for(y=ymin1;y<ymax1;y++)
                                          {
                                           g_m[x][y]=0;
                                           }
                    }
for(x=xmin2;x<xmax2;x++)
                    {
                    for(y=ymin2;y<ymax2;y++)
                                         {
                                         g_m[x][y]=0;
                                         }
                    }
for(x=xmin3;x<xmax3;x++)
                    {
                    for(y=ymin3;y<ymax3;y++)
                                          {
                                            g_m[x][y]=0;
                                          }
                     }

return g_m[x][y];
}

//************************** 6-Nodal voltage  ***********************************

  float compute_nodal_voltage(float *Vi_elm, int x, int y)
```

```
  {
  float current,conductance,port_1,port_2,port_3,port_4;
float ambinet_T=273;
  port_1 =(2*Vi_elm[0])/rpz;
  port_2 =(2*Vi_elm[1])/rpz;
  port_3 =(2*Vi_elm[2])/rpz;
  port_4 =(2*Vi_elm[3])/rpz;
  current =port_1+port_2+port_3+port_4+I_G;
  conductance =4/rpz;
  Vn_elm[x][y]= ambinet_T +(current/conductance);
  return Vn_elm[x][y];
  }

//************************* 7-Ageing calculation   **********************************
 void ageing_calc(float *Vn_elm,int x,int y)
  {
  float j,AF,T_use,T_stress,A_1,A_2,Part_1,Part_2;
  float MTTF;
  float n=1;
  T_use=*Vn_elm;
  T_stress=*Vn_elm;
  j=I/Area;
  if (Temp_grad==0||Temp_grad== ambinet_T)
  {Temp_grad=1;
  }else;
  Part_1=(material[x][y].doping)*(diffusivity/(Blotz_man* ambinet_T));
  Part_2=(heat_tr/(T_use));
  J_thermo_mig=(Part_1)*(Part_2)*(-Temp_grad);
  A_1=pow(j,n);
  A_2=E_a/(Blotz_man*T_use);
  MTTF=(Area/A_1)* exp(A_2);
  AF=exp((E_a/Blotz_man)*((1/ ambinet_T)-(1/T_stress)));
  fprintf (outfp4," %g ,",J_thermo_mig );
  return ;
  }

//************************* 8- Test-1 ***********************************************
  void stress_test_1(float *Vn_elm)
  { float cold_T=75;int x,y;
            *Vn_elm=*Vn_elm-cold_T;
                               return ;
}
//************************* 9- Test-2  **********************************************
 void stress_test_2(float *Vn_elm)
  { float hot_T=75; int x,y;
   *Vn_elm= *Vn_elm+hot_T;
             return;
 }
//************************ 10- Conversion factor **********************************//
```

```
float set_stimulus(void)
  {float U_tv,i_m;
  fscanf(infp2,"%g",&i_m);
U_tv=U_tv=(material[x][y].sigma*dx)*((dt*dt)/4)*((1/(2*dx*K_th))+
(2*dt/(C*material[x][y].density*dx*dx*dx)));
  i_m=U_tv*i_m;
  return i_m;
  }
//********************** 11- Transconductance updating **********************************
void g_m_transconductance(int x,int y)
  {
  delta_I[x][y]=I_plane[x+1][y]-I_plane[x][y];
  delta_V[x][y]=Vn_elm[x+1][y]-Vn_elm[x][y];
   if (delta_V[x][y]==0){g_n[x][y]=0;}else
  g_n[x][y]=delta_I[x][y]/delta_V[x][y];
  if (R_s[x][y]==0){R_s[x][y]==0;
  }else
  g_m[x][y]=g_n[x][y]/(1+(g_n[x][y]* R_s[x][y]));
  return;
  }
//********************** 12- Source resistivity region  updating *****************************
float source_resistivity()
{
Int xmin=0,xmax=11,ymin=48,ymax=50;
for(x=xmin;x<xmax;x++)
                              {
                              for(y=ymin;y<ymax;y++)
                                            {
                                            R_s[x][y]= R;
                                            }
}
 return  R_s[x][y];
 }
//********************** 13- Drain resistivity region  updating ******************************
 float drain_resistivity()
 {
  int xmin1,xmax1,ymin1,ymax1;
  xmin1=58,xmax1=70,ymin1=48,ymax1=50;
  for(x=xmin1;x<xmax1;x++)
                                {
                                for(y=ymin1;y<ymax1;y++)
                                            {
                                            R_d[x][y]=R;
                                             }
 }
 return R_d[x][y];
 }
//********************** 14- reflection coefficient  *****************************
  void reflection_coeff()
```

```
 {
 char Ref_keyword[]="Ref";
 char Ref2_keyword[]="Ref2";
 char Ref3_keyword[]="Ref3";
 char Ref4_keyword[]="Ref4";
 Ref =get_named_double(Ref_keyword);
 Ref2=get_named_double(Ref2_keyword);
 Ref3=get_named_double(Ref3_keyword);
 Ref4=get_named_double(Ref4_keyword);
}
//********************** 15- read number of regions  ******************************
 void read_regions()
 {
 int Regions,i;
 char Regions_keyword[]="Regions";
 Regions=get_named_int(Regions_keyword);
 for(i=0;i<Regions;i++)  {
                                readinput(i,Y_s);
  }
 }
//********************** 16- excitation-input type  ******************************
  void excitation__input()
  {
  int x,y,excitation_type;
  char x_keyword[]="x";
  char y_keyword[]="y";
  char Vi_0_keyword[]="Vi_elm[x][y][0]";
  char Vi_1_keyword[]="Vi_elm[x][y][1]";
  char Vi_2_keyword[]="Vi_elm[x][y][2]";
  char Vi_3_keyword[]="Vi_elm[x][y][3]";
  for (excitation_type=get_input_type(); excitation_type>-1; excitation_type=get_input_type())
  {
   switch(excitation_type)
   {
    case CONTINUOUS_INPUT:
      printf("continuous input...");
      the_input = &continuous_input_points[n_continuous_inputs];
      the_input->x=get_named_int(x_keyword);
      the_input->y=get_named_int(y_keyword);
      the_input->port_values[0]=get_named_double(Vi_0_keyword);
      the_input->port_values[1]=get_named_double(Vi_1_keyword);
      the_input->port_values[2]=get_named_double(Vi_2_keyword);
      the_input->port_values[3]=get_named_double(Vi_3_keyword);

      n_continuous_inputs++;
      break;
         case IMPULSE_INPUT:
      printf("impulse input...");
      the_input = &impulse_input_points[n_impulse_inputs];
```

```
        x = the_input->x = get_named_int(x_keyword);
        y = the_input->y = get_named_int(y_keyword);
        Vi_elm[x][y][0] = the_input->port_values[0]=get_named_double(Vi_0_keyword);
        Vi_elm[x][y][1] = the_input->port_values[1]=get_named_double(Vi_1_keyword);
        Vi_elm[x][y][2] = the_input->port_values[2]=get_named_double(Vi_2_keyword);
        Vi_elm[x][y][3] = the_input->port_values[3]=get_named_double(Vi_3_keyword);
        n_impulse_inputs++;
        break;
    };
  }; printf("inputs done...\n");
}
//********************** 17- Scatter matrix ***********************************
s_matrix scatter_phase(int x,int y)
 {
  int i,j;
  float Y_adm,Z;
  s_matrix s_m;
            for (i=0;i<r;i++)
                              {
                              for(j=0;j<c;j++)
                                              {
                                              s_m.S[i][j]=Z;
                                              }
 }
  for(i=0;i<=3;i++)
                    {
                    s_m.S[i][i] =((2*R)-Z);
                    }
 return s_m;
 }

//********************** 18- connect function ************************************
void _connect (float *a , float *b)
            {
            *a=*b;
            return;
            }
//********************** 19- Vacuum regions ************************************
void vacuum_value ()

{
int x,y ;
int xmin,xmax,ymin,ymax,p,xmin1,xmax1,ymin1,ymax1,
xmin2,xmax2,ymin2,ymax2,xmin3,xmax3,ymin3,ymax3;
xmin=11;xmax=20;ymin=48;ymax=50;
xmin1=28,xmax1=58,ymin1=48,ymax1=50;
xmin2=0,xmax2=21,ymin2=50,ymax2=51;
xmin3=28,xmax3=70,ymin3=50,ymax3=51;
for(x=xmin;x<xmax;x++)
```

```
{
for(y=ymin;y<ymax;y++)
{
Vn_elm[x][y]=0;
}
}
for(x=xmin1;x<xmax1;x++)
{
for(y=ymin1;y<ymax1;y++)
{
Vn_elm[x][y]=0;
}
}
for(x=xmin2;x<xmax2;x++)
{
for(y=ymin2;y<ymax2;y++)
{
Vn_elm[x][y]=0;
}
}
for(x=xmin3;x<xmax3;x++)
{
for(y=ymin3;y<ymax3;y++)
{
Vn_elm[x][y]=0;
}
}
return;
}
//************************* 20- Connect phase ******************************//
void connect_phase(void)
{
 int x,y;
 for (x=0;x<X_max;x++)
 {
 for (y=0;y<Y_max;y++)
 {
 if( y>0 && x>0 && x<(X_max-1)&& y<Y_max-1)
 {
 _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
 _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
 _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
 _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
 }
 if((y==0)&&(x<X_max-1))
 {
 if(x==0)
 {
 _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
```

```
                    _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
                     Vi_elm[0][0][1]=Ref2*(Vr_elm[0][0][1]);
                     Vi_elm[x][y][0]=Ref*(Vr_elm[x][y][0]);
                    }
   else
      {
       Vi_elm[x][y][0]=Ref*(Vr_elm[x][y][0]);
      _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
       _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
       _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
      }
}
if (x==0 && y>0 && y<Y_max-1)
                          {
                          _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
                          Vi_elm[x][y][1]= Ref2 * Vr_elm[x][y][1];
                          _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
                          _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
                           }
if((y==(Y_max-1))&&(x<X_max))
                           {
                           if (x==0)
                                 {
                                  Vi_elm[x][y][1]=Ref2*Vr_elm[x][y][1];
                                  Vi_elm[x][y][2]=Ref3*Vr_elm[x][y][2];
                                 }
   else
      {
      _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
      }
   if(x==X_max-1)
                    {
                     Vi_elm[X_max-1][Y_max-1][3]=Ref4*Vr_elm[X_max-1][Y_max-1][3];
                     Vi_elm[X_max-1][Y_max-1][2]=Ref3*Vr_elm[X_max-1][Y_max-1][2];
                     }
   else
      {
      _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
      Vi_elm[x][y][2]=Ref3*Vr_elm[x][y][2];
      _connect(&Vi_elm[x][y][3],&Vr_elm[x+1][y][1]);
      }
      }
  if((y<Y_max-1)&&(x==(X_max-1)))
                                {
                                Vi_elm[x][y][3]=Ref4*Vr_elm[x][y][3];

                                 _connect(&Vi_elm[x][y][0],&Vr_elm[x][y-1][2]);
                                 _connect(&Vi_elm[x][y][1],&Vr_elm[x-1][y][3]);
                                 _connect(&Vi_elm[x][y][2],&Vr_elm[x][y+1][0]);
```

```
	if(y==0)
			{
			Vi_elm[x][y][0]=Ref*Vr_elm[x][y][0];
			}
		}
	}
  }
return;
}

//*****************************************************************************//
```

III. Tables

Table 1: IV characteristics data for Figure 6.18

cycles	Vds=20	Vds=40	Vds =60	Vds= 80
1	2.01E-03	4.02E-03	6.03E-03	8.04E-03
2	2.01E-03	3.99E-03	5.98E-03	7.97E-03
3	1.11E-02	2.23E-02	3.35E-02	4.46E-02
4	1.16E-02	2.33E-02	3.49E-02	4.66E-02
5	1.17E-02	2.33E-02	3.50E-02	4.66E-02
6	1.17E-02	2.33E-02	3.50E-02	4.66E-02
7	1.16E-02	2.33E-02	3.48E-02	4.66E-02
8	1.17E-02	2.33E-02	3.50E-02	4.66E-02
9	1.17E-02	2.33E-02	3.50E-02	4.66E-02
10	1.17E-02	2.33E-02	3.50E-02	4.66E-02

Table 2: data for IV characteristics after ageing for Figure 6.20

cycle	Vds=20	ageing	Vds=40	ageing	Vds=60	ageing	Vds=80	ageing
1	2.01E-03	1.98E-03	4.02E-03	3.97E-03	6.03E-03	5.95E-03	8.04E-03	7.94E-03
2	2.01E-03	1.96E-03	3.99E-03	3.89E-03	5.98E-03	5.83E-03	7.97E-03	7.76E-03
3	1.11E-02	1.07E-02	2.23E-02	2.14E-02	3.35E-02	3.22E-02	4.46E-02	4.29E-02
4	1.16E-02	1.10E-02	2.33E-02	2.21E-02	3.49E-02	3.31E-02	4.66E-02	4.42E-02
5	1.17E-02	1.09E-02	2.33E-02	2.18E-02	3.50E-02	3.27E-02	4.66E-02	4.36E-02
6	1.17E-02	1.08E-02	2.33E-02	2.15E-02	3.50E-02	3.23E-02	4.66E-02	4.30E-02
7	1.16E-02	1.06E-02	2.33E-02	2.12E-02	3.48E-02	3.17E-02	4.66E-02	4.24E-02
8	1.17E-02	1.05E-02	2.33E-02	2.09E-02	3.50E-02	3.14E-02	4.66E-02	4.18E-02
9	1.17E-02	1.04E-02	2.33E-02	2.06E-02	3.50E-02	3.10E-02	4.66E-02	4.13E-02
10	1.17E-02	1.02E-02	2.33E-02	2.03E-02	3.50E-02	3.06E-02	4.66E-02	4.07E-02

Table 3: data for IV characteristics after ageing for Figure 6.21

cycle	Vds=20	ageing	Vds=40	ageing	Vds=60	ageing	Vds=80	ageing
1	2.00E-03	2.01E-03	4.01E-03	4.02E-03	5.98E-03	6.03E-03	8.01E-03	8.04E-03
2	1.99E-03	2.01E-03	3.96E-03	3.99E-03	5.93E-03	5.98E-03	7.90E-03	7.97E-03
3	1.10E-02	1.11E-02	2.21E-02	2.23E-02	3.32E-02	3.35E-02	4.42E-02	4.46E-02
4	1.15E-02	1.16E-02	2.31E-02	2.33E-02	3.46E-02	3.49E-02	4.62E-02	4.66E-02
5	1.16E-02	1.17E-02	2.31E-02	2.33E-02	3.46E-02	3.50E-02	4.62E-02	4.66E-02
6	1.16E-02	1.17E-02	2.31E-02	2.33E-02	3.45E-02	3.50E-02	4.61E-02	4.66E-02
7	1.14E-02	1.16E-02	2.29E-02	2.33E-02	3.42E-02	3.48E-02	4.59E-02	4.66E-02
8	1.15E-02	1.17E-02	2.29E-02	2.33E-02	3.44E-02	3.50E-02	4.58E-02	4.66E-02
9	1.15E-02	1.17E-02	2.29E-02	2.33E-02	3.44E-02	3.50E-02	4.58E-02	4.66E-02
10	1.15E-02	1.17E-02	2.29E-02	2.33E-02	3.43E-02	3.50E-02	4.57E-02	4.66E-02

Table 4: drain source current with different gate voltage applied (data for Figure 6.7)

Vgs=2	Vgs=1	Vgs=0	Vgs=-1
0	0	0	0
2.04E-03	2.03E-03	2.01E-03	1.99E-03
0.0153	0.0134	1.11E-02	0.009572
0.01615	0.01425	1.16E-02	0.010054
0.01617	0.01426	1.17E-02	0.010059
0.01618	0.01427	1.17E-02	0.010059
0.01618	0.01427	1.16E-02	0.010059
0.01618	0.01427	1.17E-02	0.010059
0.01618	0.01427	1.17E-02	0.010059
0.01618	0.01427	1.17E-02	0.010059

Table 5: drain source current with different gate voltage applied (data for Figure 6.8)

Vgs= 2.0	Vgs=1.0	Vgs=0.0	Vgs=-1
0	0	0	0
4.05E-03	4.00E-03	3.99E-03	3.97E-03
0.02698	0.02502	2.23E-02	0.0211
0.028501	0.026403	2.33E-02	0.02227
0.028513	0.026414	2.33E-02	0.0222
0.028513	0.026415	2.33E-02	0.0222
0.028513	0.026415	2.33E-02	0.0222
0.028513	0.026415	2.33E-02	0.0222
0.028513	0.026415	2.33E-02	0.0222
0.028513	0.026415	2.33E-02	0.0222