Physics and technologies of silicon LDMOSFET for radio frequency applications

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Declaration

This dissertation contains the results of research undertaken by the author under the supervision of Prof. M.M.De Souza and Dr. G. Cao, between August 1999 and February 2004 at Emerging Technologies Research Centre in De Montfort University.
The contents of this dissertation have not been submitted in whole, or in part for any other degree or diploma at any academic institutions.

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Acknowledgement

Upon the completion of my thesis for Ph.D., I would like to express my appreciation for those who gave me help to my study and my life during the time I carried out the research work.

First of all, I would like to thank my supervisor, Prof. M. M. De Souza, for her supervision, suggestion and discussion. I appreciate her constant encouragement and support during the whole process of my Ph.D. study. Her suggestion on technical issues as well as the construction and English is valuable for my thesis writing.

I also would like to thank Dr. Cao, my second supervisor, for his supervision and understanding. His suggestion on the technical issues is very helpful for my research work and thesis writing. His contribution towards my thesis writing is highly appreciated.

I would like to say thanks to Prof. Sankara Narayanan for his constructive suggestion and illuminating discussion. His wide knowledge and extensive experience in power microelectronics are beneficial for my research work.

Other stuff and students from Emerging Technologies Research Centre have also given me help during my study. Special thanks are given to Dr. M. Sweet and Dr. R. Cross for sparing time correcting the language of my thesis. Thanks Dr. S. Hardikar and Dr. O. Spulber for the suggestion on paper writing. Thanks are also given to Dr. Chris and Mr. Feng for the technical discussion.

I would also like to express my appreciation to SEMELAB plc. for their financial support. I would like to thank Dr. Steve Sverdloff, Dr. John Walker, Dr. John Bruce and Dr. David Hinchly for their support. In addition, I would also like to thank Dr. John Walker for his technical discussion.

I am very grateful to the encouragement and support from my parents and my brother. Whenever I am at highs or lows, their support is always there. I would like to express my deep appreciation and love to my family members. Without their support, I would not have been so far.

Abstract

This thesis is devoted to the investigation of devices and technologies of Lateral Double Diffused-
Semiconductor
Metal-Oxide-Semiconductor -Field-Effect-Transistor for Radio Frequency (RP) applications. Theoretical analysis and extensive 2-D process and device simulation results are presented.

Theoretical analysis and simulations are carried out on RESURF LDMOS in both bulk and SOI substrate in terms of breakdown characteristics, transconductance, on-resistance and CV characteristics.

Quasi-saturation is a common phenomenon in DMOS devices. In this work, the dependence of quasi-saturation current on device physical and geometrical parameters is investigated in SOI RF LDMOS. Physical insight is gained into quasi-saturation on SOI RF LDMOS with different top silicon thickness and the same drift dose. It reveals that the difference in thick and thin film SOI lies in the different potential drop in the drift region. The influence of RESURF effect on quasi-saturation is also presented. It is shown that quasi-saturation current level can be affected by RESURF due to its influence on the drift dose.

The mechanism of self-heating is presented and the influence of top silicon thickness, buried oxide thickness, voltage bias is studied through simulations. The change of peak temperature and its location with bias is due to the shift of electric field with voltage bias. A back-etch structure and fabrication process have been proposed to achieve a superior thermal performance. The negative differential conductance is not present in the non-isothermal IV curves. The temperature rise in the back-etch structure is less than 1/4 of that in the bulk structure.

An RF LDMOS with a step drift doping profile on SIMOX substrate is evaluated. The fabrication process for the drift formation is proposed. The presented results demonstrate that step drift device has higher breakdown voltage than the conventional uniformly doped (UD) device, which provides the possibility to integrate LDMOS with low voltage CMOS for 28V base station application. This structure also has the advantage of suppressed kink effect due

to the reduced electric field within the drift region. The step drift structure also features lower capacitance, improved drain current saturation behaviour and reduced self-heating at class AB bias point.

For the first time, a novel sandwich structure for lateral RF MOSFET has been analysed based on silicon-on-nothing (SON) technology. The influence of device parameters on BV, CV and thermal performance has been investigated. Partial SON structure is found preferable in terms of heat conduct ability. Comparison on the electrical and thermal performance is made between SON LDMOSFET and conventional SOI alternative with BV of 40V. It is found that SON structure shows improvement in output capacitance and substrate loss. However, the temperature rise in SON device is higher compared to SOI alternative. The performance of the proposed sandwich SON structure has also been investigated in 28V base station applications, which requires breakdown voltage of 80V.

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Chapter 1 Introduction

1.1 General requirement of device performance for RF applications

Transistors constitute the core of most RF subsystems, such as power amplifiers, low noise amplifiers, mixers etc. The performance of a RF system is dependent upon the transistors residing within the subsystems. The performance of the transistors is frequency dependent as the impedance of the internal and external parasitic inductance and capacitance of the transistors change with frequency. Generally, the cut-off frequency of the transistors needs to be 10 times higher than the operation frequency. With the wireless telecommunication system marching into the third-generation (3G), 900MHz to 2.4GHz frequency is used. To operate the transistors under such high RF frequencies, a high cut-off frequency F_t and maximum oscillation frequency F_{max} are needed. The cut-off frequency is defined as the frequency at which the current gain is unit and the maximum oscillation frequency is defined as the frequency at which the power gain is unit. Besides the frequency characteristics, the requirements for RF power amplifier applications are high output power, high power gain, high power added efficiency and high linearity. Power gain, defined as $G = \frac{P_{out}}{P_{in}}$, reflects the amplification ability of the power amplifier, where P_{out} is the output power and P_{in} is the input power. Power added efficiency, defined as $PAE = \frac{P_{out} - P_{in}}{P_{DC}}$, where P_{DC} is the power supplied from DC source to the power amplifier, is the ability of an amplifier to convert the DC power of the supply into the AC power delivered to the load. Linearity is another figure of merit in amplification applications. A linear circuit has an output that is proportional to the input. Any nonlinearity of the circuit results in a signal distortion in the output. In 3G system using WCDMA (Wideband Code Division Multiple Access) transmission scheme, which involves a high degree of amplitude modulation, a high linearity is desirable. The performances of RF power amplifiers mentioned above are highly related with the device characteristics, such as IV characteristics, transconductance, CV characteristics and on-resistance. With the development of communication systems, the requirements upon high performance RF transistors are becoming more and more stringent. For example, the transfer of the communication system from single-carrier to multi-carrier demands more strictly on the linearity of the amplification. In a multi-carrier system, more than one carriers are present in a designated band. The interaction between individual carrier frequencies, referred as Intermodulation Distortion (IMD), introduces unwanted signal added to the original, due to the non-linearity. Improving the performance of RF transistors is thus becoming a challenging task.

1.2 Why silicon

For frequency above 4GHz, GaAs MESFET is the device of choice for low/medium power amplification and signal generating circuits. This is due to the electron mobility, which is six times greater than silicon, enabling the device to be operated at millimetre wavelengths (above 30G). In comparison to GaAs, opting for a silicon-based technology offers a more cost-effective solution with higher level of integration and breakdown voltages due to the higher electric field strength of silicon. Furthermore, the thermal conductivity of silicon is a factor of two higher than that of GaAs. So that silicon devices are more suitable for high power applications, where a large amount of generated heat needs to be removed from the device effectively.

1.3 Bipolar and MOS

Until the beginning of the 1970's, hardly any transistors were operated beyond 1 GHz. Microwave amplification was achieved by using either vacuum tubes or semiconductor diodes with a negative resistance or a non-linear capacitance. Later, their application was replaced by silicon bipolar transistors. Recently more attention is given to silicon MOSFET for RF application. For power amplifier applications, in comparison with MOSFET, bipolar transistors have limited high frequency power gain due to the emitter bonding wires and the high base-collector feedback capacitance [1]. MOSFET devices have several advantages over BJT due to the feature of the device structure and intrinsic characteristics. In LDMOSFET, the source is connected from the bottom and the source bonding wire is eliminated, leading to a higher power gain at high frequency. From the linearity point of view, bipolar transistor shows an exponential current-voltage characteristic, while the characteristics of MOSFETs feature square-law behaviour, indicating an inherent linearity of the device performance [2]. Furthermore MOSFETs have high input impedance, thus large current can be controlled with low drive requirements. This reduces circuit complexity and cost, compared to the active low-impedance network required to bias the emitter-base junction of a BJT. Moreover, bipolar transistors exhibit thermal runaway and secondary breakdown phenomenon, which results in device failure. In contrast, the drain current of MOSFETs displays a negative temperature coefficient, due to the negative temperature coefficient of carrier mobility, thus eliminating the thermal runaway and second breakdown. Therefore, MOSFET's do not require the ballasting that stabilises minority carrier BJTs. With the development of technologies,

dramatic improvements on the voltage and power ratings have made MOSFET a very competitive counterpart to bipolar devices.

1.4 Vertical and Lateral Double-Diffused power MOS for RF applications

1.4.1 Vertical Double-Diffused MOS for RF applications

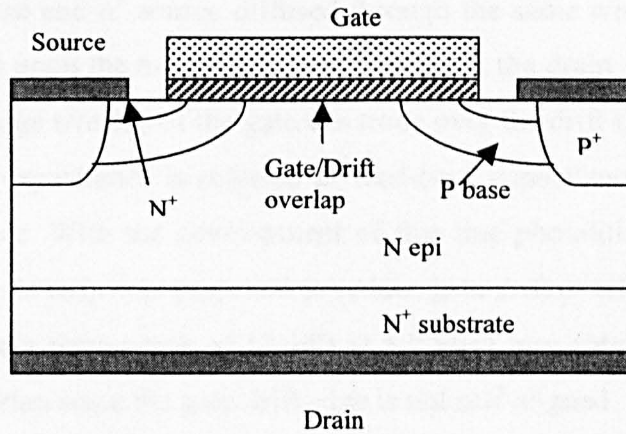

Figure 1.1 A schematic cross-section of VDMOS for s witching applications.

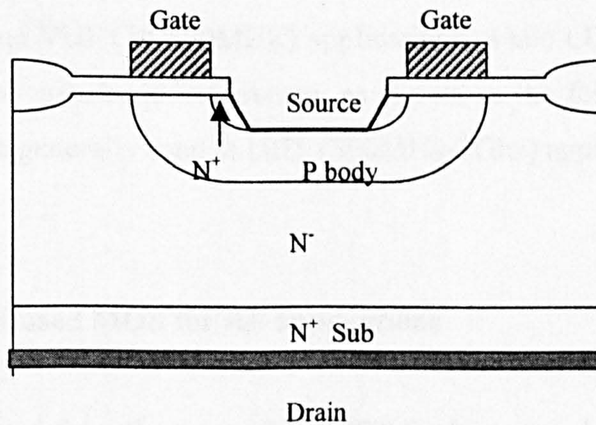

Figure 1.2 A schematic cross-section of VDMOS with low input and feedback capacitance

Vertical Double-Diffused MOS (VDMOS) and Lateral Double-Diffused MOS (LDMOS) are two basic MOSFET structures used in RF applications. RF VDMOSFETs originated from the conventional power VDMOSFETs for switching applications. Shown in Figure 1.1 is the device structure of an N-type power VDMOSFET. The most common circuit layout for MOS devices is common source configuration, when the source is grounded and the drain is connected to the DC supply. A short channel is needed to achieve a high operation frequency. This was obtained by using the double diffusion technology in 1960's, due to the lack of fine-line photolithography [3]. The channel length is determined by the difference in lateral diffusion depth of P base and n^+ source diffused through the same window. A lightly doped epitaxial layer is grown upon the n-type substrate to support the drain voltage. The drawback of the structure is the large overlap of the gate electrode over the drift region forming the gate drift capacitance. This capacitance is referred as feed-back capacitance C_{rss}, reduces the RF power gain of the device. With the development of fine-line photolithography techniques, a structure with narrow gate strip was proposed to reduce gate drift overlap, as shown in Figure 1.2. Using this structure a power gain of 12.4dB at 500MHz was obtained [1]. The structure still has a gate/drift overlap since the gate/drift edge is not self-aligned.

In a VDMOS structure, like bipolar transistor, the drain electrode is at the bottom of the device, therefore an insulating material such as beryllium oxide BeO must be used for drain isolation when packaging the device. This insulating material leads to extra thermal resistance between the device and the case, reducing the maximum power density. The source of DMOS is located at the surface of the die. Therefore, wire bonds are required to connect the source to the package leads. The inductance of the wire bonds tends to reduce high-frequency gain due to negative feedback. Due to these reasons, VDMOSFETs are generally used in HF (3-30MHz) and VHF (30-300MHZ) applications, while LDMOSFETs with lower C_{gd} and eliminated source wire bond inductance, as shown in the following section, obtain higher power gain and are generally used at UHF (300MHz-3Ghz) applications.

1.4.2 Lateral Double-Diffused MOS for RF applications

RF LDMOSFETs originated from the power MOSFET for high speed switching applications, whose schematic cross-section is shown in Figure 1.3. Different from a VDMOS, the drain electrode is located on the top instead of the bottom of the wafer. A schematic cross-section of a RF LDMOS is shown in Figure 1.4. Different from the structure in Figure 1.3, the gate/drift edge is self-aligned in RF LDMOS, since gate poly-silicon is used as a mask during drift

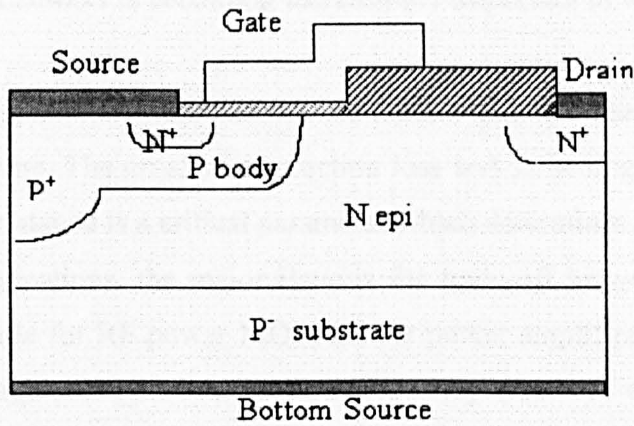

Figure 1.3 A schematic cross-section of LDMOSFET for switching applications.

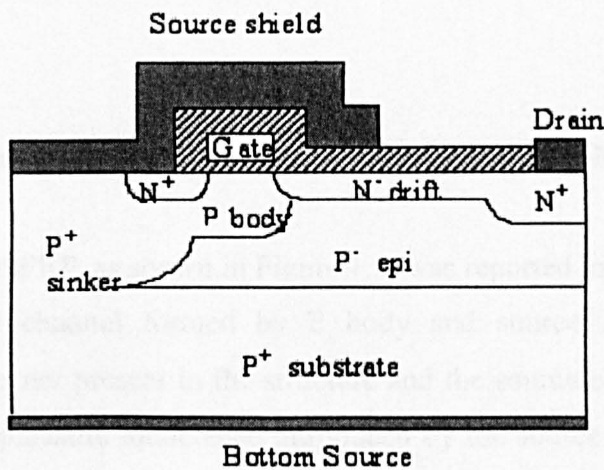

Figure 1.4 A schematic cross-section of LDMOSFET for RF applications.

implantation. This leads to a lower gate/source and gate/drift overlap capacitance compared to the power LDMOS for switching applications. The shallow drift region also leads to a lower capacitance related to the depletion in the drift region, which contributes to the gate/drift capacitance, C_{dg}. In addition, a source shield, also known as Faraday plate, is commonly adopted on RF LDMOSFET. It refers to the source metal, which extends on top of the drift region, shielding the gate electrode from the drain electrode to reduce C_{dg}. By bringing source contact to the bottom of the device via a P^+ sinker, the source lead inductance is removed. This is beneficial to high frequency power gain. Furthermore, the chip is directly mounted onto metal flange, leading to an improved grounding and lower thermal resistance. Due to

these advantages, RF LDMOS is becoming increasingly important in wireless communication applications [5-8].

In switching applications, the devices are maintained at on-sate or forward blocking state for most of the time. The on-state conduction loss and switching loss compose the total power loss. The on-resistance is a critical parameter which determines the on-state conduction loss. In switching applications, the major issue is the trade-off between breakdown voltage and on-resistance. While for RF power MOSFET for power amplifier applications, the main task is to obtain a high maximum-oscillation frequency (f_m), cut off frequency (f_t), high linearity as well as high output power, power efficiency and power gain. The presence of the parasitic component, including the parasitic capacitance, inductance and resistance, reduces the output power level, power efficiency and power gain. The non-linear parasitic components also degrade the linearity of the device and therefore must be reduced to minimum. Various technologies and device structures are proposed to achieve better performance by reducing the parasitics, improving the transconductance and increasing the maximum drain current. Some of the technologies and device structures of RF LDMOSFETs will be discussed in the following section.

1.5 Development of technologies and devices structures of RF LDMOSFET

The first lateral RF MOSFET, as shown in Figure 1.5, was reported in 1972 [9]. This structure has a double diffused channel formed by P body and source implantation/drive-in in sequence. A p^+ sinker is not present in the structure and the source electrode is on the top of the device. Due to the parasitic inductance introduced by the source electrode, this structure has a low gain at high frequencies, like the VDMOS. In a narrow-band amplifier, 10-dB gain was achieved at 1Ghz and 16dB was achieved at 500MHz. To meet the increasingly stringent requirements for high performance RF transistors and subsystems, numerous efforts have been made to improve its performance.

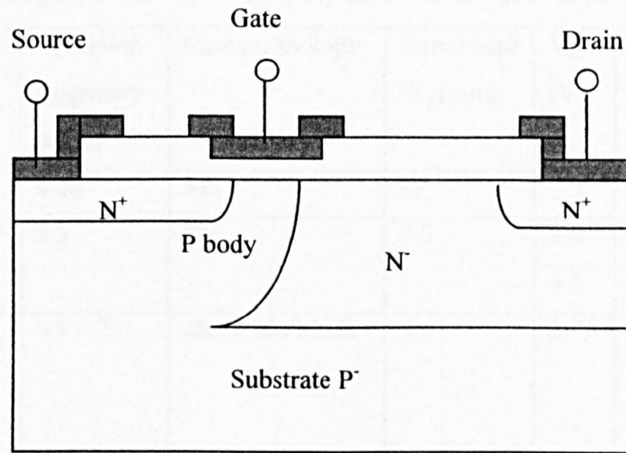

Figure 1.5 A schematic cross-section of LDMOS for RF applications.

1.5.1 Development of technologies of RF LDMOSFET

1.5.1.1 Sub-micron technology

The RF MOSFET device performance is a function of gate length. The MOS channel capacitance contributes to the input capacitance C_{iss}, which is an important factor determining the cut-off frequency. The channel resistance is one of the components which compose the on-resistance of LDMOSFET. Reducing gate length is an effective way to achieve a high cut-off frequency and low on-resistance for low voltage RF LDMOSFETs. For mobile handset applications, the supply voltage has been constantly reduced for lower cost and lower power consumption. To meet this requirement, the RF MOSFETs have been scaled down from generation to generation by employing sub-micron photolithography. Effort has been made to maintain a high power added efficiency (PAE) while reducing the supply voltage in order to reduce the power consumption and to increase talk time in mobile phones. Table 1.1 shows the low voltage RF power MOSs reported in the literature [10-14].

Table 1.1 Low voltage RF power MOSs reported in the previous literature.

year	Gate length L_g (μm)	Operation frequency (GHz)	Gate technology	Gate width W_g (mm)	V_d (V)	P_{out} (mW)	PAE (%)	Ref.
1983	1.3	0.86	Mo	69	7.5	5000	60	[10]
1992	0.8	1.5	Mo	7.5	6.0	2000	55	[11]
					4.8	1200	50	[12]
1995	0.35	0.9 – 2.0	MoSi/Mo/MoSi	1.6	3.5	250	55	[13]
						230	36	
						130	33	
1996	0.2	2	Co Salicide	0.8	3	127	50	[14]
					2	105	54	
					1	56	53	

1.5.1.2 Metallisation

Gate resistance leads to the reduction of power gain and maximum oscillation frequency. For a one-side contacted gate, the gate resistance derived from the transmission-line theory is expressed as $R_g = WR_{gsq}/(3L)$, where W/L is the gate width/length ratio and R_{gsq} is the gate sheet resistance [11]. Since metal has low resistance, Molybdenum has been used as the gate material [12,13]. The limit of the fabrication technology of Mo gate in mass production is 0.7μm. To obtain an even shorter gate length, gate silicidation has been adopted. Currently, WSi_2 and MoSi are the two most widely used materials. A metal-shorted Si-gate is another option for a short gate length with low gate resistance, as illustrated in Figure 1.6. This structure has a shorter gate length than metal gate structures, while a low gate resistance is obtained by the metal-shorted silicon gate. The shorted metal can be formed by Al and Au [14, 15]. As well as forming the gate structure, silicidation is also adopted in the source and drain region to reduce the source and drain resistance [16].

Electromigration is a concern for metallization. Electromigration is the mass transport of the metal atoms from one point to another as a result of the current flowing in the conductor. It leads to the formation of voids at some points in the metal line and hillocks or extrusions at other points. As a result, the open circuit or short circuit form in the metal connection. Al is known as having a low resistance to electromigaration. Due to this, gold, which shows a high resistance to electromigation, has been the primary choice for RF power device.

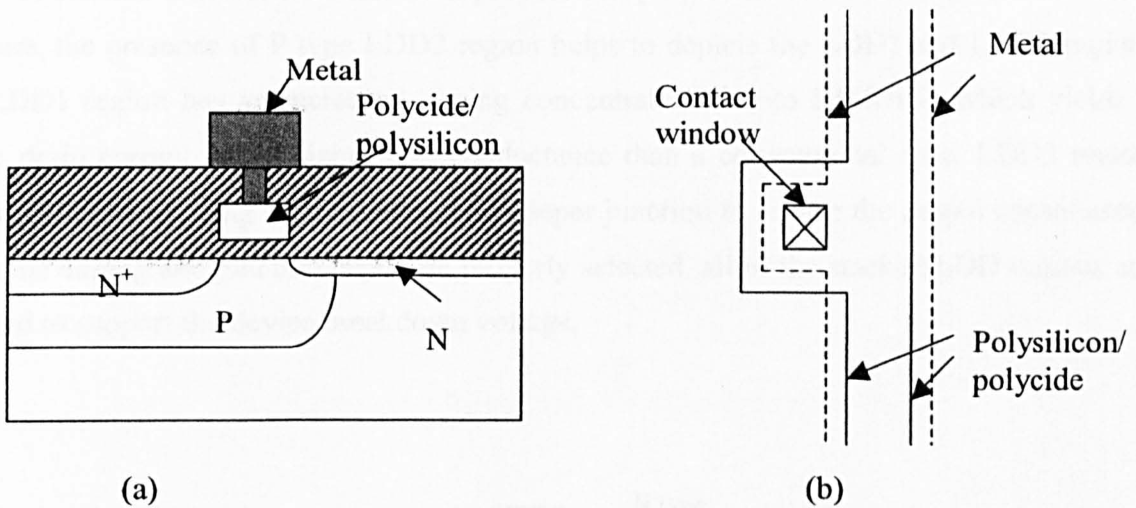

Figure 1.6 (a) a schematic cross-section of RF MOSFET with metal-shorted gate
(b) layout of the metal-shorted gate

1.5.2 Development of device structures of LDMOSFET

Various device structures have been proposed to improve the electrical and thermal performance of RF LDMOSFET. A graded gate structure was proposed [17, 18] to improve the trade off between transconductance and gate drain capacitance. The cross-section of the device structure is shown in Figure 1.7. In a conventional structure, a thicker gate oxide layer is needed to reduce the gate overlap capacitance and to ensure a high breakdown voltage. However this thicker gate oxide layer leads to a lower transconductance. The graded gate structure has a thinner gate oxide at the centre and a thicker gate oxide at the edge, which yields high transconductance and reduces gate overlap capacitance. The thicker oxide at gate edge is obtained by re-oxidation after gate patterning, by which a bird's beak shape of oxide is formed. The shape of the bird's beak is determined by the re-oxidation temperature and time.

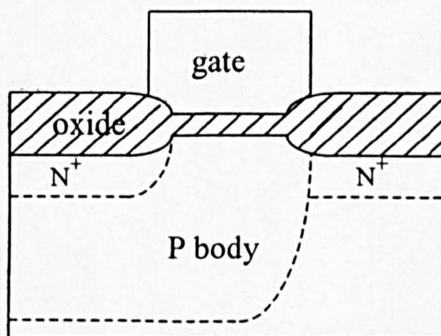

Figure 1.7 Graded gate structure in RF LDMOSFET.

A stacked drift structure has been proposed in [19], as illustrated in Figure 1.8. In this structure, the presence of P type LDD2 region helps to deplete the LDD1 and LDD3 region. The LDD1 region has an increased doping concentration due to RESURF, which yields a higher drain current and a higher transconductance than a conventional case. LDD3 region works with a low doping concentration and deeper junction to reduce the output capacitance. When the doping and junction depth are properly selected, all of the stacked LDD regions are depleted to support the device breakdown voltage.

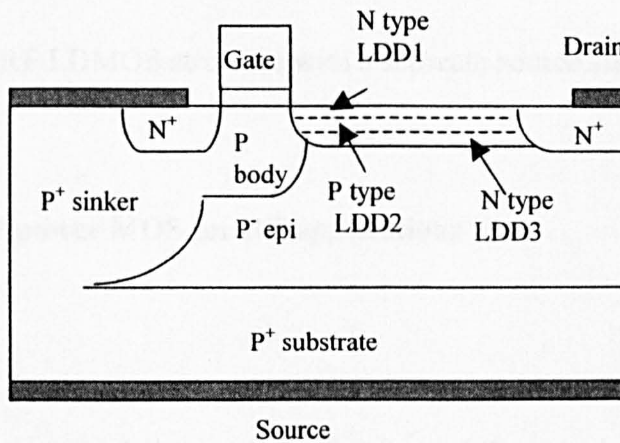

Figure 1.8 A schematic cross-section of RF LDMOS with stacked drift structure

In early RF LDMOSFET structures, the source shield extends over the gate and drift region. By using a separated source shield on top of drift region, the gate source parasitic capacitance caused by the gate sourced shield overlap can be reduced [20]. Philips proposed a RF LDMOS structure with a separate shield metal [21], as illustrated in Figure 1.9. Combined with a gold metalised polysilicon gate structure, this device shows high gain of 12dB at high output power of 70W at 2GHz and low intermodulation distortion.

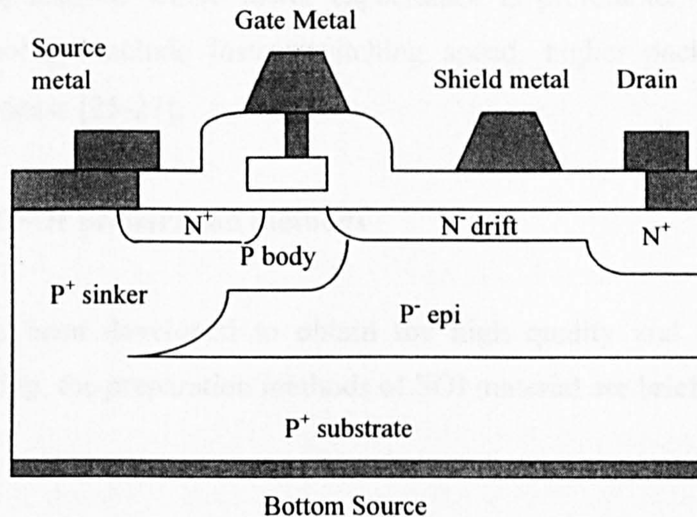

Figure 1.9 RF LDMOS structure with a separate source shield.

1.5.3 Development of SOI power MOS for RF applications

1.5.3.1 SOI technology

SOI (Silicon-on-insulator) is regarded as a technology providing ideal isolation for circuit integration. For conventional bulk technology, the isolation between the devices is achieved by reverse biased p-n junctions, known as Junction Isolation (JI) technologies. In conventional JI technology, the semiconductor substrate is associated with undesirable effects such as high leakage currents, parasitic bipolar components, and more importantly, interference between individual active devices or circuits built in the same integrated chip. For example, bipolar power devices tend to inject carriers into the substrate, where they may travel hundreds of microns and can interfere with other power devices and with the low voltage logic and control circuitry. SOI technology provides a dielectric isolation (DI), in which a layer of insulator provides the isolation between devices. The most widely used SOI technology uses a buried oxide as the insulation layer. In RF IC applications, the SOI technology makes it possible for the integration of low-voltage logic control circuitry, analogue circuits and RF circuits on the same chip. SOI is a natural solution for the shortcomings of JI technology.

An important characteristic of SOI technology for RF applications is the reduced parasitic capacitance [22-24]. In JI technology, presence of large isolation PN junctions leads to higher parasitic capacitance. While in SOI technology, the PN junctions are replaced by the buried oxide layer and local oxide, which reduces the junction capacitance. This is of great

importance for RF applications where lower capacitance is preferable. Other advantages offered by SOI technology include faster switching speed, higher package density and improved radiation hardness [25-27].

1.5.3.2 Comparison of SOI preparation methods

Various methods have been developed to obtain the high quality and low cost of SOI substrate. In the following, the preparation methods of SOI material are briefly described.

1.5.3.2.1. SIMOX

Separation by Implantation of Oxygen (SIMOX), is a technology which uses a high energy oxygen implantation to form the buried oxide layer whilst keeping a thin layer of single crystalline silicon on the surface [28]. A high dose of oxygen of about $10^{18}/cm^2$ is implanted into a single crystal substrate while the wafer is kept at a high temperature, of about 600°C, to avoid amorphization of the surface silicon. After annealing at 1300°C, the implanted oxygen introduces a layer of buried silicon oxide below the silicon surface. The process flow is illustrated in Figure 1.10.

The advantage of the SIMOX technology is the good uniformity of the top silicon thickness, which usually varies less than 100Å across a wafer. On the other hand, the implantation introduces defects in the SOI material, which makes the quality of the top silicon layer and the buried oxide a main concern. With the development of this technology, the defect density has been brought down to $10^4 cm^{-2}$ by optimising the implantation condition. A typical SIMOX wafer has maximum top silicon thickness of 0.2μm and buried oxide thickness of 0.4μm or less. Due to the limited buried oxide layer thickness, this technology is more suitable for low voltage IC application.

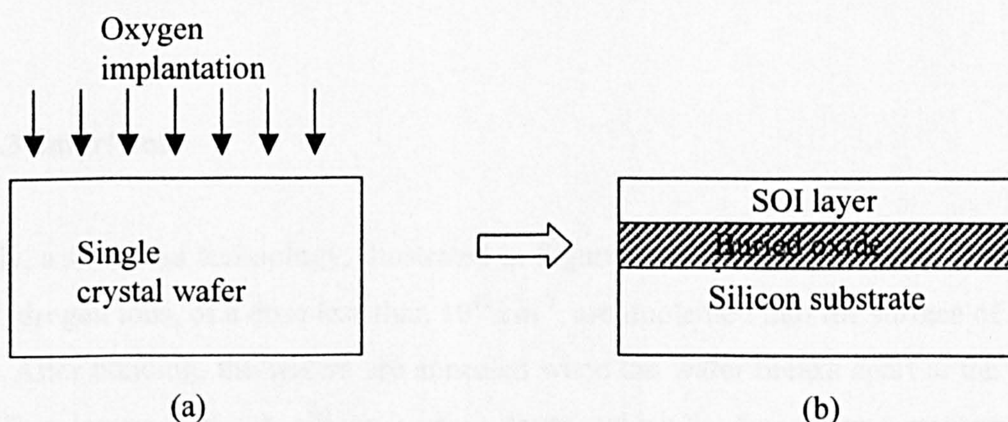

Figure 1.10 Process flow of SIMOX technology.

1.5.3.2.2. Wafer bonding

Wafer bonding technology starts with two conventional single crystal wafers. The surface of at least one of these wafers is thermally oxidized to obtain the required buried oxide thickness. After surface cleaning, the surfaces of the two wafers are then wetted and simply pressed together followed by annealing. One of the wafers is then thinned down by etch-back [29-32], whereas the other wafer remains to serve as a handle wafer. Mechanical grinding and polishing for etch-back has been used. The shortcoming of this technology is the large thickness non-uniformity across the wafer. To improve the uniformity, other sophisticated chemical etching methods using various kinds of selective etches and etch-stop layers have been reported [33-35].

Wafer bonding technology offers the advantage of high-quality, single crystal top silicon layer and a high-quality buried oxide. Furthermore, the thickness of the top silicon and the buried oxide layer is not limited as in the SIMOX technology. Wafer bonding is thus suitable for high voltage power applications [36]. Figure 1.11 illustrates the process flow of the wafer bonding technology.

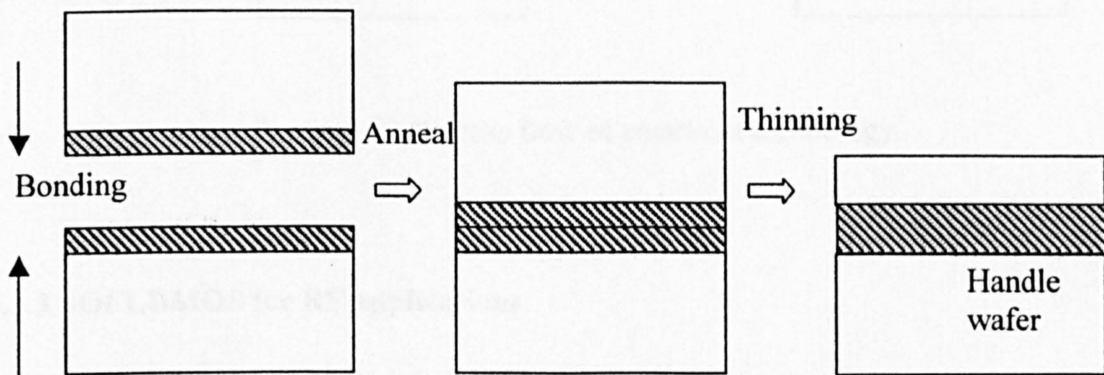

Figure 1.11 process flow of wafer bonding technology.

1.5.3.3.3 Smart cut

Recently, a smart cut technology, illustrated in Figure 1.11, has been developed by SOITEC [37]. Hydrogen ions, of a dose less than 10^{17} cm^{-2}, are implanted into the surface of one of the wafers. After bonding, the wafers are annealed when the wafer breaks apart at the implanted layer. This leaves a rough silicon surface layer, which is then chemo-mechanical touch polished to produce a smooth silicon surface on the final SOI wafer. Compared to the

traditional technology using wafer bonding and etch back or epitaxial lift-off, smart cut approach uses a thermal activation to separate the handle wafer and the device wafer. Inherently this process offers better control and a single donor substrate, the device wafer in Figure 1.12, can be used for many times for further substrate transfer.

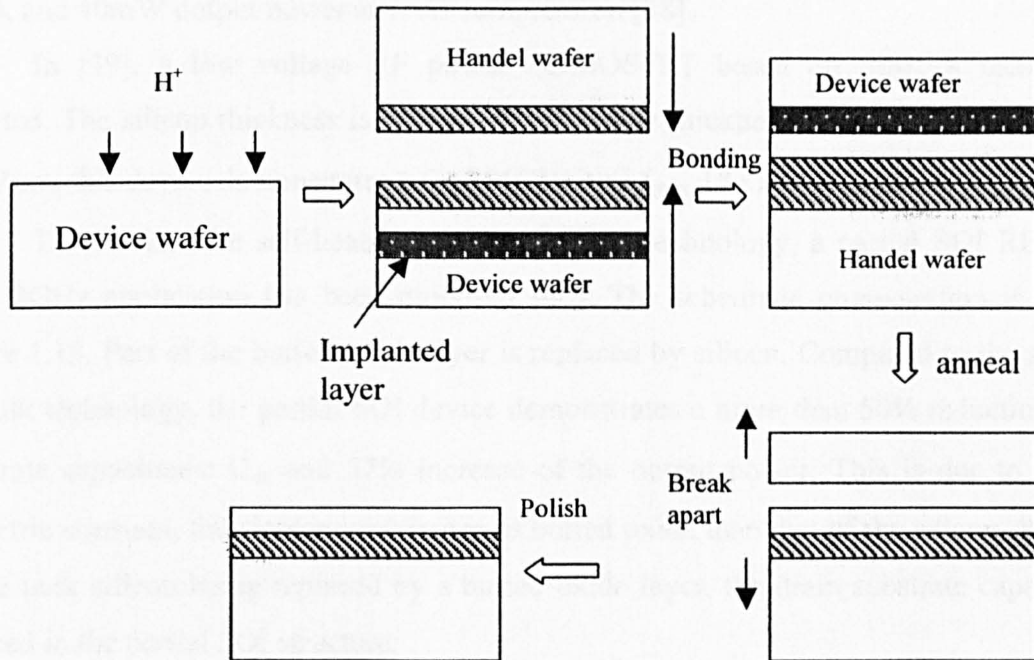

Figure 1.12 Process flow of smart cut technology.

1.5.3.3 SOI LDMOS for RF applications

Due to the interest in integrated RF systems, there has recently been increasing attention in RF SOI MOSFET. Along with the aforementioned advantages, the use of an SOI substrate for integration may also present several challenges. One of the major concerns with this technology is heat dissipation, since the thermal conductivity of the buried oxide is about 100 times less than that of the single-crystal silicon. Another phenomenon in thin layer SOI is the floating body-effect. Some other concerns include the quality of the SOI and buried oxide layers in the SOI starting material and the increased opportunity for charge trapping at the back interface of the buried oxide layer. The investigation of SOI RF LDMOS is focused on device development with a SOI CMOS compatible process, reduced self-heating and elimination of body-contact problem.

A 28V RF power LDMOSFET for 1GHz applications has been reported [38]. Beginning with a SIMOX substrate with top silicon thickness 0.2μm and buried oxide thickness 0.4μm, a p-type epitaxial layer is grown. The device structure is then formed on top of this top silicon layer. To obtain the body contact, an interleaved finger arrangement was used in which narrow p^+ implants were inserted into a typical n^+ source implant, as shown in Figure 1.13. The Class A amplifier developed using this device yields a power added efficiency (PAE) of 25%, which is identical to a similar bulk LDMOSFET, power gain of 16dB, and 40mW output power at 1-dB compression [38].

In [39], a low voltage RF power LDMOSFET based on SIMOX technology is reported. The silicon thickness is 200nm. Buried oxide thickness is 400nm. For a gate length of 0.7μm, this device demonstrates a f_t of 14GHz and f_{max} 18 GHz with BV of 20V [39].

To alleviate the self-heating problem in SOI technology, a partial SOI RF LDMOS FOR 2GHz application has been proposed [40]. The schematic cross-section is shown in Figure 1.14. Part of the buried oxide layer is replaced by silicon. Compared to the alternative on bulk technology, the partial SOI device demonstrates a more than 50% reduction in drain substrate capacitance C_{ds} and 37% increase of the output power. This is due to the lower dielectric constant, thus lower capacitance of buried oxide than that of the silicon. With a part of the bulk silicon being replaced by a buried oxide layer, the drain substrate capacitance is reduced in the partial SOI structure.

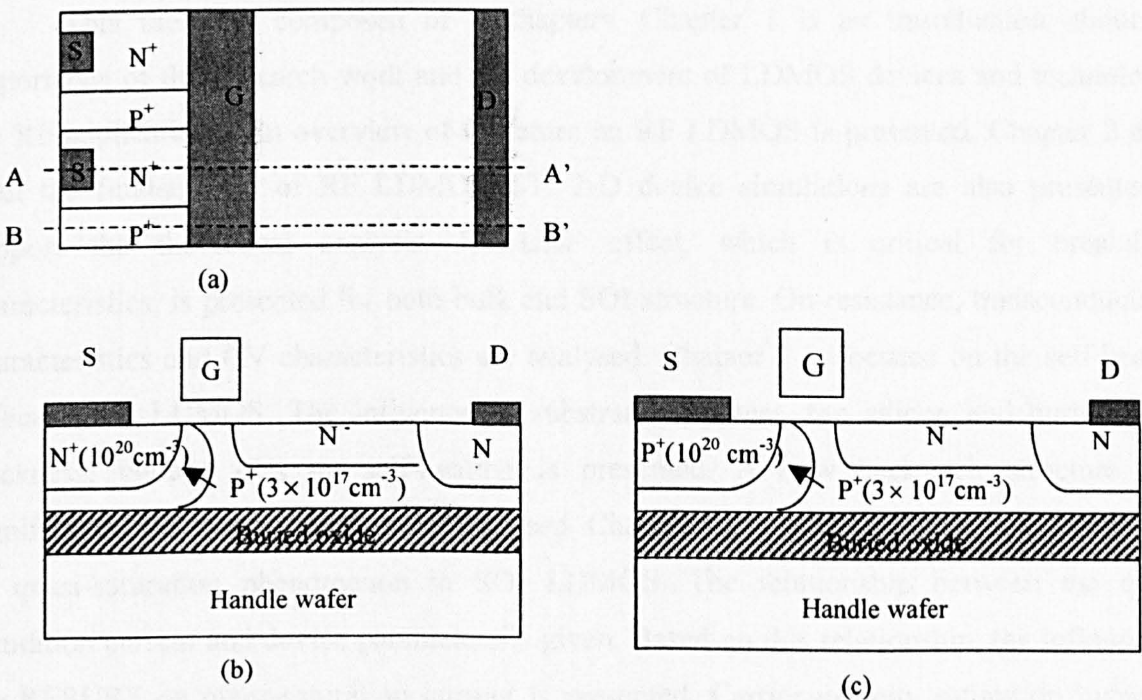

Figure 1.13 Device structure showing (a) top view and outline A-A' and B-B' through (b) MOS (c) body tie regions, respectively.

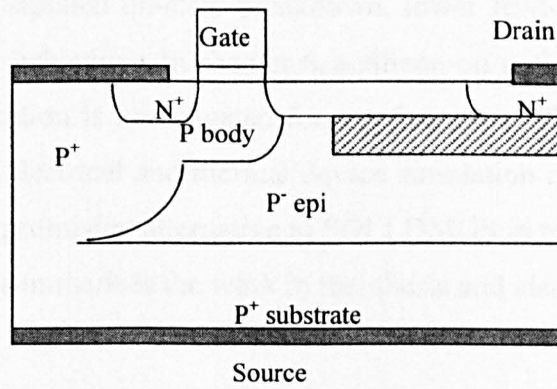

Figure 1.14 A schematic cross-section of a partial SOI RF LDMOS structure.

1.6 Motivation and organization of the work

The continuing development in telecommunication has created a demand for cost effective, high-performance RF subsystems and optimisation needs to be performed at the device level to extract maximum performance. This raises the requirement for developing cost effective, linear, high gain RF transistors. In this work, investigation has been carried out on the device physics of RF LDMOS in order to obtain an enhanced understanding. New device processes and structures have been proposed for the improvement in device electrical and thermal performance.

This thesis is composed of 7 chapters. Chapter 1 is an introduction about the importance of this research work and the development of LDMOS devices and technologies for RF applications. An overview of literature on RF LDMOS is presented. Chapter 2 deals with the fundamental of RF LDMOSFET. 2-D device simulations are also presented to support the theoretical analysis. RESURF effect, which is critical for breakdown characteristics, is presented for both bulk and SOI structure. On-resistance, transconductance characteristics and CV characteristics are analysed. Chapter 3 is focused on the self-heating effect in RF LDMOS. The influence of substrate thickness, top silicon and buried oxide thickness, voltage bias on self-heating is presented. A new back-etch structure with significantly reduced self-heating is proposed. Chapter 4 provides an insight into the physics of quasi-saturation phenomenon in SOI LDMOS. The relationship between the quasi-saturation current and device parameters is given. Based on this relationship, the influence of the RESURF on quasi-saturation current is presented. Carrier velocity saturation, which is regarded as the reason for quasi-saturation in previous literature, is found to be untrue. In chapter 5, the step drift structure on thin film SOI is evaluated. It shows that the step drift SOI

LDMOS has a superior performance in higher off-state breakdown voltage, suppressed kink effect in IV curves, postponed on-state breakdown, lower feed-back capacitance, improved drain current saturation behaviour. In chapter 6, a silicon-on-nothing (SON) structure suitable for high voltage application is investigated for the first time. The physical principle of this device is analysed and electrical and thermal device simulation results presented. It is shown that SON LDMOS is a promising alternative to SOI LDMOS in terms of lower drain substrate capacitance. Chapter 7 summarises the work in this thesis and also contains the future work.

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Chapter 2 Device Physics and Characteristics

Abstract

In this chapter, device physics and characteristics of LDMOSFET are analysed. Breakdown performance and the RESURF effect in both bulk and SOI LDMOSFET's are analysed, together with on-state resistance and transconductance. RESURF and non-RESURF LDMOSFET are compared in terms of on-resistance and on-state breakdown voltage. CV characteristics are obtained by analysing the capacitance component in the LDMOSFET structure based on a SOI substrate. The 2-D numerical simulations using device simulator MEDICI are carried out to verify the theoretical analysis.

2.1 Breakdown performance

Breakdown voltage is one of the most important characteristics for high voltage devices. In lateral power devices, RESURF (Reduced-SURface-Field) effect is widely employed to obtain a high breakdown voltage.

2.1.1 RESURF in bulk device

RESURF principle was first proposed by J. A. Appels in 1979 [1]. This concept enables a high breakdown voltage of lateral power devices. The main idea is to reduce the surface electric field by enabling interaction between a P/N junction at the surface and the other one in the bulk. To illustrate this, a lateral diode is shown in Figure 2.1. There are two separate P/N junctions, the diffused P^+NN^+ junction at the surface and the bulk N^+NP^- junction. The breakdown occurs at either of the two junctions depending on the electric field level. In reality, the electric field is much higher at P^+NN^+ junction because of the higher doping concentration and the junction curvature. In Figure 2.1(a), the two P/N junctions at the surface and in the bulk are apart from each other. The depletion layers of the two PN junctions do not interact with each other and RESURF does not take place. By reducing the distance between the two junctions, the depletion layer from both junctions merge at a certain voltage, which extends the depletion layer further towards the N^+ region. As a result, the depletion layer is much wider, leading to a reduced lateral electric field along the surface of the device, as demonstrated in Figure 2.1(b).

When the depletion region in the epi reaches the N^+ region, a peak electric field is present at the epi/N^+ interface due to the junction curvature there. Along the silicon surface, the other peak electric field is present at the P^+/N epi junction. It has been found that there is an optimum RESURF condition, in which case the epi layer is fully depleted with symmetrical electric field along the surface as shown in Figure 2.1 (c). A peak electric field is located at the P+/N epi junction at the silicon surface. The other peak electric field at the N epi/ N+ interface is attributed to the junction curvature there. Such a condition corresponds to an optimum amount of charge in the drift region. The drift charge can be expressed as, $N_{epi} \cdot d_{epi}$, where N_{epi} and d_{epi} are the doping concentration and the thickness of the epitaxial layer, respectively. When the drift charge is higher than this optimum value, the depletion layer will not extend towards the N^+ region effectively and the peak electric field appears at the vertical P^+/N epi junction. On the other hand, when the drift charge is less than the optimum value, the depletion layer extends to the N^+ region at lower voltage,

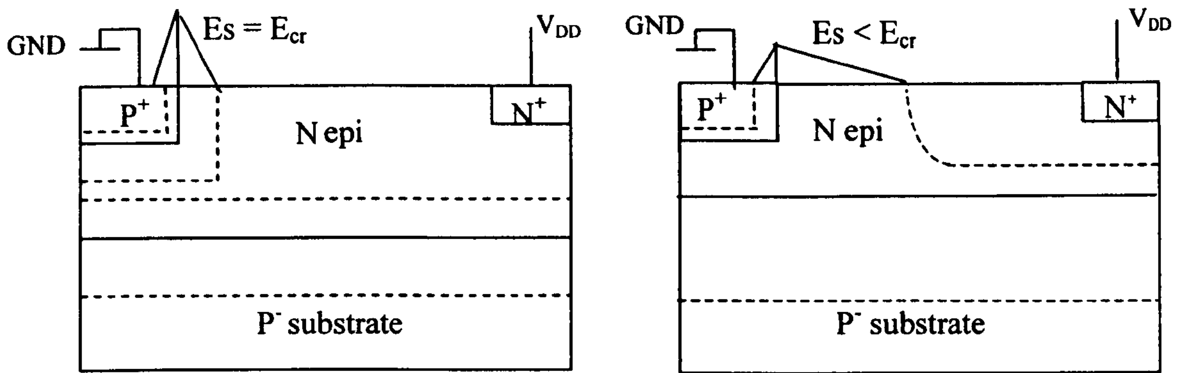


Figure 2.1 (a) Figure 2.1 (b)

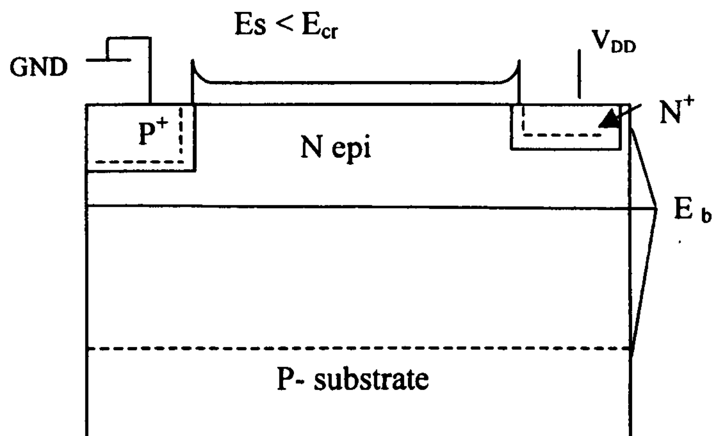


Figure 2.1 (c)

Figure 2.1 High voltage diode structure demonstrating RESURF effect.

so that the peak electric field presents at the N epi/N^+ junction. The optimum charge is at the level of 1e12cm^{-2} depending on the substrate doping concentration [1]. By reducing the lateral electric field along the silicon surface using RESURF, the avalanche breakdown can be shifted from the surface to the junction in the bulk, which allows a large increase in the maximum BV.

RESURF concept depicted above is widely adopted in LDMOSFET. In a N channel LDMOSFET, as shown in Figure 1.4, the drift region is surrounded by a P base region and a P^- epi region. The vertical P channel/N^- drift junction and the lateral N^- drift/P^- epi junction are naturally joined together, due to which RESURF takes effect. The maximum achievable breakdown voltage of a RESURFed LDMOSFET is limited by that of the drain/epi junction, which can be expressed as $V_B \cong 60(E_g/1.1)^{3/2}(N_B/10^{16})^{-3/4}$ [2], assuming a one-sided abrupt

junction. By reducing the lateral electric field along the silicon surface using RESURF, the avalanche breakdown can be shifted from the surface to the junction in the bulk to obtain the maximum BV. The other factors affecting the breakdown voltage of RF LDMOSFET are the channel punch through and the reach through in vertical direction. Punch through occurs when the depletion from the channel/N^- drift junction reaches the source region at a drain voltage below the rated avalanche voltage of the device. It provides a current path between source and drain and causes a soft breakdown characteristics. In the LDMOSFET structure, the depletion region at the N^+ drain/P^- epi junction extends downwards with the increase of the drain voltage. When the depletion region reaches the P^+ substrate before avalanching takes place, reach-through occurs. After that, a further increase in drain voltage causes the electric field at N^+ drain/P^- epi quickly reach the critical value of $2\times10^5 V/cm$ and avalanche breakdown occurs. Punch through and reach through leads to premature breakdown and must be avoided in the design.

2.1.2 RESURF in SOI device

In the SOI structure, a buried oxide layer is inserted between the epi layer and the substrate. The epi/substrate junction, which plays an important role in the bulk structure, does not exist in SOI structure. However, RESURF does take effect in the SOI structure due to the depletion from the interface of the top silicon layer and the buried oxide. The top silicon layer, buried oxide layer and substrate silicon act as a MOS capacitor. With a positive voltage applied on the N type top silicon region whilst the P type substrate grounded, the depletion layer forms at the top silicon and buried oxide layer interface. In the depletion region a positive charge is present. According to charge balance, at the interface of buried oxide and substrate, negative space charge is present, causing a depletion layer to form, as illustrated in Figure 2.2.

Figure 2.3 shows a SOI LDMOSFET for RF applications. Different from the bulk structure, a buried oxide layer is present under the top silicon layer. The source contact is on the top of the device, while the highly doped P^+ region under the source servers as a body contact. As in a bulk structure, source shield is present to reduce the gate/drift capacitance, C_{dg}. There is an optimum drift dose under RESURF in SOI structures as in bulk structures. Figure 2.4 shows the BV versus the total drift charge in SOI LDMOSFET. The SOI LDMOSFET has a top silicon thickness of 0.5μm, buried oxide thickness of 1.0μm and drift length of 3μm. The optimum drift charge is roughly 2.0e12cm^{-2}, which corresponds to a maximum breakdown voltage of 85V. The electric field distributions for various drift doses

are shown in Figure 2.5. For the optimum drift dose, the electric field distribution is nearly symmetric, whereas, when the drift dose is higher or less than the optimum value, the peak electric field appears at the channel or drain end of the drift, respectively.

The grounded source shield on top of the drift region affects RESURF by enhance the depleting of N type drift region. This results in a higher optimum drift dose under RESURF. As shown in Figure 2.4, incorporation of source shield leads to the optimum drift dose increase from $1e12/cm^2$ to $2e12/cm^2$ for the structure under study, indicating a 100% increase. The maximum BV decreases slightly for 5%.

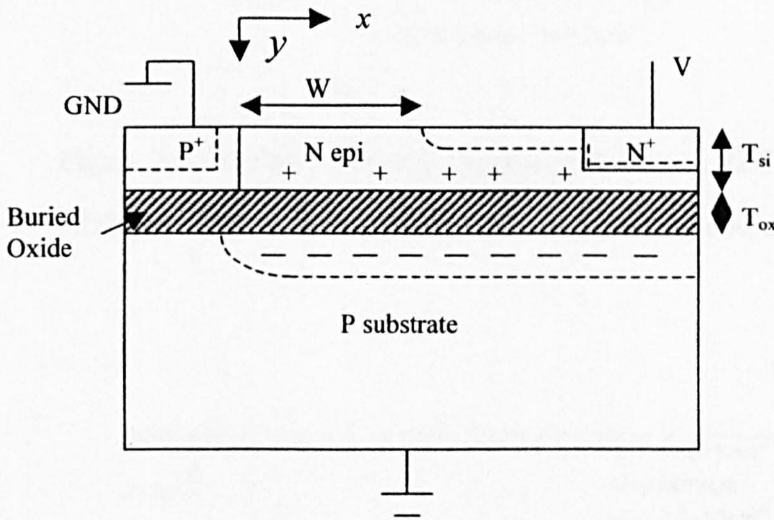


Figure 2.2 A schematic cross section of diode structure with RESURF taking effect.

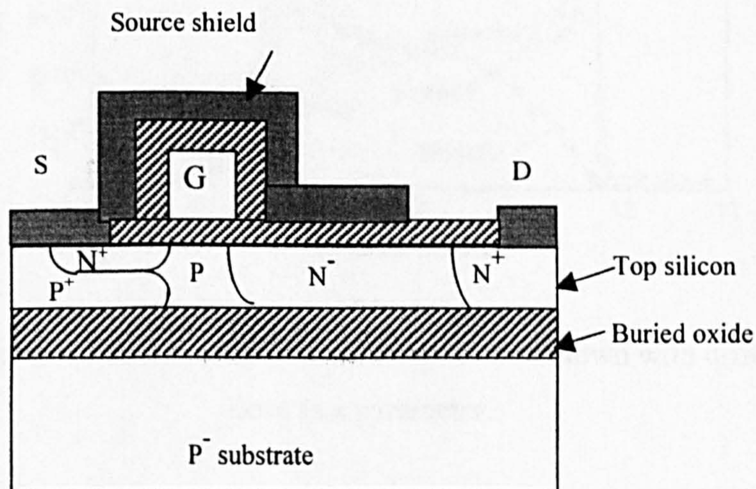


Figure 2.3 A schematic cross section of a RF LDMOSFET on SOI substrate.

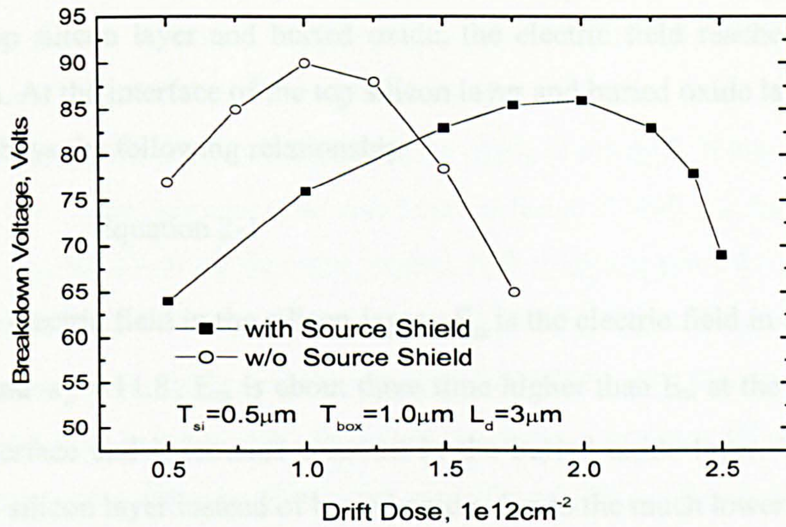


Figure 2.4 Breakdown voltage versus drift dose in RESURF RF LDMOSFETs on SOI substrate with and without source shield.

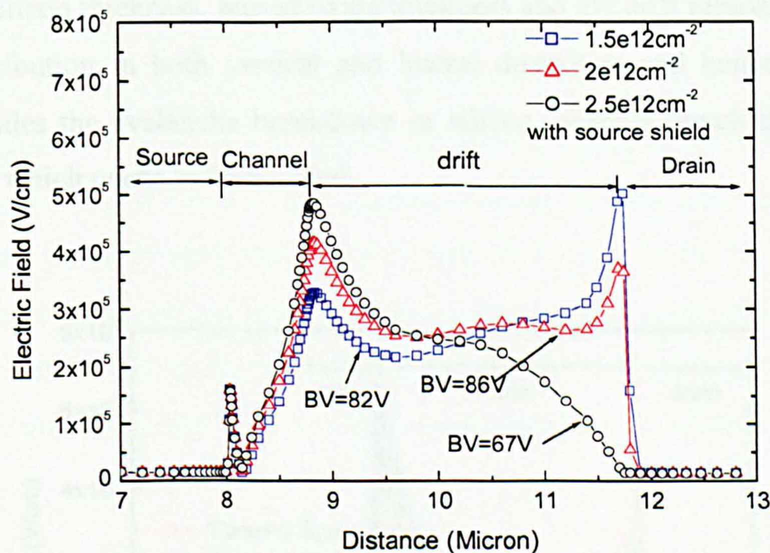


Figure 2.5 Electric field distributions at breakdown with drift dose as a parameter.

Avalanche breakdown may occur in lateral and/or vertical direction in the top silicon layer. Lateral breakdown in SOI structure is the same as in bulk structure. However, due to the buried oxide, SOI structure has a different electric field distribution in the vertical direction from bulk structure. With a uniform doping concentration in the top silicon layer,

the electric field is linearly distributed along the vertical direction in this layer. Near the interface of the top silicon layer and buried oxide, the electric field reaches its maximum value in the silicon. At the interface of the top silicon layer and buried oxide layer, the electric field distribution obeys the following relationship

$$\frac{E_{si}}{E_{ox}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}, \qquad \text{Equation 2-1}$$

where E_{si} is the electric field in the silicon layer, E_{ox} is the electric field in the oxide layer. since $\varepsilon_{ox} = 3.9$ and $\varepsilon_{si} = 11.8$, E_{ox} is about three time higher than E_{si} at the top silicon and buried oxide interface and it remains constant in the buried oxide layer. The breakdown occurs in the top silicon layer instead of buried oxide, due to the much lower critical electric field of silicon, about 2e5V/cm, compared to 9e6V/cm~3e7V/cm of oxide, depending on the thickness and quality of silicon oxide film [2]. When the electric field in the top silicon near the silicon/buried oxide interface reaches 2e5V/cm, vertical breakdown occurs. However, in an ultra thin silicon layer, the critical breakdown electric field for silicon can reach higher value due to the limited impact ionization path in the vertical direction. Impact ionisation along both the lateral and the vertical directions contributes to avalanche breakdown in SOI devices. The top silicon thickness, buried oxide thickness and the drift region length influence the potential distribution in both vertical and lateral directions and hence the breakdown performance. Besides the avalanche breakdown in silicon, channel punch through may also take place in SOI, which needs to be avoided.

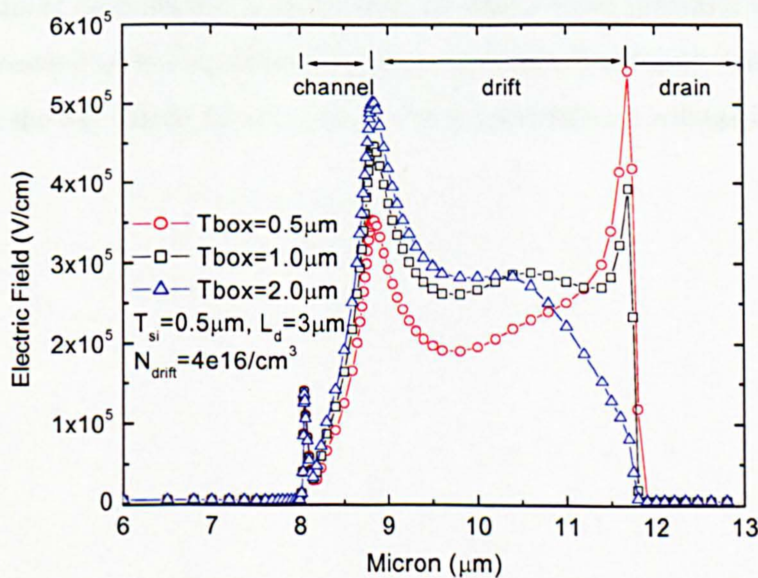


Figure 2.6 Electric field distribution along the silicon surface at breakdown with buried oxide thickness as a parameter.

Figure 2.6 shows the influence of the buried oxide thickness upon RESURF in a SOI RF LDMOSFET. For T_{box}=1.0μm, RESURF is at the optimum under drift charge of $4e16cm^{-2}$, where electric field peaks are equal at both ends of the drift. If the oxide thickness is reduced to 0.5μm, the peak appears at the drain end of the drift with the same drift charge. To obtain the optimum RESURF for this case, higher drift charge is needed. On the contrary, a lower drift dose is needed to achieve the optimum RESURF, when the oxide thickness is increased to 2μm. The above results reveal a stronger RESURF with thinner T_{box}. With the same voltage, electric field in oxide increases with a reduction in oxide thickness, which in turn leads to higher electric filed in silicon/buried oxide interface. Therefore, according to Gauss law, more space charge in the top silicon layer is required to support the higher electric field In general, RESURF is more effective with thinner T_{box} as the vertical electric field is stronger. On the contrary, it is less effective with thicker T_{box}.

Figure 2.7 shows the maximum breakdown voltage versus T_{box} with the top silicon thickness as a parameter. It is shown that BV increases with the increase of T_{box} and the increase of T_{si}. with T_{box} reduced from 2.0μm to 0.5μm, BV decrease slightly. However, it decreases significantly from 69V to 52V when T_{box} decreases from 0.5μm to 0.2μm. Figure 2.8 shows the impact ionisation rate contour at breakdown for T_{box}=0.2μm, T_{si}=0.5μm. The highest impact ionisation rate is located at the top silicon/buried oxide interface under the drain, where the vertical electric field is the highest. It means that the avalanche breakdown at the vertical direction is the limiting factor. This leads to a much lower BV for T_{box}=0.2μm than the other structures with thicker buried oxide, in which more potential is dropped on the buried oxide layer instead of the top silicon layer. As a result, the impact ionisation along the vertical direction in the top silicon layer is lower and the breakdown voltage is higher.

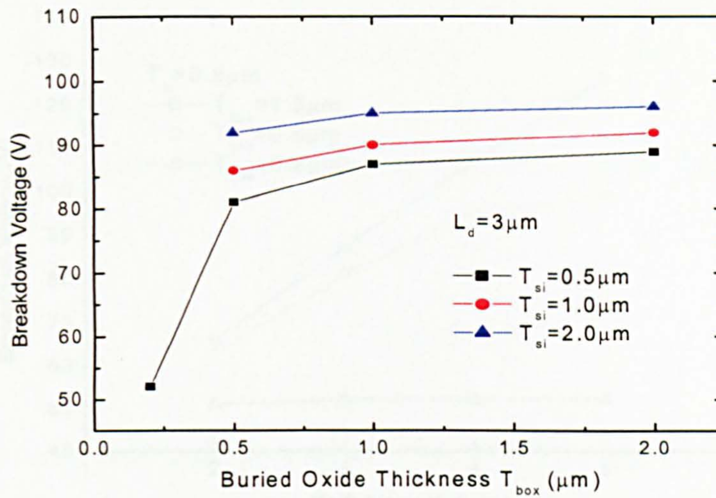


Figure 2.7 Breakdown voltage versus buried oxide thickness with top silicon thickness as a parameter.

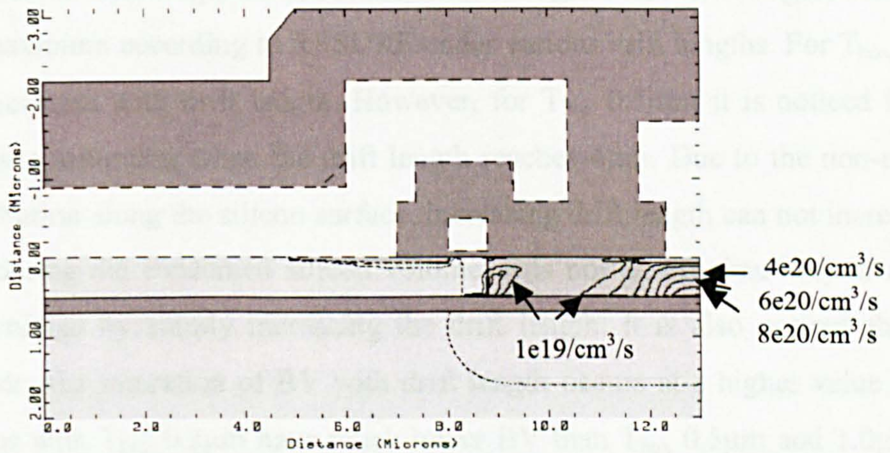


Figure 2.8 SOI LDMOS structure showing the impact ionization contour at breakdown for device with top silicon thickness 0.5μm, buried oxide thickness 0.2μm and drift length 3μm.

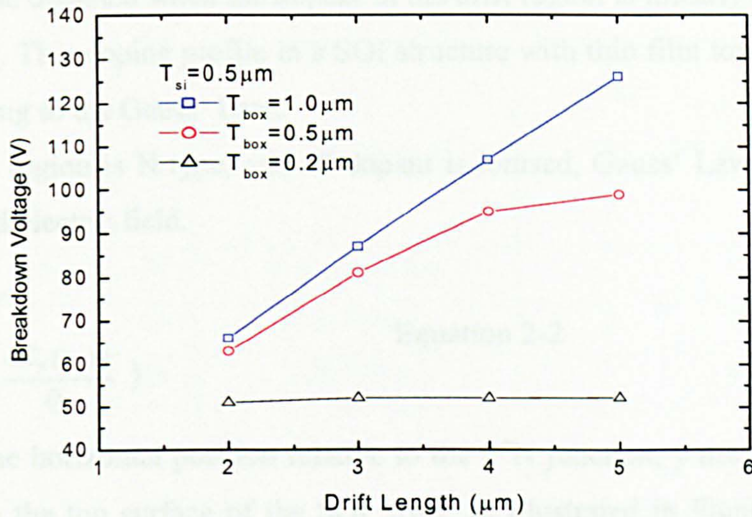


Figure 2.9 Breakdown voltage versus drift length for SOI RF LDMOS with top silicon thickness as a parameter.

The influence of drift length on the breakdown voltage is shown in Figure 2.9. BV is optimised to the maximum according to RESURF under various drift lengths. For T_{box} 0.5μm and 1.0μm, BV increases with drift length. However, for T_{box} 0.5μm, it is noticed that the increase of BV starts saturating when the drift length reaches 4μm. Due to the non-uniform electric field distribution along the silicon surface, increasing drift length can not increase BV effectively. Considering the consumed silicon volume, it is not an efficient way to achieve high breakdown voltage by simply increasing the drift length. It is also noticed that with thicker buried oxide, the saturation of BV with drift length occurs at a higher value of drift length. The devices with T_{box} 0.2μm have much lower BV than T_{box} 0.5μm and 1.0μm. The BV is unchanged with the increase of drift length in the case of T_{box}=0.2μm. This is because the impact ionisation is dominated by the impact ionisation in the vertical direction and therefore further increasing the drift length does not change the breakdown voltage.

2.1.3 Ideal RESURF in thin SOI

With a uniform doping profile in the top silicon layer, the lateral electric field distribution is non-uniform. For the structure illustrated in Figure 2.1(a), the lateral electric field has two peaks, one at the P^+/N epi vertical junction, one at the N^+/N epi junction. This non-uniform electric field distribution limits the breakdown voltage. In the case that the lateral electric field is uniformly distributed, the potential drop on the device at breakdown can reach the ideal.

This situation can be obtained when the dopant in the drift region is linearly distributed in the lateral direction [3]. This doping profile in a SOI structure with thin film top silicon layer can be deduced according to the Gauss' Law:

Assuming the drift region is N type, and all dopant is ionised, Gauss' Law yields a relation between doping and electric field.

$$N(x) = \frac{\varepsilon_{si}\varepsilon_0}{q}\nabla \cdot \vec{E}(x,y) = \frac{\varepsilon_{si}\varepsilon_0}{q}\left(\frac{\partial E_x(x,y)}{\partial x} + \frac{\partial E_y(x,y)}{\partial y}\right) \qquad \text{Equation 2-2}$$

Here x measures the horizontal position relative to the P^+N junction, y measures the vertical position relative to the top surface of the SOI layer, as illustrated in Figure 2.2. When the lateral component of the electric field is uniform, it yields

$$\frac{\partial E_x(x,y)}{\partial x} = 0. \qquad \text{Equation 2-3}$$

Combined with Equation 2.3, integrating Equation 2.2 over the entire N^- region gives the charge distribution in the N^- region as [3],

$$Q(x) = \frac{\varepsilon_{si}\varepsilon_0 V}{qWt}x, \qquad \text{Equation 2-4}$$

where

$$t = \frac{T_{si}}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}}T_{box}, \qquad \text{Equation 2-5}$$

V is the applied reverse bias voltage relative to the P^+ region and the substrate, T_{Si} is the top silicon thickness, T_{box} is the buried oxide thickness, ε_{si} is the silicon relative permittivity and ε_{ox} is the buried oxide relative permittivity. Equation 2-4 reveals that the drift dose is linearly distributed along the silicon surface. The slope of the doping distribution is related to the top silicon thickness, buried oxide thickness and drift length, as given by [4]

$$slope = \frac{9.5\times10^{16}cm^{-3}um^{-1}}{T_{si}(\frac{T_{si}}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}}T_{ox})\ln(70.3L)}, \qquad \text{Equation 2-6}$$

Linearly doped drift has been widely used to obtain a high breakdown voltage [3, 5-6]. However, in RF devices, the source shield placed over the drift affects the potential distribution in the device. For a comparison, four RF LDMOSFETs were constructed with the combination of with and without source shield, uniform and linear drift doping profile. These devices are optimised to obtain the maximum breakdown voltage with the same drift length of 3μm. Table 2.1 lists the device parameters.

Table 2.1 device parameters of the optimised devices for comparison.

Devices	BV (V)	Drift doping level/slope	Drift length (μm)	T_{si} (μm)	T_{box} (μm)
Linear drift doping, w/o SS (Source Shield)	83	7.2e16/cm^{3}μm	3	0.2	0.4
Linear drift doping, with SS	76	8.8e16/cm^{3}μm	3	0.2	0.4
UD, w/o SS	65	1.2e17/cm^3	3	0.2	0.4
UD, with SS	68	1.6e17/cm^3	3	0.2	0.4

It can be seen that the linear doped structure without the source shield has the maximum breakdown voltages of 83V. The doping profile of this device is shown in Figure 2.10. In base station applications, about 80V breakdown voltage is desired. For the LDMOSFET on SIMOX substrate, using a linear drift doping significantly improves the BV and enable the device to be used on base station applications. However, the presence of the source shield in linear doped device decreases the breakdown voltage.

The potential distributions of these devices are shown in Figure 2.11. It can be seen that the potential is linearly distributed in the linear doped structure without the source shield, leading to the maximum breakdown voltages among the four devices. When a source shield is present, the potential distribution is no longer linearly, as in an Uniformly Doped (UD) devices, leading to a decreased breakdown voltage. In RF LDMOSFET, the influence of the linear doping is degraded.

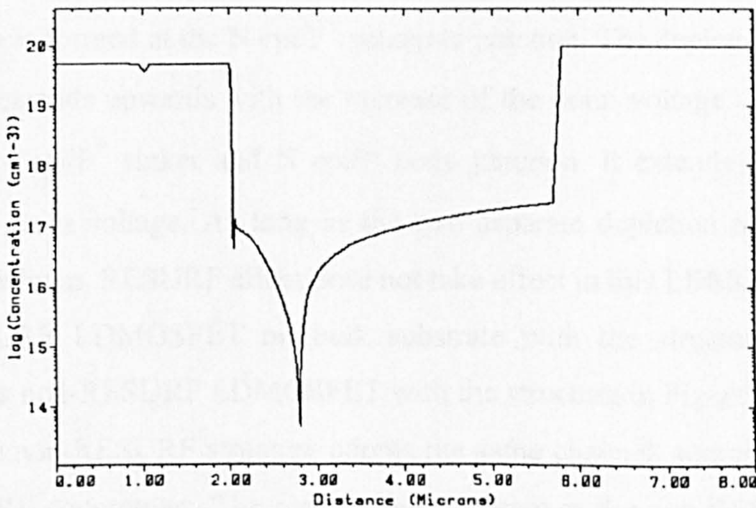


Figure 2.10 Doping distribution along the device surface in a SOI LDMOSFET with ideal RESURF effect.

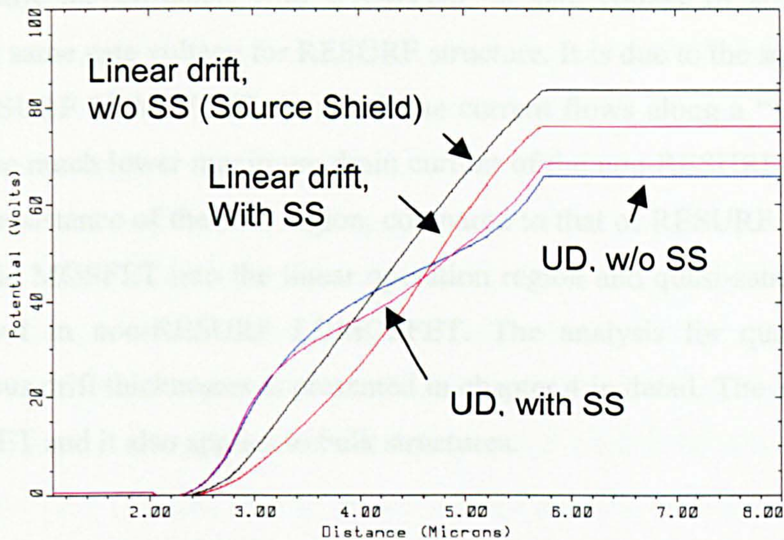


Figure 2.11 Potential distribution along silicon surface in SOI LDMOSFET's with linear and uniform drift doping profile, with and without source shield.

2.1.4 Comparison of RESURF and non-RESURF LDMOSFET

Figure 2.12 shows the 2D schematic cross-section of a non-RESURF LDMOSFET. Different from a RESURF LDMOSFET, the P^- epi region is replaced by N^- epi region which serves as the drift region. Furthermore, the P^+ sinker is present to act as a body contact region as in a RESURF device, but not merged with the P^+ substrate. When a drain bias is applied, depletion region is formed at the N epi/P^+ substrate junction. The depletion is mainly in the N epi region and extends upwards with the increase of the drain voltage. The depletion is also formed at the N epi/P^+ sinker and N epi/P body junction. It extends downwards with the increase of the drain voltage. As long as the two separate depletion regions do not merge together at breakdown, RESURF effect dose not take effect in this LDMOSFET.

A RESURF LDMOSFET on bulk substrate with the structure in Figure 1.4, is compared with a non-RESURF LDMOSFET with the structure in Figure 2.12. To make a fair comparison, the non-RESURF structure adopts the same channel, source and drain design as those of RESURF counterpart. The source shield is kept in the non-RESURF structure. The other device parameters are listed in Table 2.2. Both devices have a BV of about 80V. The RESURF LDMOSFET obtains the optimum RESURF at breakdown. The non-RESURF device is optimised to obtain the required BV with a minimum drift length. The IV

characteristics for both devices are shown in Figure 2.13. The non-RESURF structure shows a much higher specific on-resistance, with 5.7e4Ω·cm^2 at gate voltage of 20V, compared to 1.5e4Ω·cm^2 at the same gate voltage for RESURF structure. It is due to the square shape drift region in non-RESURF LDMOSFET, in which the current flows along a "V" pattern, as is well know [7]. The much lower maximum drain current of the non-RESURF LDMOSFET is due to the higher resistance of the drift region, compared to that of RESURF LDMOSFET. It pushes the intrinsic MOSFET into the linear operation region and quasi-saturation occurs at lower current level in non-RESURF LDMOSFET. The analysis for quasi-saturation in devices with various drift thicknesses is presented in chapter 4 in detail. The analysis is based on SOI LDMOSFET and it also applies to bulk structures.

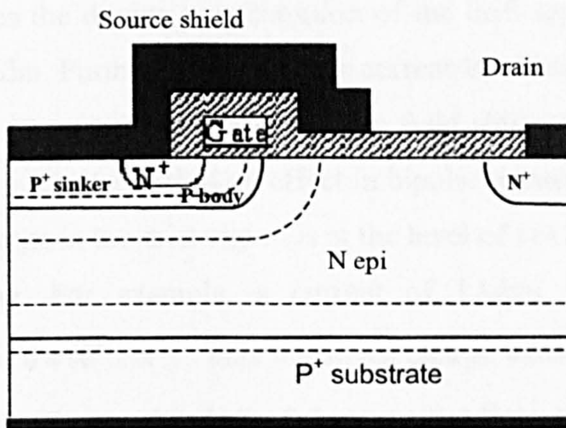


Figure 2.12 A schematic cross-section of a non-RESURF LDMOSFET.

Table 2.2 List of device parameters for RESURF and non-RESURF devices.

	RESURF device	Non-RESURF device
Gate length (μm)	0.8	0.8
Drift length (μm)	3	10
Drift doping concentration (/cm^3)	1e17	3e15
Drift region thickness (μm)	0.2	15
P epi doping concentration (/cm^3)	6e14	–
P+ Substrate doping concentration (/cm^3)	5e19	5e19

For a RESURF LDMOSFET, the voltage handling capability decreases at high current level due to Kirk effect [8]. Figure 2.14 shows the electric field distribution along the electron flow direction in the drift region under various gate voltages for RESURF device. It shows that the peak electric field is located at the drift/P body end at low gate voltage. With the increase of the gate voltage, therefore the drain current, the peak electric field at the P body/drift junction is reduced. At even higher gate voltages the peak electric field shifts to the drift/drain junction. The change of electric field distribution with gate voltages is attributed to the electrons flowing into the drift region, which change the total charge in the drift region. Figure 2.15 shows the electron concentration distribution in the drift region under various gate voltages. At low gate voltage of 0V, the drift region near P body is completely depleted with the presence of positive charges. When the concentration of the electrons flowing into the drift region reaches the doping concentration of the drift region, the electric field profile is changed to nearly flat. Further increase of the current level leads to the total charge in the drift become negative. As a result, the peak electric field shifts to the N^- drift/N^+ drain junction. This phenomenon is similar with Kirk effect in bipolar transistors [9]. According to RESURF effect, the total charge in the drift region is at the level of 1e12 cm^{-2}. A high current involves a comparable charge. For example, a current of 1A/cm involves at least a charge of $N \times d = I(v_s qW) = 6 \times 10^{11} cm^{-2}$. This negatives charge adds to the positive charge of the n-type drift region, leading to the shift of the potential lines towards the drain. It changes the optimum RESURF condition and leads to a limited on-state breakdown voltage. The other reason for peak electric field shift to drain is attributed the non-uniform current path in the drift region. Figure 2.16 shows the 2-D device structure illustrating the depletion region under V_g of 4V and 20V. At V_g of 4V, the current path width increases along the electrons flow direction. At high current level, the current path reduces along the electrons flow direction, narrower at the drain than near the P body, due to the depletion reduction near the P body region. The drain current in a neutral region, a region where the total charge is zero, is expressed as $I = Nq\mu EbW$, where N is the doping concentration, q is the unit charge, μ is the carrier mobility, E is the electric field, b is the width of current path and W is the width of the device. In the case the current path width b reduces, the electric field E increases to maintain the current continuity. For a non-RESURF LDMOSFET, the shift of electric field under high current level also occurs as shown in Figure 2.17. However, under low/medium current level of V_g 4V and 8V, the on-state breakdown voltage is higher than the off-state BV. At off-state, the breakdown occurs due to the high electric field at the P body/drift junction in a non-RESURF device. Under current flow, the total positive charge reduces and thus the peak electric field at P body/N drift junction. It leads to a slightly higher on-state breakdown voltage compared to the off-state breakdown voltage.

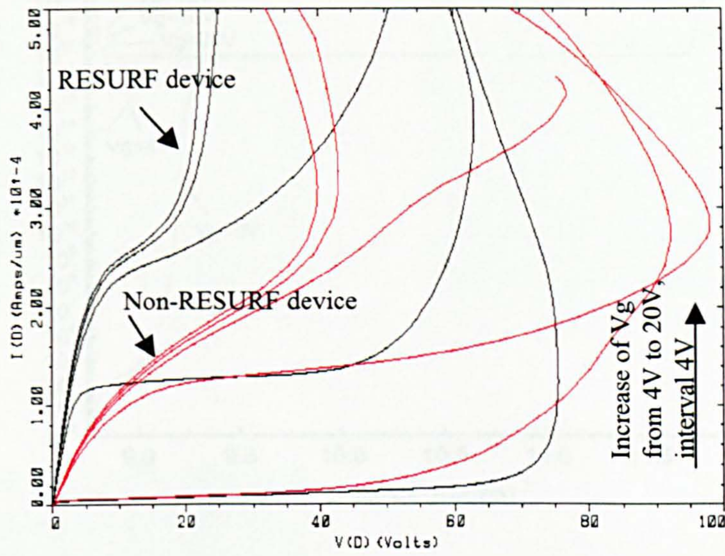


Figure 2.13 IV characteristic of RESURF and non-RESURF LDMOSFET.

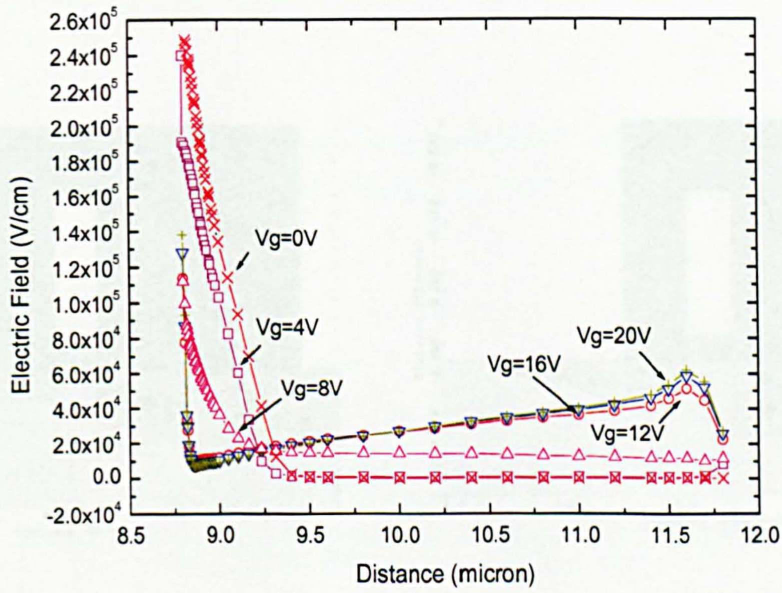


Figure 2.14 Electric field distribution in the drift region along the electrons flow direction for RESURF LDMOSFET.

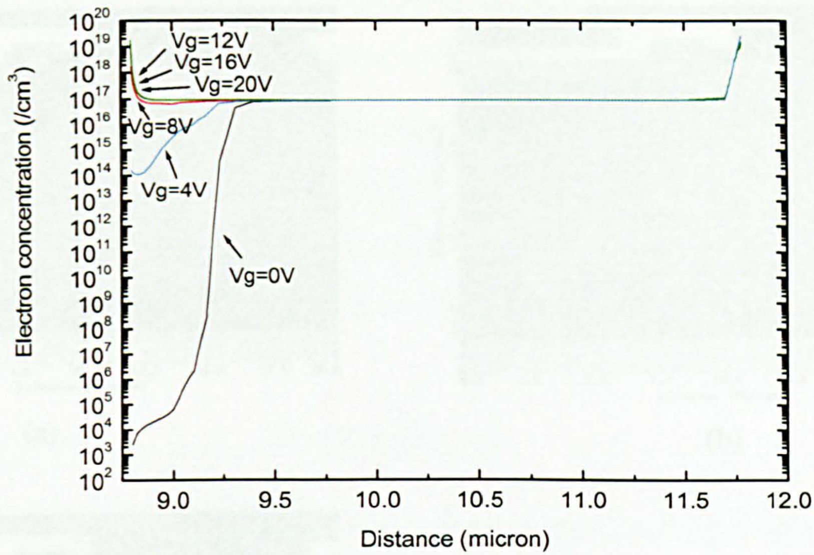


Figure 2.15 Electron concentration distribution in the drift region along the electron flow direction for RESURF LDMOSFET.

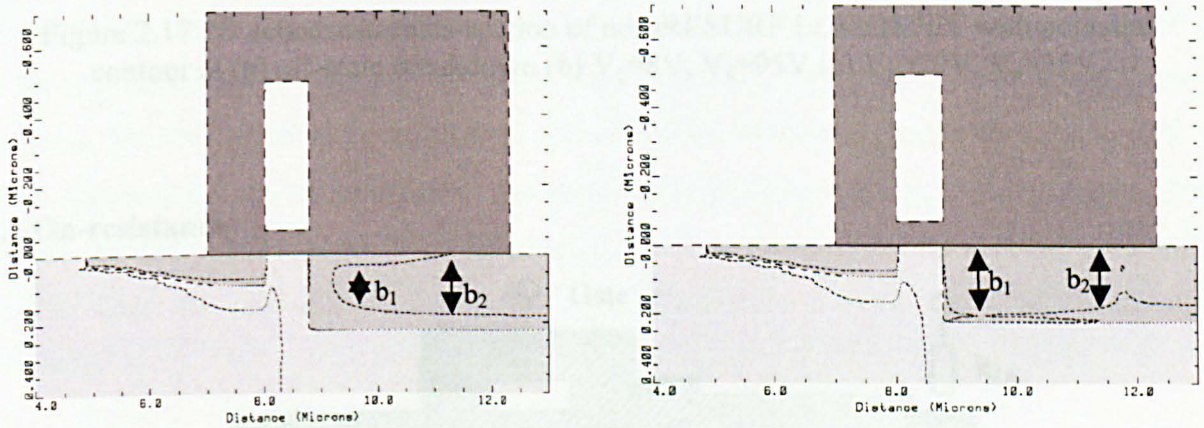
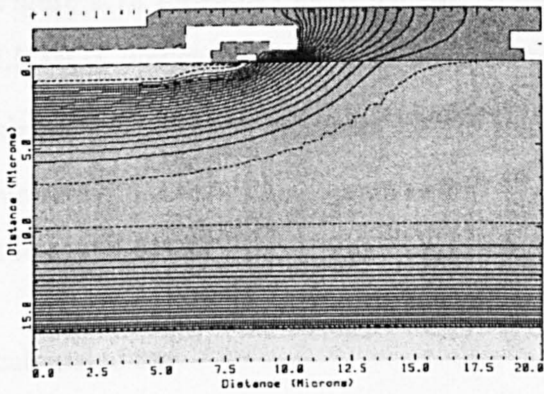
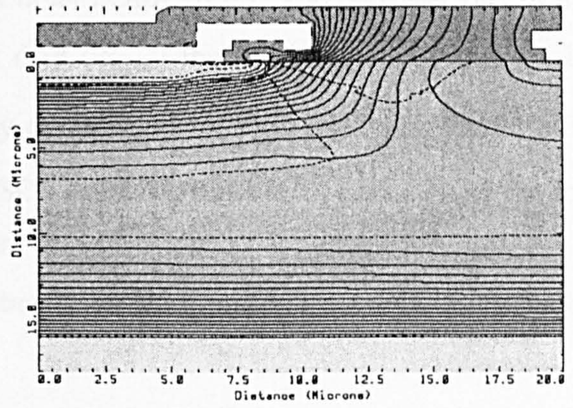


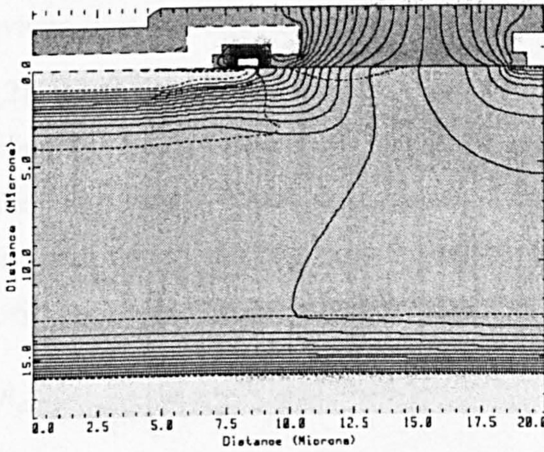
Figure 2.16 2D schematic cross-section with depletion boundary for RESURF LDMSOFET at (a) V_g=4V, V_d=10V (b)V_g=20V, V_d=10V.



(a)



(b)



(c)

Figure 2.17 2D schematic cross-section of non-RESURF LDMOSFET with potential contour at (a) off-state breakdown (b) V_g=8V, V_d=95V (c) V_g=20V, V_d=35V.

2.2 On-resistance

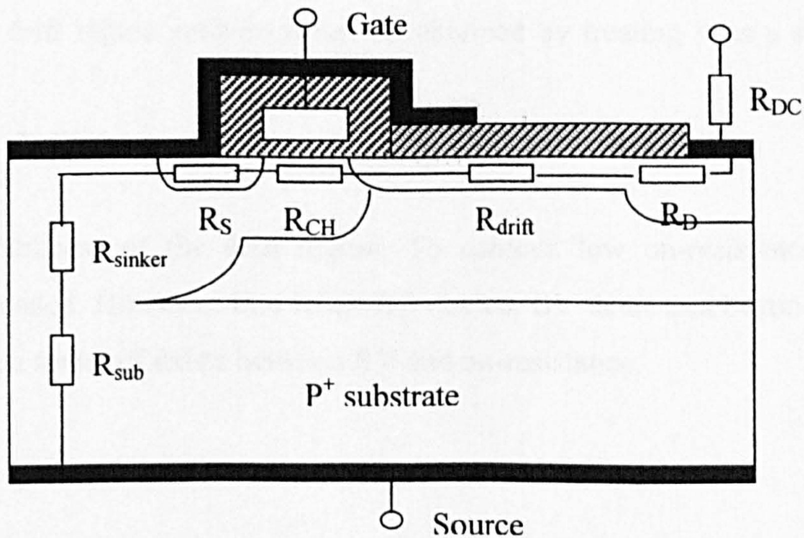


Figure 2.18 A schematic cross section RF LDMOSFET with the resistance component illustrated.

Figure 2.18 illustrates the resistance components in an LDMOSFET. The on-resistance of the LDMOS device is the sum of the resistance of drift (R_{drift}) the MOS channel (R_{ch}) the P$^+$ sinker ($R_{\sin ker}$), the substrate (R_{sub}), the heavily doped source (R_S) and drain (R_D) in bulk structure and the drain contact region (R_{DC}). In SOI structure, the source contact is at the top surface of device. Therefore, R_{sinker} does not exist.

The channel resistance is gate and drain bias dependent. In the linear region, it can be calculated by,

$$R_{ch} = \left(\frac{L_g}{W_g}\right)\left(\frac{1}{\mu_n C_i (V_g - V_T)}\right), \qquad \text{Equation 2-6}$$

where μ_n is the effective carrier mobility which depends on the electric field in the channel [2]. When devices are operated with gate voltage much higher than the threshold voltage, the channel resistance becomes negligible and the on-resistance is dominated by the resistance of the long, lightly-doped drift region. Assuming the current low along a semi-circular path in the drift region, starting from the current source flowing to a current sink, the resistance of the drift region can be described as [10]

$$R_{drift} = \frac{\rho}{W_g \pi}\left[\ln\left(\frac{L - r_1}{r_1}\right) + \ln\left(\frac{L - r_2}{r_2}\right)\right] \qquad \text{Equation 2-7}$$

where ρ is the resistivity of the drift region, L is the effective drift region length, W_g is the device width, and r_1 is the effective radii of the current source at the end of the channel, and r_2 is the effective radii of the current sink at the n$^+$ contact, respectively. This model further assumes that the current flow in the drift region is semi-circular in nature, originating from a point source at the end of the channel and terminating at a point sink in the drain region. In a simpler model which assumes uniform current flow through the drift region rather than semi-circular flow, the drift region resistance can be obtained by treating it as a silicon resistor, whereby

$$R_{drift} = \rho\frac{L}{tW} \qquad \text{Equation 2-8}$$

where t is the thickness of the drift region. To achieve low on-resistance a high drift concentration is needed. However, in a RESURF device, BV decreases beyond the optimum charge. Therefore, a trade off exists between BV and on-resistance.

2.3 Transconductance

LDMOSFET can be considered as a drift region in series with an intrinsic MOSFET. The drift region are modelled as a JFET or a resistance in the equivalent circuit of a LDMOSFET [11]-[13]. The intrinsic MOSFET determines the transconductance g_m of the LDMOSFET [13]. To analyse the g_m characteristic of LDMOSFET, it is necessary to understand the g_m characteristics of a basic MOSFET.

2.3.1 Transconductance characteristics of MOSFET

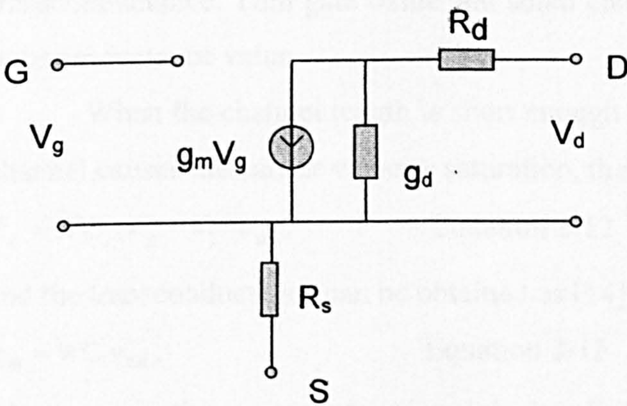


Figure 2.19 DC or Low frequency small signal equivalent circuit of MOSFET [2].

Figure 2.19 shows a DC or low frequency small signal equivalent circuit of MOSFETs. G_d is drain-source conductance, defined as $G_d = \frac{\partial I_d}{\partial V_d}$. R_d and R_s are the drain and source region contact resistance. Transconductance g_m reflects the gate control capability of the device and is an important figure of merit for MOSFET. Transconductance of MOSFET is defined as

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_{dD}} \qquad \text{Equation 2-8}$$

where V_g and V_d are gate and drain voltage, respectively. I_d is the drain current. For a MOSFET with uniform doping channel region, the transconductance in linear region $V_d \ll (V_g - V_T)$, is given by

$$g_m = \left(\frac{W}{L}\right)\mu_n C_i V_d . \qquad \text{Equation 2-9}$$

While in saturation region, when channel is pinched off at drain, the transconductance is determined by:

$$g_m = \left(\frac{W}{L}\right)\mu_n C_i (V_g - V_T),$$ Equation 2-10

$$C_i = \frac{\varepsilon_{ox}}{t_{gox}},$$ Equation 2-11

where W/L is the gate width to length ratio, C_i is the unit-area gate oxide capacitance, μ_n is the effective carrier mobility in the channel region, ε_{ox} is the permitivity of silicon oxide and t_{gox} the gate oxide thickness.

From the above equation, it is obvious that transconductance in the saturation region is in a linear relationship with the gate voltage. At a certain gate bias, gate width to length ratio W/L and unit area gate oxide capacitance C_i are the critical factors determining the transconductance. Thin gate oxide and small channel length are usually used to obtain a high transconductance value.

When the channel length is short enough that the longitudinal electrical field along the channel causes the carrier velocity saturation, the drain current is given by

$$I_d = WC_i(V_g - V_T)v_{sat},$$ Equation 2-12

and the transconductance can be obtained as [14]

$$g_m = WC_i v_{sat},$$ Equation 2-13

where v_{sat} is the carrier saturation velocity, 1e7 cm/s for silicon. Transconductance reaches the maximum value, independent of gate voltage, when the carrier velocity saturates. Comparing Equation 2-9 and Equation 2-13, it can be seen that when $\frac{V_g - V_T}{L} = \frac{v_{sat}}{\mu_n} = E_c$, transconductance transfers from the non-velocity saturation region to velocity-saturation region [14]. The transfer occurs when the gate voltage reaches the value given by the following

$$V_g = E_C L + V_T$$ Equation 2-14

From this equation, a shorter channel length leads to the transition occurring at a lower gate voltage.

2.3.2. Transconductance for LDMOSFET

LDMOSFET has g_m characteristics different from that of MOSFET with the same channel region design. For a comparison, both devices have been simulated using 2D device simulator MEDICI and g_m characteristics for both devices are plotted in Figure 2.20. MEDICI models

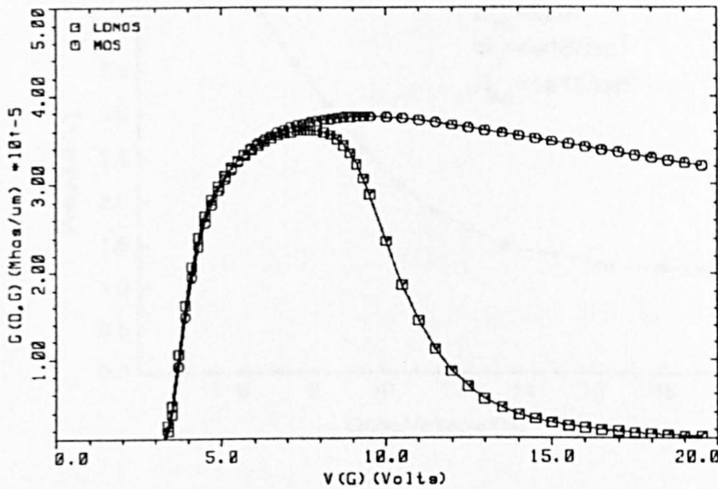


Figure 2.20 Transconductance of LDMOSFET and MOSFET.

used in the device simulation take into account the dependence of mobility on impurity concentration, phonon scattering, surface roughness scattering, and charged impurity scattering, carrier generation due to impact ionisation, Shockley-Read-Hall recombination with fixed lifetimes, Auger recombination and band gap narrowing. Both devices are biased in the saturation region at low gate voltages, with drain voltage 10V for the LDMOSFET, and 4V for the MOSFET. It is shown that for both devices, the transconductance initially increases with the gate voltage and it can be described by Equation 2-10. With the gate voltage increasing further, transconductance for both devices remain constant within a range of gate voltage due to carrier velocity saturation in the MOS channel region. Here, the g_m characteristics are described by Equation 2-13. The further increase of the gate voltage leads to a steep fall-off of transconductance in the LDMOSFET, in comparison to a gradual reduction of g_m in MOSFET.

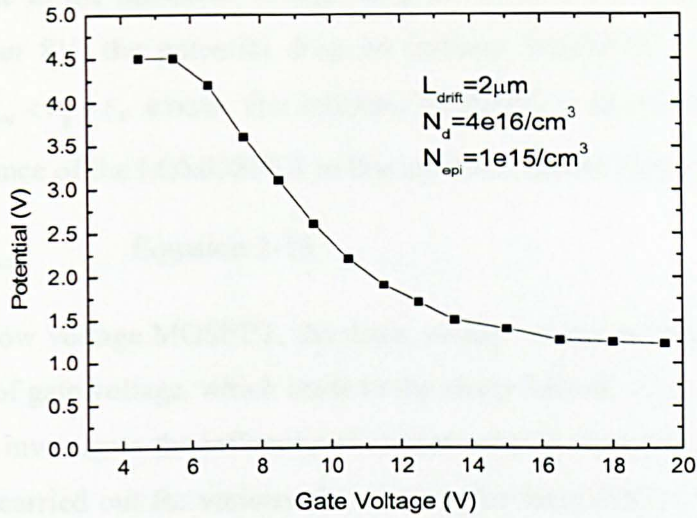


Figure 2.21 Potential drop across the intrinsic MOS channel versus gate voltage in LDMOSFET.

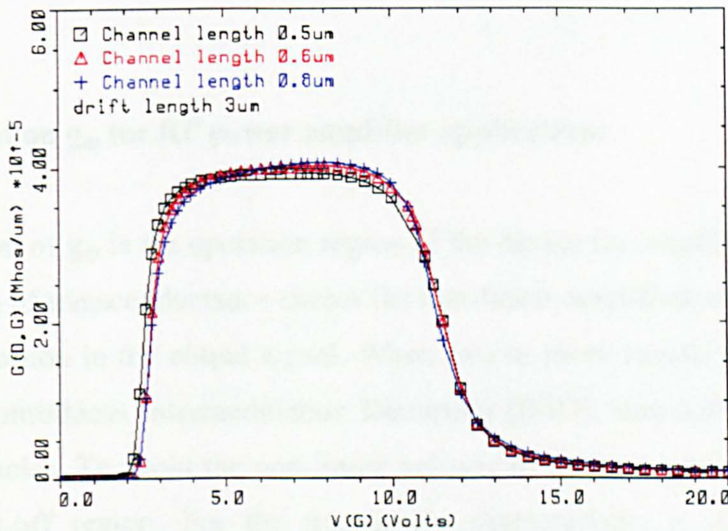


Figure 2.22 Transconductance characteristics for devices with channel length 0.5μm, 0.6μm and 0.8μm.

The sharp fall-off of g_m in LDMOSFET is attributed to the presence of the drift region, which changes the potential drop on the intrinsic MOSFET. Figure 2.21 shows the relationship between V_g and the potential at channel/drift junction, V_{mos}, which is the drain potential applied on the intrinsic MOSFET. It is shown that a high percent of potential is dropped in the MOS channel region at low gate voltages. The intrinsic MOSFET is in the saturation operation region. With the increase of gate voltage, less potential is dropped in the

channel region due to the increased voltage drop in the drift. At even higher gate voltages, starting from about 8V, the potential drop on intrinsic MOSFET is low enough that the relationship of $V_{mos} < V_g - V_T$ exists. The intrinsic MOSFET is in the linear operation region. The transconductance of the LDMOSFET in this situation can be expressed as,

$$g_m = \left(\frac{W}{L}\right)\mu_n C_i V_{mos}. \qquad \text{Equation 2-15}$$

Different from a low voltage MOSFET, the drain voltage of the intrinsic MOSFET decreases with the increase of gate voltage, which leads to the sharp fall-off of g_m.

To further investigate the influence of carrier velocity saturation on g_m characteristics, simulations were carried out for various channel lengths from 0.5μm, 0.6μm to 0.8μm, with results plotted in Figure 2.22. The g_m characteristics are nearly the same for these three channel lengths, as predicted by Equation 2-13 under velocity saturation. Therefore, reducing channel length may not bring benefit to tansconductance. However, it leads to lower input capacitance hence is beneficial for a higher cut-off frequency, as will be shown in the section 2.4.

2.3.3 Requirement on g_m for RF power amplifier applications

The constant region of g_m is the operation region of the device for amplification applications. The fall-off region of transconductance causes the non-linear amplification of the input signal, which causes distortion in the output signal. When two or more signals applied at the input, the non-linearity introduces Intermodulation Distortion (IMD), sum-and-difference products of applied frequencies. To avoid the non-linear behaviour, the transistors are usually backed off from the fall-off region. For the transistor's characteristic, it is desirable that the transconductance is constant, wide and with a high value.

2.4 Capacitance in RF LDMOSFET

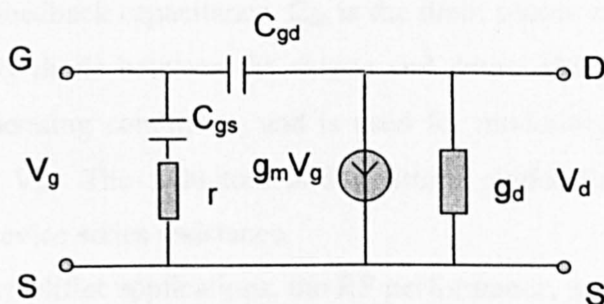


Figure 2.23 High frequency equivalent circuit of MOSFET [2].

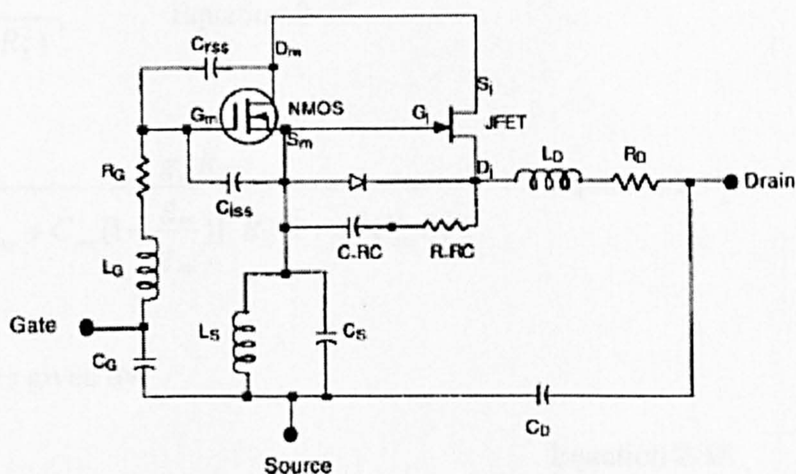


Figure 2.24 Lumped circuit model of RF LDMOSFET [13].

Under high frequency AC operation, the influence of capacitance on the device performance is not negligible. In this case, gate source capacitance C_{gs} and gate drain capacitance C_{gd} are added to the low frequency equivalent circuit of low voltage MOSFETs, as shown in Figure 2.23 The ohmic resistances of source and drain region are omitted in this figure. To analysis the RF performance of LDMOSFET, a circuit model for high frequency application is needed. Figure 2.24 shows a lumped circuit model for RF LDMOSFET proposed by Malay Trivedi etc [13]. The nMOSFET models the main device. The JFET is used to model the drift region. The C_{iss} is the input capacitance, C_{rss} is the feedback capacitance and C_{oss} is the output capacitance. These capacitances are expressed as

$C_{iss} = C_{gs} + C_{rss}$ Equation 2-20

$C_{rss} = C_{gd}$ Equation 2-21

$C_{oss} = C_{ds} + C_{rss}$ Equation 2-22

where C_{gs} is the capacitance between gate and source. C_{gd} is the capacitance between gate and drain, also referred as feedback capacitance. C_{ds} is the drain source capacitance. The diode is used to model the body diode between the source and drain. This diode is always reverse biased under actual operating conditions, and is used for modelling the variation of output capacitance C_{oss} with V_{ds}. The inductors and resistors model the contact and bonding parasitics, along with device series resistance.

For RF power amplifier applications, the RF performance, such as output power level, power gain and cut-off frequency, are functions of input capacitance C_{iss}, feedback capacitance C_{rss} and output capacitance C_{oss}. Based on the lumped equivalent circuit of RF LDMOSFET in Figure 2.24 the output power and power gain can be expressed as [13]

$$P_{out} = \frac{V_{in}^2 g_m^2 R_L}{2(1+\omega^2 C_{oss}^2 R_L^2)}, \quad \text{Equation 2-16}$$

$$G_P = \frac{P_{out}}{P_{in}} = \frac{g_m^2 R_L}{\omega^2 [C_{iss} + C_{rss}(1+\frac{g_m}{g_{mj}})]^2 R_G (1+\omega^2 C_{oss}^2 R_L^2)} \quad \text{Equation 2-17}$$

Cut-off frequency is given by

$$f_t = \frac{g_m}{2\pi C_{in}} \quad \text{Equation 2-18}$$

Taking into account the Miller effect in inverting amplifiers, C_{in} is given by

$$C_{in} = C_{gs} + (1 - A_V)C_{rss} = C_{iss} - A_V C_{rss} \quad \text{Equation 2-19}$$

In above equation, the feedback capacitance C_{rss} is increased by $(1-A_v)$ times at the input circuit. For any inverting amplifier (phase shift of 180° between input and output leading to negative value of A_V), the input capacitance is increased by a Miller effect capacitance, whose value is determined by the feedback capacitance and the gain of the amplifier as shown in Equation 2-20 [15].

$$C_M=(1-A_V)C_f \quad \text{Equation 2-20}$$

where C_f is feedback capacitance, C_M is the Miller effect capacitance and A_V is the gain of the amplifier. Figure 2.25 demonstrates the impact of Miller effect capacitance, where R_i is equivalent input resistance.

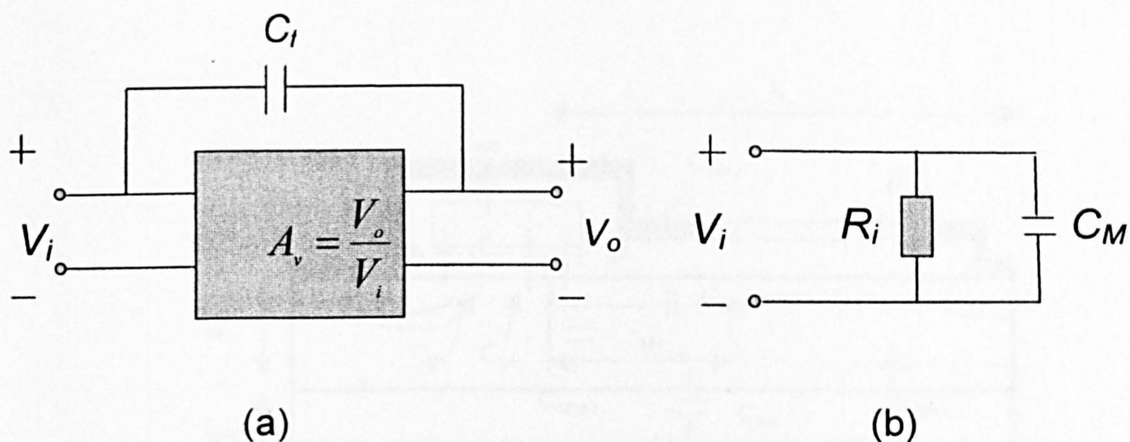


Figure 2.25 (a) circuit network with feedback capacitance C_f (b) equivalent input circuit demonstrating the impact of Miller effect capacitance.

According to Equation 2-16 to Equation 2-18, reduction on C_{iss}, C_{rss} and C_{oss} leads to higher output power, power gain and higher cut-off frequency. Generally, to improve the device performance, capacitance needs to be reduced to a minimum. In this section, the capacitance in RF LDMOSFET on a SOI substrate is analysed. The influence of device physical parameters, drift region doping concentration, substrate doping concentration, SOI thickness, buried oxide thickness and drift region length on parasitic capacitance are investigated based on a SOI RF LDMOSFET.

2.4.1 Capacitance in SOI RF LDMOSFET

The capacitors in SOI LDMOSFET structure are shown in Figure 2.26. The gate source capacitor C_{gsi}, gate drain capacitor C_{gdi}, depletion capacitors C_{ddep1} and C_{ddep2}, depletion capacitor C_{sub}, and the buried oxide capacitor C_{box} are identified in the figure. C_{gsi} (C_{gdi}), which are bias-dependent, reflects the change of the channel charge in correspondence with the variation of the voltage between gate and source (gate and drain). The depletion capacitor C_{sub} is formed in P type substrate, when the drain is applied a positive voltage and the substrate is grounded.

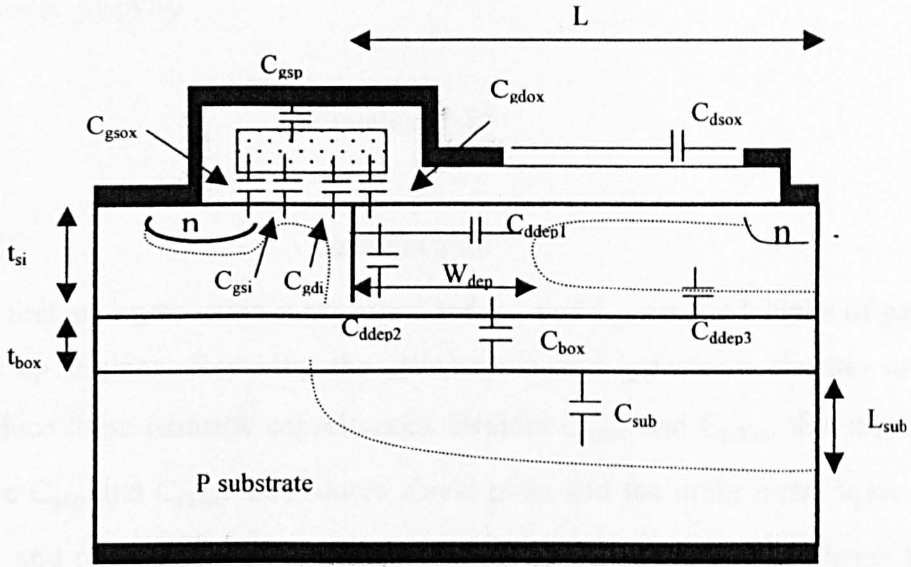


Figure 2.26 A schematic section of SOI RF LDMOS with the capacitor components illustrated.

It should be noted that the capacitors C_{ddep1} and C_{ddep2} represent the same depletion region in the drift. However, this depletion region has a different contribution to the feed-back capacitance C_{rss} and output capacitance C_{oss} in the form of C_{ddep1} and C_{ddep2}. The expression for C_{ddep1} and C_{ddep2} are given by,

$$C_{ddep1} = {(W \cdot t_{si})\varepsilon_{si}}/{W_{dep}}, \qquad \text{Equation 2-23}$$

$$C_{ddep2} = {(W \cdot W_{dep})\varepsilon_{si}}/{t_{si}} \qquad \text{Equation 2-24}$$

The depletion width is bias dependent. However, due to the two-dimensional feature, it is difficult to obtain an analytic expression for it. The increase of the top silicon thickness t_{si} and the decrease of depletion width W_{dep} lead to the increase of C_{ddep1} and have the opposite influence to C_{ddep2}.

The capacitor formed by overlap of electrodes and the capacitors between metal electrodes in a short distance contribute to the parasitic capacitance. In this structure, the parasitic capacitors include gate source oxide capacitor C_{gsox}, gate drain oxide capacitor C_{gdox},

formed by the overlap of the gate electrode with the source and drift implantation region. Their capacitance is given by

$$C_{gsox} = WL_{gs} \cdot C_i \qquad \text{Equation 2-25}$$

and

$$C_{gdox} = WL_{gd} \cdot C_i \qquad \text{Equation 2-26}$$

where C_i is the unit area gate oxide capacitance and L_{gs} and L_{gd} are the lengths of gate source and drain overlap regions. Reducing the gate/source and gate/drain overlap area is an approach to reduce these parasitic capacitances. Besides C_{gsox} and C_{gdox}, the other parasitic capacitances are C_{gsp} and C_{dsox}. The source shield plate and the drain metal layer form the capacitor C_{dsox} and overlap of source shield plate over the gate electrode forms the oxide capacitor C_{gsp}. However, the source plate shields the gate from drain, leading to a reduction of the gate drain capacitance C_{gd} [16].

All the capacitors in the device contribute to the C_{iss}, C_{rss} and C_{oss}. In the device, C_{rss} is given by,

$$C_{rss} = C_{gd} = C_{gdi} + C_{gdp} \qquad \text{Equation 2-27}$$

$$C_{gdp}^{-1} = C_{gdox}^{-1} + C_{ddep1}^{-1} \qquad \text{Equation 2-28}$$

From above equations it is shown that a decrease C_{ddep1} will lead to the decrease of C_{rss}.

The input capacitance is given by,

$$C_{iss} = C_{gs} + C_{gd} = C_{gsp} + C_{gsox} + C_{gsi} + C_{gd} \qquad \text{Equation 2-29}$$

In comparison with C_{gs}, it is found in the simulation that the contribution of C_{gd} to input capacitance is negligible. Actually the input capacitance is mainly determined by the capacitance between the source and gate metal electrodes.

Output capacitor C_{oss} is expressed as in Equation 2-30 and C_{ds} is composed of two capacitances, drain top source capacitance C_{ds1} and drain substrate capacitance C_{ds2}. C_{ds2} can be calculated as two capacitance $C_{ds}^{'}$ and $C_{ds}^{''}$ in parallel according to the contribution of C_{ddep2} and C_{ddpe3}.

$$C_{oss} = C_{ds} + C_{gd} = (C_{ds1} + C_{ds2}) + C_{gd} \qquad \text{Equation 2-30}$$

$$C_{ds2} = C_{ds}^{'} + C_{ds}^{''} \qquad \text{Equation 2-31}$$

$$C_{ds}^{'\,-1} = C_{ddep2}^{-1} + C_{box1}^{-1} + C_{sub1}^{-1} \qquad \text{Equation 2-32}$$

$$C_{ds}^{''\,-1} = C_{ddep3}^{-1} + C_{box2}^{-1} + C_{sub2}^{-1} \qquad \text{Equation 2-33}$$

where

$$C_{box1} = {W \cdot W_{dep} \cdot \varepsilon_{ox}} / {t_{ox}}$$ Equation 2-34

$$C_{sub1} = {W \cdot W_{dep} \cdot \varepsilon_{si}} / {L_{sub}}$$ Equation 2-35

$$C_{box2} = {W \cdot (L - W_{dep}) \cdot \varepsilon_{ox}} / {t_{ox}}$$ Equation 2-36

$$C_{sub2} = {W \cdot (L - W_{dep}) \cdot \varepsilon_{si}} / {L_{sub}}$$ Equation 2-37

where L_{sub} is the depletion depth in the silicon substrate layer from buried oxide/silicon interface and L is the total length of the drift region. According to Equation 2-30 to Equation 2-34 and Equation 2-36, an increase of the buried oxide thickness will reduce the capacitance of C_{ds2} and therefore output capacitance C_{oss}.

In a RF LDMOSFET on bulk substrate, the buried oxide is not present in the device structure. As a result, the difference in capacitance lies in the buried oxide related capacitance C_{box} and C_{sub} being replaced by drift/epi junction capacitance.

2.4.2 Influence of device structural parameters on capacitance characteristics

The influence of the device geometric and physical parameters on capacitance characteristics are simulated using 2-D device simulator MEDICI, based on the device structure shown in Figure 2.26. The top silicon thickness, buried oxide thickness, drift doping concentration, drift length and substrate doping concentration are varied in the study.

2.4.2.1 Influence of top silicon on capacitance characteristics

In Figure 2.27 is shown C_{oss} and C_{rss} versus drain voltage with top silicon thickness 0.2μm, 0.5μm and 1.0μm. At V_d=0, the devices have the same C_{rss} value of 1.2e-16F/μm. With the increase of V_d, C_{rss} decreases with the increase of V_d. It decreases quicker for thinner T_{si}. For T_{si} of 0.2μm and 0.5μm, C_{rss} reaches a constant value at drain voltage of 7.5V and 18V, respectively. C_{rss} of T_{si} of 1.0μm does not reach a constant value within the range of applied drain voltage.

The decrease of C_{rss} with V_d is due to the spread of the depletion region from channel/drift junction towards drain with the increase of V_d, leading to a decrease of C_{ddepl} and therefore a decrease of C_{rss}, according to Equation 2-27 and Equation 2-28. When the

drift region is depleted totally, the C_{rss} reaches the minimum and remains constant with the further increase of drain voltage. On a thinner top silicon layer, the depletion from channel/drift junction extends further towards drain region. As a result, C_{rss} decreases quicker and reaches the minimum value at a lower drain voltage.

C_{oss} of these three devices show the similar trend as C_{rss}, all decreasing with the drain voltage. At V_d of 0V, a higher T_{si} shows a higher C_{oss}, with T_{si} of 0.2μm, 0.5μm and 1.0μm corresponding to C_{oss} of 5.36e-16F/μm, 6.09e-16F/μm and 7.3e-16F/μm, respectively. For T_{si} of 0.2μm and 0.5μm, C_{oss} reach the constant value at drain voltage of 7.5V and 18V, which are the same as in the case of C_{rss}. Similarly, C_{oss} of T_{si} of 1.0μm does not reach a constant value within the range of applied drain voltage. As C_{rss} is a component of C_{oss}, the change of C_{oss} and C_{rss} with V_d show similar trend. The difference of C_{oss} at V_d=0 for various T_{si} comes from the difference in drain/top source capacitance C_{ds1}, shown in Figure 2.28. At V_d of 0V, for T_{si} of 0.2μm, 0.5μm and 1.0μm C_{ds1} are 1.62e-16F/μm, 2.35e-16F/μm and 3.57e-16F/μm, respectively. For a thicker top silicon, C_{ds1} is higher, due to the larger area of the capacitor C_{ddepl}. C_{ds1} shows the similar trend with C_{oss} and C_{rss}, decreasing with the increase of drain voltage. The decrease of the C_{ds1} with V_d comes from the decrease of C_{ddepl} with the expending of the depletion region from channel/drift junction towards drain.

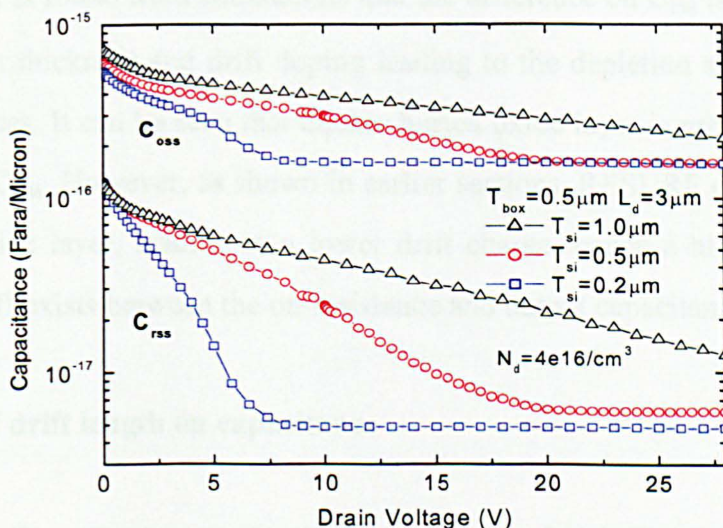


Figure 2.27 C_{rss} and C_{oss} versus drain voltage with top silicon thickness varying from 1.0μm, 0.5μm and 0.2μm.

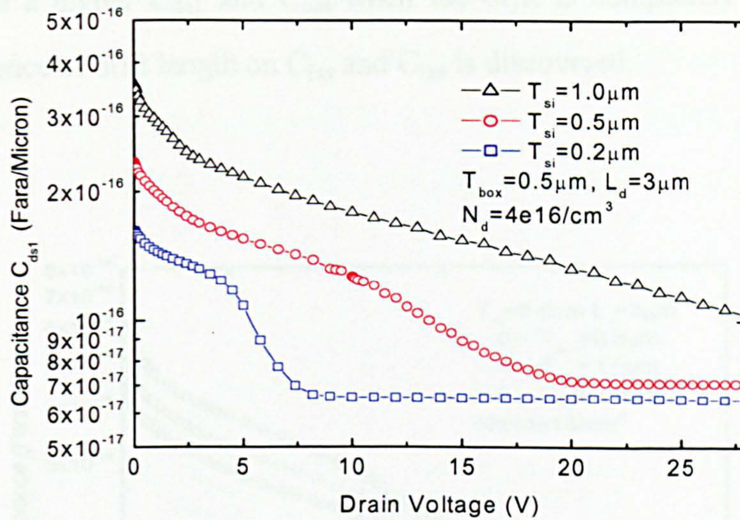


Figure 2.28 C_{ds1} versus drain voltage with top silicon thickness varying from 1.0μm, 0.5μm to 0.2μm.

2.4.2.2 Influence of buried oxide thickness on capacitance

The devices with buried oxide thickness of 0.5μm, 1.0μm, 2.0μm are compared to investigate the influence of buried oxide layer thickness on capacitance characteristics. As shown in Figure 2.29, C_{oss} decreases with the increase of t_{ox}, due to the reduction of buried oxide capacitance. Also, it is found from simulations that the difference on C_{rss} is negligible, due to the same top silicon thickness and drift doping leading to the depletion situation. C_{iss} is the same for three devices. It can be seen that thicker buried oxide layer is preferable for a lower output capacitance C_{oss}. However, as shown in earlier sections, RESURF effect is weaker for a thicker buried oxide layer, leading to a lower drift charge, hence a higher on-resistance. Therefore, a trade off exists between the on-resistance and output capacitance C_{oss}.

2.4.2.3 Influence of drift length on capacitance

Figure 2.30 shows the output capacitance characteristics for devices with different drift length. It is obvious that device with longer drift length has a higher C_{oss} due to the larger area of capacitance components. Minimizing the drift length whilst sustaining a desired breakdown voltage is necessary to keep C_{oss} to a minimum. However C_{oss} for shorter channel length saturates with a higher value. It is due to the shorter depletion length W_{dep}, leading to a higher

C_{ddpel} and therefore a higher C_{ds1} and C_{oss} when the drift is completely depleted. In the simulation, no influence of drift length on C_{iss} and C_{rss} is discovered.

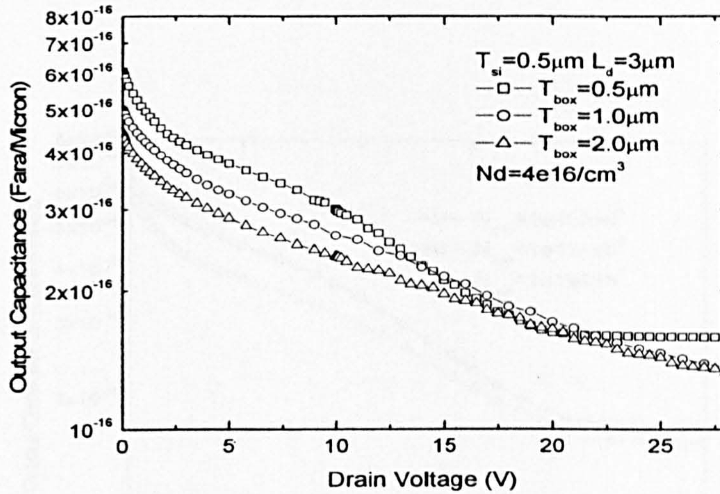


Figure 2.29 C_{oss} versus drain voltage with buried oxide thickness as a parameter.

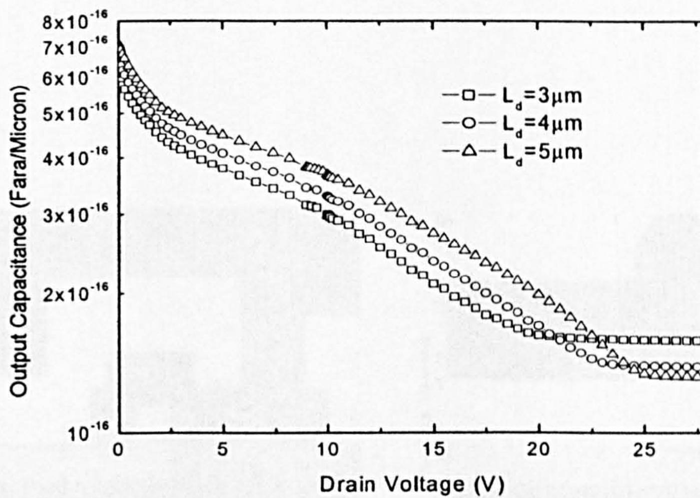


Figure 2.30 Output capacitance C_{oss} versus drain voltage with drift length as a parameter.

2.4.2.4 Influence of substrate doping concentration on capacitance

The output capacitance of devices with substrate doping $1e15cm^{-3}$, $1e17cm^{-3}$ and $1e19cm^{-3}$ are shown in Figure 2.31. Device with $1e15cm^{-3}$ substrate doping has the lowest C_{oss}. The

difference in C_{oss} for N_{sub} of 1e17cm^{-3} and N_{sub} of 1e19cm^{-3} is negligible. The lower C_{oss} in substrate of 1e15cm^{-3} is because of the larger depletion depth in its substrate region than that in the other two devices, as shown in Figure 2.32. This leads to the lower C_{sub} for substrate of 1e15cm^{-3}, hence lower C_{oss}. These results show that high resistivity substrate is preferable to obtain a low C_{oss}.

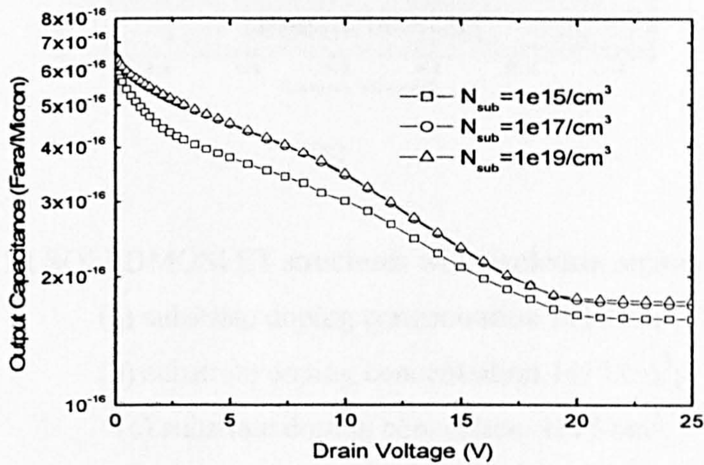
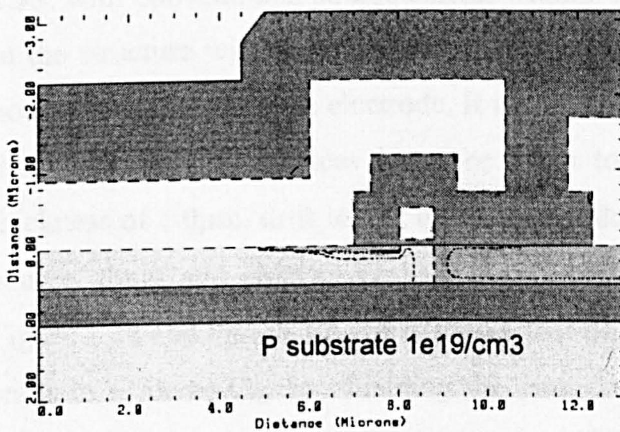
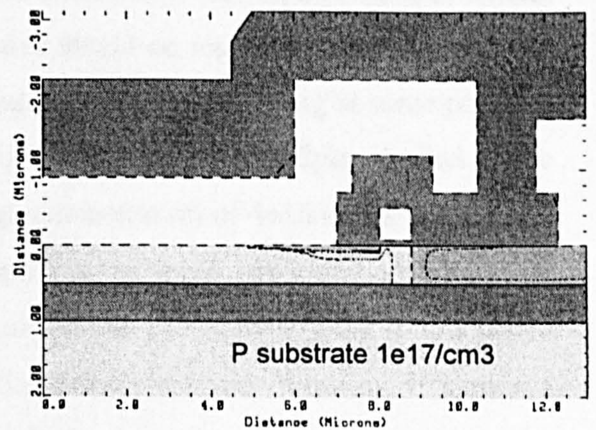


Figure 2.31 Output capacitance C_{oss} characteristics with substrate doping concentration as a parameter.



(a)



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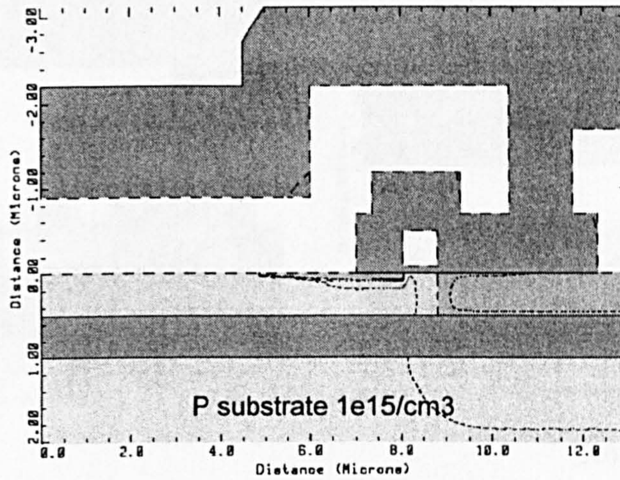
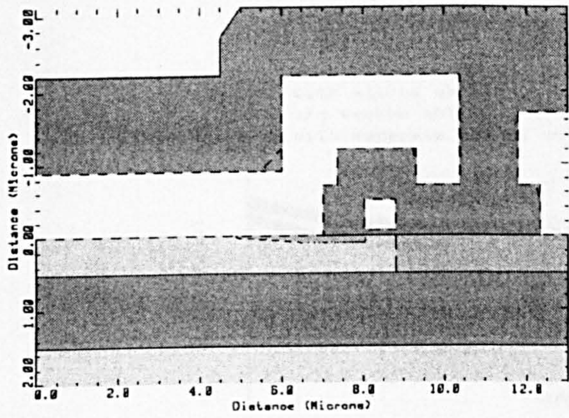


(c)

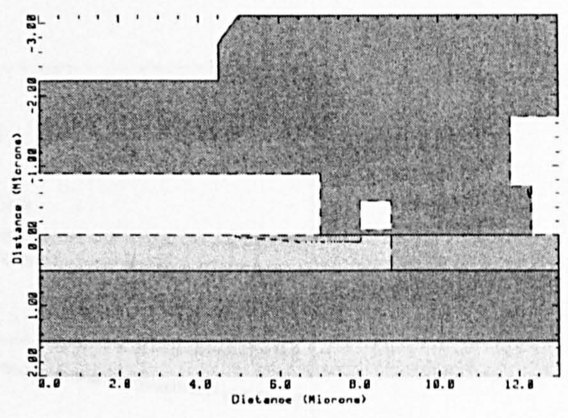
Figure 2.32 SOI LDMOSFET structures with depletion region shown for
(a) substrate doping concentration 1e19/cm^3;
(b) substrate doping concentration 1e17/cm^3;
(c) substrate doping concentrate 1e15/cm^3.

2.4.2.5 Influence of source shield on capacitance

Three device structures are used to investigate the influence of source shield on the capacitance characteristic. The schematic cross sections of the structures are shown in Figure 2.33, with conventional source shield, without source shield and with separate source shield. In the structure with separate source shield, the source shield on top of the drift region does not overlap with the gate electrode. It works as a source shield by grounding at some point on the wafer. All the devices have the same top silicon thickness of 0.2μm, buried oxide thickness of 1.0μm, drift length of 3μm, drift doping concentration of 4e16/cm^3 and the same source, drain and channel design. The C_{iss}, C_{rss} and C_{oss} of three structures are shown in Figure 2.34 and Figure 2.35. It is shown that the incorporation of a conventional source shield leads to a lower C_{rss} by shielding the gate from the drain electrode. Whereas, it causes a higher C_{iss}, due to the overlap of source shield with the gate electrode. Compared to the conventional source shield structure, a separate source shield leads to a lower C_{iss}, due to the elimination of gate/source shield overlap, while it maintains the shielding effect leading to a low C_{rss}.



(a)



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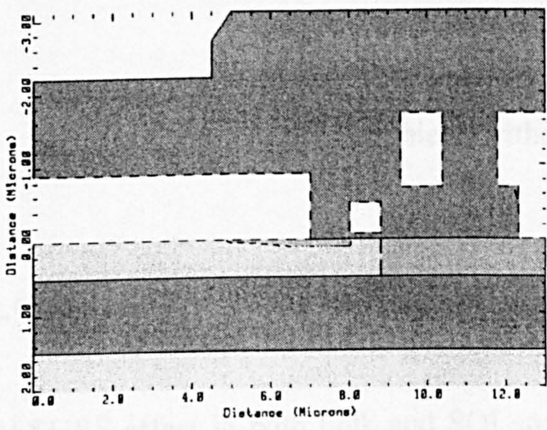

(c)

Figure 2.33 Schematic cross-sections of SOI RF LDMOSFETs (a) with source shield extending over the gate electrode on top of the drift region (b) without source shield (c) with separate source shield.

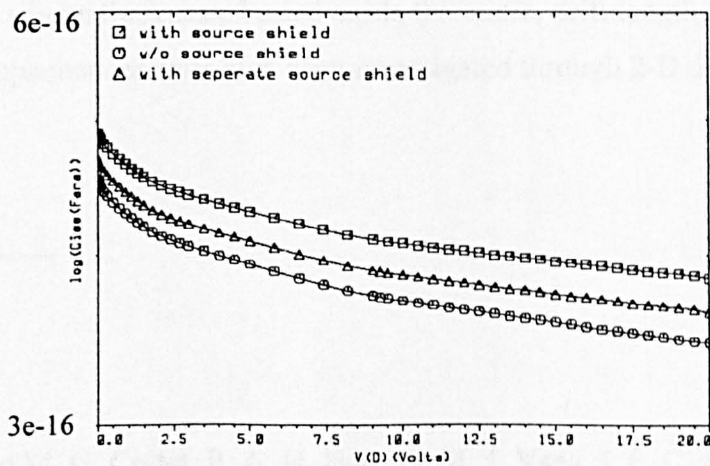

Figure 2.34 C_{iss} versus drain voltage for RF LDMOSFOET with conventional source shield, without source shield and with separate source shield.

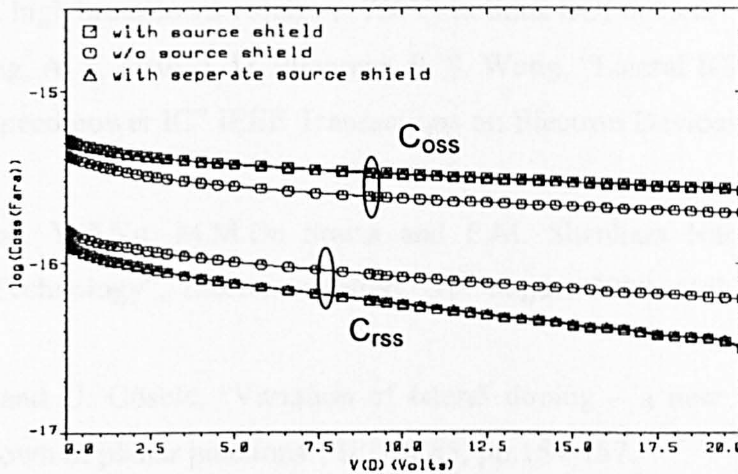

Figure 2.35 C_{rss} and C_{oss} versus drain voltage for structures with conventional source shield, without source shield and with separate source shield.

2.5 Summary

RESURF effect in both bulk and SOI structure have been discussed. It is revealed that the buried oxide thickness has a strong influence on the optimum RESURF condition. A thinner buried oxide layer leads to a higher drift dose for the optimum RESURF condition. Influence of source shield on ideal RESURF has been investigated. The introduction of source shield influences the potential distribution in the drift region. Therefore, a linearly doped drift is not ideal for RF LDMOSFET in which a source shield is present. On-resistance, transconductance and CV characteristics have been analysed. The influence of device geometric and physical parameters, the top silicon thickness, buried oxide thickness, drift length and substrate doping concentration, on capacitances have also been investigated through 2-D device simulations.

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Chapter 3 Self-Heating In RF LDMOSFET

Abstract

In this chapter, the mechanism of self-heating, components of thermal resistance and electro-thermal simulation boundaries are introduced followed by the analysis of the influence of gate and drain biases on self-heating of RF LDMOSFET. The simulated I-V and transconductance characteristics under self-heating are presented and compared with those without self-heating effect. The simulations show that the non-isothermal transconductance decreases from the isothermal transconductance. A novel structure based on back-etch technology is proposed in order to improve self-heating. Electro-thermal simulations on the back-etch structure are carried out and the results are compared to a conventional device structure. It shows that the back-etch device alleviates self-heating effect with improvement in the negative differential conductance and transconductance fall-off.

3.1 Introduction

Self-heating phenomenon is a major concern in power devices. Power dissipation in the device causes heat generation, which leads to a temperature rise in the device. Device characteristics are sensitive to the temperature as many underlying variables change exponentially with it, such as carrier mobility, carrier saturation velocity and junction leakage current [1]. In addition, the resistivity of silicon also increases with the temperature due to mobility reduction as a result of increased phonon scattering. Due to these, device characteristics under self-heating deviate from those under room temperature. It has been known that self-heating is manifested as negative differential conductance in MOSFET I-V characteristics [2,3]. In RF applications, devices under self-heating are found to deliver less output power than devices in iso-thermal situation [4]. To obtain the device characteristics without self-heating, devices are usually measured under pulsed instead of constant excitation condition [5]. In short channel MOSFET's, self-heating also causes higher leakage current under alleviated temperature, which in return, leads to higher impact ionization. This leads to the turn on of the parasitic bipolar transistor and the premature breakdown.

Another problem caused by self-heating is interconnect reliability. Electromigration in interconnect lines occurs when the metal atoms move along the current path under a high current density. Voids and hillocks resulted may cause line opens and shorts eventually. The electromigration lifetime of an interconnect is characterised by its mean time to failure (MTF), which is modelled by Black's equation

$$MTF = AJ^{-N}\exp(\frac{E_a}{kT})$$

Where A, N and E_a are constants, J is current density, k is Boltzmann's constant and T is temperature [6]. As the MTF of a line is exponentially related to its temperature, a high operating temperature will reduce the MTF drastically.

In SOI structures, self-heating is even more severe due to the presence of the high thermal-resistivity buried oxide layer. The thermal conductivity of a silicon dioxide is only 0.014 W/cmK, about two orders of magnitude lower than that of silicon. In small dimension devices, the silicon area for heat conduction is less and self-heating is more severe [7].

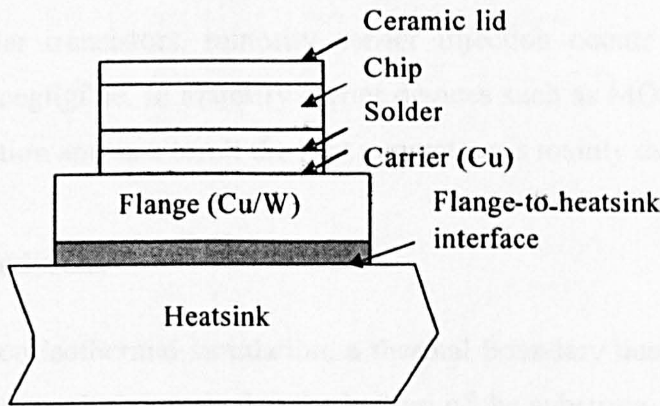
3.2 Thermal resistance

The temperature rise ΔT is given by the product of the power dissipation P_d, and the thermal resistance R_{th}:

$\Delta T = P_d \cdot R_{th}$

Besides the thermal resistance of the chip itself, in practice the package layers bring thermal resistance in the heat transfer path, as shown in Figure 3.1. In LDMOSFET devices, the heat generated in the active region travels to the heat sinker and outside ambient through the silicon substrate, the solder, the carrier and the Cu/W flange. The total thermal resistance in the heat conduction path is the sum of thermal resistance of the chip and the package layers. The thermal resistance is also temperature dependent due to the temperature dependence of thermal conductivity and specific heat. An electrical circuit is an equivalent to the thermal network with power dissipation in the device being the thermal analogue of current, temperature rise being the analogue of voltage and the thermal resistance being the analogue of electrical resistance, as demonstrated in Figure 3.1. In addition to the heat conduction at the vertical direction, heat also conducts at the lateral direction [8]. The effective thermal resistance is determined by the heat conduction in both lateral and vertical directions.

The instantaneous temperature rise will change with the instantaneous input power. The average temperature rise in the device is determined by the average power dissipation. For RF power amplifier applications, the average power dissipation is $P_d = I_d V_{ds} + P_{in} - P_{out}$.



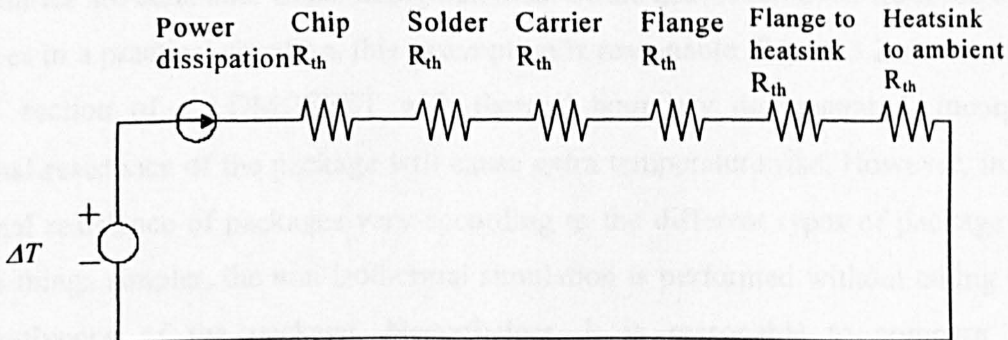


Figure 3.1 (a) a schematic cross-section of chip with different package layers. (b) an electric circuit equivalent to the thermal network for the structure in (a).

3.3 Heat Flow Equation

2-dimentional non-isothermal simulations are carried out using MEDICI to take into account self-heating effect. In non-isothermal simulations, temperature is not a constant value throughout the whole device. The heat flow equation is solved together with Poisson's equation and the current-continuity equations. The heat flow equation is given by [9]:

$$mc\frac{\partial T}{\partial t} = H + \vec{\nabla}(\lambda(T)\vec{\nabla}(T))$$

where λ is the thermal conductivity of the material, H is the thermal generation term, c is the specific heat of the material, m is the mass density of the material, T is the temperature. For silicon, $\lambda = \left(0.003 + (1.56e-3)\times T + (1.65e-6)\times T^2\right)^{-1} W/Kcm$, $c = 850.9 + (152.2e-3)\times T - 158.2e5T^{-2}(J/Kg/K)$. For silicon oxide, $\lambda = 0.014W/Kcm$, $c = 3000J/Kg/K$. A simplified heating generation rate per unit volume is given by $H = J\cdot E + UE_g$, where J is the current density, E is the electric field, U is the recombination rate and E_g is the band gap of the semiconductor. The first term is the Joule heating caused by the electrical resistance associated with the semiconductor device. Recombination of carriers also releases energy and gives rise to the second term. In p-n diodes and bipolar transistors, minority carrier injection occurs and recombination heat generation is not negligible. In majority carrier devices such as MOSFETs, there is very little carrier recombination and as a result the heat generation is mainly due to Joule heating [10].

3.4 Boundary conditions

To perform the non-isothermal simulation, a thermal boundary needs to be specified. In this work, a thermal electrode is attached at the bottom of the substrate and the temperature of the electrode is fixed at 300K. This electrode emulates the effect of heat sinker whereas the other boundaries are adiabatic. Considering that most of the heat is removed from the bottom of the devices in a practical situation, this assumption is reasonable. Figure 3.2 shows the schematic cross section of a LDMOSFET with thermal boundary demonstrated. Incorporating the thermal resistance of the package will cause extra temperature rise. However, in practice the thermal resistance of packages vary according to the different types of package designs. To make things simpler, the non-isothermal simulation is performed without taking into account the influence of the package. Nevertheless, it is reasonable to compare the thermal performance between different device structures based on the same boundary condition.

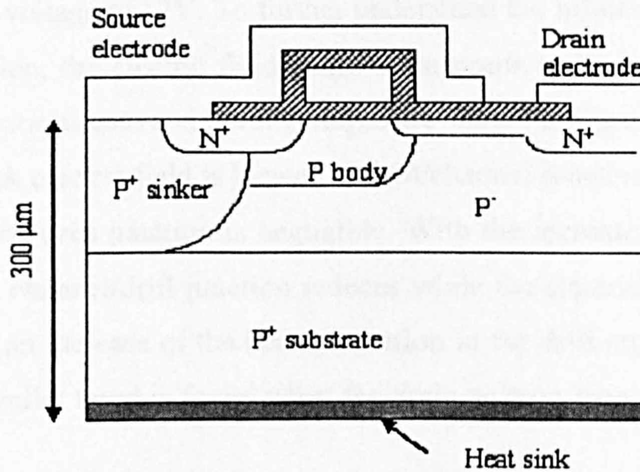


Figure 3.2 Thermal boundary for non-isothermal simulation in this work

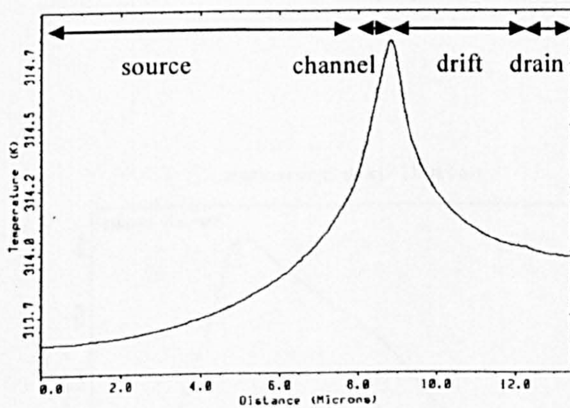
3.5 Simulation Results and Discussion

3.5.1 Temperature Distribution and Bias Condition

Temperature distribution is affected by the heat generation and heat conduction within the device. Since heat generation is a function of current density and electric field, the temperature distribution should change with the applied bias. In this work, the influence of the gate and drain bias on the temperature distribution are investigated. First, gate bias changes from 4V to 12V with a fixed drain bias. The temperature distributions at various gate biases are shown in Figure 3.3. It is shown that at gate voltage of 4V, the peak temperature is at the channel/drift junction and the temperature in the device increases with the increase of the gate voltage. With the increase of the gate voltage, the drift region becomes a high temperature region compared to the source region. At high gate voltage of 12V, the location of the peak temperature moves into the drift region. Next, gate bias is fixed and drain bias is changed from 10V to 40V, the temperature distributions shown in Figure 3.4. The influence of the drain bias shows similar trends as that of the gate bias.

To understand the change of temperature distribution with gate and drain bias, the heat generation at drain bias of 10V and gate bias varied from 4V to 10V are plotted in Figure 3.5. At a low gate voltage of 4V, the heat generation within the drift region is negligible compared to the heat generation at the drift/channel junction, which explains the peak temperature location. With the increase of gate bias, heat generation increases and heat generation in the drift region increases to a large extent that it can not be neglected anymore. Due to the

contribution of the heat generated in the drift region, the peak temperature moves into this region at a high gate voltage of 12V. To further understand the influence of the gate and drain bias on heat generation, the electric field distribution needs to be investigated. The electric field distribution at various gate and drain voltages are shown in Figure 3.6 and 3.7. As shown in Figure 3.6, the peak electric field is located at drift/channel junction. At gate voltage of 4V, the electric field in the drift junction is negligible. With the increase of the gate voltage, the peak electric field at channel/drift junction reduces while the electric field in the drift region increases. It leads to an increase of the heat generation in the drift region with the increase of gate voltages. The similar trend is found when the drain voltage increases, as shown in Figure 3.7.



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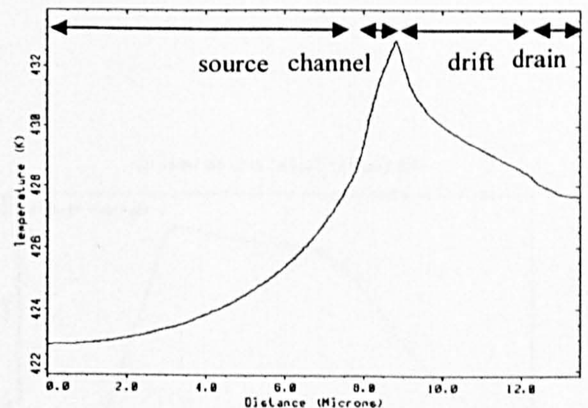

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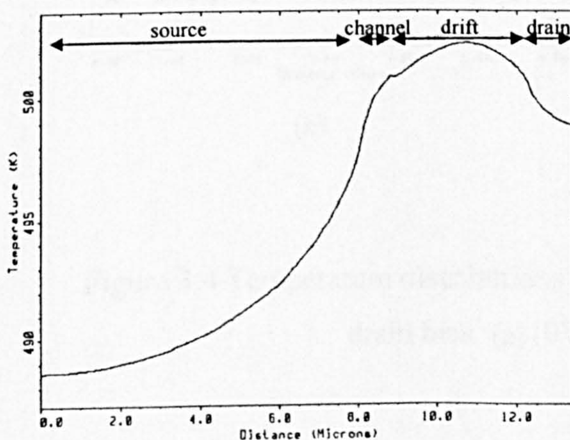
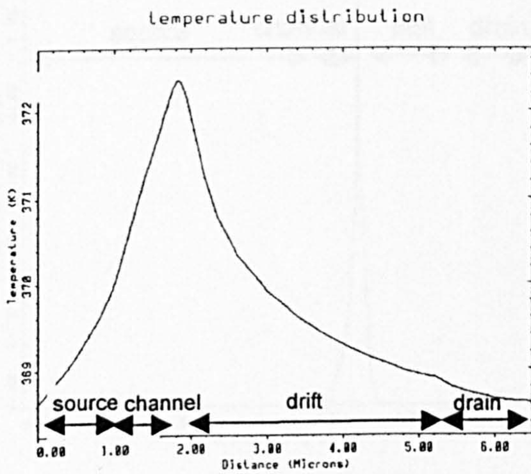


(c)

Figure 3.3 Temperature distributions at (a) V(G)=4V, V(D)=10V; (b) V(G)=8V, V(D)=10V; (c) V(G)=12V, V(D)=10V.



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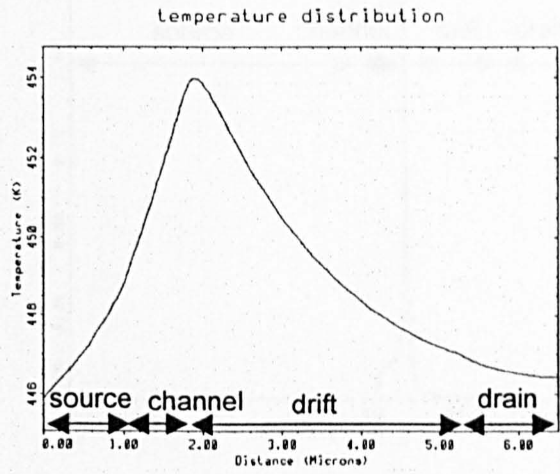

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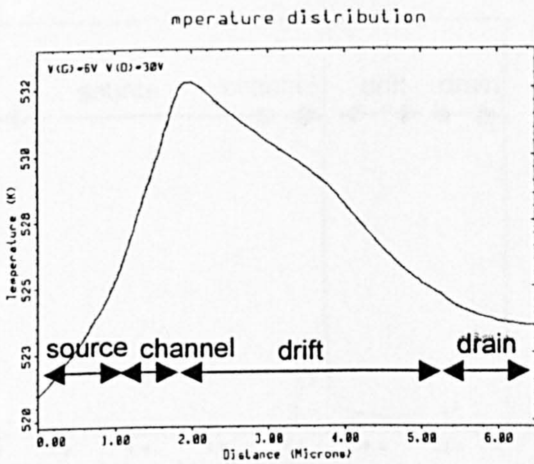

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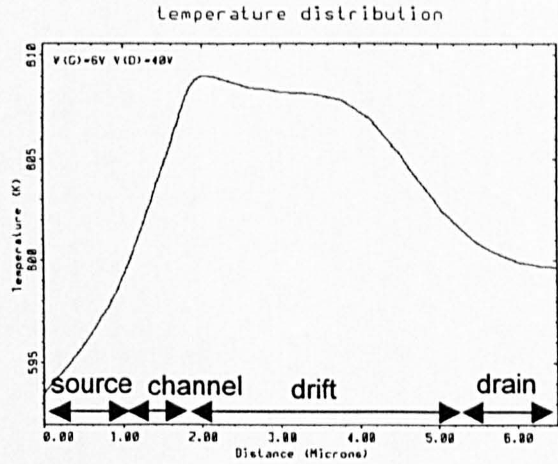
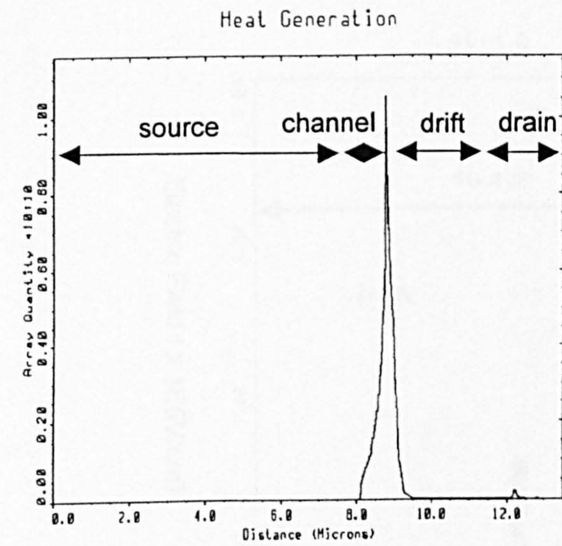


(d)

Figure 3.4 Temperature distributions along the silicon surface at gate bias of 6V and drain bias (a)10V (b) 20V (c) 30V (d) 40V.



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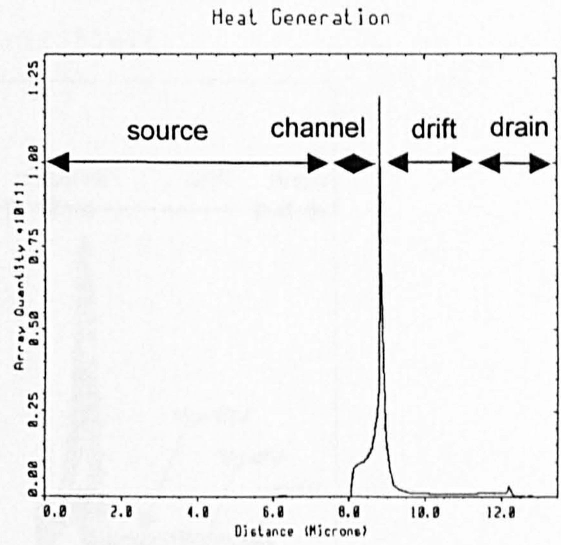

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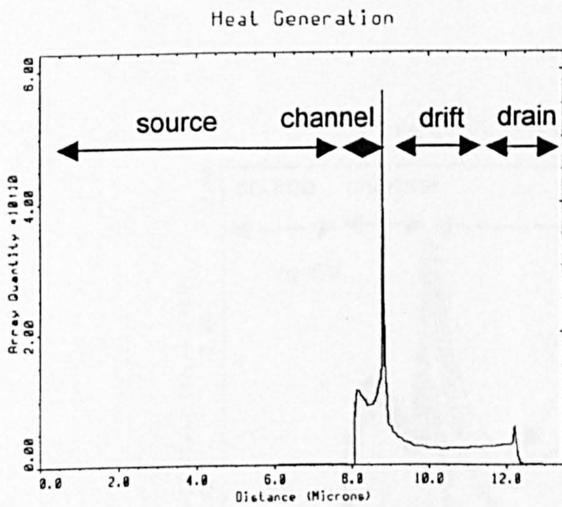

(c)

Figure 3.5 Heat generation along silicon surface with gate bias at (a) 12V (b) 8V (c) 4V and drain bias of 10V.

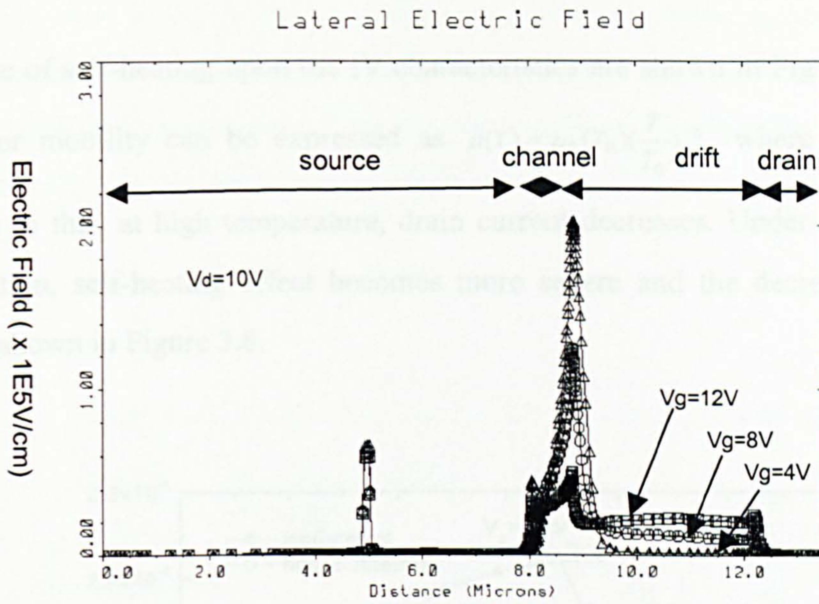

Figure 3.6 Electric field distributions along the silicon surface with the gate bias varying from 4V, 8V to 12V.

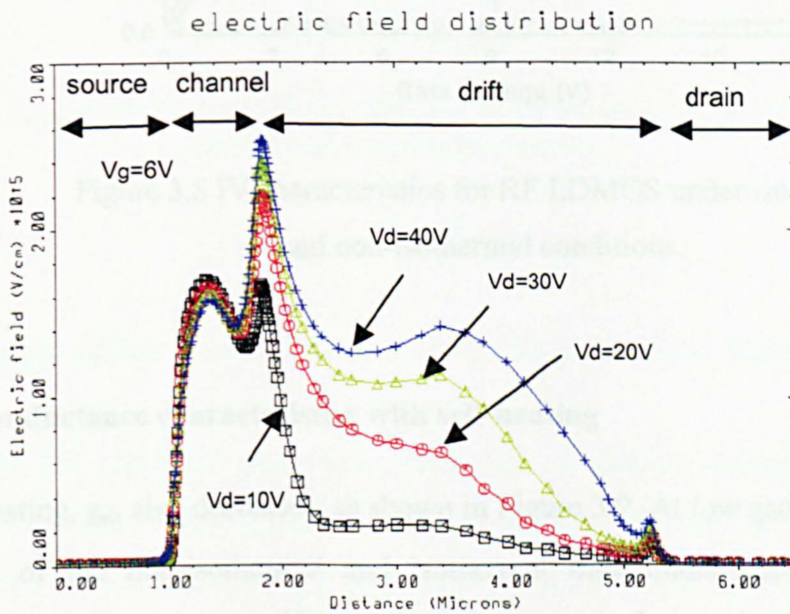

Figure 3.7 Electric field distributions along the silicon surface with the drain bias varying from 10V, 20V, 30V to 40V.

3.5.2 I-V characteristics with self-heating effect for LDMOSFET.

The influence of self-heating upon the IV characteristics are shown in Figure 3.8. According to [1], carrier mobility can be expressed as $\mu(T)=\mu_0(T_0)(\frac{T}{T_0})^{-n}$, where n=2.5 in case of DMOS. Due to this, at high temperature, drain current decreases. Under high drain or gate biases condition, self-heating effect becomes more severe and the decrease of I_d is more dramatic, as shown in Figure 3.8.

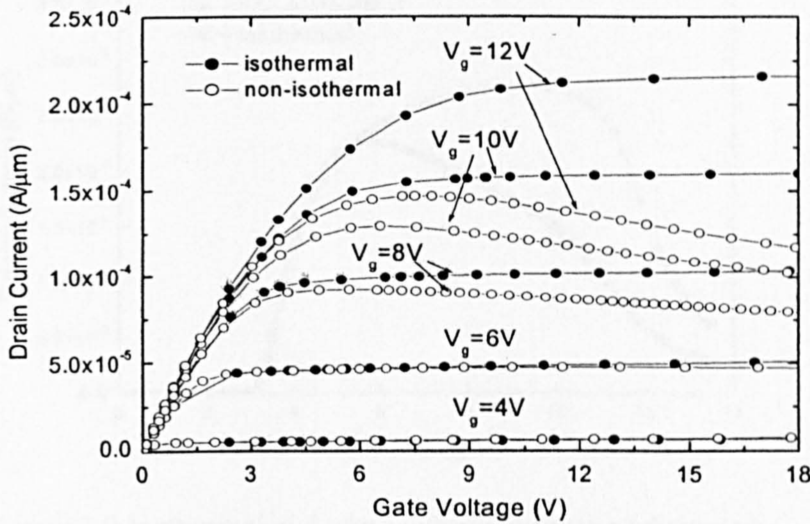

Figure 3.8 IV characteristics for RF LDMOS under isothermal and non-isothermal conditions.

3.5.3 Transconductance characteristics with self-heating

Due to self-heating, g_m also decreases, as shown in Figure 3.9. At low gate voltages up to 6V, the deviation of the non-isothermal and isothermal transconductance is negligible. As discussed in chapter 2, at the gate biases where g_m curve is flat, carrier velocity saturates in the channel region. According to $g_m = W_g C_i v_{sat}$ (Equation 2-13), and $C_i = \frac{\varepsilon_{ox}}{t_{ox}}$ (Equation 2-11) transconductance is determined by the carrier saturation velocity and the geometric parameters W and t_{ox}. At these biases, g_m reduction under self-heating is attributed to the negative temperature dependence of saturation velocity as $v_{sat} = K\exp(-T/\Theta)$ [11]. At higher gate voltages, the transconductance is expressed as $g_m = \left(\frac{W_g}{L_g}\right)\mu_n C_i V_{mos}$.

Transconductance is the function of carrier mobility within the channel together with the geometric parameters W, L, t_{ox} and the voltage V_{mos}. At these biases, g_m reduction under self-heating is caused by carrier mobility reduction at elevated temperature. For power amplifier applications, wide and flat transconductance characteristics are desirable. Transconductance fall-off under self-heating degrades the linearity of amplification and reduces the output power level.

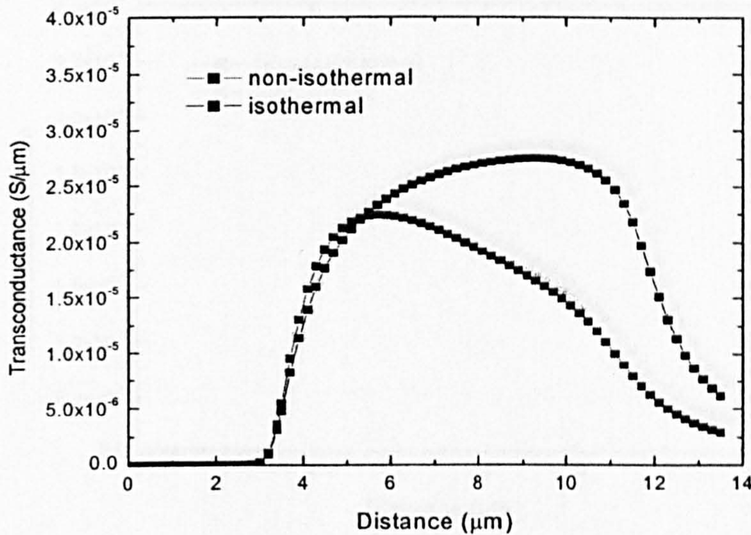

Figure 3.9 Isothermal and non-isothermal transconductance characteristics for bulk structure.

3.5.4 Effect of top silicon thickness and buried oxide thickness of SOI on self-heating

To investigate the effect of top silicon thickness on device performance three device structures are compared using non-isothermal DC simulations. The power dissipated in the device under DC condition is given by $P_d = I_d \times V_d$, where I_d and V_d is the drain current and voltage. The buried oxide is 1.0 µm thick whereas the top silicon thickness varies from 3µm to 0.2µm. The temperature rise versus power dissipation are shown in Figure 3.10. As shown, thicker T_{si} corresponds to less temperature rise under the same power dissipation, due to improved lateral thermal conduction in case of a thicker top silicon layer. A thicker buried oxide layer leads to a higher temperature rise. To minimise the temperature rise and reduce the self-heating effect, thinner buried oxide is preferable.

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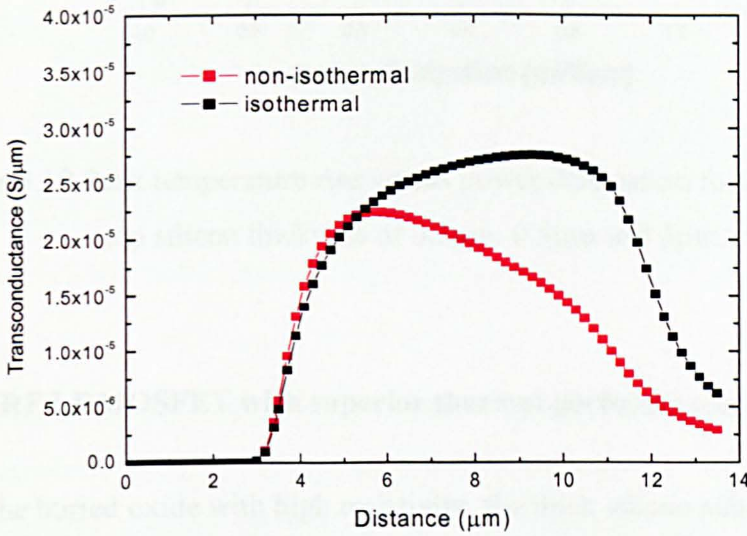

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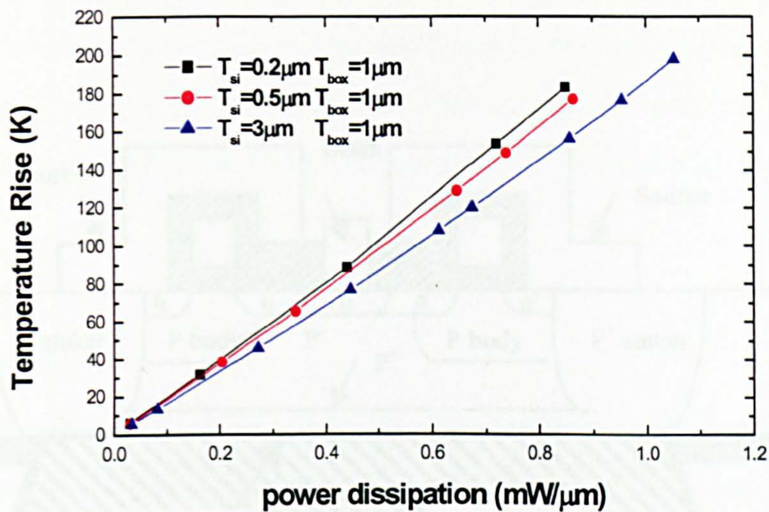


Figure 3.10 Peak temperature rise versus power dissipation for devices with top silicon thickness of 0.2μm, 0.5μm and 3μm.

3.6 Back-etch RF LDMOSFET with superior thermal performance

In addition to the buried oxide with high resistivity, the thick silicon substrate also contributes to the total thermal resistance, which leads to a severe self-heating in SOI. In this section, a novel back-etch RF LDMOSFET with superior thermal performance is proposed. This is achieved by removing the buried oxide layer and the thick substrate, which significantly alleviate self-heating [12]. The proposed back-etch structure offers a promising alternative to the conventional bulk and SOI structure.

3.6.1 Device structure

The back-etch device structure is shown in Figure 3.11. The device is fabricated on the top silicon layer as in a conventional structure whereas the silicon substrate and buried oxide layer under the active region are replaced by a thick metal layer, which serves as the electrical ground and a heat sinker. The device source region contacts with the bottom metal, through P^+ sinker

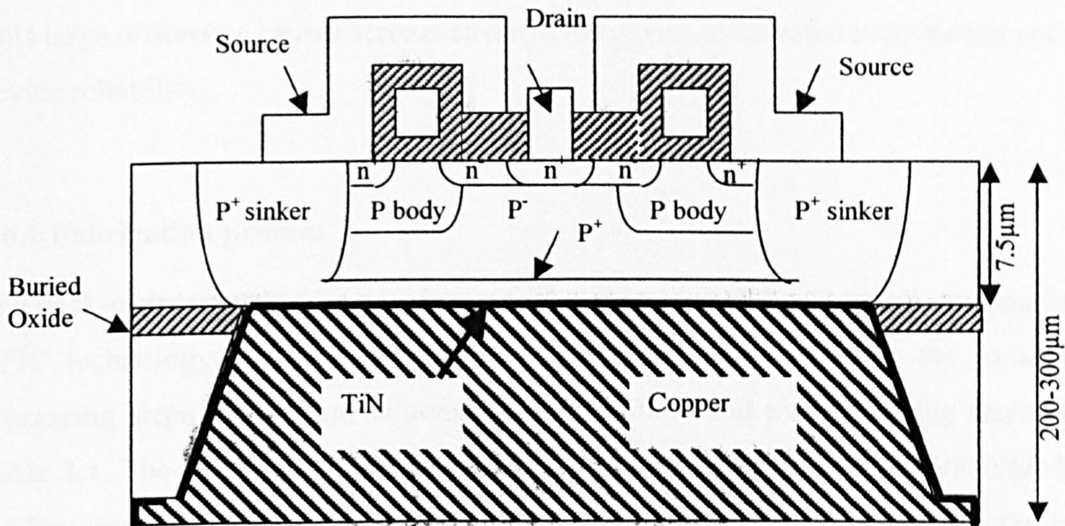


Figure 3.11 A schematic cross-section of back-etch RF LDMOSFET structure.

region. To provide an ohmic contact between the P^- type top silicon and the bottom metal, a P^+ layer is present at the interface of top silicon and bottom metal. The heat generated in the active region transfers through the top silicon layer into the thick metal layer to outside ambient. Compared to a conventional RF LDMOSFET based on SOI or bulk technology, the thick silicon layer is eliminated, leading to a reduction of the thermal resistance. In comparison to a conventional SOI device structure, the buried oxide layer is also eliminated. The use of metal with high electrical and thermal conductivity instead of a thick silicon substrate leads to a low thermal resistance. Self-heating effect can be alleviated in this back-etch structure. Furthermore, using metal as the substrate provides some improvement in electrical performance, shown later through the simulations.

Copper is used as the bottom metal plate due to its high electrical and thermal conductivity and high resistance to electromigration, which is a major concern for aluminium interconnects. Copper has the second highest electrical conductivity only after silver. The electrical conductivity of aluminium, 37.6×10^6/mohm, is only 60% of copper, 59.6 $\times10^6$/mohm. Furthermore, the thermal conductivity of copper, 401W/mK at 300K, is about 1.7 times higher than that of aluminium, 237W/mK. Due to those advantages, copper has been used as the interconnect material in IC technology. Care needs to be taken while processing copper since it can deteriorate device characteristics. If process-induced copper contamination remains on the surface [13] copper can diffuse through the silicon dioxide quickly even at low temperature [14], and causes failure of contacts by diffusion through the metallization layers into silicon. Various diffusion barrier materials have been proposed, such as TiN, Tantalum

based barrier, PSG and BPSG [13], [15]-[16]. A thin layer of TiN can be adopted as the diffusion and adhesion barrier of copper. The disadvantage of copper is that the coefficients of thermal expansion for copper and silicon are 17×10^{-6}/K and 2.5×10^{-6}/K respectively [17]. This large difference causes serious stress in the device at elevated temperature and affects the device reliability.

3.6.2 Fabrication process

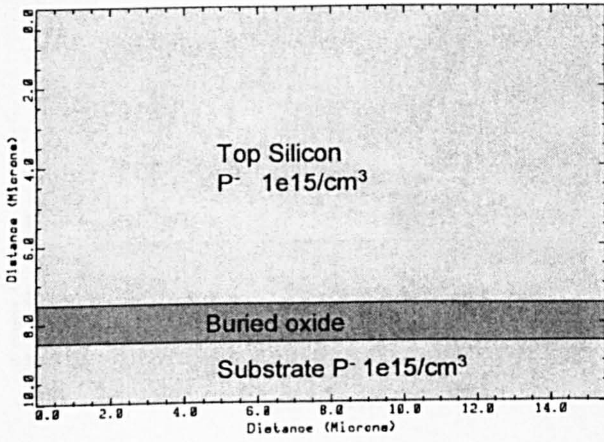
The back-etch technology is based on a SOI starting material and is fully compatible with the RFIC technology proposed in [18]. The back-etch technology has the same front-wafer processing steps as in a conventional SOI technology and the processing steps are listed in Table 3.1. The front-wafer process has been simulated using TMA's TSUPREM-4 [19], with the key process steps shown in Figure 3.12. The front-wafer process limits the temperature and thermal budget of the back-wafer processing. Due to the presence of aluminium interconnect on the front-wafer, the temperature of the back-wafer processing is limited up to 450°C. To illustrate the back-wafer processing, 2-D device schematic cross-sections are illustrated in Figure 3.13.

After completing the front processing, a 200nm thick of ECR SiO_2 is deposited on the front wafer as the protecting layer. Even though copper film does not grow at the front of the wafer during copper CVD at the backside, there is a certain amount of copper contamination (> 10^{12}/cm^2) on the front of the wafer [13], which is difficult to remove using conventional HF base cleaning. To avoid this, a layer of ECR (Electron-Cyclotron-Resonance) SiO_2 is deposited on the front wafer before the copper CVD, as adopted in [13]. It is shown in the literature that the copper concentration reduces to less than 10^{11}/cm^2 after a 100nm thick of ECR SiO_2 is removed by a buffered HF solution. Following ECR SiO_2 deposition, the silicon substrate under the active region of the device is then selectively etched from the backside of the wafer using the buried oxide layer as a etch stop layer, as shown in Fig.3.13 (b). Then the exposed buried oxide layer is etched away, as shown in Fig.3.13 (c). Following above process, a blanket boron implantation from the backside of the wafer is performed. To activate the implanted carriers, annealing is needed. A normal annealing usually requires a temperature above 600°C. To avoiding the influence of high temperature on aluminium metallization, a laser annealing can be used. Using a laser annealing for a short period (<10^{-7}s), heat does not transfer far into the substrate, and only a thin layer of film less than 1μm is affected [20]. The structure after implantation and annealing is shown in Figure 3.13 (d). A 50nm of TiN layer is sputtered followed by copper CVD of about 200μm thick. The deposited copper plate undergoes Chemical-Mechanical Polishing (CMP) to provide a flat surface at the

back side of the wafer. Cleaning after CMP can be performed as in [13], which is composed by an ultra clean water scrub, an organic alkali scrub, followed by dip in diluted HF and a water rinse. Finally the 200nm thick of ECR SiO_2 on the front surface of the wafer is removed.

Table 3.1 a list of front-wafer process in back-etch technology.

Process steps	Condition and requirement
SOI wafer	Top silicon, p-type, 7.5μm, 1e15/cm^3 Silicon substrate, p-type, 200μm, 1e15/cm^3, Buried oxide, 1μm
Buffer oxide	T=950°C, dry O_2, 28min
P^+ sinker region definition	Mask
P^+ sinker implantation	Boron, 1e16/cm^2, 80KeV
Drive-in	T=1200°C, 140min
Etch oxide	All the oxide on top of the silicon surface
Gate oxidation	Thickness=70nm
Polysilicon deposition	Thickness=0.4μm
Polysilicon implantation	Arsenic, 5e15/cm^2, 100KeV
Nitride deposition	Thickness=0.1μm
Gate definition	Mask
Nitride etch	RIE
Poly etch	RIE
Etch oxide	Thickness=40nm
P base lithography	Mask
P base implantation	Boron, 3e13/cm^2, 60KeV
P base drive-in	Ramp up to 1100°C, nitrogen, 120min
Drift implantation	Blanket implantation, Arsenic, 2.1e12/cm^2, 60KeV
S/D definition	Mask
S/D implantation	Arsenic, 6e14/cm^2, 80KeV
annealing	T=950°C, 30min
Etch nitride	All the nitride on top of the silicon surface
S/D contact definition	Mask
Aluminium deposition	Sputter, thickness=1.0μm
Metal definition	RIE
Oxide deposition	PVD, thickness=1.0μm



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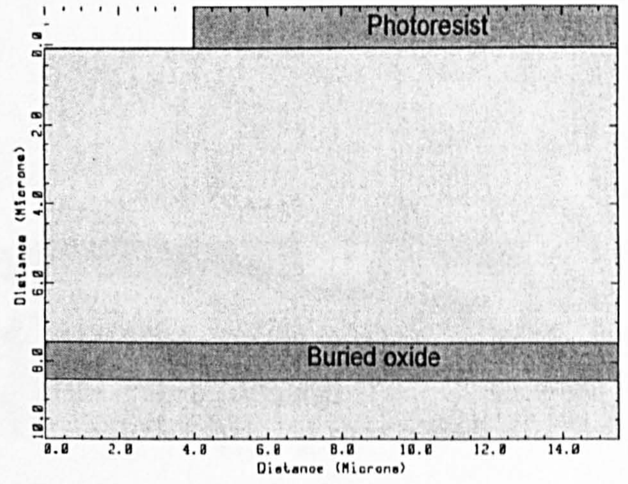

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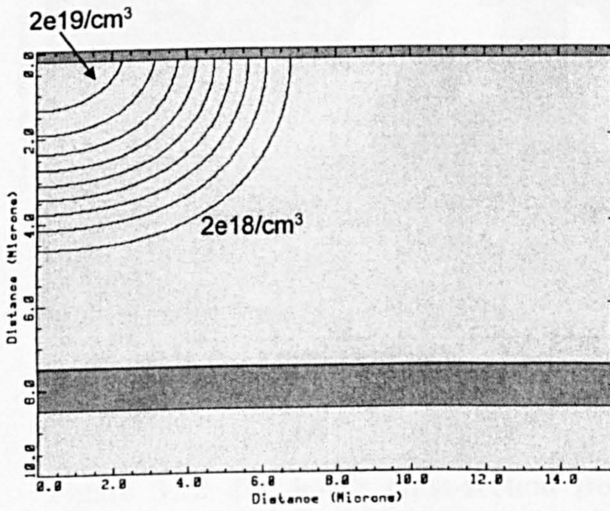

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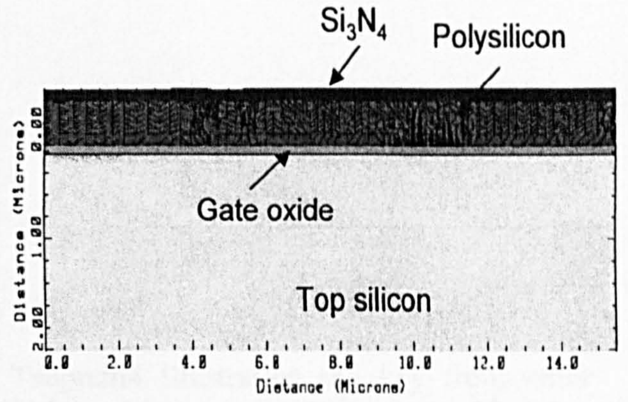

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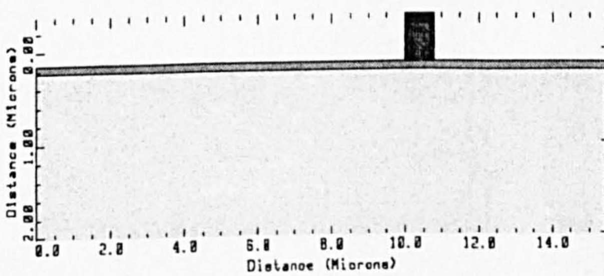

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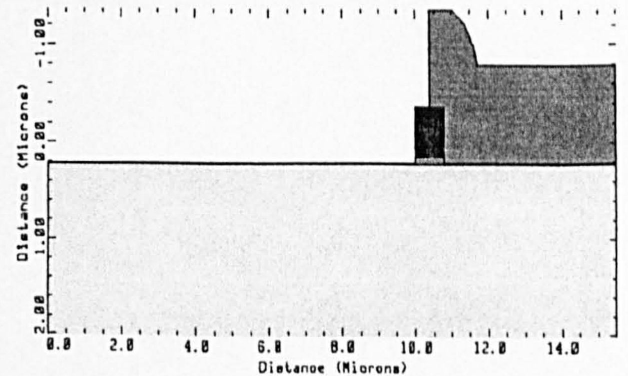

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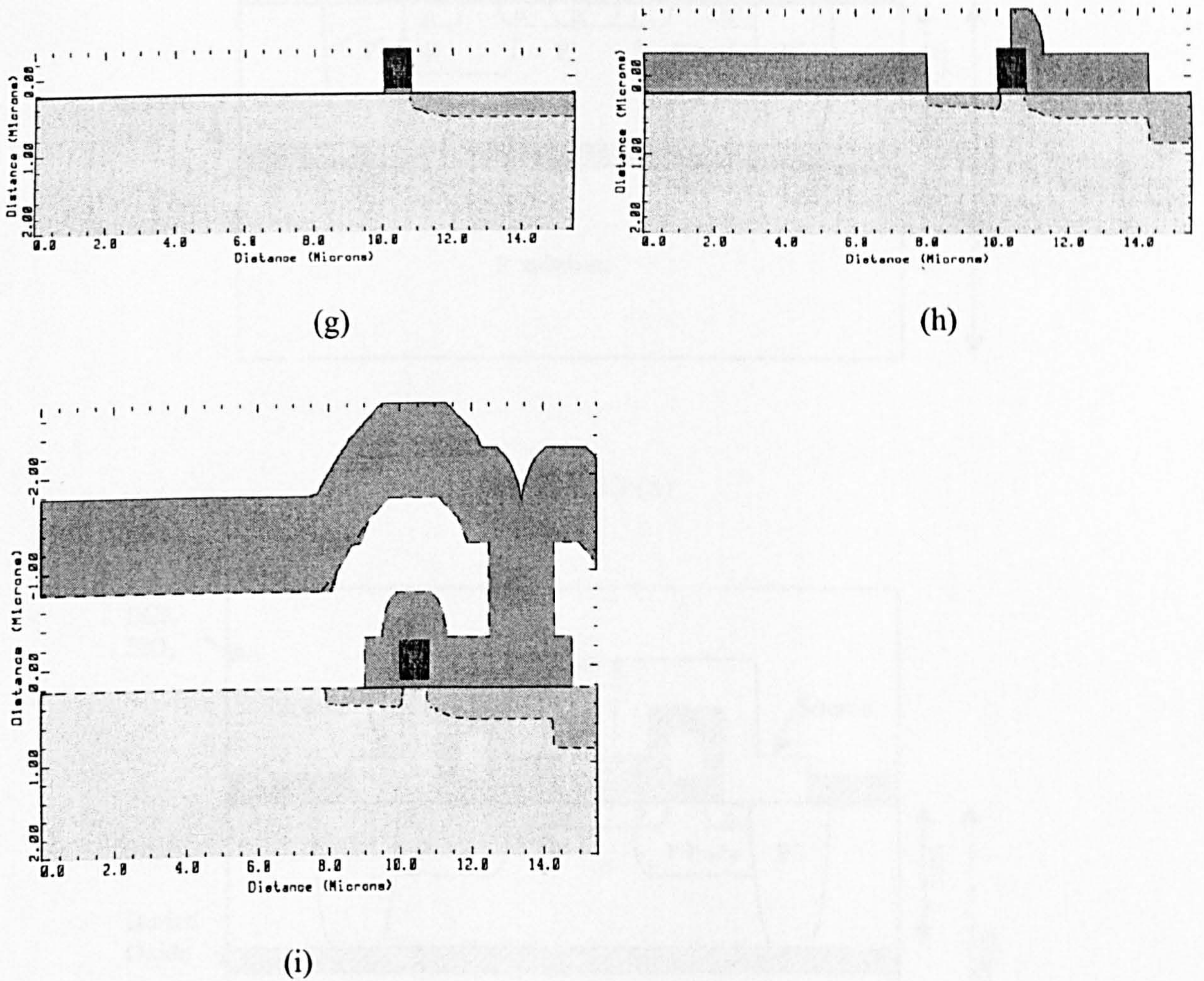


Figure 3.12 2D device cross-section from Tsuprem4 illustrating the key front-wafer process steps, (a) starting SOI material, (b) P^+ sinker implantation (Boron), (c) P^+ sinker drive-in, (d) gate oxidation formation, poly-silicon deposition, Arsenic implantation and silicon nitride deposition, (e) gate patterning, (f) P body implantation (Boron), P body drive-in, (g) drift implantation (Arsenic), (h) source and drain region implantation (Arsenic), (i) metallization.

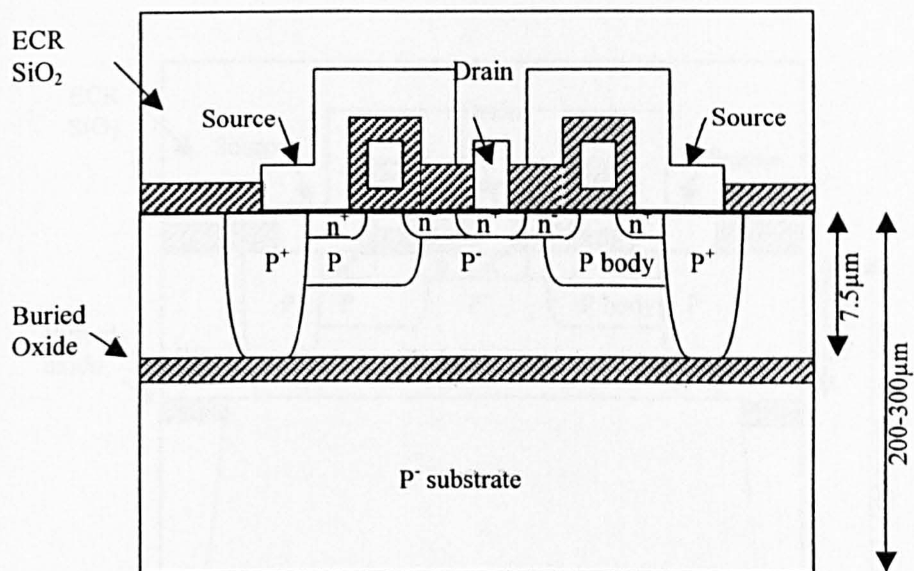


Figure 3.13 (a)

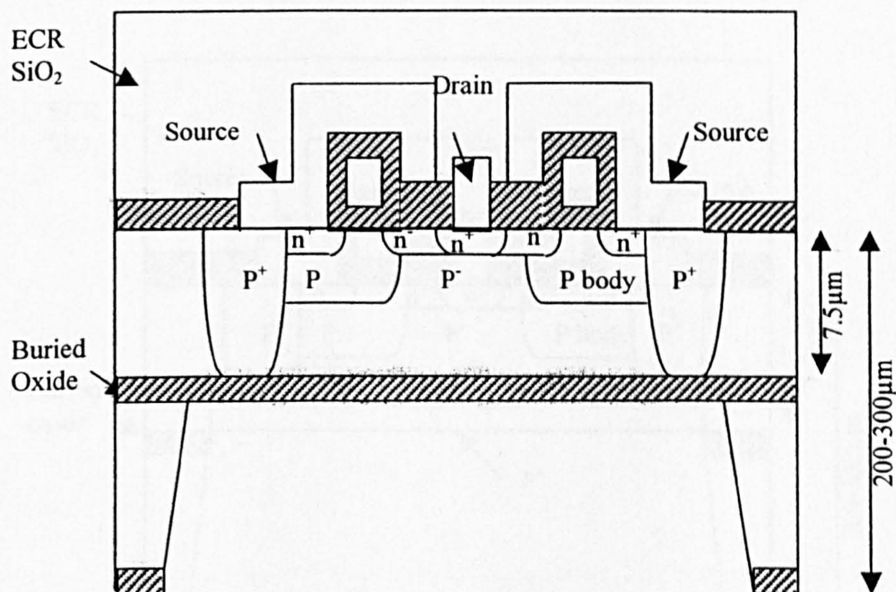


Figure 3.13 (b)

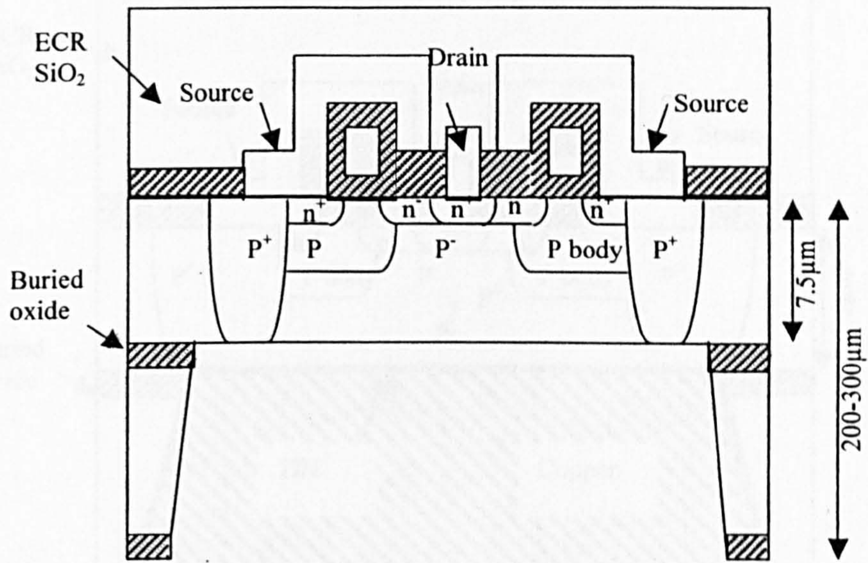


Figure 3.13 (c)

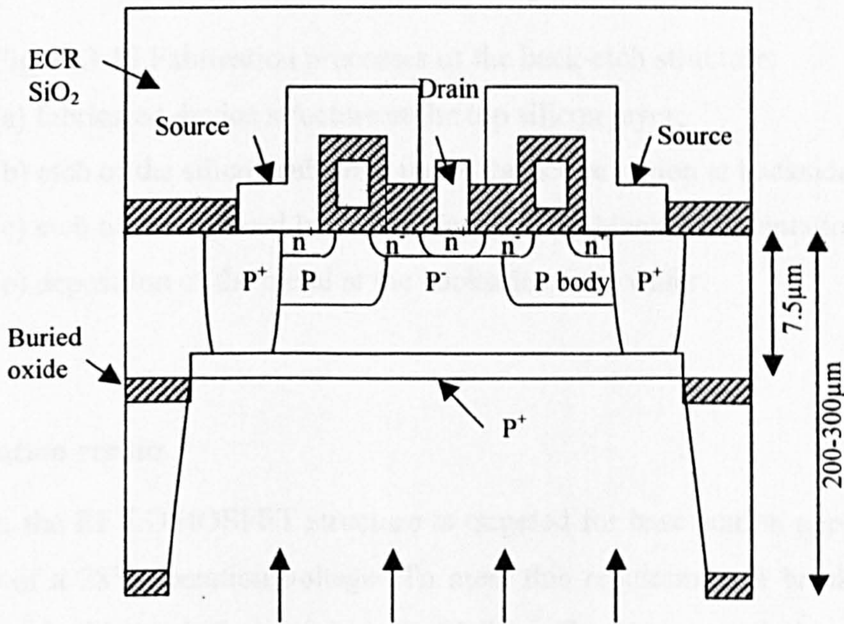


Figure 3.13 (d)

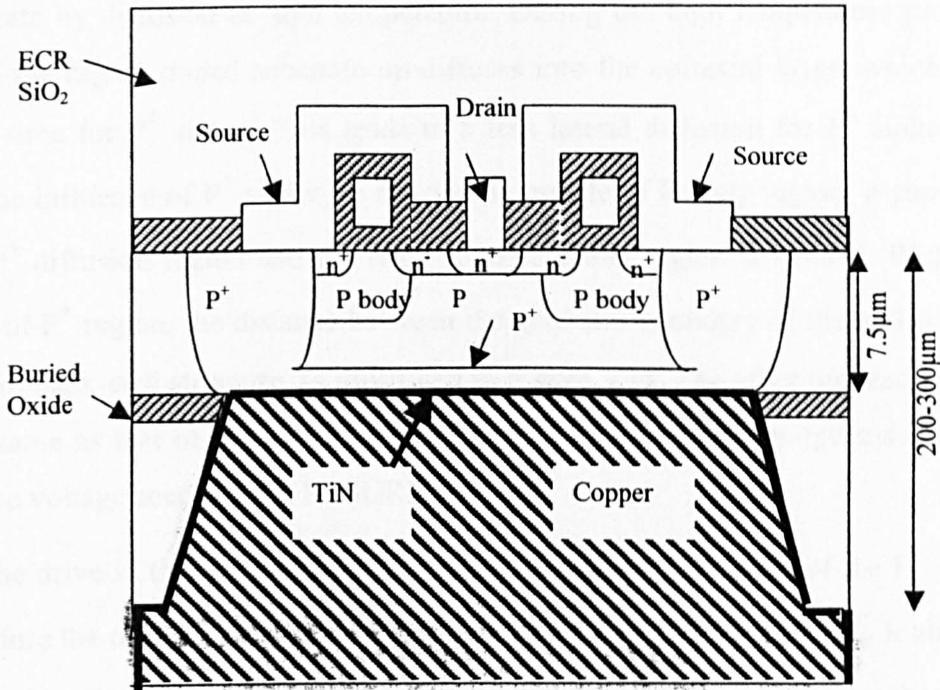


Figure 3.13 (e)

Figure 3.13 Fabrication processes of the back-etch structure:

(a) fabricated device structure at the top silicon layer;

(b) etch of the silicon substrate under the active region at backside of the wafer;

(c) etch of the exposed buried oxide layer; (d) blanket implantation of boron;

(e) deposition of the metal at the backside of the wafer.

3.6.3 Simulation results

In this work, the RF LDMOSFET structure is targeted for base station applications with the requirement of a 28V operation voltage. To meet this requirement a breakdown voltage of 85V is designed with the drift region length of 3.5μm. To prevent reach through at the vertical direction, the influence of epi layer thickness on breakdown voltage is investigated, as shown in Figure 3.14. For an epi layer of 15μm thick with doping concentration of 1e15cm^{-3}, the breakdown voltage is roughly 93.5V. With the decrease of the epi layer thickness, the breakdown voltage remains the same until epi thickness reaches 7μm. Therefore an epi layer of 7.5μm is used in this structure. The doping concentration in the p body region is 1×10^{17} /cm^3 at the source end and 1×10^{15} /cm^3 at the drift end.

For a comparison, a bulk RF LDMSOFET is generated using TSUPREM 4. A P$^+$ substrate with a doping concentration of 5×10^{19} /cm^3 and a P$^-$ epitaxial layer of thickness 8μm

is used. In the bulk structure, P^+ sinker region is formed to connect the top source region and the substrate by diffusion at high temperature. During the high temperature processing, the dopant in the highly doped substrate up-diffuses into the epitaxial layer, which reduces the diffusion time for P^+ sinker. This leads to a less lateral diffusion for P^+ sinker region. To prevent the influence of P^+ sinker on the doping profile of P body region, a gap between the edge of P^+ diffusion region and the edge of the channel region is needed. With less lateral diffusion of P^+ region, the distance between the gate and boundary of the cell is 2μm shorter than that of back-etch structure, as illustrated in Figure 3.15. The other process parameters are kept the same as that of the back-etch structure. Both structures are optimised to maximum breakdown voltage according to RESURF principle.

The drive-in time of the P^+ region is critical for the resistance of the P^+ sinker region and therefore the on-resistance (R_{on}) of the device, as shown in Figure 3.16. It also influences the threshold voltage V_{th}, when the lateral diffusion of P^+ sinker region reaches the channel region during long time drive-in process. With the increases of the drive-in time from 100 minutes to 140 minutes under temperature 1200°C, the R_{on} decreases significantly. With the further increase of the drive-in time to 140 minutes the R_{on} is nearly unchanged. However, further increase of the drive-in time to 180 minutes increases the R_{on}, due to the increase of the V_{th}. To prevent the influence of the P^+ sinker region on the channel region and obtain a low on-resistance, drive-in time of 140 minutes under 1200°C is preferable.

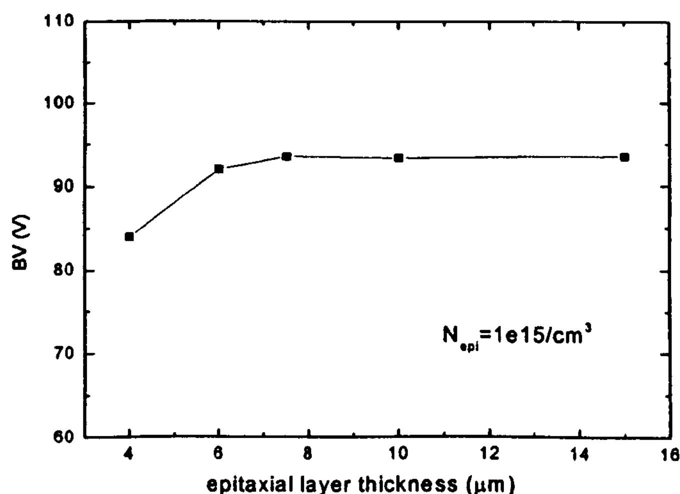
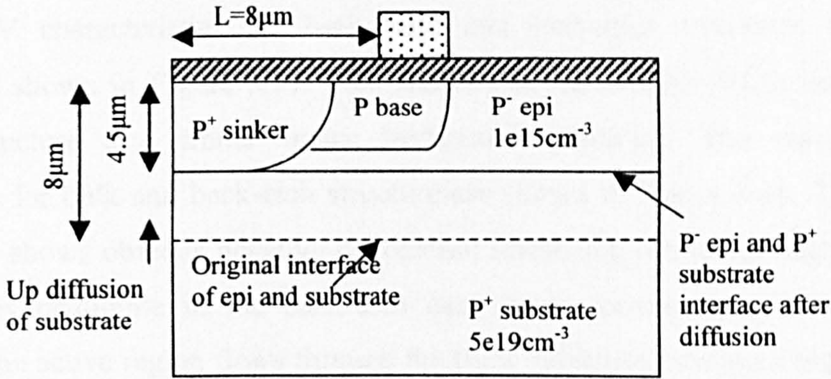
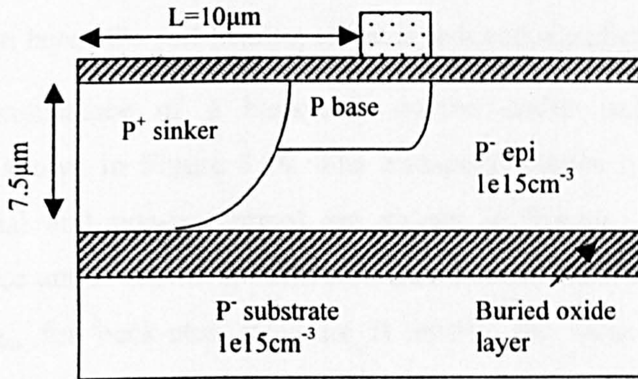


Figure 3.14 Breakdown voltage versus epi layer thickness for back-etch structure.



(a)



(b)

Figure 3.15 2D schematic cross-sections of LDMOSFET's after P base formation. (a) bulk technology with P^+ substrate up diffusion demonstrated; (b) back-etch technology with longer distance between gate electrode and device boundary.

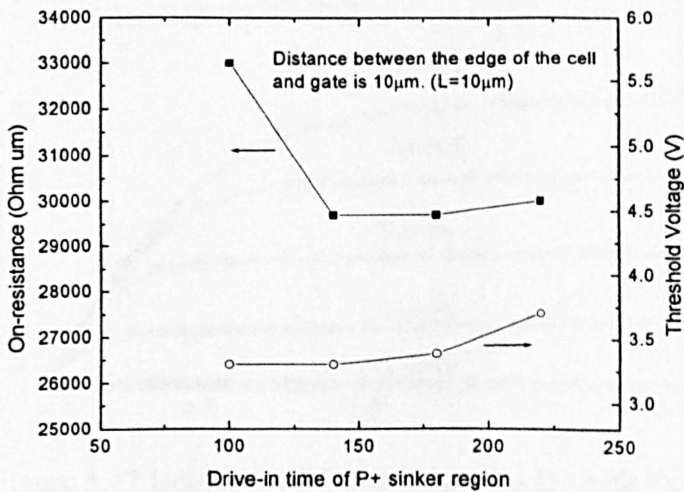


Figure 3.16 On-resistance and threshold voltage versus drive-in time of P^+ sinker region.

The isothermal characteristics are simulated using MEDICI. The simulated static isothermal I-V characteristics for both bulk and back-etch structures generated from Tsuprem4 are shown in Figure 3.17. This shows that the current levels for both bulk and back-etch structure are similar under isothermal condition. The non-isothermal I-V characteristics for bulk and back-etch structure are shown in Figure 3.18. The conventional bulk structure shows obvious negative differential resistance, while the negative differential conductance is negligible in the back-etch case. In a conventional bulk structure, heat generated in the active region flows through the thick substrate, causing a higher temperature rise compared to a back-etch structure. This causes the drain current decrease and a negative differential resistance. However, in the back-etch structure no serious decrease of drain current is observed. With the presence of the metal layer of high thermal conductivity instead of a thick silicon layer, the self-heating effect is reduced significantly in back-etch structure.

Transconductance of a back-etch device under isothermal and non-isothermal conditions are shown in Figure 3.19. The transconductance of a conventional bulk device under isothermal and non-isothermal are shown in Figure 3.9. These results show that transconductance under non-isothermal condition decrease from the isothermal case. While in Figure 3.19, g_m for back-etch structure is nearly the same under isothermal and non-isothermal situations.

The maximum temperature rise versus power dissipation is illustrated in Figure 3.20. At the same power dissipation 0.8mW/μm the temperature rise in the conventional bulk structure is roughly 90K, while it is only about 20K in the back-etch structure.

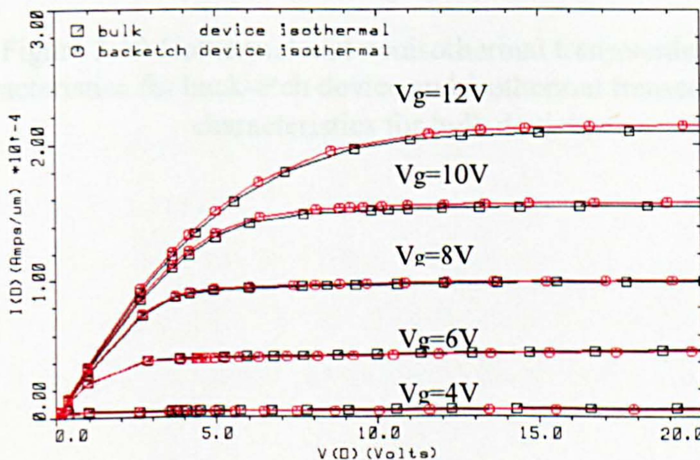


Figure 3.17 Isothermal IV characteristics for both back-etch device and conventional bulk device.

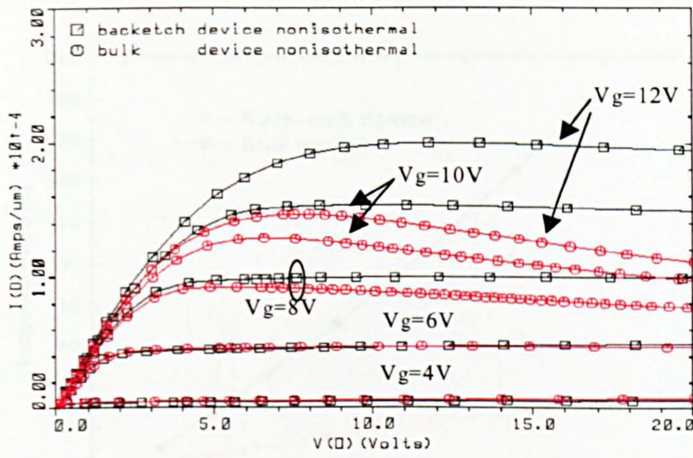


Figure 3.18 Non-isothermal IV characteristics for back-etch device and conventional bulk device.

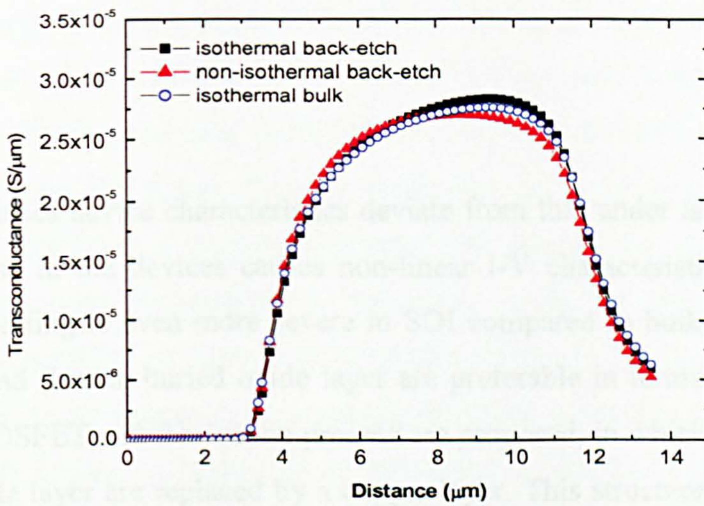


Figure 3.19 Isothermal and nonisothermal transconductance characteristics for back-etch device and isothermal transconductance characteristics for bulk device.

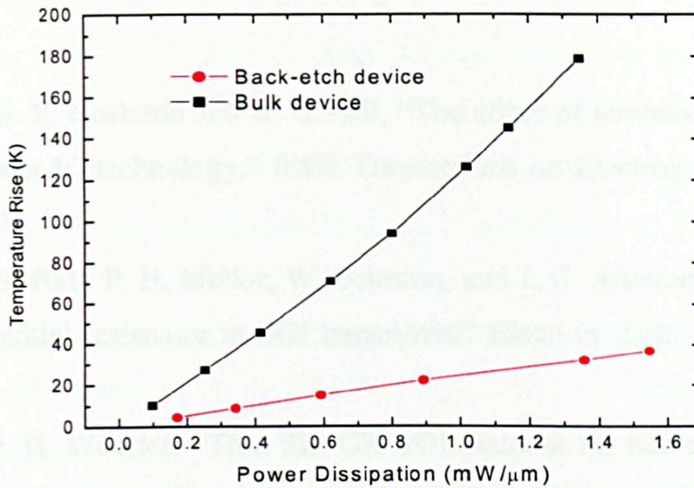


Figure 3.20 Temperature rise versus power dissipation for bulk structure and back-etch substrate.

3.7. Summary

Self-heating causes device characteristics deviate from that under isothermal conditions. The temperature rise in the devices causes non-linear I-V characteristics and transconductance fall-off. Self-heating is even more severe in SOI compared to bulk technology. Thicker top silicon layer and thinner buried oxide layer are preferable in terms of self-heating. A back-etch RF LDMOSFET and fabrication process are proposed, in which the buried oxide and the silicon substrate layer are replaced by a copper layer. This structure demonstrates significant improvement in thermal performance, while it has almost the same electrical performance as bulk alternative under isothermal condition. Without the thick silicon substrate the etch-back LDMSOFET even has a slightly higher transconductance, which leads to a slightly higher cut-off frequency, 8.8GHz, compared to 8.3GHz of the bulk structure. Besides the method of replacing the thick silicon substrate with high thermal conduct metal, the other options of reducing self-heating includes reducing the package thermal resistance and adopting new method of heat removing, such as removing heat from the top side of the silicon device.

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Chapter 4 Quasi-saturation on RF SOI LDMOSFET

Abstract

In this chapter, the quasi-saturation phenomenon on RF SOI LDMOS is investigated. The influence of device parameters, such as the dose in the drift region, on the quasi-saturation current level is presented. The physical mechanism of quasi-saturation in both thin and thick film SOI structures is analysed. Effect of RESURF and self-heating on quasi-saturation is also discussed.

4.1 Introduction

Quasi-saturation is a common phenomenon in power MOS devices. Previously, quasi-saturation in bulk VDMOS has been investigated. It has been pointed out that quasi-saturation occurs only when the carrier velocity saturates in the lower drain region [1]. SOI LDMOSFET has a different structure from VDMOS. Therefore quasi-saturation in the SOI LDMOSFET structures requires further investigation. The top silicon thickness and buried oxide thickness and drift doping level are critical parameters for SOI LDMOSFET. In this chapter the influence of these device parameters on the quasi-saturation is investigated.

4.2 Definition of quasi-saturation in DMOSFET

Quasi-saturation is defined as the insensitivity of the drain current to the increase in gate voltage at high drain current levels [2], as demonstrated in Figure 4.1. Quasi-saturation limits the drain current capability of a DMOS and causes poor linearity in RF power amplifiers. To obtain reasonable linearity, the device is usually "backed-off" from the quasi-saturation region, leading to lower output power [2]. Therefore, increasing the quasi-saturation current can improve the transconductance characteristics, as illustrated in Figure 4.2. In the following, drain saturation current is used as a measure to investigate the influence of device parameters on quasi-saturation effect.

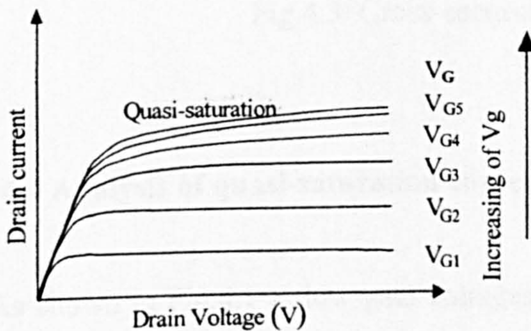

Figure 4.1: LDMOSFET I-V curve showing the quasi-saturation effect.

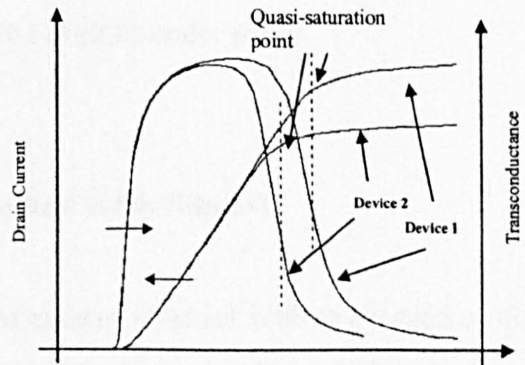

Figure 4.2: Transfer characteristics and transconductance with quasi-saturation present

4.3 Device structure

The structure under study is shown in Figure 4.3. The gate oxide thickness and length are 70nm, 0.8μm, respectively. The drift length L_d, drift doping N_d, top silicon thickness T_{si} and buried oxide thickness T_{box} have been varied in the investigation. The doping concentration of the p body region is 1e17cm^{-3} at the source end and 1e14 cm^{-3} at the drift end. Energy balance equation has been used in the 2D MEDICI simulation to take into account local carrier heating in the high and spatially rapidly varying electric fields [3]. The self-heating effect in SOI structures is investigated by carrying out the 2-D electro-thermal simulation, in which a thermal electrode is attached at the bottom of the device to simulate the effect of a heat sink, which is set to a temperature of 300K. The other boundaries are set as adiabatic.

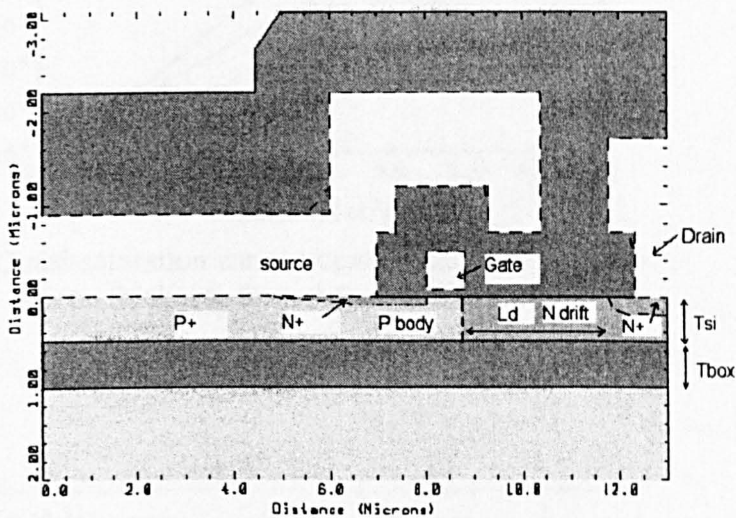

Fig.4.3 Cross-section of a SOI LDMOS under study.

4.4 Analysis of quasi-saturation current on thin and thick film SOI

As shown in Fig.4.1 at low gate voltages the drain current increase with the increase of gate voltage. However, at high gate voltages, the drain current shows nearly no further increase. In this work, the drain current at the gate voltage of 20V and drain voltage 10V is regarded as quasi-saturation current. As at this bias, the devices are well into quasi-saturation. Figure 4.4 shows the quasi-saturation current versus the drift dose with respect to top silicon thickness. The buried oxide thickness is kept to 0.5μm in all cases. As demonstrated, at the same drift

dose, I_{qsat} is higher in thin film SOI with T_{si} between 1.0μm and 0.5μm than the thick film SOI with T_{si} between 1.0μm and 3.0μm. Figure 4.5 shows the IV characteristics of devices with T_{si} of 0.5μm, 1.0μm and 2.0μm under the same drift dose of 3.0e12/cm^2. Quasi-saturation can be seen in this figure. In order to understand the influence of physical parameters on the quasi-saturation current, two structures, Device 1 and Device 2 with T_{si} of 0.5μm and 2.0μm, are considered. The device parameters are listed in Table 4.1. The drift dose is kept the same in these two devices.

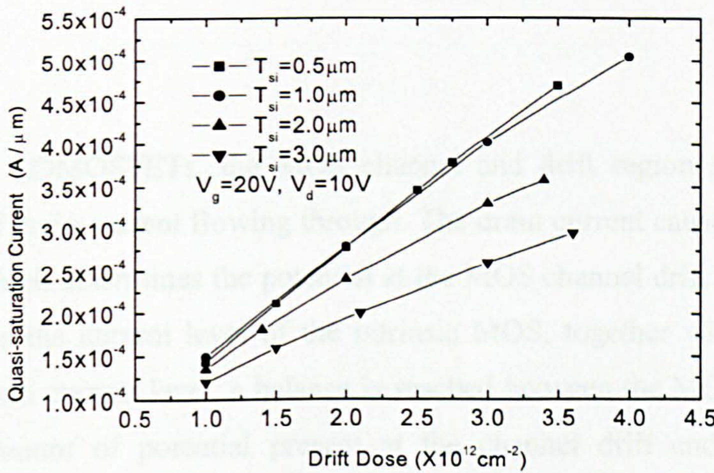

Fig.4.4 Quasi-saturation current versus drift dose with top silicon thickness from 0.5μm to 3.0μm.

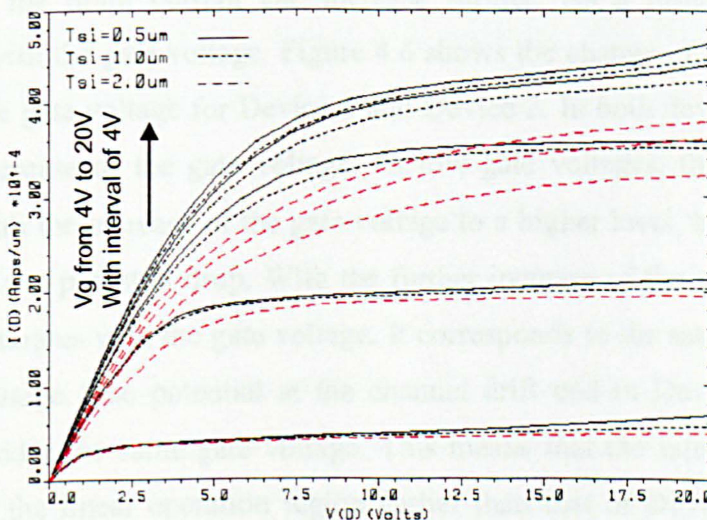

Figure 4.5 IV characteristics of devices with top silicon thickness of 0.5μm, 1.0μm and 2.0μm and buried oxide thickness of 0.5μm under the same drift dose of 3.0e12/cm^2.

Table 4.1 Device parameters for Device 1 and Device 2 under study.

	Device 1	Device 2
T_{si} (μm)	0.5	2.0
T_{box} (μm)	0.5	0.5
N_d (cm^{-3})	6e16	1.5e16
$N_d \cdot T_{si}$ (cm^{-2})	3e12	3e12
Drift length L_d (μm)	3	3
Gate oxide thickness (nm)	70	70
Gate length (μm)	0.8	0.8
Gate width (μm)	1.0	1.0
BV (V)	79	92

In LDMOSFETs, the MOS channel and drift region are in series, with the same amount of drain current flowing through. The drain current causes a potential drop in the drift region, which determines the potential at the MOS channel drift end. This potential, in return, determines the current level of the intrinsic MOS, together with the gate voltage. Under a certain drain current level, a balance is reached between the MOS and the drift region with a certain amount of potential present at the channel drift end. At low current level, the MOSFET is in the saturation operation region. At a high current level, the potential drop in the drift region is high enough that it pushes the MOS into the linear region. In this case, a further increase of drain current pushes the MOS further into the drift region, which in turn slows down the increase of drain current with the gate voltage. The higher the drain current, the slower the drain current can increase further. As a result, the drain current shows saturation with the gate voltage. Figure 4.6 shows the change of potential at the channel drift end with the gate voltage for Device 1 and Device 2. In both devices, the potential decreases with the increase of the gate voltage. At low gate voltages, the potential is high for both devices. With the increase of the gate voltage to a higher level, both devices undergo a sharp decrease of the potential drop. With the further increase of the gate voltage, the decrease of potential saturates with the gate voltage. It corresponds to the saturation of drain current with the gate voltage. The potential at the channel drift end in Device 1 is higher than that in Device 2 under the same gate voltage. This means that the intrinsic MOSFET of Device 2 moves into the linear operation region earlier than that of Device 1. As a result, Device 2 shows a saturation of drain current at a lower gate voltage. However, at low gate voltages, the difference of potential does not lead to any difference in the drain current level since both Device 1 and Device 2 are in the saturation operation region. At high gate voltages, such as

20V, both devices are in the quasi-saturation region. The lower potential at the channel drift end in Device 2 leads to lower quasi-saturation current for Device 2.

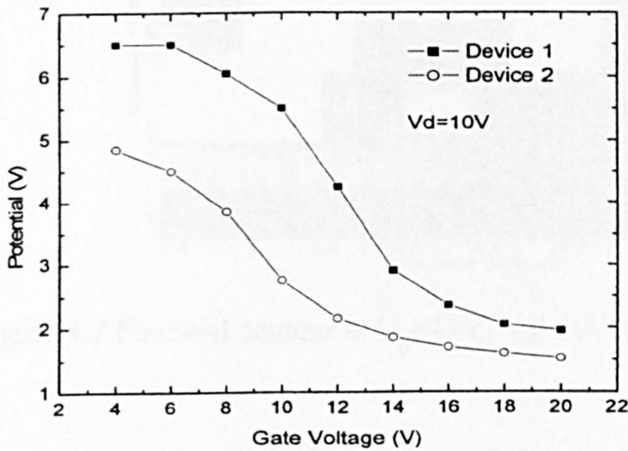

Figure 4.6 The potential at channel drift end versus the gate voltage for Device 1 and Device 2.

To investigate the cause of difference in potential drop at the channel of Device 1 and Device 2, the 2-D potential contour under the same current level of 3e-4A/μm for both Devices are shown in Figure 4.7 and Figure 4.8, respectively. It is shown that more potential is dropped in the drift region near channel in Device 2 compared to that in Device 1. Due to this, in contrast to Device 1, Device 2 is already in the quasi-saturation region under the same drain current level. The high potential drop in the drift near channel in Device 2 is attributed to the high electric field near channel (Figure 2.9) at high current level caused by velocity saturation and a result of the current path widening. The drain current can be expressed as $I \approx nqvbW$. When the current flows into the drift region from the channel, it spreads and the current path width widens. In case carrier velocity saturates, the velocity is a constant value. According to the current continuity, the carrier density n decreases, maintaining a constant current along the current flow path. When the current path width b increases to such an extent that the carrier density reduces to less than the doping density N, positive charge is present, as in a VDMOSFET structure [1, 4-8]. The net charge distribution along the current flow path in Device 2 is plotted in Figure 2.10. Positive and negative charge can be identified in this figure. The bell-shape electric field is not present in Device 1 as shown in Figure 2.11, due to the negligible current path widening and higher doping concentration in the drift region. According to the charge distribution in Figure 2.12, the positive charge caused by path width widening and carrier velocity saturation is not present in Device 1.

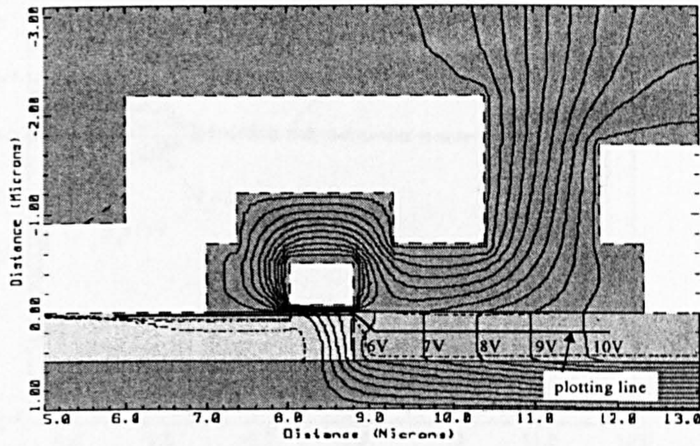

Figure 4.7 Potential contour at V_g=11V, V_d=10V, I_d=3e-4 A/μm for Device 1.

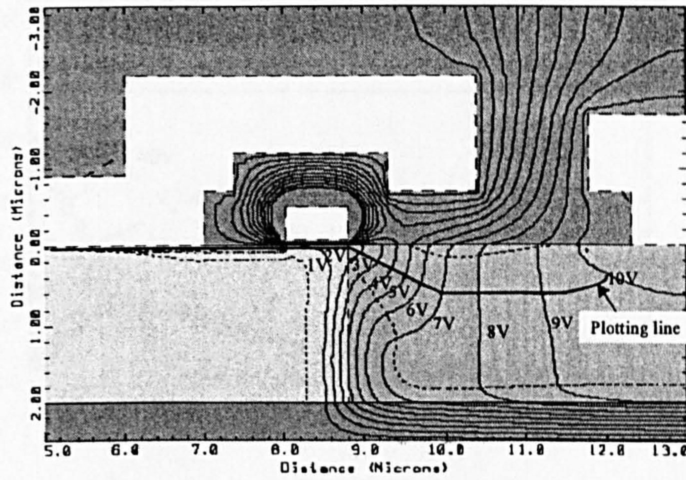

Figure 4.8 Potential contour at V_g=16V, V_d=10V, I_d=3e-4A/μm for Device 2.

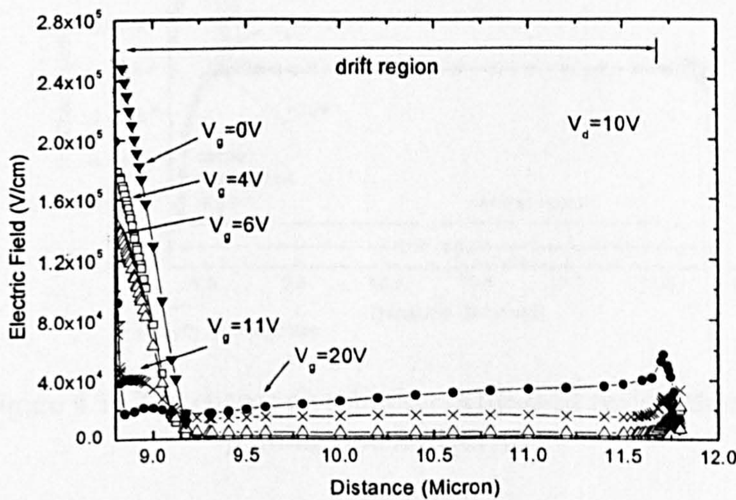

Figure 4.9 Electric field distribution in the drift region along the plotting line for Device 1.

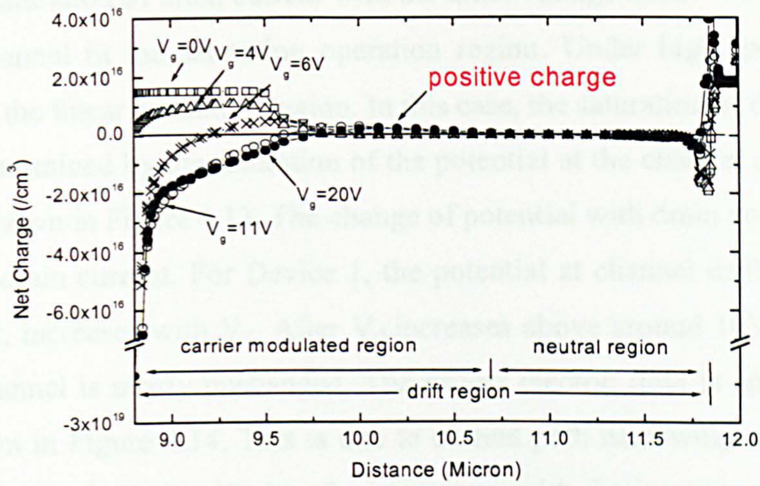

Figure 4.10 Net charge distribution along the plotting line for Device 2.

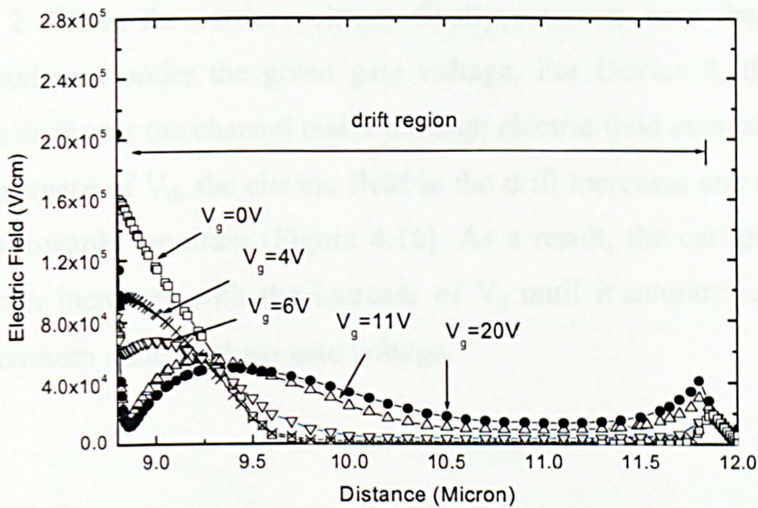

Figure 4.11 Electric field distribution along the plotting line for Device 2.

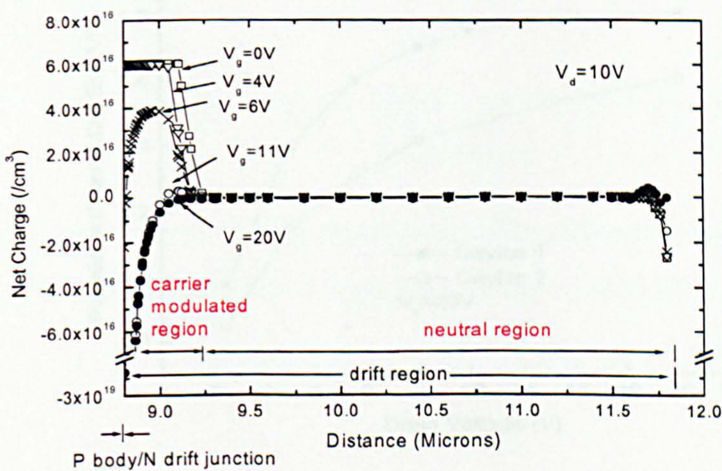

Figure 4.12 Net charge distribution in the drift region along the plotting line for Device1.

The saturation of drain current with the drain voltage under low gate voltages is due to the MOS channel in the saturation operation region. Under high gate voltages, the MOS channel is in the linear saturation region. In this case, the saturation of drain current with drain voltage is determined by the saturation of the potential at the channel drift end with the drain voltage, as shown in Figure 4.13. The change of potential with drain voltage shows the similar trend as the drain current. For Device 1, the potential at channel drift end and therefore the drain current, increases with V_d. After V_d increases above around 10V, the potential drop in the MOS channel is nearly unchanged. The excess electric field is applied at the drift drain end, as shown in Figure 4.14. This is due to current path narrowing near the drain when the depletion from the buried oxide interface increases with the increase of V_d. This leads to the increase of electric field near drain (Figure 2.15) for the same reason as depicted in section 2.1.4, chapter 2. When the carrier velocity finally saturates near drain, the drain current reaches the maximum under the given gate voltage. For Device 2, the carrier velocity is saturated in the drift near the channel under the high electric field even at low drain voltage of 5V. With the increase of V_d, the electric field in the drift increases and the high electric field region extends towards the drain (Figure 4.16). As a result, the carrier velocity at the drift region near drain increases with the increase of V_d until it saturates and the drain current reaches the maximum under a given gate voltage.

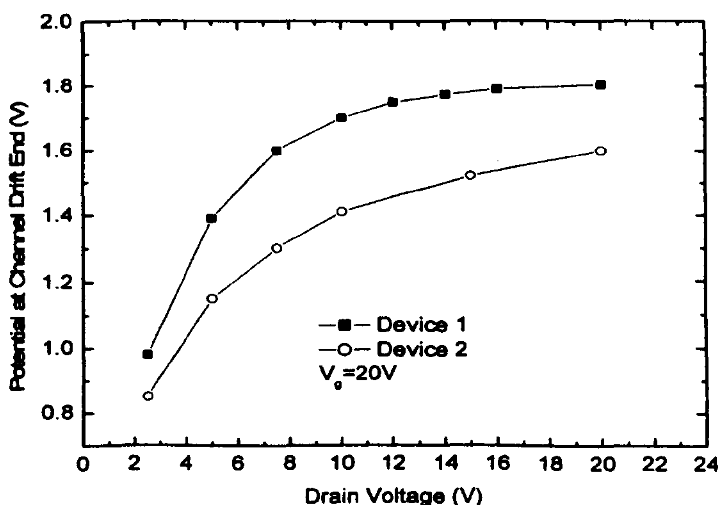

Figure 4.13 Potential at the channel drift end versus the drain voltage V_d for Device1 and Device2.

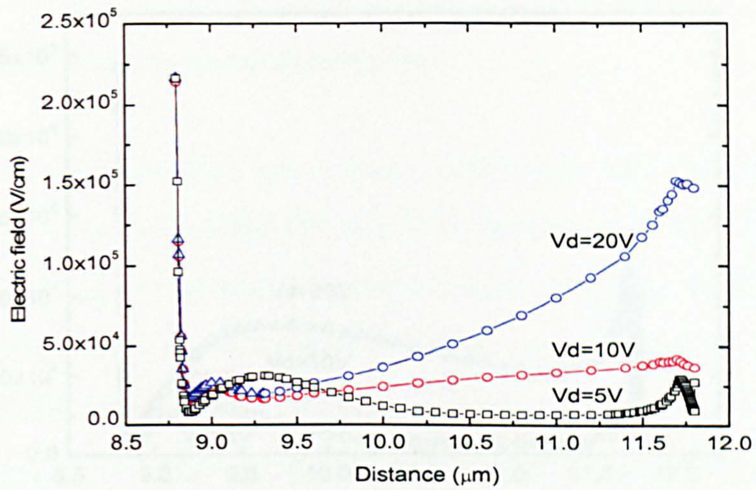

Figure 4.14 Electric field distribution in the drift region under various drain voltages for Device 1.

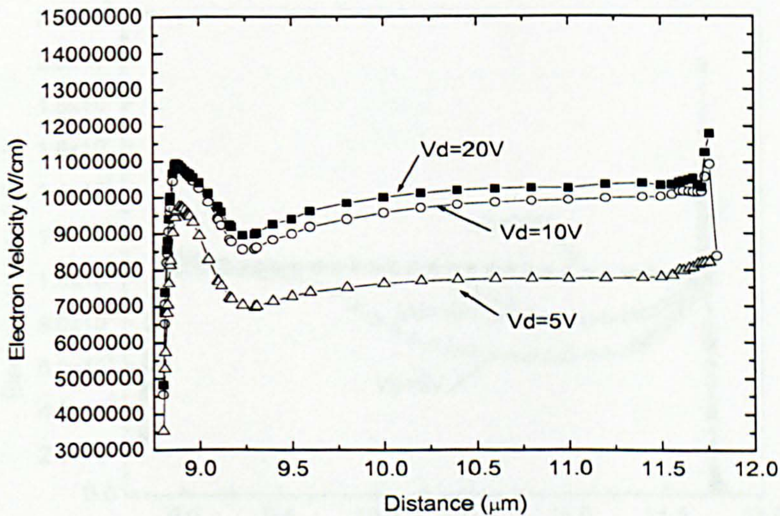

Figure 4.15 Electron velocity distribution along the current flow line in the drift region of Device 1 with drain voltage of 5V, 10V and 20V.

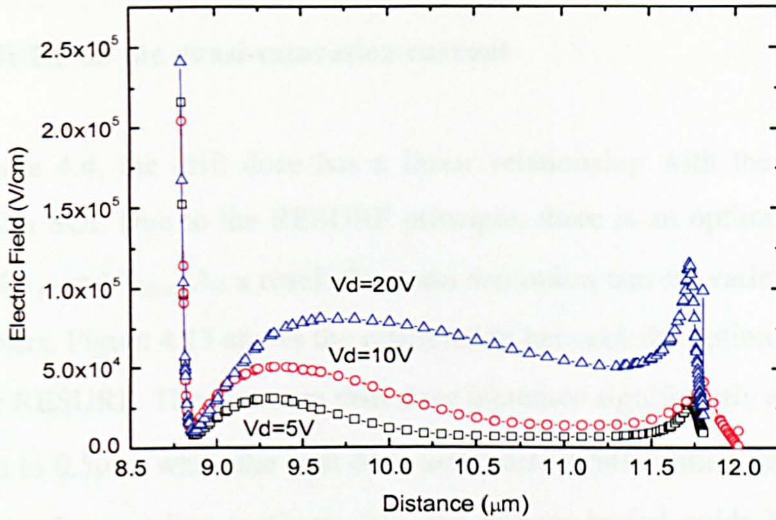

Figure 4.16 Electric field distribution along the current flow line in the drift region of Device 2 with drain voltage of 5V, 10V and 20V.

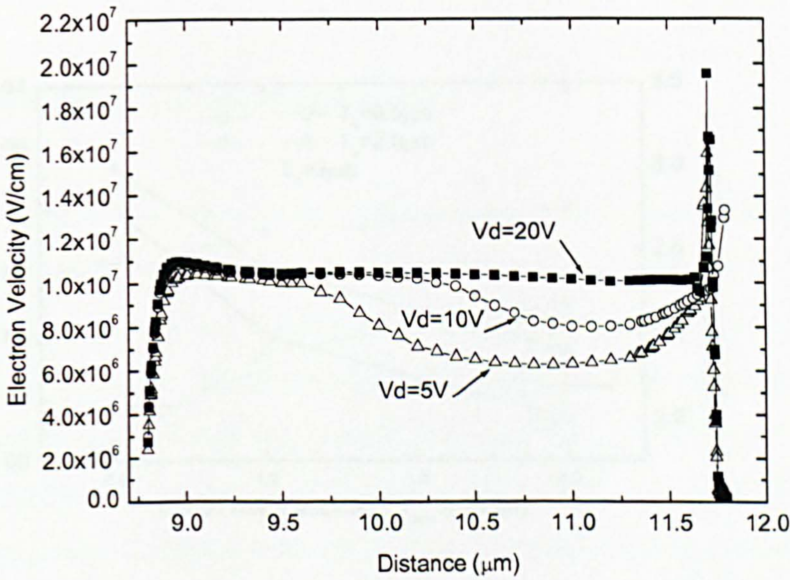

Figure 4.17 Electron Velocity distribution along the current flow path in the drift region of Device 2 with drain voltage of 5V, 10V and 20V.

4.5 Effect of RESURF on the quasi-saturation current

As shown in Figure 4.4, the drift dose has a linear relationship with the quasi-saturation current for thin film SOI. Due to the RESURF principle, there is an optimum drift dose for different values of T_{si} and T_{box}. As a result the quasi-saturation current varies with the device geometric parameters. Figure 4.13 shows the relationship between the optimum drift dose and T_{si} and T_{box} under RESURF. The optimum drift dose increases significantly as T_{box} is reduced from 2.0μm down to 0.5μm, while the drift dose increases slightly with a decrease of T_{si}. As analysed in Chapter 2, according to Gauss law, the thinner buried oxide leads to a higher optimum drift dose due to the higher electric field and thus higher charge density present in the top silicon layer. Due to the higher drift dose, the device with a T_{box} of 0.5μm displays a higher quasi-saturation current, compared to the devices with a T_{box} of 1.0μm and 2.0μm, as shown in Figure 4.14.

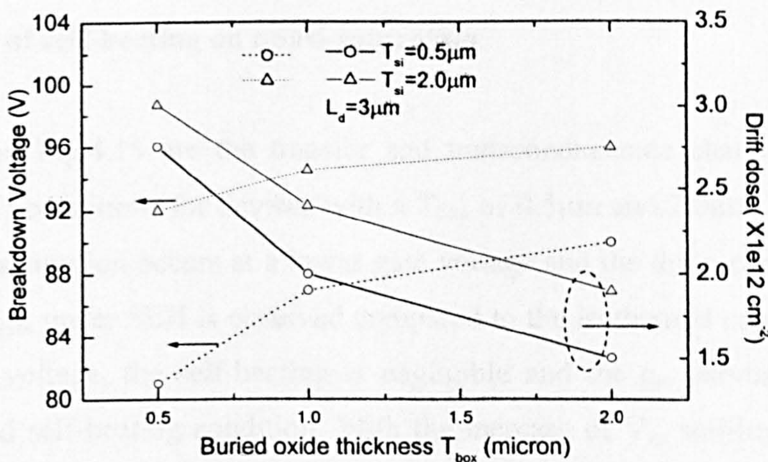

Fig.4.13 Optimum drift dose and breakdown voltage versus T_{box} with T_{si} of 0.5μm and 2.0μm.

To make a comparison, three devices with T_{box} of 0.5μm, 1.0μm and 2.0μm and T_{si} of 0.5μm are optimised to the same breakdown voltage of 85V, with the drift length of 3μm, 2.7μm, 2.6μm respectively. The transfer IV and transconductance characteristics for these three devices are shown in Figure 4.15. Due to its highest drift dose, the device with a T_{box} of 0.5μm has the highest current capability and the widest g_m curve. The saturation of drain current with gate voltages and g_m fall-off leads to a poor linearity and lower output power in

power amplifier applications. The device with a T_{box} of 0.5μm is thus preferable for a better linearity and higher output power compared to the devices with a T_{box} of 1.0μm and 2.0μm.

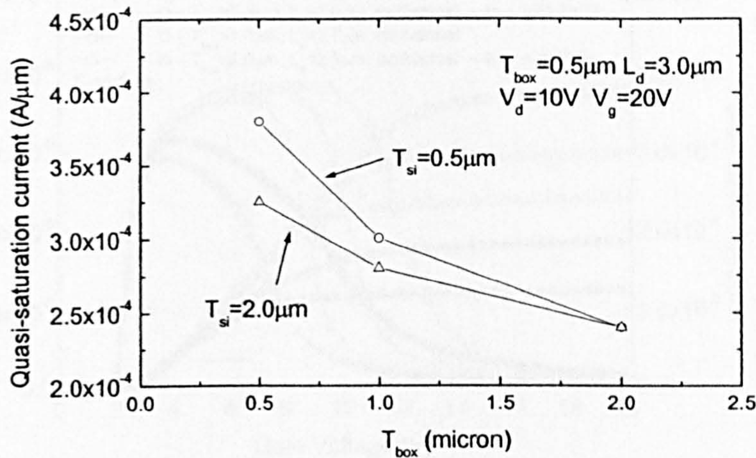

Figure 4.14 Quasi-saturation current versus T_{box} under optimum RESURF condition with T_{si} 0.5μm and 2.0μm

4.6 Influence of self-heating on quasi-saturation

Also shown in Fig.4.15 are the transfer and transconductance characteristics under SElf-Heating (SEH) conditions for devices with a T_{box} of 0.5μm and 2.0μm. For both devices, the drain current saturation occurs at a lower gate voltage and the drain current is reduced under SEH. A poor g_m under SEH is observed compared to the isothermal case for both devices. At the low gate voltage, the self-heating is negligible and the g_m curves are the same under isothermal and self-heating condition. With the increase of V_g, self-heating is more serious due to the higher power dissipation in the device. Therefore, the g_m under SEH condition decreases from the isothermal case

The decrease of the quasi-saturation current at high gate voltages under SEH is due to the carrier saturation velocity degradation at an elevated temperature. Shown in Figure 4.16 is the carrier velocity under various gate voltages with and without SEH. It also leads to the degradation of the transconductance.

Furthermore, comparing the transconductance and transfer IV characteristics for devices with a T_{box} of 0.5μm and 1.0μm. With SEH, the device with a T_{box} of 0.5μm has a higher quasi-saturation current and a better transconductance characteristics. This is due to the

thinner buried oxide layer in this device and the higher quasi-saturation current and wider transconductance under isothermal condition.

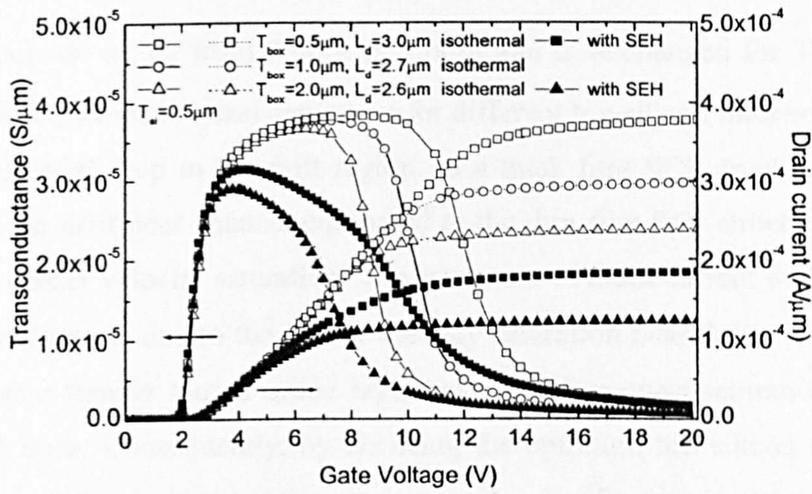

Fig.4.15 Transfer characteristics with and without SEH for three devices with a T_{box} of 0.5μm, 1.0μm, 2.0μm and a breakdown voltage of 80V.

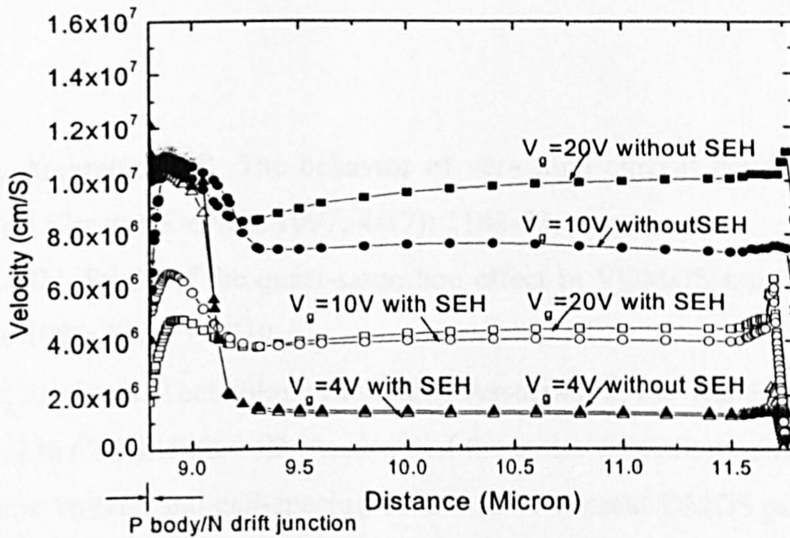

Fig.4.16 Electron velocity distribution in the drift region along the current flow path under various gate voltages in the device with a T_{si} of 0.5μm and a T_{box} of 0.5μm.

4.7 Summary

In this work, the quasi-saturation phenomenon is investigated. The quasi-saturation current versus drift dose is presented. In SOI LDMOSFETs, with a certain drift dose, I_{qsat} increases with the decrease of T_{si} from 3.0μm to 1.0μm and is unchanged for T_{si} between 1.0μm to 0.5μm. The difference in quasi-saturation for different top silicon thickness is attributed to the different potential drop in the drift region. In a thick film SOI structure, higher potential is dropped in the drift near channel compared to the thin film SOI structure, due to the current spread and carrier velocity saturation. The saturation of drain current with drain voltage under high gate voltages is due to the carrier velocity saturation near drain. It has been shown that devices with a thinner buried oxide layer have a higher quasi-saturation current due to the higher drift dose. Consequently, by choosing the optimum top silicon thickness and buried oxide thickness, the quasi-saturation current can be significantly increased. Under self-heating condition, the quasi-saturation current and g_m decrease from the isothermal case. This is due to the decrease of the carrier saturation velocity with the elevated temperature.

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Chapter 5 A High Performance RF LDMOSFET In Thin Film SOI Technology With Step-Drift Profile

Abstract

In this chapter, a Radio Frequency (RF) LDMOSFET with a step-drift doping profile, on a conventional thin film SOI substrate is investigated. The fabrication process for the drift formation is also proposed. A comparison is made between the step-drift LDMOS and the conventional Uniformly Doped drift (UD) LDMOS. It is demonstrated that step-drift device shows improvement in the kink effect, off-state breakdown, on-state breakdown, CV characteristics, drain current saturation behaviour and self-heating.

5.1 Introduction

Recently there has been increasing interest in developing thin-film SOI MOSFET for RF power amplifier applications [1-6]. Thin film SOI based on SIMOX technology, is the platform for the lower voltage SOI CMOS circuits [7]. Investigation of RF power MOSFET on SIMOX is of interest for the wireless System-On-Chip, which provides the integration of digital, analogue, and RF circuit on the same chip.

In the literature, mostly the breakdown voltages of the SOI MOSFET's reported to date are below 40Volts. However, for base station applications, about 85 volts breakdown voltage is needed. Moreover, the floating body effect is an important issue in such thin SOI MOSFET. This effect causes a kink in the I-V characteristics, which gives rise to distortion during power operation and produces poor power efficiency [8]. The floating body effect also leads to premature on-state breakdown, which limits the Safe Operating Area (SOA) of the device.

To avoid floating-body effect, the substrate of the MOSFET is usually grounded through a body-contact, a highly doped region shorted with the source region. There are several options available to achieve the body-contact in thin SOI. It includes the under-source body contact [5], by which a highly doped body-contact region is formed under the source region, and the body tie which is formed by interleaving the P^+ region into the source region [9], as shown in Chapter 1. However, even with these measures, kink effect in SOI may not be eliminated completely due to the high electric field in the device, as will be shown in the simulation results of UD devices as described below. In this work, using a step-drift doping profile, the thin film SOI RF LDMOSFET proposed demonstrates the eliminated kink effect and improved SOA thanks to the reduction of electric field.

Step-drift structure has been previously used in a RESURF MOSFET 6H-SiC [10], in which a two-zone drift region was used in order to prevent a high electric field near the channel/drift junction and the breakdown of the gate oxide. In addition, a step drift structure with two drift zones has also been used in RF LDMOSFET on bulk silicon to achieve lower feed-back capacitance [11]. This was achieved by using a lightly doped and shallow drift zone near the channel. In this work, a step-drift RF LDMOSFET structure with three drift zones on a thin film SOI layer is evaluated using numerical simulation. Besides the capacitance characteristics, the influence of the step drift doping profile on off-state breakdown voltage, on-state breakdown voltage, IV characteristics has been simulated and analysed. The device performance is compared with a UD device in the following section.

5.2 Device structure

The device structure under study is shown in Figure 5.1. A source shield is present in the structure. An under-source body contact is adopted, by utilising a P^+ region with a thickness of 0.1μm. The thickness of the P^+ region is determined by the depth of the N^+ source region, which is formed by ion implantation. The concentration of 5e19cm^{-3} is used for P^+ region ensuring that the body contact is not limited by its doping concentration. The drift region consists of three zones, D1, D2 and D3, with the doping concentration the lowest in D1 and highest in D3. To achieve the step drift doping profile, three drift implantations are carried out in sequence, as illustrated in Figure 5.2. The first implantation is performed into the D3 region, followed by the second implantation into both D3 and D2 regions. The last implantation is a blanket implantation forming the D1 region. The step-drift doping profile is optimised to achieve the maximum breakdown voltage. And as a comparison, a device with Uniform Doping (UD) is also investigated. Both devices are generated using TMA's TSUPREM-4 [12]. The electric characteristics of the step drift structure and the UD structure are simulated in 2-D device simulator MEDICI [13].

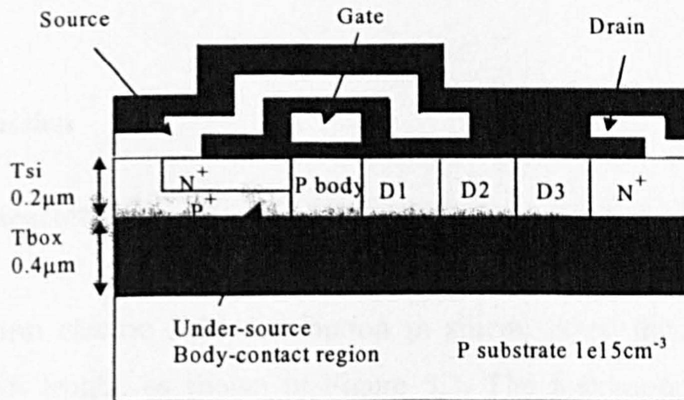

Figure 5.1 Device structure under study

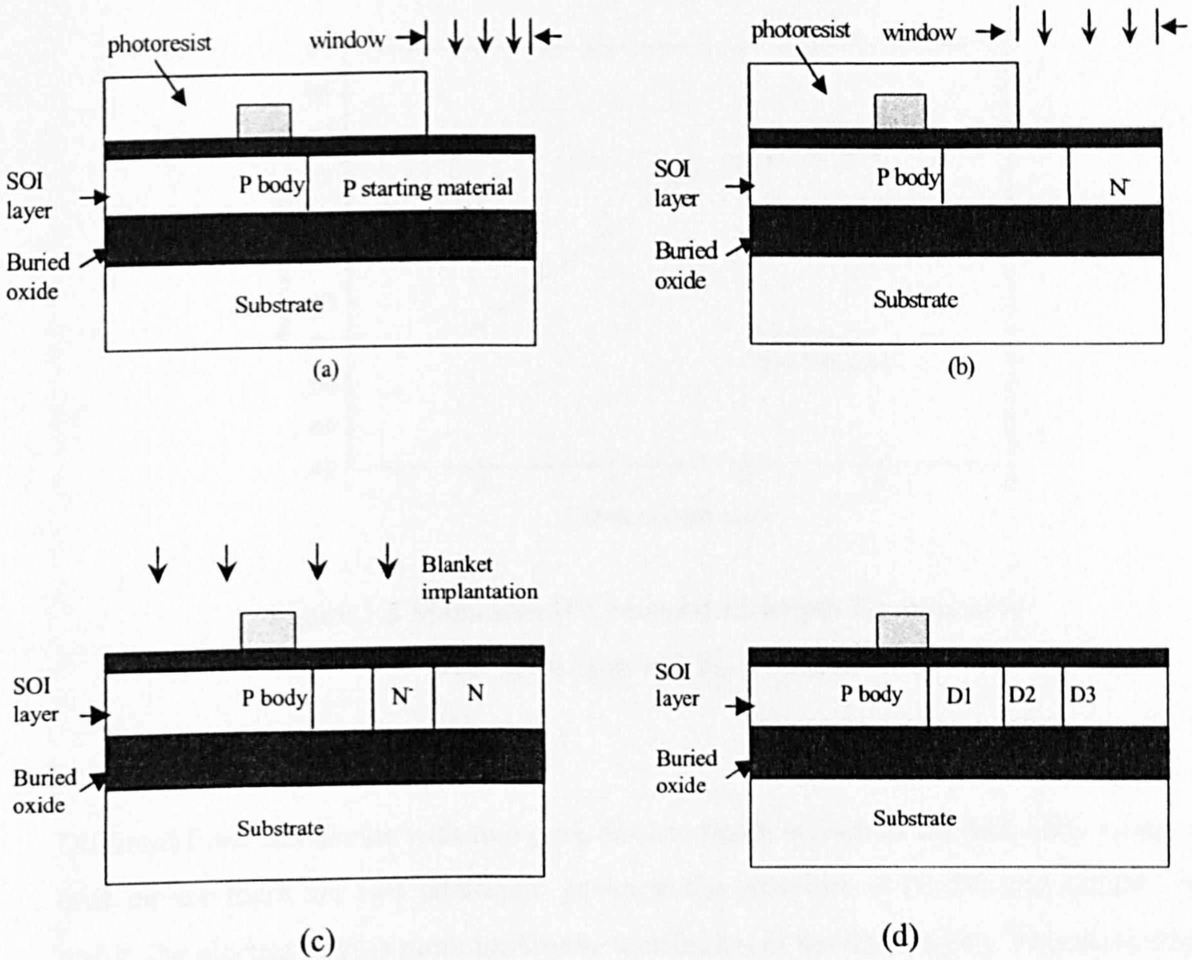

Figure 5.2 Proposed process sequences for step-drift formation

5.3 Results and discussion

5.3.1 Breakdown characteristics

Due to the non-uniform electric field distribution in silicon layer, the breakdown voltage saturates with the drift length, as shown in Figure 5.3. The maximum achievable BV on SIMOX substrate is about 78V with drift length at least 5μm for UD structure. Therefore, it is not suitable for high voltage base station applications, where the breakdown voltage of above 80V is needed and short drift length is desirable.

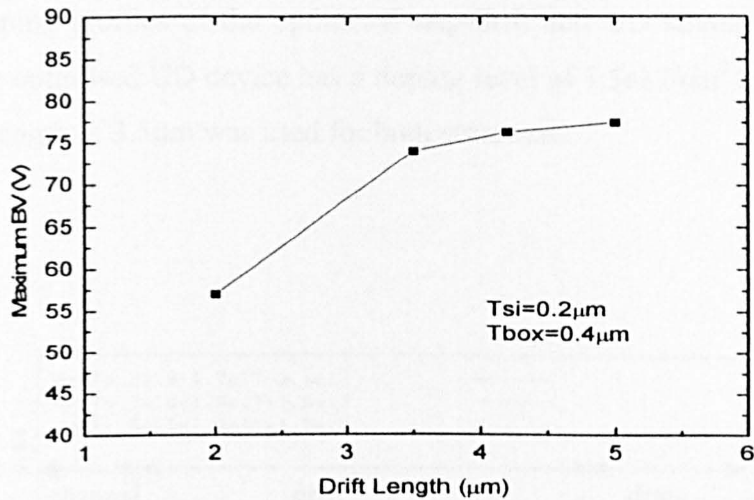

Figure 5.3 Maximum BV versus drift length for structures with T_{si}=0.2μm and T_{box}=0.4μm.

Different from UD device with two peak electric fields at both of the drift ends, in the step drift device there are two additional peaks at the junction of D1/D2 and D2/D3. As a result, the electric field is more uniformly distributed in the drift region. Therefore, higher voltage can be supported in the step drift region. By adjusting the length and doping level of D1, D2 and D3 regions, the electric field distribution in the step-drift device can be modified. The distribution of the electric field at Pbody/D1, D1/D2, D2/D3, D3/drain junction is determined by the doping level on both sides of the junctions. The maximum breakdown voltage is obtained when the electric field is more evenly distributed and the total impact ionisation is minimised. In this case, when the peaks of the electric field in the drift region are the same height the maximum breakdown voltage is obtained. As regard to the doping distribution, the doping levels in each region D1, D2 and D3 are equal to the average doping concentration in the same region of a device under ideal RESURF – with linear distributed doping. Figure 5.4 shows the electric field distribution at breakdown for devices with three different doping profiles of drift region. Device 1 with drift doping level of 8e16cm^{-3}/1.7e17cm^{-3}/2.3e17cm^{-3} has the highest BV of 93V due to the electric field being nearly evenly distributed. Therefore, it is taken as the optimum design for the step-drift device. The other two devices have much higher peak electric fields at the channel end and drain end of the drift region, resulting in lower breakdown voltage. The original source files for process simulation are attached in the thesis as Appendix C. The device parameters of the optimised step-drift device, as well as that of the UD device, are listed in table 5.1. To make a reasonable comparison, the device

parameters are kept the same for both devices, except the doping profile of the drift region. The doping profiles of the optimised step-drift and UD structures are shown in Figure 5.5. The optimised UD device has a doping level of 1.5e17/cm^3 in the drift region. A drift region length of 3.5μm was used for both structures.

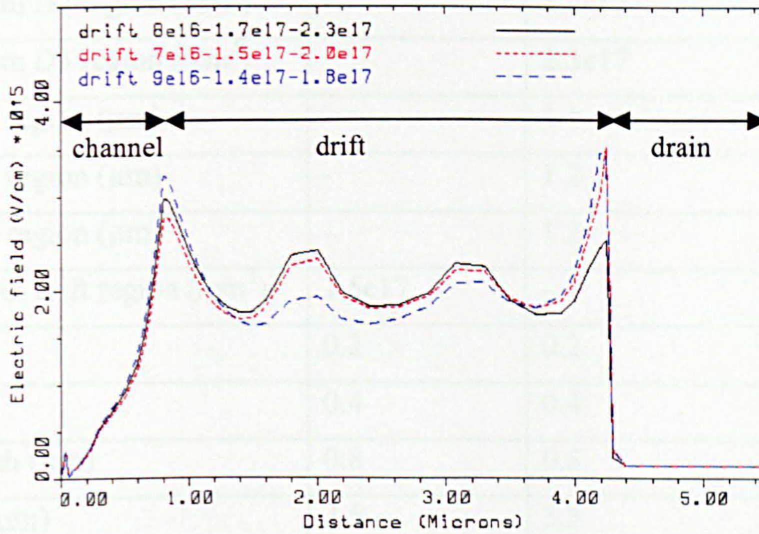

Figure 5.4 shows the electric field distribution under various drift doping profile.

Table 5.1 device parameters for UD and step drift device

Parameters	UD device	Step drift device
Doping level in D1 region (/cm^3)	-	8e16
Doping level in D2 region (/cm^3)	-	1.7e17
Doping level in D3 region (/cm^3)	-	2.3e17
Length of D1 region (μm)	-	1.1
Length of D2 region (μm)	-	1.2
Length of D3 region (μm)	-	1.2
Doping level in drift region (/cm^3)	1.5e17	-
T_{si} (μm)	0.2	0.2
T_{box} (μm)	0.4	0.4
Channel length (μm)	0.8	0.8
Drift length (μm)	3.5	3.5
Gate oxide thickness (nm)	70	70

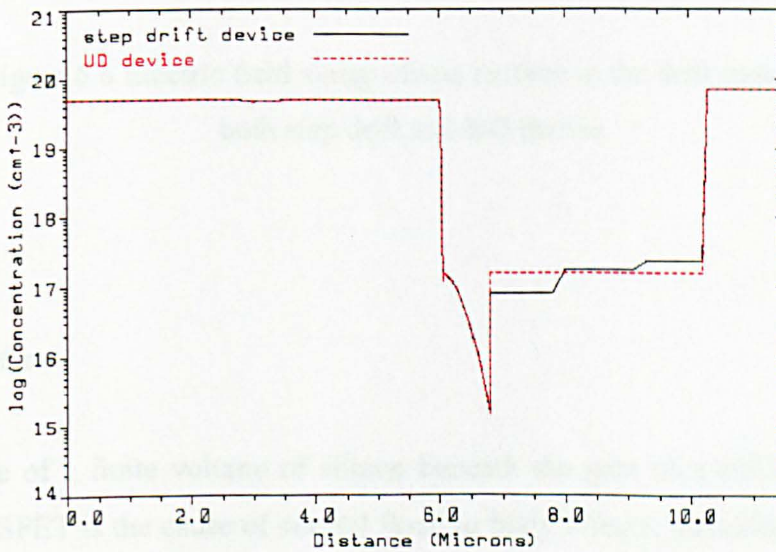

Figure 5.5 Doping profile along silicon surface for both step drift and uniform drift device

As the simulation shows, the UD device has the maximum breakdown voltage of 74V with the drift length of 3.5μm. Compared to the UD device, step-drift device, which shows a BV of 93V, enables a 26% increase in breakdown voltage. This significant increase can be explained by different electric field distribution at breakdown, as shown in Figure 5.6. The UD device has a non-uniform electric field distribution, with two high peak electric fields at the channel end and the drain end of the drift region, and a low level of electric field of 1.2e5V/cm in the middle of the drift region. The step-drift device has a nearly uniform electric field distribution at breakdown, which means a higher potential drop or breakdown voltage.

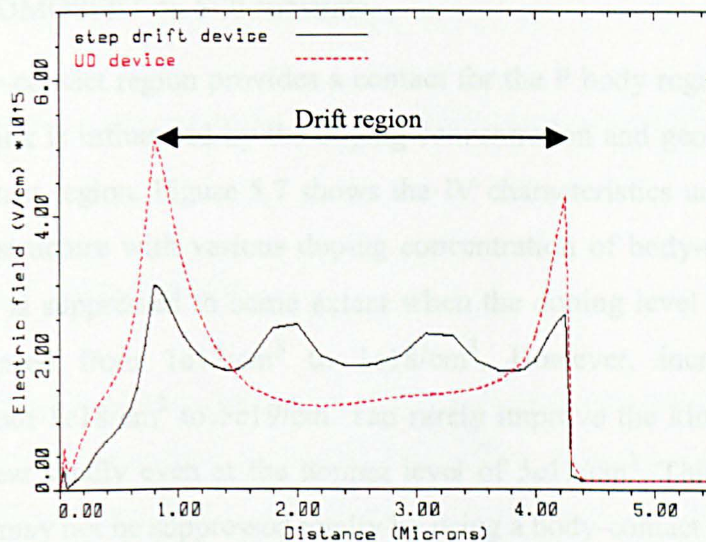

Figure 5.6 Electric field along silicon surface in the drift region for both step drift and UD device.

5.3.2 Kink effect

The presence of a finite volume of silicon beneath the gate of a silicon-on-insulator n-channel MOSFET is the cause of several floating body effects, including kink effect [14]. Kink effect is manifested as a drain current increase on I-V curves at a certain drain voltage. It is undesirable since it degrades the linearity of the IV characteristics, which prevents the devices from being used for analog applications requiring a high linearity of output signal. Furthermore, it can cause current overshoot [15] in the device and it is difficult to model and implement in circuit simulators [16].

5.3.2.1 Mechanism of kink effect in SOI MOSFET

Kink effect is caused by injection of holes into the floating substrate of a SOI MOSFET [17,18]. In a MOSFET, the high electric field exists in the channel region near the drain. When carriers travel through this region, holes are generated by impact ionisation. Once generated, holes migrate to the lowest potential region, the P body region, which is the floating substrate of the MOSFET. The accumulation of holes raises the potential of this floating region and the source-substrate junction becomes forward-biased. This leads to a reduction of the depletion region in the source junction, which gives rise to a reduction in the threshold voltage according to the well-known source-substrate bias effect [19], and to a kink in the output characteristics of the device. For the same reason the kink effect presents in RF LDMOSFET on SOI substrate.

The body-contact region provides a contact for the P body region with the ground. Obviously the kink is influenced by the doping concentration and geometrical parameters of the body contact region. Figure 5.7 shows the IV characteristics under gate voltage of 4V for the UD structure with various doping concentration of body-contact region. It is shown that kink is suppressed to some extent when the doping level in the body-contact region is increased from 1e17/cm^3 to 1e18/cm^3. However, increasing the doping concentration from 1e18/cm^3 to 5e19/cm^3 can rarely improve the kink further. The kink does not disappear totally even at the doping level of 5e19/cm^3. This shows that in UD device, the kink may not be suppressed totally by using a body-contact region.

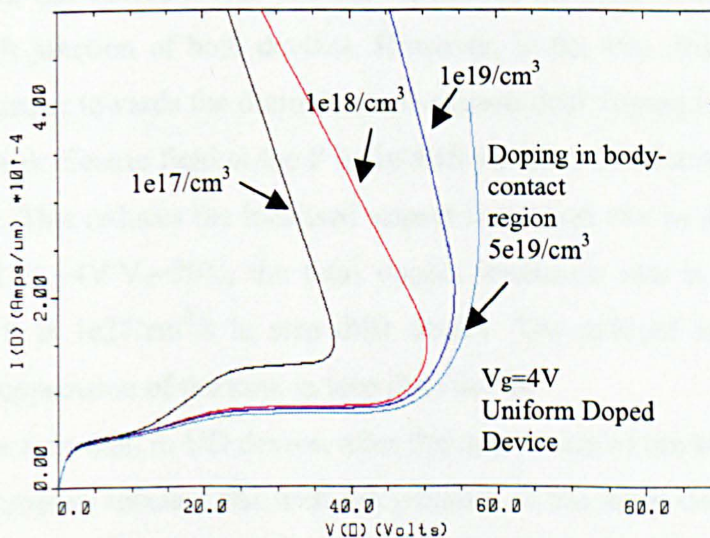

Figure 5.7 IV characteristics for devices with various doping level in the body-contact region.

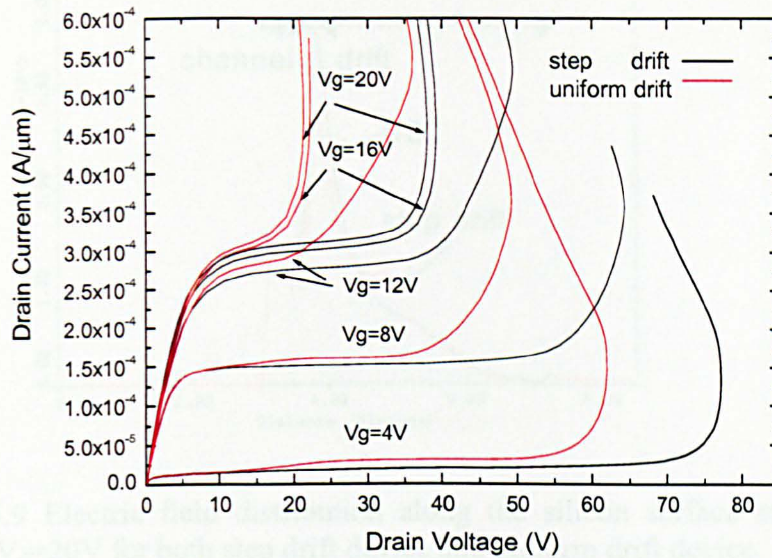

Figure 5.8 I-V characteristics for both step drift device and uniform drift device.

5.3.2.2 Kink in IV characteristics

The I-V characteristics of both step drift and UD devices are shown in Figure 5.8. As can be seen, the step-drift structure shows no kink effect. However, it occurs in the I-V characteristics of UD device at V_g=4V/V_d=18V, V_g=8V/V_d=16V. To reveal the reason, the electric field distribution at V_g=4V/V_d=20V in UD device is plotted in Figure 5.9, just after the occurrence of the kink. To make a comparison, the electric field distribution at the same bias in UD device is also plotted. As shown, the peak electric field is present at the p body/drift junction of both devices. However, in the step drift device, the electric field spreads further towards the drain due to the lower drift doping level in D1 region and therefore the peak electric field at the P body/drift junction is reduced compared to that in the UD device. This reduces the localised impact ionisation rate as shown in Figure 5.10. At the bias of V_g=4V/V_d=20V, the total impact ionisation rate is 2.5e27/cm^3/s in UD device, while it is 1e27/cm^3/s in step drift device. The reduced impact ionisation rate results in the suppression of the kink in step drift device.

It can be seen that, in UD device, after the occurrence of the kink in the UD device, the I-V characteristics remains flat with the increase of the drain voltage until the device finally breaks down. This can be explained by the unchanged peak electric field value at the P body/N drift junction when the drain voltage increases until V_d=60V as shown in Figure 5.11.

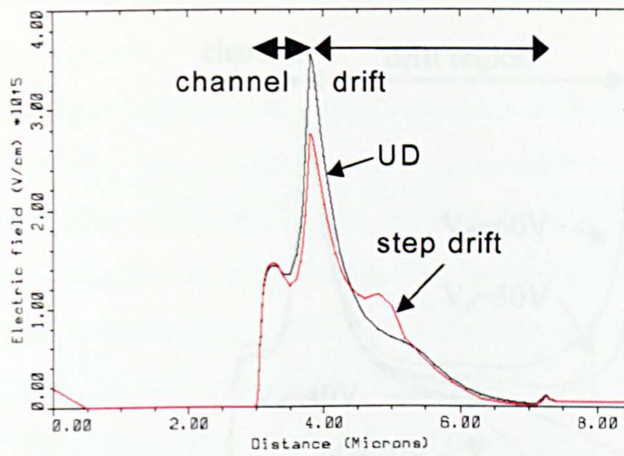

Figure 5.9 Electric field distribution along the silicon surface at V_g=4V, V_d=20V for both step drift device and uniform drift device

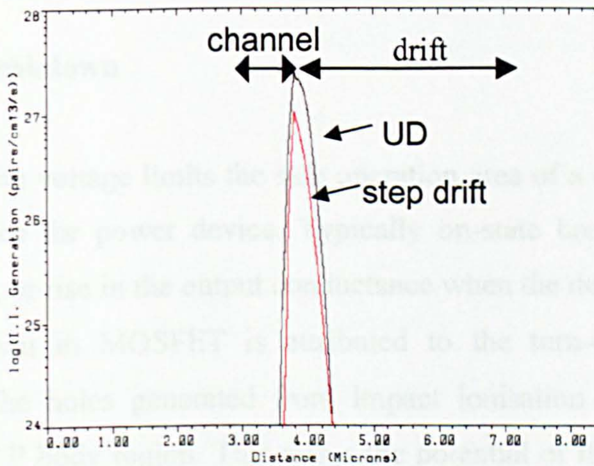

Figure 5.10 Impact ionization rate at V_g=4V, V_d=20V for step drift device and UD device.

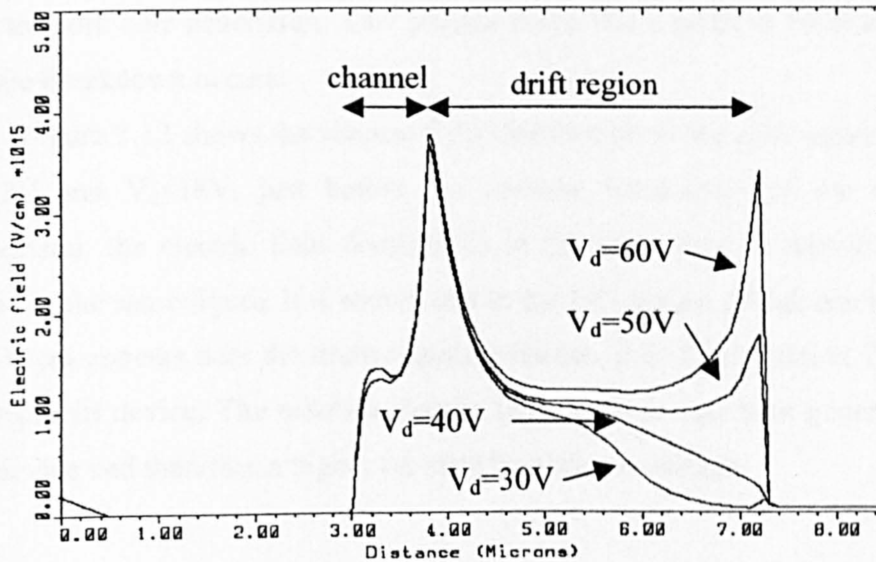

Figure 5.11 Electric field distribution along silicon surface under V_g=4V, V_d=30V, 40V, 50V and 60V in UD device.

5.3.3 On-state breakdown

On-state breakdown voltage limits the safe operation area of a device and is a parameter of primary importance for power device. Typically on-state breakdown is thought of as a significant upturn, or rise in the output conductance when the device is in on-state operation. On-state breakdown in MOSFET is attributed to the turn-on of the parasitic bipolar transistor [20]. The holes generated from impact ionisation under a high electric field accumulate in the P body region. This raises the potential of the P body region and finally triggers the parasitic bipolar transistor composed of the N^+ source region, the P body region and the N^- drift region. The on-state breakdown of both the UD device and the step-drift device can be inferred from Figure 5.8. On-state breakdown occurs when the drain current increases sharply with the drain voltage. The on-state breakdown voltage of the UD device is 20V under gate voltage of 20V. While it is 36V in the step-drift device at the same gate voltage, which corresponds to an 80% increase under this bias condition.

To investigate the influence of the drain voltage on the on-state breakdown voltage, the electric field distributions along the silicon surface at a gate voltage of 4V and various drain voltages, are shown in Figure 5.11. For a drain voltage below 60V, the electric field at the drift/drain junction is low. While at V_d=60V, a sharp increase of the electric field at the drift drain end can be observed. This high electric field generates a large amount of

electrons and holes, which leads to a higher drain current. In turn, the higher drain current leads to more hole generation. This process plays like a positive feedback and finally the on-state breakdown occurs.

Figure 5.12 shows the electric field distribution in the drift region of UD device at V_g=12V and V_d=18V, just before the on-state breakdown of the UD. To make a comparison, the electric field distribution at the same bias in step-drift device is also plotted in the same figure. It is shown that in the UD device, a high electric field of nearly 2.1e5V/cm appears near the drain region, whereas, it is 1.1e5V/cm at D1/D2 junction in the step drift device. The reduced electric field leads to less hole generation in the step-drift device and therefore a higher on-state breakdown voltage.

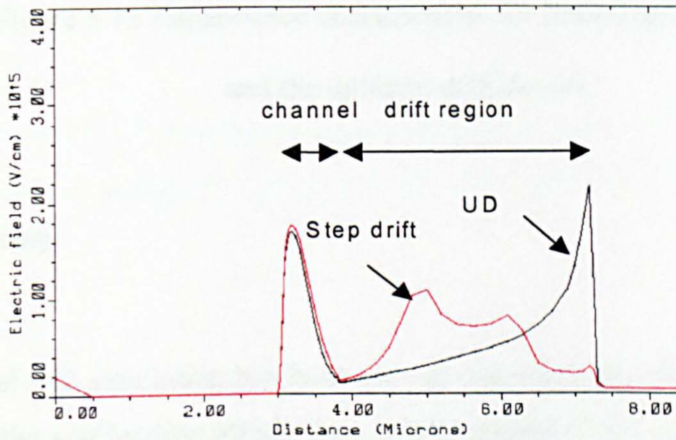

Figure 5.12 Electric field distribution along silicon surface at V_g=20V, V_d=18V for both step-drift device and uniform drift devices

5.3.4 Capacitance

The capacitance characteristics for both the UD and the step-drift LDMOSFET are presented in Figure 5.13. As shown, the step-drift device has a lower feedback capacitance C_{rss}. It is due to the lower drift doping near channel in the drift region, which results in a wider depletion region in the drift therefore a lower capacitance C_{ddpel}. C_{ddpel} in the drift contributes to the feedback capacitance C_{rss}, as shown in Equation 2-27 and Equation 2-28. As a result, step drift device has a lower C_{rss} , which means a high power gain.

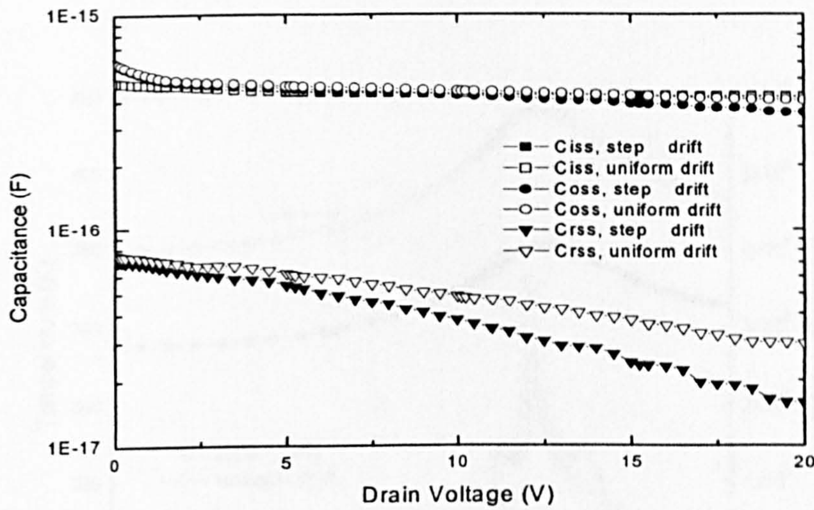

Figure 5.13 Capacitance characteristic for both step-drift device

and the uniform drift device

5.3.5 Self-heating

Non-isothermal 2-D simulation has been carried out using the MEDICI simulator in order to investigate the self-heating effect. As a power amplifier, the LDMOSFET's are usually operated at AB class, where the device is biased just above cut off. In base station applications with supply voltage of 28V, the LDMOSFETs are typically biased at about V_g=4V, V_d=28V. The self-heating at this bias contribute to the self-heating of the device in operation. The temperature distributions in both devices at this bias are plotted in Figure 5.14. As can be seen, the peak temperature rise in the UD device is about 20K higher than that in the step drift device. The difference between the UD device and step drift device is due to the drift doping profile, which causes the different drain current and electric field level, therefore the different self-heating level. As indicated in Figure 5.14, there is a higher peak electric field present in the UD device at the P body/N drift junction compared to that in the step-drift device. Furthermore, the UD device has a higher drain current due to the present of the kink at the bias point as shown in Figure 5.8. Since the Joule heating is determined by the electric field and current level, more heat is generated in the p body/drift junction in UD device due to the higher peak electric field and also higher drain current at

the bias point. Consequently a higher temperature rise is present in the p body/drift junction of the UD device.

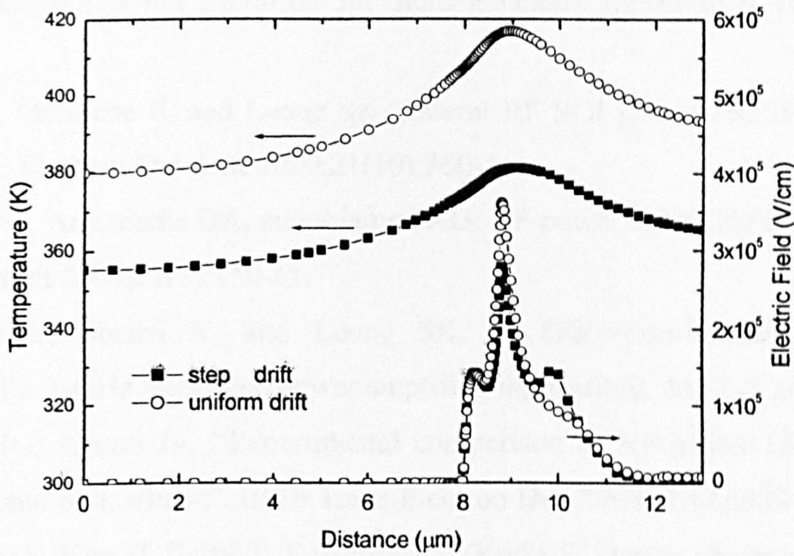

Figure 5.14 Temperature distribution and electric field distribution along silicon surface at V_g=4V, V_d=28V for both UD and step drift device.

5.4 Summary

The enhanced performance of a SOI LDMOSFET has been demonstrated with a step doping profile. Compared to a Uniformly Doped drift (UD) device, this step drift device has an increased voltage handling capability and suppressed parasitic bipolar behaviour, which is demonstrated by the elimination of kink and higher on-state breakdown voltage. The feedback capacitance is also slightly reduced. Even though this technology requires extra masks for drift formation compared to the UD structure, the performance advantages indicate that the proposed device is well suited for RF IC integration in mainstream SOI technologies.

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Chapter 6 A LDMOSFET on SON For RF Applications

Abstract

A novel RF LDMOS on partial Silicon-on-Nothing (SON) is investigated [1]. In comparison to SOI technology, the empty space in SON has a lower dielectric constant ($\varepsilon = 1$) than the buried oxide in SOI ($\varepsilon = 3.9$). This leads to reduced drain substrate capacitance, hence lower substrate loss. However, due to the low breakdown strength of air, the SON MOSFET is limited to low voltage application. A SON LDMOS is investigated for high voltage application for the first time. Extensive simulation results of BV and CV characteristics of SON LDMOSFET's are presented. A comparison is made between LDMOSFET's using SON and SOI technologies in terms of the breakdown voltage, forward IV, transconductance, capacitance, substrate loss and thermal behaviour. SON LDMOS is shown to be a promising alternative to the SOI structure in terms of capacitance characteristics and substrate loss.

6.1 Why use SON ?

For RFIC on bulk Si, substrate loss is a major concern. It represents the energy dissipated in the silicon substrate. Substrate loss degrades Q of passive components [2-5]. For LDMOSFETs, substrate loss degrades the efficiency, gain and the maximum frequency f_m of RF amplifiers [6-9]. Previously, by reducing the drain substrate capacitance C_{dsub}, the maximum oscillation frequency f_{max} of LDMOS was shown to be increased by 30% [10]. The SOI substrate has been found to be a good alternative for lower substrate loss [6,8]. With the increasing demand for high performance RF LDMOSFET, further reduction in capacitance and substrate loss is desired. In this chapter, a SON LDMOSFET with an empty space layer is investigated for RF power applications. With the dielectric constant of air ($\varepsilon \approx 1$) being lower than that of silicon dioxide ($\varepsilon = 3.9$), an empty space layer has a much lower capacitance than the buried oxide, according to the expression of unit area dielectric layer capacitance as

$$C = \frac{\varepsilon\varepsilon_0}{t} \qquad \text{Equation 6-1,}$$

where ε is the permittivity of the dielectric material, ε_0 is the permittivity in vacuum, t is the thickness of the dielectric layer. A lower capacitance and substrate loss of SON structure compared to SOI technology is possible.

6.2 Fabrication technology of SON devices

A low-voltage SON MOSFET was firstly proposed by Malgorzata Jurczak et al. to overcome a short channel effect and issues related to thin gate oxides in devices down to 100nm [11]. A schematic cross-section of the SON MOSFET is shown in Figure 6.1 and the key process steps are illustrated in Figure 6.2. [12]. The fabrication process of the SON transistor starts from a conventional silicon substrate. Then the epitaxy of SiGe layer is performed. On top of that a silicon epitaxial layer is grown. Following that, the conventional CMOS process steps are subsequently carried out until the formation of the spacers. Then the trenches in source/drain regions are formed using anisotropic plasma etching in order to provide access to SiGe, which is then selectively etched. The removal of SiGe from underneath of the top Si layer forms an air tunnel, or an empty space layer. Despite the air tunnel, the gate does not collapse because it bridges the active area and is supported at both ends by the STI. Finally, the Source/Drain regions are rebuilt by epitaxy. The advantage of this process is that both silicon films and empty space layers can be much thinner and much better controlled than in

any conventional SOI technology, since the epitaxial process is capable of producing the layers at nanometer scale with excellent uniformity and a resolution below 1nm.

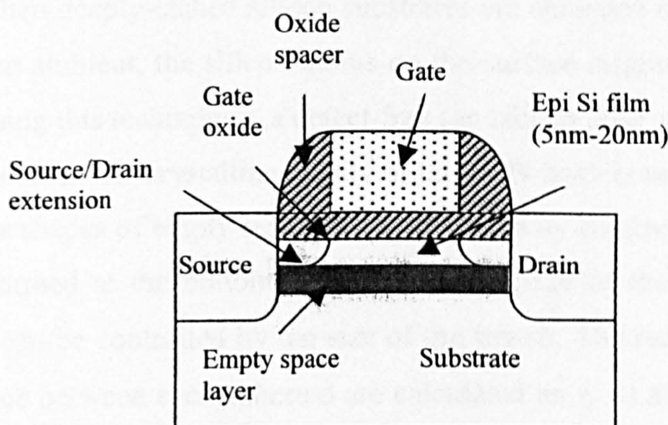


Figure 6.1 schematic cross section of the SON MOSFET for low voltage application.

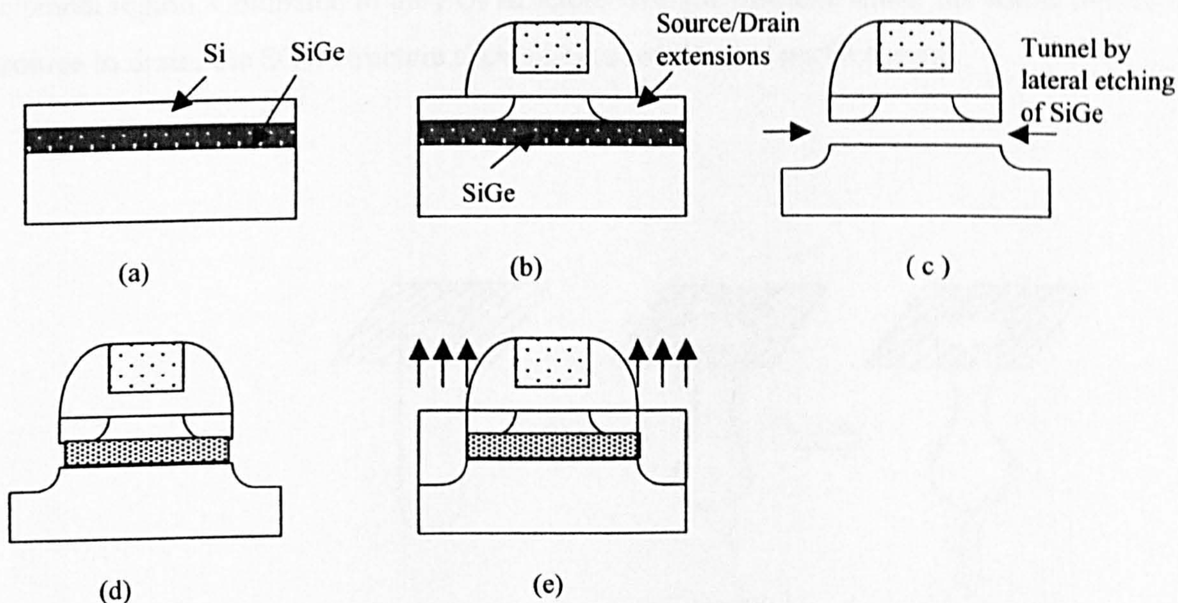


Figure 6.2 Fabrication process of the SON MOSFET: (a) epitaxy of SiGe and Si layer on isolated bulk wafer; (b) conventional CMOS process steps until the formation of the nitride spacers; (c) formation of the shallow trenches in the S/D regions and formation of the tunnel under the Si film; (d) filling the tunnel with oxide (optional step); (e) selective epitaxy of S/D regions, implantation and Rapid Thermal Anneal (RTA).

In 1999 Tsutomu Sato etc. from Toshiba proposed a new technology of forming an empty space layer in silicon [13, 14]. The sequence for the empty space formation is schematically summarized in Figure 6.3. It makes use of the self-organising migration properties on the silicon surface. When deeply-etched silicon substrates are annealed in a deoxidising ambient, such as a hydrogen ambient, the silicon atoms on the surface migrate so as to minimize the surface energy. Using this technology, a defect-free top silicon layer and an empty space layer can be easily fabricated. The crystalline quality of the SON layer is comparable to that of bulk silicon and various shapes of empty space can be obtained by connecting the spherical empty space, which is formed at the bottom of a trench. The size of the sphere is an important parameter, which can be controlled by the size of the trench. The radius of the empty sphere (r_b) and the distance between each sphere d are calculated as $r_b = 1.88 r_a$ and $d = 8.89 r_a$, where r_a is the radius of the initial cylindrical trench rod as shown in Figure 6.4. The fabricated SON MOS transistor demonstrates a comparable electric performance with that of the conventional devices and is shown to have a flat silicon surface and a good $Si\text{-}SiO_2$ interface property [14]. The SON device shows 8% reduction on junction capacitance due to the present of empty space layer [14]. The investigated SON structure has an empty space layer only under the channel region. Compared to the SOI structure with the insulator under the whole device from source to drain, the SON structure shows improved thermal performance.

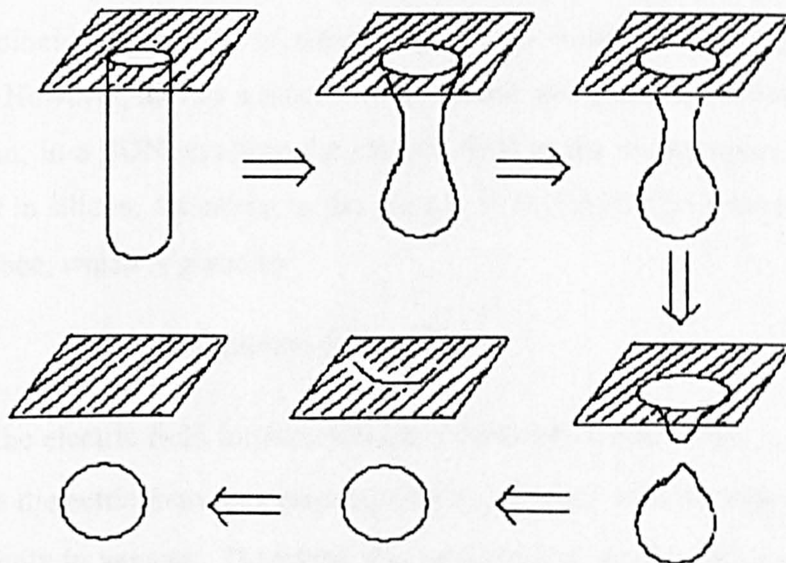


Figure 6.3 the self-organizing sequence for the empty space formation in silicon.

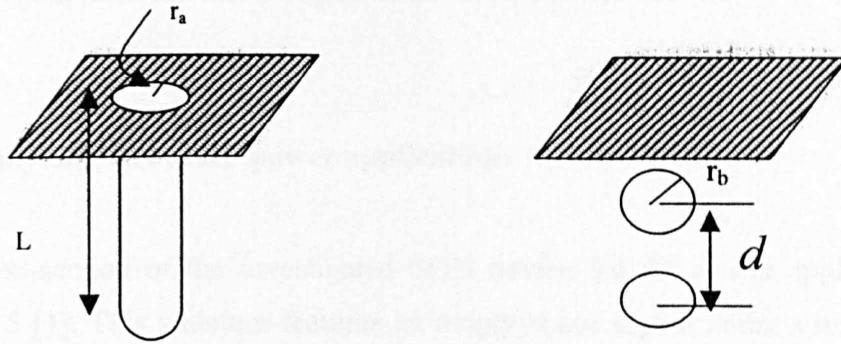


Figure 6.4 Relationship between the initial shape of trench and the size of the spherical empty spaces.

6.3 Challenge of applying SON technology in RF power applications

The SON devices reported are for low power applications. In RF power LDMOSFET, high electric field is present in the device due to the high drain voltage applied. In the conventional SOI structure, most of the drain voltage is supported by the lightly-doped drift region in the lateral direction. In the vertical direction, most of the drain voltage is supported by the buried oxide layer. Silicon dioxide is capable of supporting a high electric field with an electric strength of 1e7V/cm. However, air has a much lower electric strength of 3e4V/cm to support a high BV. In addition, in a SON structure the electric field in the empty space is about 12 times higher than that in silicon, according to the electric field distribution relationship at the dielectric layers interface, which is given by

$$\frac{\varepsilon_0 \varepsilon_1}{E_2} = \frac{\varepsilon_0 \varepsilon_2}{E_1} \qquad \text{Equation 6-2,}$$

where E_1 and E_2 are the electric field for two dielectric materials respectively, ε_1 and ε_2 are the permittivity of the dielectric materials respectively, in this case 11.8 for silicon and 1 for air, ε_0 is the permittivity in vacuum. Therefore, if a conventional device structure is used in SON technology, the achievable BV will be very low, limited by the air. In order to apply SON technology to RF power applications, new structures need to be used. Furthermore, air has a much poorer thermal conductivity, 0.026W/mK, compared to silicon dioxide, 1.4W/mK,

at 300K [15]. The presence of the empty space layer thus increases the thermal resistance of the heat conduction path from the active region of the device to the bottom.

6.4 Solution to applying SON to RF power applications

The schematic cross-section of the investigated SON device for RF power applications is shown in Figure 6.5 [1]. This structure features an empty space region under a buried oxide layer with a silicon layer between the two dielectric layers. To improve the hear conduct ability in the structure, the empty space layer under the source and part of the channel region is replaced by silicon. This partial empty space structure is beneficial for heat conduction.

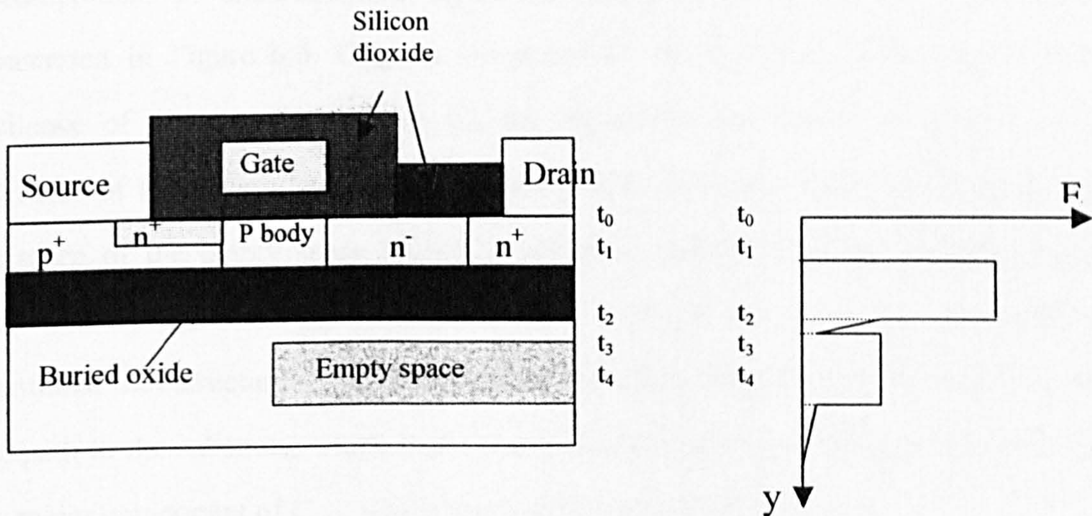


Figure 6.5 (a) schematic cross section of SON RF LDMOS device with sandwich structure. (b) electric field distribution along the vertical direction in SON sandwich structure.

6.4.1 Breakdown in RF SON LDMOFET

The SON sandwich structure has a different electric field distribution in the vertical direction from that in a conventional SOI structure, as shown in Figure 6.5 (b). The electric field distribution in the top silicon layer and buried oxide layer is the same as in the conventional SOI structure. At the interface of the top silicon and buried oxide layer, the electric field distribution is described by Equation 6-2. As in a conventional MOS capacitor, there is positive charge in the top silicon layer near the top silicon and buried oxide interface.

Conversely, there is negative charge present in the silicon gap layer near the buried oxide and silicon gap interface. When the drain voltage is high enough, an inversion layer is present in the silicon gap layer. The high density of electrons in the inversion layer leads to a sharp decrease of the electric field towards the substrate according to Gauss law, as can be seen from Figure 6.5 (b). Near the interface of the silicon and empty space layer, the electric field in the empty space layer is about 12 times higher than that in the silicon gap. However, the electric field in the empty space is still less than the dielectric strength of air, 3e4V/cm. In the SON sandwich structure most of the drain voltage is supported by the buried oxide, thus the SON sandwich structure has the same breakdown voltage as a SOI alternative.

6.4.2 Capacitance in SON RF LDMOSFET

The components of drain-substrate capacitance C_{dsub} in the SON sandwich structure are demonstrated in Figure 6.6. C_{dsub} is composed by the following capacitances in series: capacitance of the top silicon layer C_{si}, the capacitance of buried oxide layer C_{box}, the capacitance of the silicon layer between buried oxide layer and empty space layer C_{gap}, the capacitance of the empty space layer C_{es} and the capacitance of the substrate C_{sub}. The introduction of C_{es} and C_{gap} in SON structure leads to a lower C_{dsub}, compared to the conventional SOI structure. C_{dsub} together with the drain-substrate resistance provides an AC signal path to the substrate, which leads to a loss of the signal at the drain terminal. C_{dsub} is also a major component of C_{oss}, which needs to be reduced to minimum.

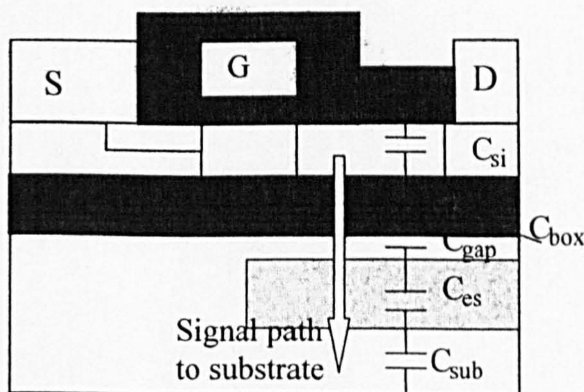


Figure 6.6 Capacitance components of C_{dsub} in SON sandwich structure with the signal path to substrate illustrated.

6.5. Simulation Results

Simulations have been carried out for both SON and conventional SOI LDMOSFET. The devices investigated are targeted at mobile phone handset applications operating with a battery supply of 12.5V. To make a fair comparison, both SON and SOI devices are optimised for the desired BV of 40V. The SOI LDMOSFET considered has a top silicon thickness of 0.2μm and buried oxide layer of 0.4μm, based on SIMOX technology. The same top silicon thickness and buried oxide thickness are used in the SON structures. The other parameters, the thickness of the empty space layer, the length of the empty space layer and the doping of drift region and substrate are varied in the study. Both the conventional SOI and partial SOI structures are investigated. In a later section, the comparison of the electrical and thermal performance is also given for SON and SOI devices for 28V applications.

6.5.1 Electrical performance of SON RF LDMOSFET

6.5.1.1 BV Characteristics of SON RF LDMOSFET

Figure 6.7 shows the BV versus the drift dose with the empty space layer thickness as a parameter for a SON RF LDMOSFET. The BV characteristics of a SOI structure is also shown in the figure. Both devices have the drift doping of $7e16/cm^3$. As can be seen, the SON sandwich structure has nearly the same BV as that of the SOI structure. Due to the very low electric field in the empty space layer, it has nearly no influence on the breakdown voltage and the optimum drift dose.

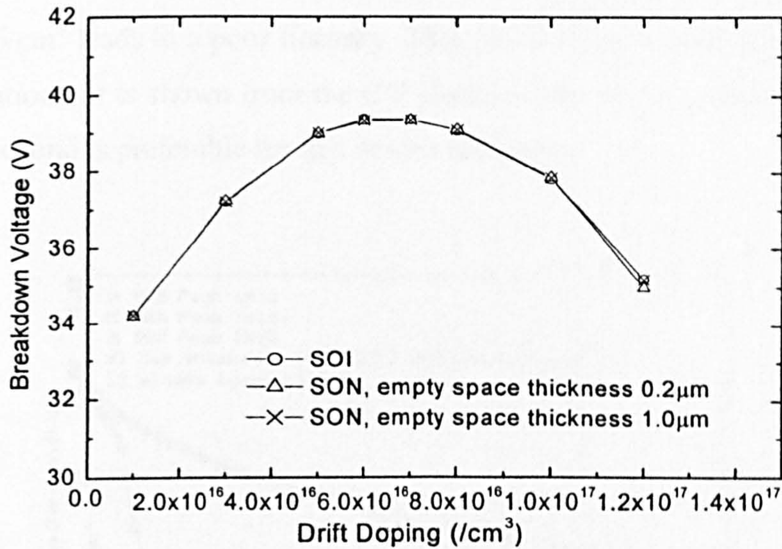


Figure 6.7 Breakdown voltage versus drift doping concentration for SOI and SON with empty space thickness of 0.2μm and 1.0μm.

6.5.1.2 Influence of substrate doping on CV characteristics

To investigate the influence of the substrate doping level on CV characteristics of the SON structure, the substrate doping level is varied from 1e15/cm^3, 1e16/cm^3 to 5e18/cm^3. The thickness of the silicon gap layer is kept constant at 0.07μm for both devices. The C_{oss} versus drain voltage for these devices is shown in Figure 6.8. At zero bias, the device with a substrate doping of 1e15/cm^3 has the lowest C_{oss} of 2.5e-16F/μm while for a doping level of 5e18/cm^3, C_{oss} is much higher, at 3.8e-16F/μm. For a doping level of 1e16/cm^3, the C_{oss} is the same as that of 5e18/cm^3 at zero bias. However, with an increase of the drain voltage to 1.5V, it decreases sharply to a level similar to doping level of 1e15/cm^3.

The various capacitance characteristics can be explained by the change of depletion region with the drain voltage under various substrate doping. Figure 6.9 (a) and (b) show the depletion region in the case of substrate doping 1e16/cm^3 at drain biases of 0V and 1.5V, respectively. At zero bias, the depletion layer depth under the buried oxide layer is very small, which leads to a high C_{OSS}. While it extends to the empty space layer at drain voltage 1.5V. This brings the empty space capacitance in series with that of the buried oxide and top silicon layer, which leads to a sharp decrease of C_{oss} with the drain voltage. In the device with the substrate doping 1e15/cm^3, the depletion under the buried oxide layer extends to the empty space layer at drain voltage as low as 0V, due to the low substrate doping. While in the device with substrate doping 5e18/cm^3, the depletion layer is too thin to contact with the empty space

layer even at high drain voltage. The dramatic variation of C_{oss} with drain voltage in the case of substrate 1e16/cm^3 leads to a poor linearity. This needs to be avoided in device design for amplifier applications. It is shown from the CV characteristics that a substrate doping as low as 1e15/cm^3 or beyond is preferable for this device structure.

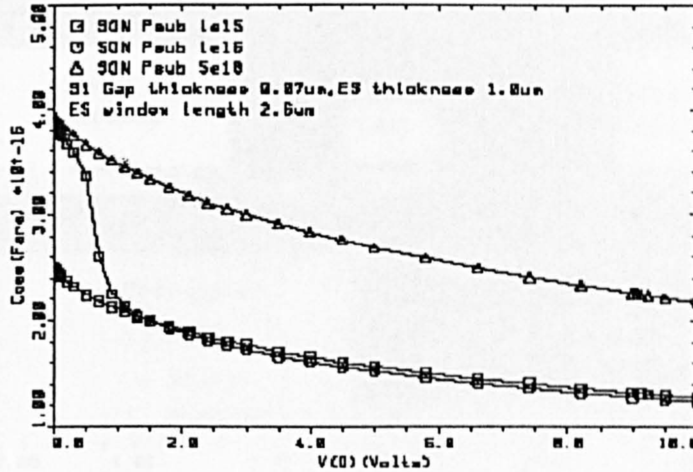


Figure 6.8 C_{oss} versus drain voltage of SON structure with various substrate doping.

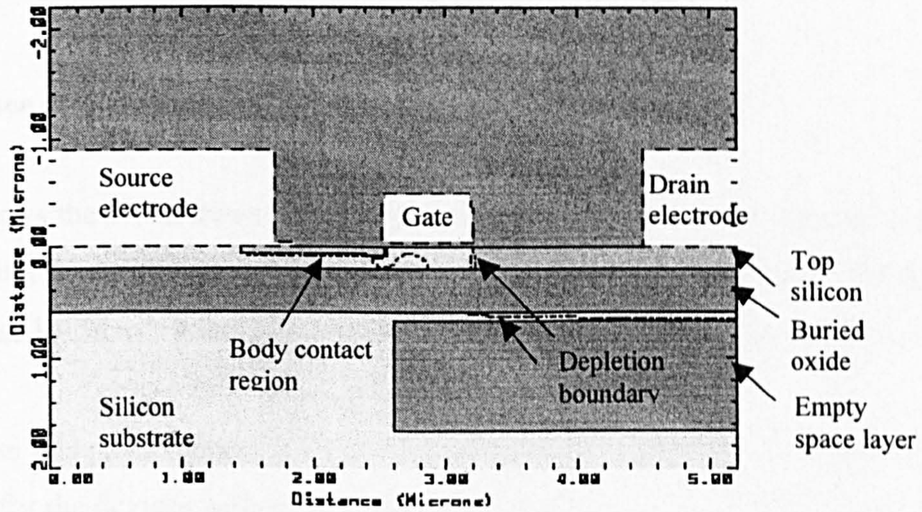


Figure 6.9 (a)

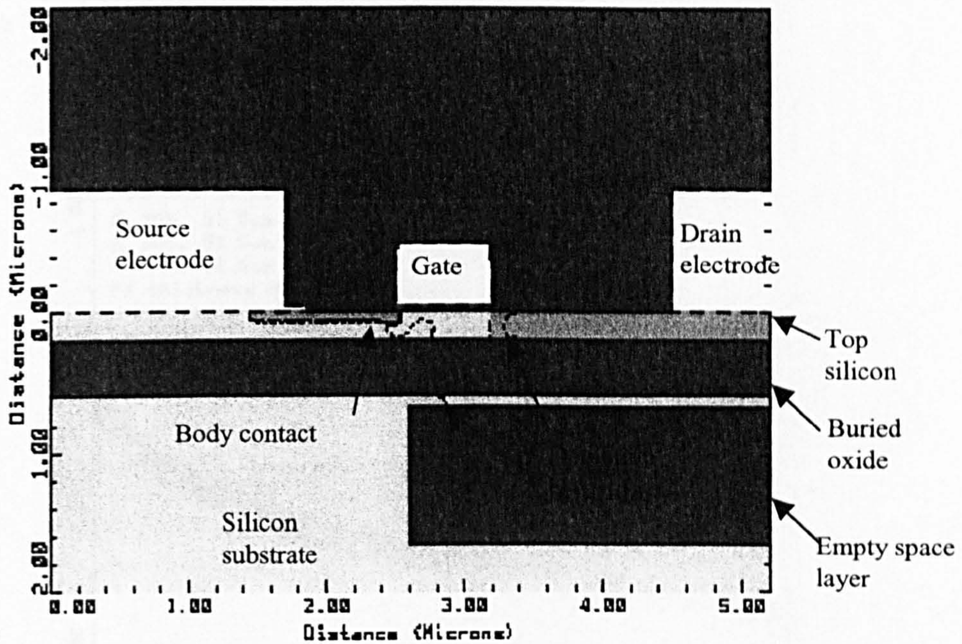


Figure 6.9 (b)

Figure 6.9 2D device structures with depletion region illustrated at (a) V_d=0V (b) V_d=1.5V for the device with substrate doping 1e16/cm^3.

6.5.1.3 Influence of the silicon gap thickness on CV characteristics

Figure 6.10 shows the CV characteristics of the sandwich SON structure with the silicon gap thickness varying from 0.07μm to 0.3μm. The substrate doping level in the three devices is kept the same at 1e15/cm^3. It can be seen that C_{oss} decreases with the increase of silicon gap thickness.

To analyse this phenomenon, the 2D device structures with depletion region are shown in Figure 6.11 for the devices with silicon gap 0.07μm and 0.3μm. Both devices are biased at gate voltage of 0V and drain voltage of 0V. When the depleted silicon gap layer is in contact with the empty space layer, the C_{dsub} is composed by the capacitance of the empty space layer in series with the capacitance of the buried oxide and the top silicon layer. Conversely, when the depleted silicon gap layer does not contact with the empty space layer, the capacitance of the empty space layer does not contribute to the C_{dsub}, leading to a higher C_{dsub}. As a result, it is desirable that longer depletion region in the silicon gap layer is in contact with the empty

space layer. In the device with 0.07μm thick silicon gap, about 2.25μm long depletion region contacts with the empty space layer. While in the device with 0.3μm thick silicon gap, the contact region is only about 1.82μm long. As a result, the device with 0.07μm silicon gap has the lowest C_{dsub} and thus lowest C_{oss}.

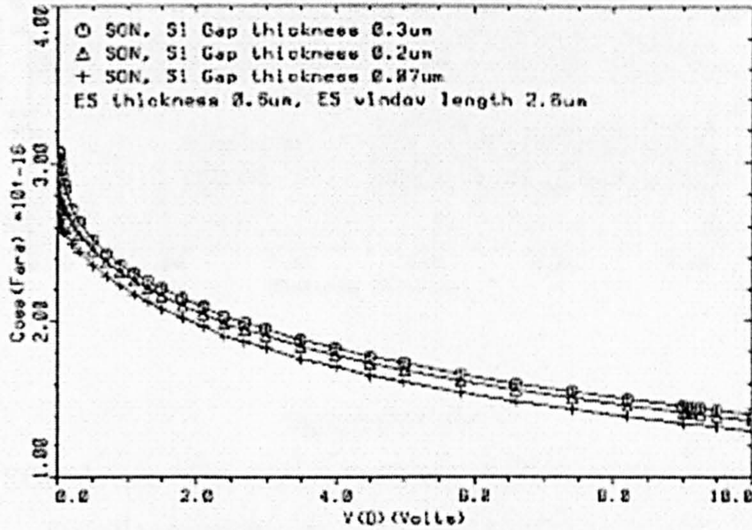


Figure 6.10 C_{oss} versus drain voltage for SON device with Si gap thickness of 0.07μm, 0.2μm and 0.3μm.

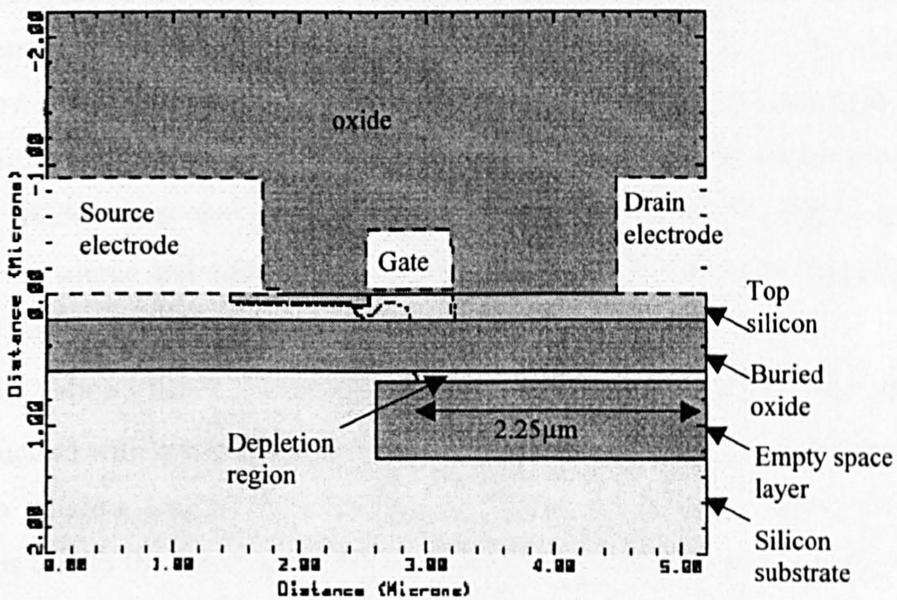


Figure 6.11 (a)

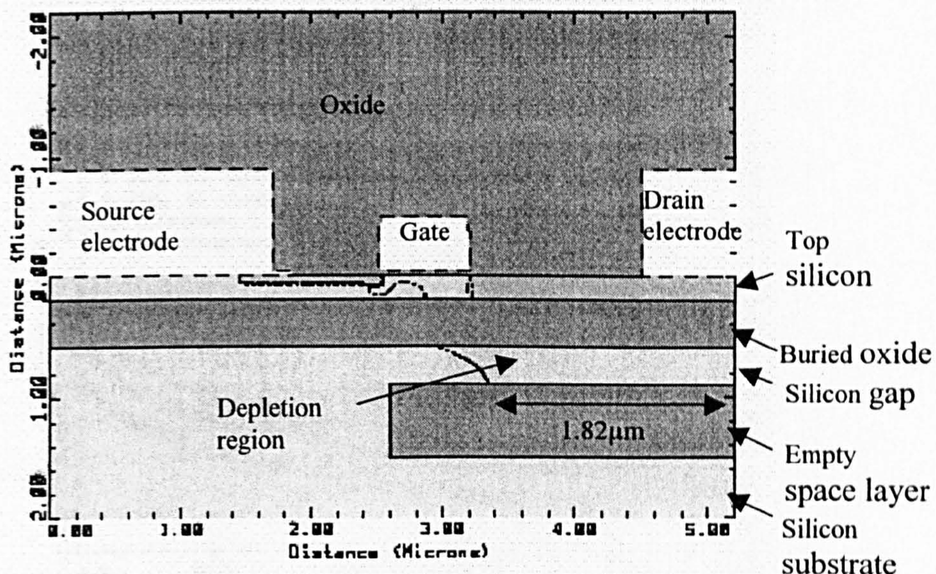


Figure 6.11 (b)

Figure 6.11 2-D SON device cross-sections with the depletion region illustrated at zero bias for silicon gap thickness (a) 0.07μm and (b) 0.3μm.

6.5.1.4 Influence of window length of the empty space on CV Characteristics

It is preferable to reduce the length of the empty space layer to a minimum, in order to improve the thermal conducting in the device. The structure with part of the empty space layer replaced by silicon is referred as partial SON structure. The window length is varied from 0μm to 4.3μm, in order to investigate its influence on device electrical performance. The device with the window size of 0 μm corresponds to a structure with the empty space layer extending from the source and drain. Whereas, for a device with a window length of 4.3μm, the empty space layer only lies under the drain region.

Figure 6.12 shows the C_{oss} versus drain voltage for structures with various window lengths. The structure with a window length of 2.6μm has the same CV characteristics as the structure with a window length of 0μm. With a further increase in window length, C_{oss} increases. This is due to the lower capacitance of the empty space layer compared to that of the silicon layer. Figure 6.13 shows the depletion region in a partial SON structure. In the region where part of the empty space layer is replaced by silicon, the empty space layer does not contribute to C_{dsub}, leading to an increased C_{oss}. Since the depletion region in the silicon

gap layer does not extend beyond 2.6μm, further reduction of the window length does not influence the C_{dsub}. With the window length of 2.6μm, the C_{oss} reaches a minimum.

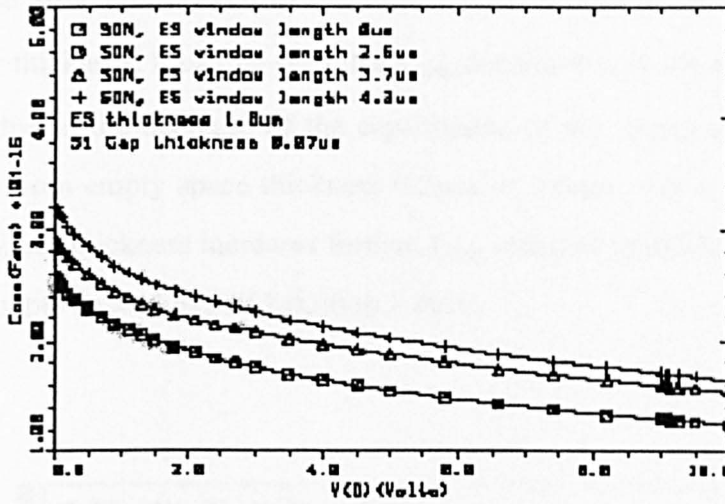


Figure 6.12 CV characteristics for the devices with various empty space window length 0μm, 2.6μm, 3.7μm and 4.3μm.

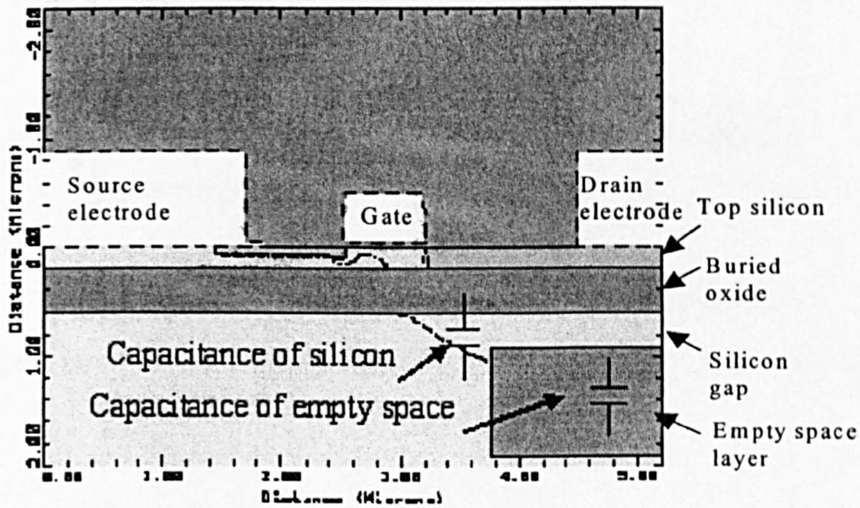


Figure 6.13 2-D SON LDMOSFET cross-section with the depletion region at zero bias illustrated with the window length of 3.7μm.

6.5.1.5 Influence of the empty space thickness on CV characteristics

Figure 6.14 shows the C_{oss} versus drain voltage with the empty space thickness as a parameter for SON sandwich structure. Shown in the Figure 6.15 is the C_{oss} at zero bias versus the empty space layer thickness. It can be seen that C_{oss} decreases with the increase of the empty space thickness, due to the decrease of the capacitance of the empty space layer. The C_{oss} decreases sharply from empty space thickness 0.2μm to 0.6μm, with a reduction of 8.59%. When the empty space thickness increases further, C_{oss} changes gradually, with a reduction of 1.16% from the empty space layer of 1.0μm to 1.4μm.

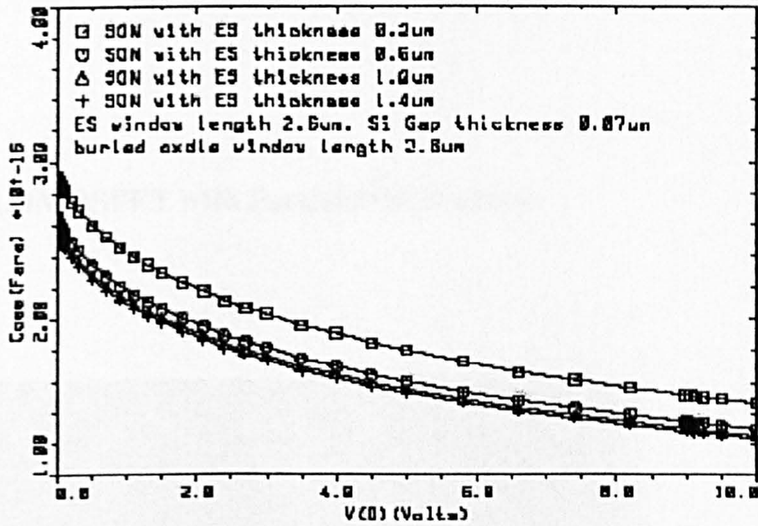


Figure 6.14 CV characteristics of SON RF LDMOSFET's with the empty space layer thickness of 0.2μm, 0.6μm, 1.0μm and 1.4μm.

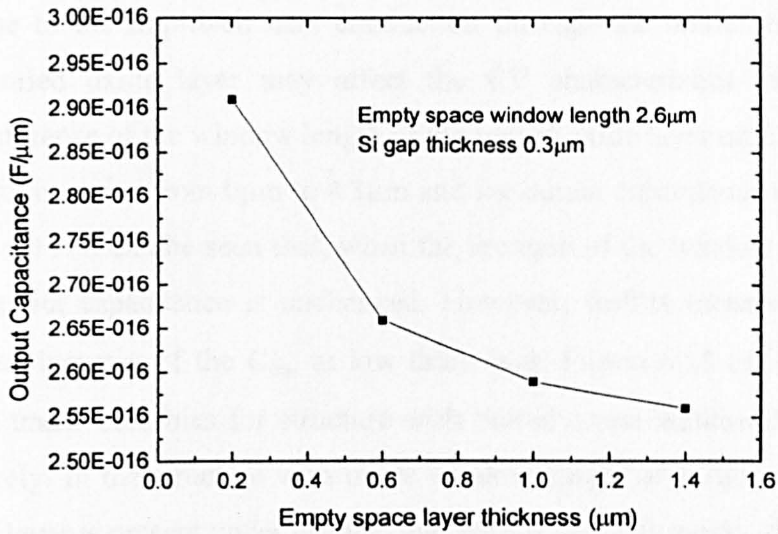


Figure 6.15 Output capacitance versus empty space thickness.

6.5.2. SON RF LDMOSFET with Partial SOI structure

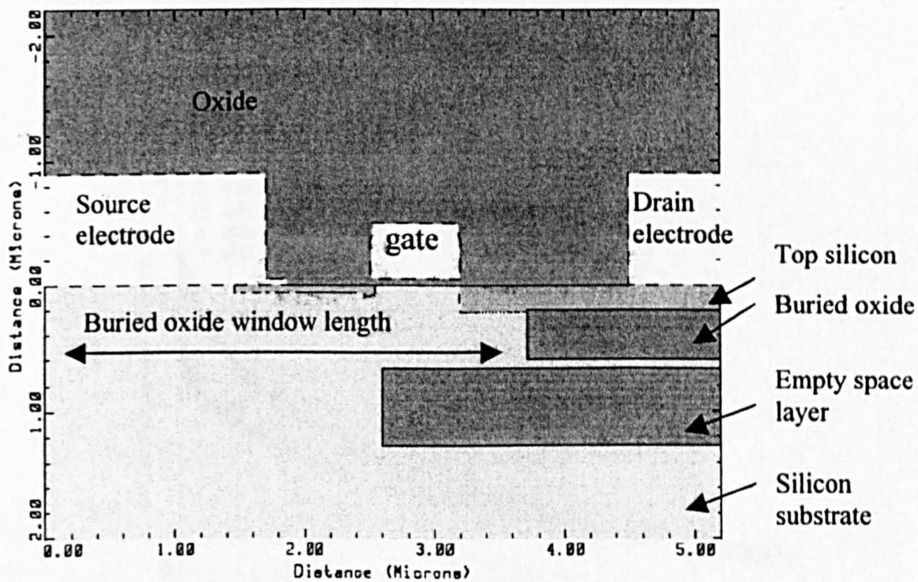


Figure 6.16 Device structure with partial SOI and partial empty space layer.

The presence of the buried oxide of low thermal conductivity limits heat conduction in the device. Partly removing the buried oxide under the source region is a way of improving self-heating. A SON structure with partly removed buried oxide layer, partial SOI layer, as shown

in Figure 6.16, is of interest. For a better thermal performance, a longer buried oxide window is preferable, due to the improved heat conduction through the oxide window. However, removing the buried oxide layer may affect the CV characteristics of the device. To investigate the influence of the window length of the buried oxide layer on CV characteristics, the window length is varied from 0μm to 4.3μm and the output capacitance characteristics are shown in Figure 6.17. It can be seen that, when the increase of the window length from 0μm to 2.6μm, the output capacitance is unchanged. However, further increase of the window length leads to an increase of the C_{oss} at low drain bias. Figure 6.18 (a) and (b) show the depletion region under zero bias for structure with buried oxide window length 2.6μm and 3.7μm, respectively. In the structure with oxide window length of 3.7μm, silicon instead of the buried oxide layer is present under channel and part of the drift region, different from that in the structure with oxide window length of 2.6μm. In this region, the capacitance of silicon instead of the capacitance of the buried oxide layer contributes to the C_{dsub}. Due to the higher dielectric constant of silicon compared to the buried oxide, the silicon layer has higher capacitance. Therefore, the structure with oxide window length of 3.7μm has a higher C_{oss}. When the oxide window length is reduced beyond 2.6μm, the depletion region in the device is unchanged, resulting in an unchanged C_{oss}. For a lower C_{oss}, the SON with partial SOI structure with a buried oxide window length of 2.6μm is a good option.

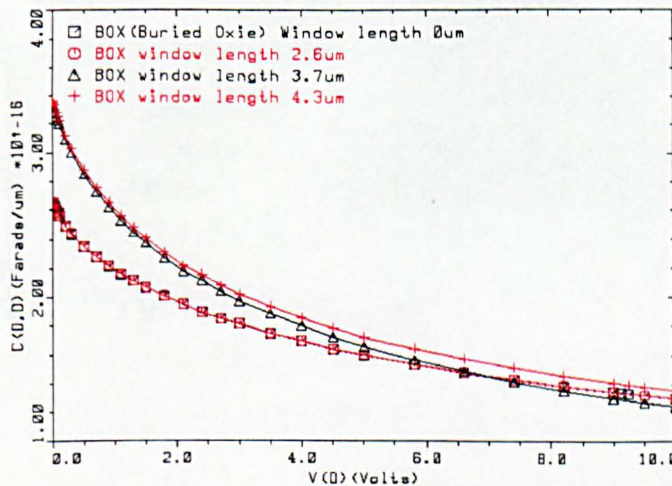
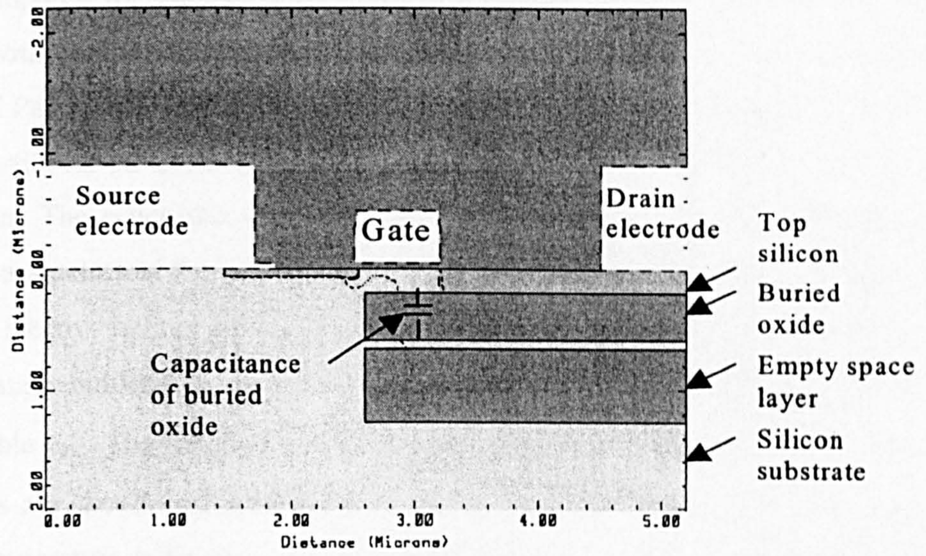
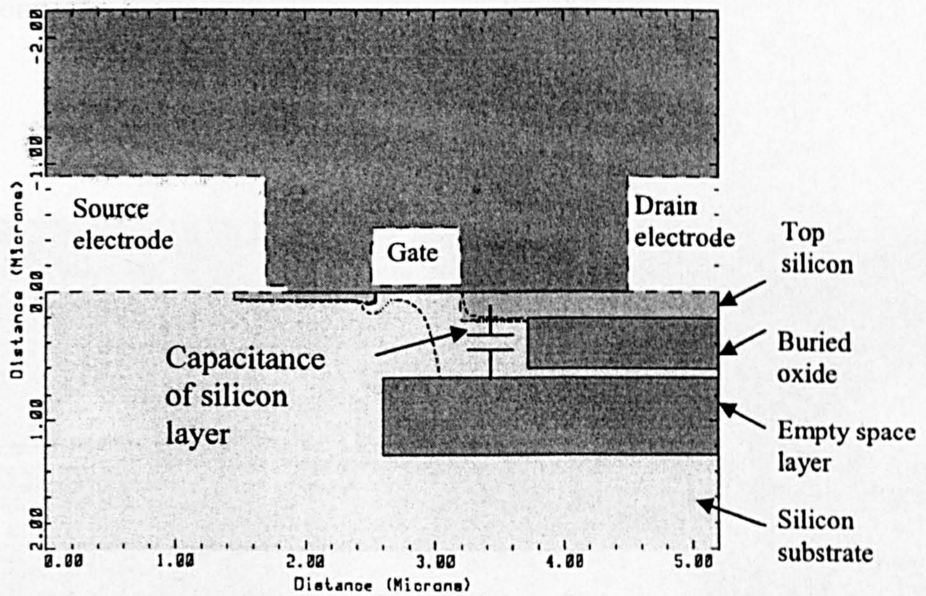


Figure 6.17 output capacitance of structures with buried oxide window length of 0μm, 2.6μm, 3.7μm and 4.3μm, respectively.



(a)



(b)

Figure 6.18 (a) Device structure with depletion region for structure with buried oxide window length 2.6μm.
(b) device structure with depletion region for structure with buried oxide window length 3.7μm.

6.5.3 Self-heating in SON RF LDMOSFET

Self-heating is compared for various SON device structures, the Full SOI Full ES (Empty Space) structure, with the buried oxide layer and empty space layer extending from source to drain, the Full SOI Partial ES structure with part of the empty space layer replaced by silicon, and Partial SOI Partial ES structure with part of the buried oxide layer and empty space layer replaced by silicon. The schematic cross-sections of these device structures are shown in Figure 6.19. The parameters of the devices in the study are listed in Table 6.1. Self-heating is investigated using electro-thermal simulation. The same boundary conditions as in Chapter 3 are used. The thermal conductivity, specific heat and density of air used in the simulations are summarized in Table 6.2. The temperature distribution at the same bias of V_g=3V, V_d=7.5V for these structures are shown in Figure 6.20. It can be seen that Full SOI Full ES structure has the highest temperature with the peak temperature located at the channel drift junction. The other two structures have much lower temperature rise, which demonstrates the influence of the empty space layer. Partial SOI Partial ES structure has the lowest temperature, thanks to the partial removal of the buried oxide layer, which improves the heat conduction from the device active region to the bottom.

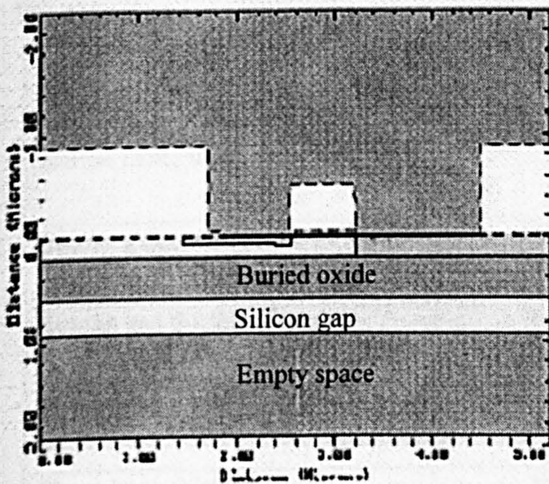


Figure 6.19 (a)

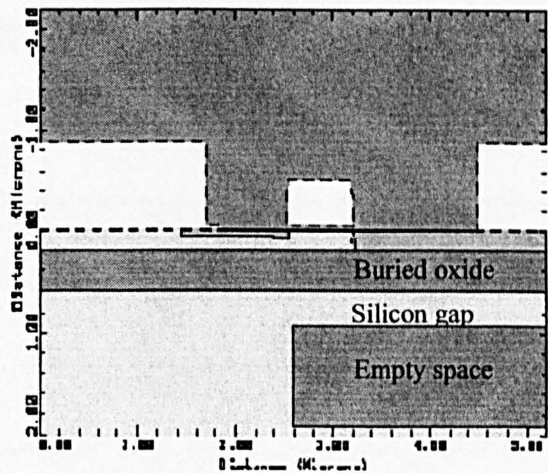


Figure 6.19 (b)

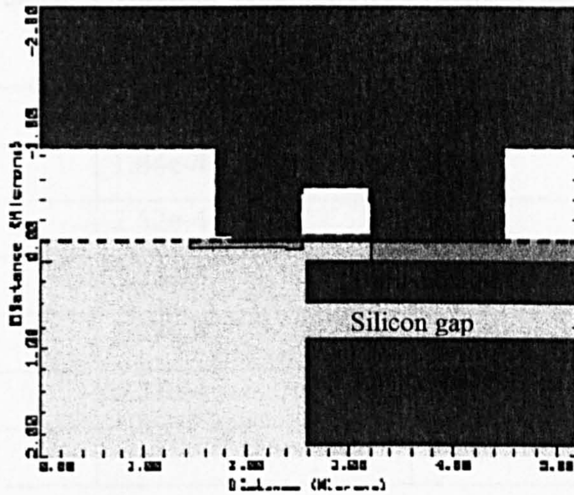


Figure 6.19 (c)

Figure 6.19 Schematic cross sections of (a) Full SOI Full ES structure, (b) Full SOI Partial ES structure (c) Partial SOI Partial ES structure.

Table 6.1 device parameters for Full SOI Full ES, Full SOI Partial ES, Partial SOI Partial ES structures.

	Full SOI Full ES structure	Full SOI Partial ES structure	Partial SOI Partial ES structure
Buried oxide window length (μm)	0	0	2.6
Empty space window length (μm)	0	2.6	2.6
Silicon gap thickness (μm)	0.3	0.3	0.3
Silicon gap doping (/cm^3)	1e15	1e15	1e15
Top silicon thickness	0.2	0.2	0.2
Buried oxide thickness (μm)	0.4	0.4	0.4

Table 6.2 Properties of air used in the electro-thermal simulation [14].

Temperature (K)	Thermal conductivity (W/cmK)	Specific heat (J/gK)	Density (g/cm^3)
100	9.4e-5	5.759	-
200	1.84e-4	6.463	-
300	2.62e-4	6.871	1.161
400	3.33e-4	-	-
500	3.97e-4	7.389	-
600	4.57e-4	-	-
1000	-	8.138	-

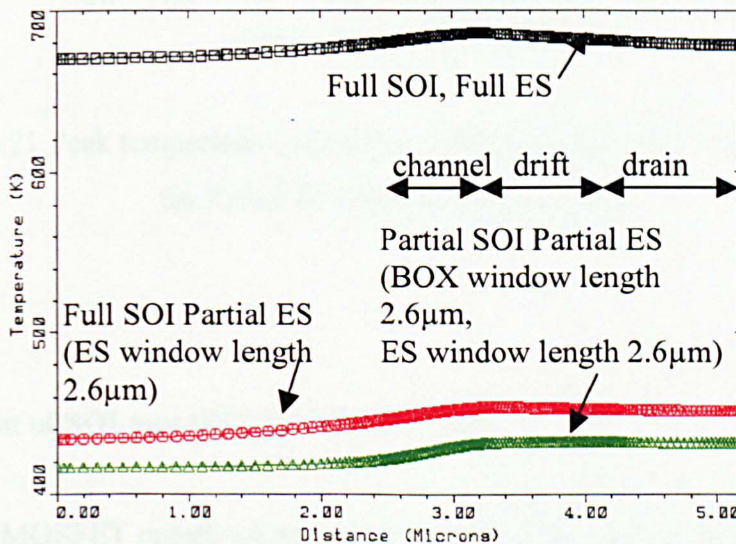


Figure 6.20 Temperature distributions for Full SOI Full ES structure, Full SOI Partial ES structure, Partial SOI Partial ES structure.

The influence of the thickness of the empty space layer on self-heating is investigated based on the Partial SOI Partial ES structure. The peak temperature rises in the devices with the empty space layer thickness varied from 0.2μm to 1.4μm are shown in Figure 6.21. It can be seen that the temperature rise is nearly unchanged for various empty space layer thicknesses. Due to the very low thermal conductivity of the empty space layer, nearly no heat flows through the empty space layer under the drift region to the bottom. Therefore, an

increase in the empty space layer thickness has nearly no influence on the temperature rise. It is an advantage when using a thick empty space layer for the benefit of lower C_{dsub} and C_{oss}.

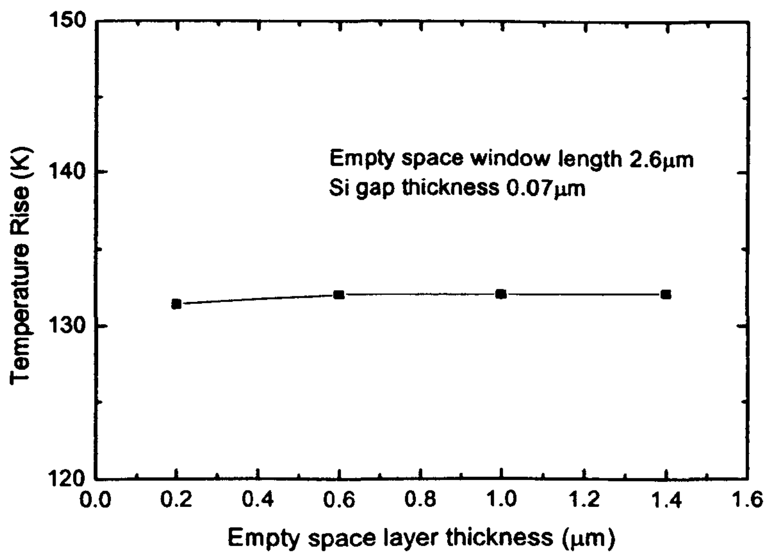


Figure 6.21 Peak temperature rise under various empty space layer thickness for Partial SOI Partial ES structure.

6.5.4 Comparison of SOI and SON RF LDMOSFET

The SON RF LDMOSFET optimised with a BV of 40V is compared with a conventional SOI alternative. Partial SOI Partial ES structure is adopted for SON LDMOSFET. The window length of the buried oxide layer and empty space layer are both 2.6μm. For a fair comparison, a partial SOI device is used with the buried oxide window length of 2.6μm. A summary of the device parameters of the two devices is shown in Table 6.3.

Table 6.3 device parameters for both SOI and SON RF LDMOSFET with BV 40V.

	SOI	SON
Top silicon thickness	0.2μm	0.2μm
Buried oxide thickness	0.4μm	0.4μm
Buried oxide length	2.6μm	2.6μm
Empty space thickness	—	1.0μm
Empty space length	—	2.6μm
Channel length	0.7μm	0.7μm
Gate oxide thickness	40nm	40nm
Drift region length	1.0μm	1.0μm
Drift region doping	7e16/cm^3	7e16/cm^3

Figure 6.22 shows the IV characteristics for both SON and SOI devices. SON and SOI RF LDMOSFET have nearly the same IV and g_m characteristics due to the same device parameters for drift, source and drain design. Figure 6.23 shows the drain substrate capacitance, C_{dsub}, versus the drain voltage for both devices. The SOI device has a C_{dsub} of 1.05e-18 F/μm at zero bias, while SON device has a C_{dsub} of 2.4e-19 F/μm, which is only 22.8% of that of SOI. The lower C_{dsub} of SON leads to a lower C_{oss} of 2.6e-16 F/μm, corresponding to a reduction of 28% compared to that SOI device. The drain substrate loss can be referred from the drain substrate conductance G_{ds}, the lower the G_{ds} the lower the substrate loss. As shown in Figure 6.24, SON has a drain substrate conductance of 1.7e-17S/μm at zero bias, only 2.8% compared to 6e-16S/μm for SOI device. This indicates that SON device has a much lower substrate loss compared to the SOI alternative, due to the lower C_{dsub} in SON device. This is an advantage of SON device in RF applications.

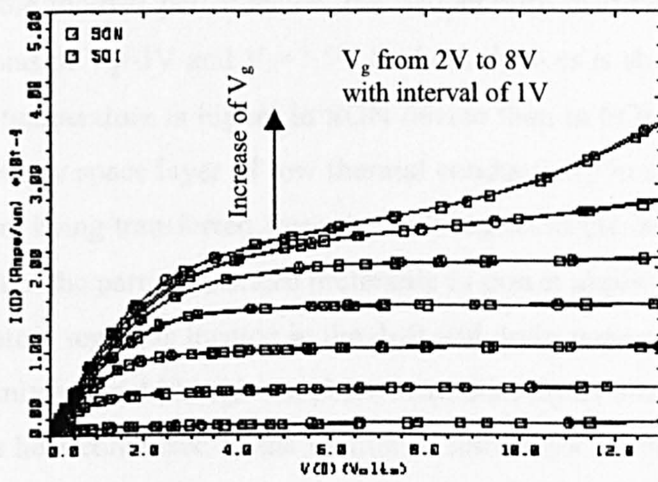


Figure 6.22 IV characteristics for both SON and SOI devices with BV of 40V.

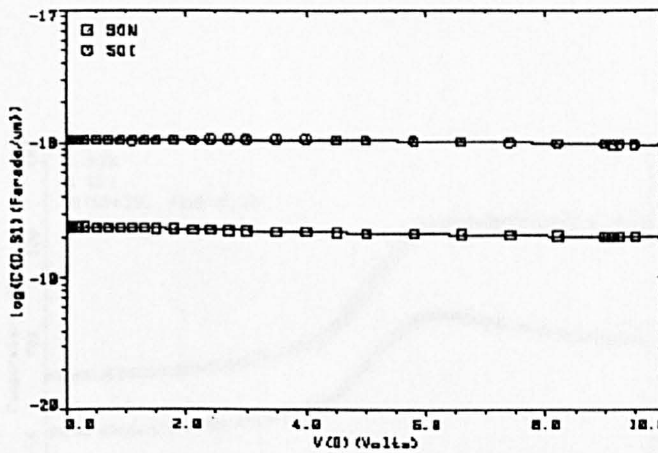


Figure 6.23 Drain substrate capacitance for both SON and SOI devices with BV 40V.

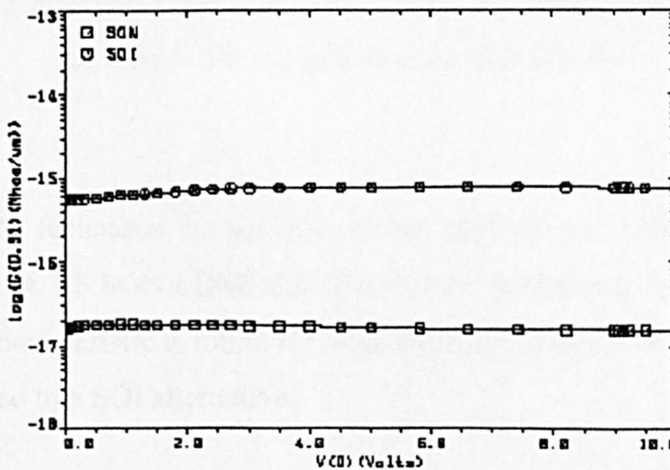


Figure 6.24 Drain substrate conductance for both SON and SOI device with BV 40V.

To compare the thermal performance, the temperature distribution along the silicon surface at the same bias of V_g=3V and V_d=7.5V for both devices is shown in Figure 6.25. It can be seen that the temperature is higher in SON device than in SOI device. This is due to the presence of the empty space layer of low thermal conductivity in the SON device, which prevents the heat from being transferred from the drift region to the bottom. The poorer heat conduction of air makes the partial structure preferable in power applications. It is also shown that the high temperature region is located in the drift and drain region in both devices. Since heat is generated mainly in the drift region and the insulation layers are present under the drift and drain region, the heat conducted to the bottom of the device is limited in these regions. The removal of the insulation layers under source and channel region improves the heat conduction through these regions to the bottom of the device, which leads to a much lower temperature rise in these regions.

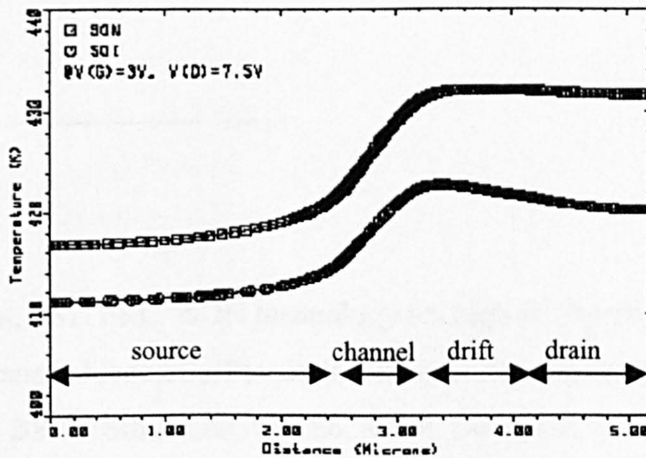


Figure 6.25 Temperature rise at V_g=3V, V_d=7.5V along the silicon surface for both SON and SOI devices with BV 40V.

The sandwich SON technique is suitable to be applied for applications with various breakdown voltages. A RF SON LDMOSFET with 80V breakdown voltage is investigated in this work. Similar characteristic is found for SON structure in terms of reduced drain substrate capacitance compared to a SOI alternative.

6.6 Summary

A novel sandwich structure for lateral RF MOSFETs has been investigated based on Silicon-On-Nothing (SON) technology. The influence of device parameters on BV, CV and thermal performance has been investigated. The silicon gap thickness and silicon gap doping level are crucial to the sandwich SON structure. A Partial SOI Partial ES structure is found preferable in terms of self-heating compared to the Full SOI and Full ES alternative. With a BV of 40V, the thermal and electrical performance of SON LDMOSFET and SOI alternative are compared. SON structure shows an improvement in output capacitance and substrate loss, therefore a higher power gain. However, the temperature rise in SON device is higher compared to that in the SOI alternative. The performance of the proposed sandwich SON structure in base station applications, requiring the breakdown voltage of 80V, has also been investigated. The SON sandwich structure in base station applications also shows advantage in output capacitance and substrate loss compared to SOI alternative.

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Chapter 7 Conclusions and Future Work

7.1 Conclusion

This work aims to provide a study on the devices and technologies development of RF LDMOS in SOI technologies for base station and mobile handset applications.

The main achievements are summarised as the following,

- RESURF mechanism on SOI structure has been analyzed together with the breakdown characteristics. The influence of buried oxide thickness on the optimum drift dose is analysed and presented. A thinner buried oxide leads to a higher optimum drift dose, which can be exploited in SOI device design. As for ideal RESURF, a linear drift doping is required in an SOI structure. However, it is found that this drift doping distribution is not effective for RF applications, due to the presence of the source shield, which changes the potential distribution in the drift region.
- CV characteristics of RF LDMOS on a SOI substrate has been analysed in detail by analysing the capacitor components in a SOI structure. It clarifies the influence of device geometrical and physical parameters on device CV characteristics.
- A back-etch RF LDMOS with superior thermal performance has been investigated together with the fabrication process, based on the analysis and understanding of self-heating. This structure shows significantly improved self-heating even compared to a bulk structure.
- Quasi-saturation in SOI LDMOS has been analysed in detail. The relationship between quasi-saturation current and device geometrical and physical parameters has been discussed. The difference in quasi-saturation current in thin and thick film SOI has been analysed. Higher potential drop in the drift region near channel in thick film SOI, caused by current spread and carrier velocity saturation is found to be the reason. The influence of RESURF on quasi-saturation is also presented. By choosing the device geometric parameters, desired device performance with high quasi-saturation current can be obtained.
- A conventional UD device on SIMOX technology is found with a maximum BV limited below 80V and the presence of kink in the IV curves. RF LDMOS on a SIMOX substrate with step-drift doping profile has been evaluated. The results show that this step drift structure is suitable for 28V applications, with an improved breakdown voltage, suppressed kink effect and postponed on-state breakdown compared to the conventional Uniformly Doped (UD) devices. Physical analysis is given to the characteristics of breakdown, kink effect and on-state breakdown.

- For the first time, a SON sandwich structure is investigated for high voltage, RF applications. The theoretical analysis and numerical simulation are presented. This structure overcomes the BV limitation by the low electrical strength of air. In comparison with the conventional SOI structure, it demonstrates lower out-put capacitance C_{oss} and drain substrate capacitance C_{ds}. These advantages suggest that a lower substrate loss, higher output power, higher power gain, and power added efficiency can be achieved.

7.2 Future work

This work has provided a physical analysis through numerical simulation of the LDMOS on SOI and SON technology. Further experiment is desired to verify the theoretical analysis and simulation results.

In this work, investigation on RF LDMOS with BV of 40V and 80V has been carried out. The device with BV of 40V is targeted at land mobile applications with 12.5V supply voltage. To minimise the power dissipation and extend the talk time, the supply voltage of mobile handset for common custom keeps decreasing. Currently, the supplying voltage is about 3.5V and the research on RF MOSFET device down to 1V has been carried out. The continuous decreasing of supplying voltage creates a huge market for low voltage power MOS for RF applications. While the supplying voltage decreases, the challenge is to maintain the high power added efficiency. The SON structure, which has shown to be superior for high power gain for 12.5V and 28V applications, thanks to the low dielectric constant of empty space layer, is also expected to show its merit on low voltage RF applications. Low voltage SON MOSFET was fabricated recently by Tsutomu Sato et. al. from Toshiba. The device shows a reduction on junction capacitance. Further investigation on low voltage SON MOSFET for RF applications can be carried out in the future.

Device package plays an important role in the self-heating effect. The device package introduces a significant percentage of thermal resistance on the heat conduction path from the device to outside environment. Device package is critical to achieve the maximum performance from RF power transistors. Conventionally, ceramic packages are used for RF transistors to handle heat and related thermal issues. Meanwhile, Motorola has developed a low cost plastic package for RF power devices. In the future work, the influence of the properties of different types of packages should be investigated to predict the device performance in practice. 3D thermal simulation can be carried out in the future using tools with 3D thermal simulation capacity such as SILVACO.

Appendix A

List of symbols

E	electric field
J	current density
V	voltage
T	temperature
V_d	drain voltage
I_d	drain current
V_g	gate voltage
V_{bi}	built-in potential
ε_o	permittivity in vacuum
q	magnitude of electronic charge
K	Boltzmann constant
μ_n	electron mobility
v	carrier drift velocity
V_T	threshold voltage
ε_{si}	silicon dielectric constant
ε_{ox}	silicon dioxide dielectric constant
v_{sat}	carrier saturation velocity in silicon
g_m	transonductance
E_m	maximum electric field for silicon
E_c	critical electric field for carrier velocity saturation in silicon
E_g	bandgap of silicon
R_{th}	thermal resistance
c	specific heat
λ	thermal conductivity
m	mass density
ρ	resistivity
C_i	unit area gate capacitance
P_{out}	output power
P_{in}	input power
P_d	power dissipation
f_t	cut-off frequency
f_m	maximum frequency

L_g	gate length
W_g	gate width
L_d	drift length
C_{iss}	in-put capacitance
C_{oss}	out-put capacitance
C_{rss}	feedback capacitance
C_{ds}	drain source capacitance
C_{gs}	gate source capacitance
C_{ds}	drain source capacitance
C_{gd}	gate-drain capacitance
C_{box}	buried oxide capacitance
C_{dsub}	drain substrate capacitance
I_{qsat}	quasi-saturation current
G_{dsub}	drain substrate conductance
V_B	breakdown voltage
W_{dep}	depletion region width
T_{si}	thickness of top silicon layer
T_{box}	thickness of buried oxide layer
t_{gox}	gate oxide thickness
E_{si}	electric field in silicon
E_{ox}	electric field in oxide
E_x	lateral electric field
E_y	vertical electric field
N_{drift}	doping concentration in the drift region
N_{sub}	substrate doping concentration
R_{drift}	resistance of drift region
R_{ch}	resistance of MOS channel region
R_{sinker}	resistance of P^+ sinker region
R_S	resistance of source region
R_D	resistance of drain region
R_{sub}	resistance of substrate
R_{SC}	resistance of front source contact
V_{mos}	potential at the channel drift end
g_{mj}	transconductance of JFET
ω	angular frequency
R_G	gate resistance

R_L load resistance

A_v voltage gain of an amplifier

Appendix B

List of abbreviation

BJT	Bipolar Junction Transistor
BPSG	Borophosphosilicate Glass
BV	breakdown voltage
CMOS	Complimentary Metal Oxide Silicon
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapour Deposition
DI	Dielectric Isolation
ECR	Electron Cyclotron Resonance
ES	Empty Space
IC	Integrated Circuit
JI	Junction Isolation
LDMOSFET	Laterally Double Diffused Metal Oxide Semiconductor Field Effect Transistor
LPCVD	Low Pressure Chemical Vapour Deposition
MESFET	MEtal-Semiconductor-Field-Effect-Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTF	Mean Time to Failure
PAE	Power Added Efficiency
RESURF	REduced SURface Field Effect
RF	Radio Frequency
RIE	Reactive Ion Etching
PSG	Phosphosilicate Glass
RTA	Rapid Thermal Annealing
SEH	SElf-Heating
SIMOX	Separation by Implantation of Oxygen
SOI	Silion On Insulator
SON	Silicon On Nothing
SOA	Safe Operation Area
2-D	Two Dimensional
UD	Uniformly Doped
VDMOSFET	Vertically Double Diffused Metal Oxide Semiconductor Field Effect Transistor
UHF	Ultra High Frequency
VHF	Very High Frequency

Appendix C

1. Source file of uniform drift device for process simulation using TSUPREM4.

```
$$$$ source file of
line x locat=0 spacing=0.6 tag=left

$ source,
line x locat=2 spacing=0.2

$ channel, 3-3.8um
line x locat=3.0  spacing=.01
line x locat=3.4  spacing=.06
line x locat=3.75 spacing=.01

$ drift, 3.8+3.5=7.3
line x locat=4.9   spacing=.05
line x locat=6.1   spacing=.05
line x locat=6.8   spacing=.05

$ drain, 7.3+1.2um=8.5
line x locat=7.3   spacing=.1
line x locat=8     spacing=.3
line x locat=8.5   spacing=.2 tag=right


line y location=0.6 spacing=0.03 tag=epi
line y location=5   spacing=0.5
line y location=15  spacing=10
line y location=100 spacing=20
line y location=200 spacing=30 tag=sub


elimin columns  x.min=2              y.min=0.5
elimin columns  x.min=2.5 x.max=4    y.min=4
elimin columns  x.min=2.8 x.max=3.2  y.min=6
elimin columns  x.min=3.6 x.max=4.2  y.min=6


region silicon xlo=left xhi=right ylo=epi yhi=sub

$$$$ p+ substrate, Boron doped, 1e15/cm-3
initial <100> boron=1e15


$$$$ top silicon 0.2u, buried oxide 0.4u.

deposit oxide   thick=.04  spaces=2
deposit oxide   thick=.16  spaces=4 dy=0.02 ydy=0.04
deposit oxide   thick=.16  spaces=4 dy=0.02 ydy=0.36
deposit oxide   thick=.04  spaces=2


deposi silicon boron=1e15 thick=.05 spaces=3 dy=.01 ydy=.01
deposi silicon boron=1e15 thick=.1  spaces=5 dy=.02 ydy=.02
deposi silicon boron=1e15 thick=.05 spaces=3 dy=.01


$**************  gate_oxide, 60 nm********

diff temp=900 time=20 f.n2=9.5 f.o2=.5   f.h2=0   f.hcl=0
diff temp=900 time=20 f.n2=5.5 f.o2=.5   f.h2=0   f.hcl=0
diff temp=900 time=16 f.n2=0   f.o2=3.3 f.h2=1.3 f.hcl=0
```

```
diff temp=900 time=16 f.n2=0   f.o2=3.3 f.h2=1.3 f.hcl=0.165
diff temp=900 time=12 f.n2=0   f.o2=3.3 f.h2=6   f.hcl=0.165
diff temp=900 time=9  f.n2=0   f.o2=3.3 f.h2=0   f.hcl=0
diff temp=900 time=10 f.n2=5   f.o2=0   f.h2=0   f.hcl=0
diff temp=900 time=20 f.n2=5   f.o2=0   f.h2=0   f.hcl=0


$$$$$$$$$$$$ poly-gate
$CVD poly
deposi poly thick=.4

$doping
implant dose=5e15 arsen energy=40


deposi nitri thick=.1
etch nitri p1.x=3   left
etch nitri p1.x=3.8 right
etch poly  p1.x=3   left
etch poly  p1.x=3.8 right

$$$$$$$$$$$$$ p-base
etch  oxide   thick=.04
depos photore thick=1
etch  photore p1.x=3.4 left

implant dose=2.4e13 boron energy=60
etch photore

method compress

$oxide thick ness
$poly side-wall:
diffu time=5   temp=900 dryo2
diffu time=7   temp=900 weto2
diffu time=10  temp=900 dryo2
diffu time=120 temp=1100


$$$$ drift
deposi  photore thick=1
etch    photore p1.x=3.4    right

implant phos dose=2.6e12 energ=60


$$$$$$$$$$$$$  S/D

deposi photore thick=1
etch   photore p1.x=3.4 left

ETCH PHOTORES

deposi photore thick=1
etch   photore start    x=1   y=-5
etch   photore continue x=1   y=1
etch   photore continue x=3.4 y=1
etch   photore end      x=3.4 y=-5

etch   photore p1.x=7.3 right
implant arsen dose=2e15 energ=80

ETCH PHOTORES
diffu temp=950 time=30
```

```
$$$$$$************ electrode$$$$$$$$$$$$

etch nitrid all
deposi oxide  thick=.1
deposi oxide  thick=.2
deposi oxide  thick=.2
etch   oxide  p1.x=1.5 left
etch   oxide  p1.x=7.8 right
deposi alumin thick=1
etch alumin start   x=5.5 y=-4
etch alumin cont    x=5.5 y=2
etch alumin cont    x=7.3 y=2
etch alumin end     x=7.3 y=-4

deposi oxide thick=1

$define electrode
electrode name=S1 bot
electrode name=S2 x=2   y=-1.0
electrode name=D  x=7.4
electrode name=G  x=3.4 y=-0.2

save out.file=TMUD medici poly.ele elec.bot
```

2. Source file of step drift device for process simulation using TSUPREM4.

```
line x locat=0 spacing=0.6 tag=left

$ source,
line x locat=2 spacing=0.2

$ channel, 3-3.8um
line x locat=3.0  spacing=.01
line x locat=3.4  spacing=.06
line x locat=3.75 spacing=.01

$ drift, 3.8+3.5=7.3
line x locat=4.9   spacing=.05
line x locat=6.1   spacing=.05
line x locat=6.8   spacing=.05

$ drain, 7.3+1.2um=8.5
line x locat=7.3   spacing=.1
line x locat=8     spacing=.3
line x locat=8.5   spacing=.2 tag=right


line y location=0.6 spacing=0.03 tag=epi
line y location=5   spacing=0.5
line y location=15  spacing=10
line y location=100 spacing=20
line y location=200 spacing=30 tag=sub


elimin columns  x.min=2                y.min=0.5
elimin columns  x.min=2.5 x.max=4   y.min=4
elimin columns  x.min=2.8 x.max=3.2 y.min=6
elimin columns  x.min=3.6 x.max=4.2 y.min=6
```

```
region silicon xlo=left xhi=right ylo=epi yhi=sub

$$$$ p+ substrate, Boron doped, 1e15/cm-3
initial <100> boron=1e15


$$$$ top silicon 0.2u, buried oxide 0.4u.

deposit oxide   thick=.04  spaces=2
deposit oxide   thick=.16  spaces=4 dy=0.02 ydy=0.04
deposit oxide   thick=.16  spaces=4 dy=0.02 ydy=0.36
deposit oxide   thick=.04  spaces=2


deposi silicon boron=1e15 thick=.05 spaces=3 dy=.01 ydy=.01
deposi silicon boron=1e15 thick=.1  spaces=5 dy=.02 ydy=.02
deposi silicon boron=1e15 thick=.05 spaces=3 dy=.01



$**************  gate_oxide, 60 nm********

diff temp=900 time=20 f.n2=9.5 f.o2=.5  f.h2=0   f.hcl=0
diff temp=900 time=20 f.n2=5.5 f.o2=.5  f.h2=0   f.hcl=0
diff temp=900 time=16 f.n2=0   f.o2=3.3 f.h2=1.3 f.hcl=0
diff temp=900 time=16 f.n2=0   f.o2=3.3 f.h2=1.3 f.hcl=0.165
diff temp=900 time=12 f.n2=0   f.o2=3.3 f.h2=6   f.hcl=0.165
diff temp=900 time=9  f.n2=0   f.o2=3.3 f.h2=0   f.hcl=0
diff temp=900 time=10 f.n2=5   f.o2=0   f.h2=0   f.hcl=0
diff temp=900 time=20 f.n2=5   f.o2=0   f.h2=0   f.hcl=0


$$$$$$$$$$$ poly-gate
$CVD poly
deposi poly thick=.4

$doping
implant dose=5e15 arsen energy=40


deposi nitri thick=.1
etch nitri p1.x=3   left
etch nitri p1.x=3.8 right
etch poly  p1.x=3   left
etch poly  p1.x=3.8 right

$$$$$$$$$$$$ p-base
etch  oxide   thick=.04
depos photore thick=1
etch  photore p1.x=3.4 left

implant dose=2.4e13 boron energy=60
etch photore
method compress
$oxide thick ness
$poly side-wall:
diffu time=5   temp=900 dryo2
diffu time=7   temp=900 weto2
diffu time=10  temp=900 dryo2
diffu time=120 temp=1100


$$$$ drift
deposi  photore thick=1
etch    photore p1.x=3.4    right
```

```
implant phos dose=1.7e12 energ=60

deposi  photore thick=1
etch    photore p1.x=4.9    right
implant phos    dose=1.6e12 energ=60

deposi  photore  thick=1
etch    photore  p1.x=6.1    right
implant phos     dose=7e11 energ=60


$$$$$$$$$$$$$  S/D

deposi photore thick=1
etch   photore p1.x=3.4 left

$implant boron dose=2.5e15 energ=60

ETCH PHOTORES

deposi photore thick=1
etch   photore start    x=1   y=-5
etch   photore continue x=1   y=1
etch   photore continue x=3.4 y=1
etch   photore end      x=3.4 y=-5

etch   photore p1.x=7.3 right


implant arsen dose=2e15 energ=80


ETCH PHOTORES
diffu temp=950 time=30


$$$$$************ electrode$$$$$$$$$$$$

etch nitrid all
deposi oxide  thick=.1
deposi oxide  thick=.2
deposi oxide  thick=.2
etch   oxide  p1.x=1.5 left
etch   oxide  p1.x=7.8 right
deposi alumin thick=1
etch alumin start   x=5.5 y=-4
etch alumin cont    x=5.5 y=2
etch alumin cont    x=7.3 y=2
etch alumin end     x=7.3 y=-4

deposi oxide thick=1

$define electrode
electrode name=S1 bot
electrode name=S2 x=2   y=-1.0
electrode name=D  x=7.4
electrode name=G  x=3.4 y=-0.2

save out.file=TMstepdrift medici poly.ele elec.bot
```

Appendix D

List of publications by author during Ph.D. study

[1] J. Luo, G. Cao, M. M. De Souza, "A high performance RF LDMOSFET in thin film SOI technology with step drift doping profile", Solid-state Electronics, 2003, Vol.47, No.11, p.1937-1941.

[2] J. Luo, G. Cao, O. Spulber, S. Hardikar, Y. M. Feng, E. M. S. Narayanan, M. M. De Souza, "Influence of Physical Parameters on Quasi-saturation in SOI RF LDMOS" Proceedings of 2002 IEEE International Conference on Semiconductor Electronics, p.314-318.

[3] M. M. De Souza, G. Cao, E.M. Shankara Narayanan, F. Youming, S.K. Manhas, J. Luo, N. Moguilnaia, "Progress in silicon RF power MOS Technologies — current and future trends", Proceedings of the Fourth International Caracas Conference on Devices, Circuits and Systems, 2002, p.D047-1-7.